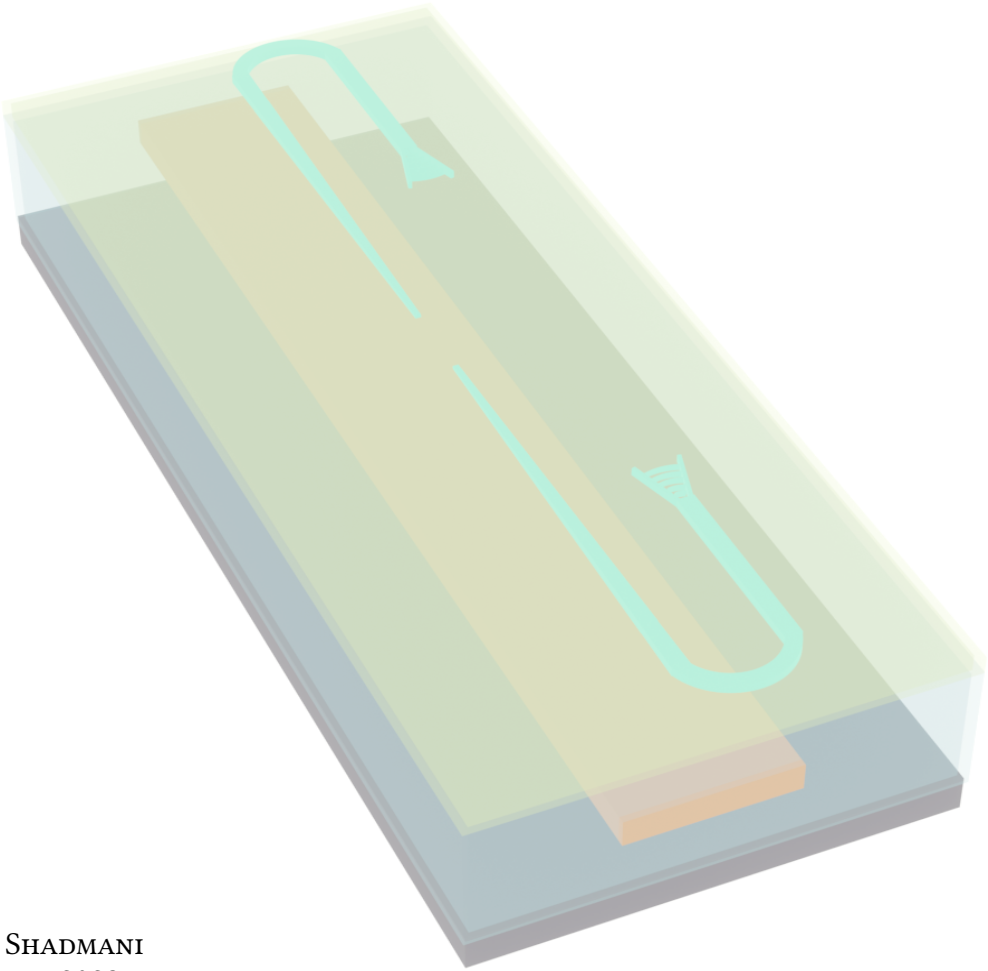
PhD Thesis

Heterogeneous integration of GaAs waveguides on low loss substrates for quantum photonic circuits



Atefeh Shadmani
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Colophon

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Heterogeneous integration of GaAs waveguides on low loss substrates for quantum photonic circuits

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Abstract

The range of building blocks required to perform quantum photonic tasks demonstrates that existing photonic components based on monolithic material systems may be inadequate. Hybrid quantum photonic circuit is emerging as an exciting field in quantum photonics. The conceptual idea behind it is to combine different building blocks, which can be generally incompatible in terms of their growth and integration conditions, in a functional circuit to form a versatile quantum photonic integrated circuit platform. For example, near-ideal single-photon sources have been realized in III-V platforms like GaAs. However, this platform suffers from a relatively high propagation loss and lacks efficient and low-loss optical components. On the other hand, there are platforms such as silicon nitride (Si_3N_4) and lithium niobate ($LiNbO_3$), which provide low-loss high-speed optical components like switches, modulators, and filters. By heterogeneous integration, we can take advantage of the strengths of each single platform and create a hybrid platform that can potentially outperform its monolithic constituents.

In this thesis, the heterogeneous integration of GaAs on-chip circuits containing self-assembled quantum dots on a Si/SiO_2 wafer is demonstrated. Here, we report fabrication techniques developed for this heterogeneous integration based on the adhesive die-to-wafer bonding method. The optical propagation loss for the GaAs waveguides fabricated on the GaAs-on-Si hybrid substrate is measured to be $< 7\,dB/mm$, which is comparable with the performance of suspended GaAs circuits. In quantum dot excitation at $T < 10\,K$, anti-bunched emission from individual quantum dots is observed, confirming that the fabrication process does not affect the quantum dot performance. We have also fabricated GaAs waveguides on top of Si_3N_4 waveguides embedded in a SiO_2 layer. A taper-based spot-size converter structure is designed in the GaAs waveguide layer, which enables optical light coupling between the GaAs and Si_3N_4 waveguide layers. The existing limitations are well understood: for example, the number of counts from quantum dot emission is not high enough, which makes it challenging to measure the auto correlation function between emitted photons and extract the exact value for $g^2(0)$. To reach a more precise estimate, a sample with a lower quantum dot density, together with a narrower filtering apparatus will be needed. To be able to measure indistinguishability of the emitted photons, it is required to integrate p-i-n heterostructure GaAs membranes and fabricate electrically contacted devices.

We proposed micro-transfer printing as an alternative method to adhesive die-to-wafer bonding for heterogeneous integration. Double-sided tapered GaAs waveguides have been designed and fabricated as the source wafer for transfer printing. In collabo-

ration with Ghent University, we performed successful transfer printing of standalone nanobeam GaAs waveguides for the first time. In optical measurements, we demonstrated the light transmission with a mean overall loss of 3 dB per device.

This thesis reports fabrication techniques and device characterizations for the heterogeneous integration of GaAs waveguides with embedded quantum dots on a SiO_2 layer, which is an important step toward the heterogeneous integration of GaAs-based devices with different material systems. This heterogeneous integration can potentially solve the major obstacle in realizing more complex photonic integrated circuits (PICs) using CMOS processes.

Sammenfatning

Rækken af byggesten, som er nødvendige for at gennemføre kvantefotoniske opgaver, viser, at de eksisterende fotoniske komponenter baseret på monolitiske materialesystemer kan være utilstrækkelige. Hybride kvantefotoniske kredsløb er et nyt og hastigt voksende felt indenfor kvantefotonik. Konceptuelt er idéen at kombinere forskellige byggeklodser, som individuelt ikke er direkte kompatible med hensyn til vækst- og integrationsmetoder, så de danner en alsidig platform til funktionelle kvantefotoniske integrerede kredsløb. For eksempel er næsten ideelle enkeltfoton-kilder blevet realiseret i III-V platforme som GaAs. Denne platform lider dog af relativt store propageringstab og mangler effektive optiske komponenter med lavt optisk tab. På den anden side tilbyder platforme som siliciumnitrid ($Si_{33}N_4$) og lithiumniobat ($LiNbO_3$) lave optiske tab og hurtige optiske komponenter som switches, modulatorer og filtre. Gennem heterogen integration kan vi skabe en hybrid platform, som kan drage fordel af styrkerne fra flere platforme, og som potentielt kan udkonkurrere sine monolitiske delkomponenter. Heterogen integration af GaAs bølgeleder-kredsløb, som indeholder selvsamlede kvantepunkter, på en Si/SiO_2 -wafer demonstreres. I denne afhandling reporteres fabrikationsteknikkerne udviklet for denne heterogene integration baseret på den adhæsive chip-til-wafer bindingsmetode. Det optiske propagationstab for GaAs bølgeledere fabrikeret på det GaAs-på-Si hybride substrat måles til $< 7\,\mathrm{dB}/mm$, hvilket er sammenligneligt med ydeevnen for suspenderede GaAs kredsløb. Kvantepunkterne exciteres optisk ved $T < 10\,\mathrm{K}$ og anti-klynget emission fra individuelle punkter observeres, hvilket bekræfter at fabrikationsprocessen ikke påvirker kvantepunkternes ydeevne. Vi har også fabrikeret GaAs bølgeledere oven på Si_3N_4 bølgeledere indlejret i et SiO_2 -lag. En tilspidsende struktur, som konverterer den optiske mode til pletstørrelse i GaAs bølgelederlaget, designes, og det muliggør kobling af lys mellem bølgelederne i GaAs- og Si3N4 -lagene. De eksisterende begrænsninger er velkendte: for eksempel er antallet af målte fotoner fra kvantepunktsemissionen ikke høj nok, hvilket gør det udfordrende at måle autokorrelationsfunktionen og dermed udtrække enkeltfotonrenheden $g^2(0)$. For at opnå et mere præcist estimat skal der bruges en prøve med lavere densitet af kvantepunkter sammen med et smalbåndet filtreringapparatur. For at måle de emitterede fotoners udartning, er det nødvendigt at integrere p-i-n heterostruktur-GaAs membraner samt fabrikere elektrisk kontaktede prøver. Vi foreslår mikro- overførselstryk som en alternativ metode til adhæsiv chip-til-wafer binding for heterogen integration. Dobbelt-siddet tilspidsende GaAs bølgeledere er blevet designet og fabrikeret som kilde-wafer for overførselstrykket. I samarbejde med Ghent University har vi succesfuldt udført overførselstryk af selvstændige nanobjælke GaAs bølgeledere for første gang. Med optiske målinger har vi demonstreret transmission

af lys med et gennemsnitligt tab på 3 dB per struktur. Denne afhandling reporterer fabrikationsteknikker og karakteriseringen af strukturer, som består af heterogent integreret GaAs bølgeledere med indlejrede kvantepunkter på et SiO_2 lag, hvilket er et vigtigt skridt mod heterogen integration af GaAs-baserede strukturer med andre materialeplatforme. Denne heterogene integration har potentialet til at løse en omfattende udfordring mod mere komplekse fotoniske integrerede kredsløb (PIC) med komplementære metal-oxid-halvleder (CMOS) fabrikationsprocesser.

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List of publications

Manuscript

1. *Integration of GaAs waveguides on a silicon substrate for quantum photonic circuits.* Atefeh Shadmani Rodrigo A. Thomas, Zhe Liu, Camille Papon, Martijn J. R. Heck, Nicolas Volet, Sven Scholz, Andreas D. Wieck, Arne Ludwig, Peter Lodahl, Leonardo Midolo. Opt. Express. 2022, 30(21), 37595-37602.

Conference presentations

1. *Integration of GaAs waveguides with quantum dots on Silicon substrates for quantum photonic circuits.* in CLEO: QELS Fundamental Science, (Optica Publishing Group, 2022), pp. FF4J–6, Atefeh Shadmani, Rodrigo A. Thomas, Zhe Liu, Nicolas Volet, Martijn J. R. Heck, Sven Scholz, Andreas D. Wieck, Arne Ludwig, Peter Lodahl, Leonardo Midolo.

2. *Towards the heterogeneous integration of single-photon sources on sin using micro-transfer printing.* in Proc. Int. Conf. Integr. Quantum Photon., (2022) Jasper De Witte, Atefeh Shadmani, Tom. Vanackere, Tom. Vandekerckhove, Peter. Lodahl, Gunther. Roelkens, Leonardo. Midolo, B. Kuyken, and Dries. Van Thourhout.

3. *Integration of GaAs waveguides on Silicon for quantum photonics.* in MNE. Turin, Italy , (2021) Atefeh Shadmani, Zhe Liu, Camille Papon, Beatrice Da Lio, Nicolas Volet, Martijn J. R. Heck, Andreas D. Wieck, Arne Ludwig, Peter Lodahl, Leonardo Midolo.

Contents

Chapter 1

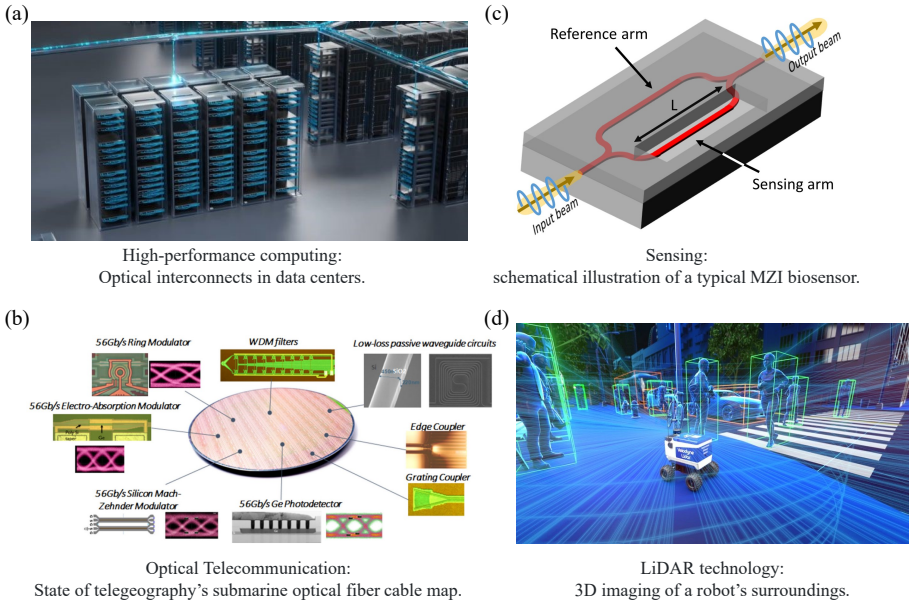
Introduction

1.1 Introduction

Today, ever-increasing amounts of data make finding new ways to store and process information a necessity. Electronics can be considered as one of the most important technologies of the 20th century due to the development of the transistors [1]. However, as stated by Moore's law [2], the number of electronic devices integrated in a single chip doubles roughly every two years. Accordingly, conventional silicon-based electronics are close to saturation. Therefore, the 21st century requires the next revolutionary technology that makes further increasing of the computing power possible. One promising possibility can be photonics, where information is processed and transported using light [3]. It comes to nano-photonics, when focousing on the interaction of light with structures and materials at the nanoscale level. Nano-photonics offer many advantages by miniaturization and therefore reduction of power-consumption and scaling up. An integrated nanophotonic system can be manufactured using different semiconductor wafers processed in a cleanroom facility. Photonic integrated circuits (PICs) represent a powerful technology that combines the benefits of nanophotonics with conventional mature electronic devices on a single substrate.

The integration of photonic and electronic components on a silicon substrate offers several advantages compared with alternative semiconductor materials (e.g. III-V, lithium niobate ($LiNbO_3$)). By integrating these two domains, silicon PICs offer significant advantages in terms of speed, bandwidth, energy efficiency, and scalability [4]. Moreover, silicon is compatible with existing complementary metal-oxide-semiconductor (CMOS) fabrication processes, which allows for the efficient and cost-effective mass

production of silicon PICs using well-established semiconductor manufacturing techniques. Therefore, silicon photonics have emerged as one of the so-called "more than moore" technologies. Silicon photonics have applications across various domains. Figure 1.1 shows the main applications of silicon photonics. It plays a crucial role in high-performance computing. Silicon photonics offers direct integration of high-speed optical interconnects into microprocessors and other integrated circuits, enabling faster and more efficient data transfer, improved communication, and increased energy efficiency. This can lead to significant improvements in the performance of computing systems such as supercomputers. Figure 1.1 (a) shows an image provided by Intel describing the use of silicon photonic interconnects in data center environments [5]. Moreover, silicon photonics has the potential to offer faster and more efficient communication networks, by increasing bandwidth and reducing power consumption. Figure 1.1 (b) shows an example of a silicon photonic platform (from imec) [6]. Providing advantages such as integration of optical transceivers in a single chip, low-loss high-speed switches, and wavelength division multiplexing (WDM), silicon photonics has significant applications in optical telecommunication.



High-performance computing:
Optical interconnects in data centers.

Sensing:
schematical illustration of a typical MZI biosensor.

Optical Telecommunication:
State of telegeography's submarine optical fiber cable map.

LiDAR technology:
3D imaging of a robot's surroundings.

Figure 1.1: Some of the main applications of silicon photonics. (a) High-performance computing. Image provided by Intel showing optical interconnects in data center environments [5]. (b) Fully integrated silicon photonics platform from Imec [6]. Silicon photonics offers integrated efficient components for optical telecommunication. (c) Example of a silicon photonic MZI biosensor, adopted from [7]. (d) Example of a 3D LiDAR robot, Image source: Velodyne [8].

In addition to its use in data centers, silicon photonics can also be used for sensing applications in a variety of industries, including environmental monitoring, chemical sensing, and biomedical sensing. For instance, figure 1.1 (c) illustrates a typical Mach–Zehnder interferometer (MZI) biosensor [7]. In this example, the input light splits into two arms, named as reference and sensing arms, and recombines at the output. The degree of interference at the output is proportional to the refractive index variation in the sensing arm. LiDAR (Light Detection and Ranging), a technology used for remote sensing and mapping, is another important application of silicon photonics [9]. LiDAR is commonly used in autonomous vehicles, robotics, and industrial automation. Instead of using radio frequency (RF) signals, LiDAR uses a light wave (laser light in many cases) to illuminate a scene based on reflection. It analyzes the reflected light by measuring the time it takes them to return to the source (TOF = Time of Flight) to gain critical information about what is going on in the area [10]. Figure 1.1 (d) shows a typical 3D lidar system [8], that scans light beams in three dimensions to create a virtual model of the environment. Measuring and processing the reflected light signals enables the vehicle to detect and identify the surrounding objects. Silicon photonics can also contribute to quantum photonic integrated circuits (QPICs) by integrating various quantum photonic components into on-chip circuits. Quantum photonic systems, such as quantum dots and quantum wells, can be designed and fabricated on silicon chips, enabling the manipulation, routing, and detection of the quantum states of light. This application will be discussed in more detail in the following section.

1.2 Quantum photonic integrated circuits

In classical silicon-based devices, information is processed in binary form. Each elementary component (bit) can be in two states, either 0 or 1 [11]. By exploiting the unique properties of photons and the laws of quantum mechanics, one can move beyond the binary system [12]. Photonic quantum technology, a science that uses the fundamental principles of quantum mechanics to control light at the quantum level, opens up new possibilities for revolutionary advancements in information gathering, processing and transport [13, 14]. In a quantum mechanical system, an object with two states can occupy either of the two states, but it can also be in an arbitrary combination (superposition) of the two states[15]. In other words, the generic state for a quantum object that can be in two states of $|0\rangle$ and $|1\rangle$, is denoted as

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{1.1}$$

where α and β are the probability amplitudes of the states $|0\rangle$ and $|1\rangle$ with $|\alpha|^2 + |\beta|^2 = 1$. This means that there are infinite quantum states for a single quantum bit (qbit) to take

and allows for the encoding and processing of quantum information in a highly efficient manner. The qbit can only be in superposition as long as you have not measured it. Once the qbit is measured, it instantly collapses to either $|0\rangle$ or $|1\rangle$ state.
Another key property of a quantum mechanical system is quantum entanglement. When two or more particles become entangled, their quantum states become correlated such that the state of one particle is immediately related to that of the other, regardless of the distance between them. For instance, having two quantum systems A and B, the entangled state is given by

$$|\psi_{A,B}\rangle = \frac{1}{\sqrt{2}} \left(|0\rangle_A |1\rangle_B + |1\rangle_A |0\rangle_B\right), \tag{1.2}$$

Which implies each A or B object can be in states $|0\rangle$ or $|1\rangle$ with 50 % probability. This phenomenon enables the creation of entangled photon pairs, which can be used for secure communication protocols (quantum cryptography) or distributed quantum computing [16]. Therefore, in a quantum mechanical system, one can also take advantage of the properties of photons, such as their ability to exist in superposition states and to be entangled, to gain a much more powerful platform compared with the conventional platforms. To scale up quantum photonics to more complex functionalities, for which tens of photons are required, the concept of quantum photonic integrated circuits (QPICs) is introduced [17–19]. QPICs are chip-scaled platforms that bring together photonics and the principles of quantum mechanics, enabling the generation, manipulation, and detection of the quantum states of light. The realization of QPICs requires the development of some indispensable components like single-photon emitters, waveguides, and detectors, on which many works have been don[17].

1.3 Solid-state single-photon emitters

One of the central building blocks in many leading quantum technologies are non-classical light sources, which produce streams of photons with controllable quantum correlations. Over the years, a variety of promising material systems have been developed for single-photon generation. Nonlinear processes, such as spontaneous four-wave mixing [20] and spontaneous parametric down conversion [21] play a crucial role in generating single photons, figure 1.2 (a), (b). This scheme can provide on-demand single-photons by controlling experimental parameters, and the emission efficiency can be high. However, the probabilistic nature of single-photons limits the reliability of this scheme, i.e., there is still a probability of generating multiple photon pairs or no photon at all in each emission event.
On the other hand, there are two-level system single-photon emitters. Figure 1.3 presents a brief overview of the different types of two-level systems that generate

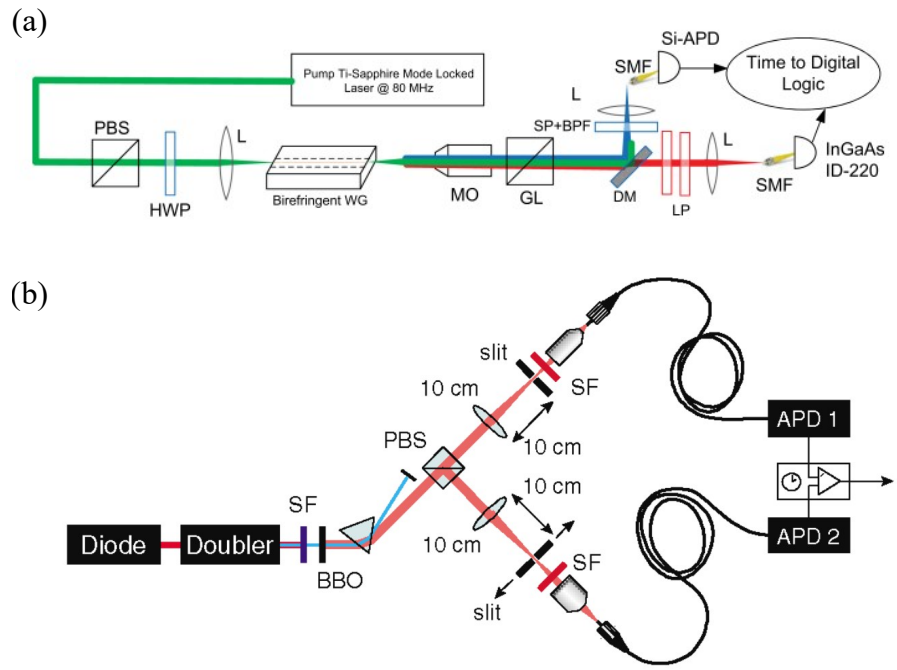


Figure 1.2: Single-photon generation based on non-linear processes. (a) Diagram of the experimental setup used to measure the count rates and photon pair correlations of the single photons generated by spontaneous four-wave mixing [20]. (b) Experimental setup for measuring photon correlations in the transverse momentum of photons, generated by spontaneous parametric down conversion, adopted from [21].

single photons. The first demonstration of a single-photon emitter was in 1977, using atomic transitions of sodium atoms, although it had low reliability and efficiency [22]. Today, it is possible to generate efficient on-demand single photons by an adiabatically driven stimulated Raman transition between two atomic ground states [23], figure 1.3 (a). However, complex setups are required, and such sources cannot be directly embedded in a circuit due to the challenges in loading atoms or ions. Moreover, the slow dynamics of atom-based sources can notably decrease the operation rate of the system. Another scheme to generate single photons is color centers, i.e., atomic defects in solid-state materials. The great advantage of color center single photon emitters, such as nitrogen-vacancy (NV) centers in diamond [24] or silicon vacancy (SiV) centers in silicon carbide [25] is their room temperature operation, which enables rapid characterization. Figure 1.3 (b) depicts the efficient coupling of single photons generated from diamond color centers into optical fibers. In color centers, not all excitations result in

single-photon emission. This emission inefficiency reduces the overall brightness and therefore restricts their use in most applications that require high photon flux.

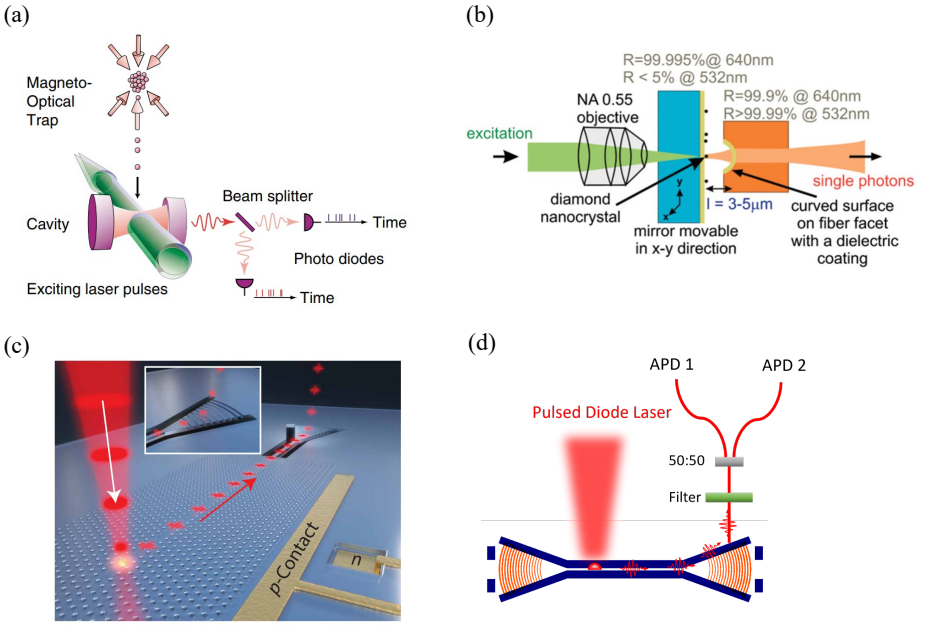


Figure 1.3: Two-level system single-photon generation. (a) Atom-based single-photon emission, adopted from [23]. Atoms released from a magneto-optical trap fall through the cavity and interact with it. The emitted atoms from the cavity are detected by a pair of photodiodes. (b) Setup used to efficiently couple single photons generated from diamond color centers into optical fibers, adopted from [24]. (c) Single photon emission from InAs quantum dots embedded in a photonic crystal waveguide, adopted from [26]. (d) Schematic illustration of a HBT measurement setup adopted from [27]

One of the most promising approaches to generate single photons is the use of quantum dots (QDs), which combine the excellent optical properties of atoms with the convenience and scalability of solid-state host systems. Figure 1.3 (c) depicts a single-photon source based on InAs QDs embedded in a photonic crystal waveguide. When a QD is excited by optical or electrical excitation, it can emit a single photon when it relaxes from the excited state to the ground state. In this scheme, the downside is the inhomogeneous distributions of QDs that cause variability between photons emitted from different emitters. Currently, high-quality deterministic single-photon emitters have been shown based on self-assembled InAs/GaAs QDs [26], which will be discussed in more detail in the next section.

When evaluating the performance of a single photon emitter, several figures of merit can be considered. The most important properties of a single-photon emitter include

high brightness and emission rate, as well as high single-photon purity and indistinguishability. Here, we take a closer look at each of these three key characteristics.

Brightness of a source refers to the maximum rate at which single photons can be emitted (or collected). It quantifies the probability of detecting single-photons at the output per excitation pulse. This feature is stated by (β-factor), which involves efficient coupling of the QD emission into the waveguides fundamental mode. Ideally, for a bright single-photon source, the (β-factor) equals 1. High brightness is an essential factor for applications requiring high photon flux or fast information processing, such as quantum cryptography or quantum key distribution.

single-photon purity of a source refers to the multiphoton emission probability. It quantifies how successfully the presence of unwanted photons, such as background noise, higher-order emissions, or multiphoton events, can be suppressed. The purity of a single-photon source can be measured in a Hanbury-Brown-Twiss (HBT) experiment [28]. Figure 1.3 (d) schematicaly illustrates a HBT measurement setup, where the generated photon stream, after passing through a grating filter to select individual QD transitions, splits into two separate paths using a 50/50 beam splitter [27]. Each path has a detector (for example an avalanche photo-diode (APD)), which clicks for each single-photon detection. The arrival times of photons, recorded by the detectors, will be sent to a correlator. The collected photon coincidences give the second-order correlation function at zero time delay $g^{(2)}(\tau = 0)$. An ideal pure single-photon source will have $g^{(2)}(\tau = 0) = 0$, i.e. the complete suppression of unwanted photons. A cleaner single-photon source with high photon purity is crucial for reliable and accurate quantum information processing.

Indistinguishability of the photons emitted by a source refers to their degree of similarity in terms of polarization, frequency, spatial and temporal shape. It quantifies how identical the photons in a stream are, by their interference visibility (V). The indistinguishability between photons emitted by a source can be measured with a Hong-Ou-Mandel (HOM) experiment [29], evaluating the two-photon interference visibility through a MZI scheme. Ideally, a high indistinguishability with visibility (V) close to 1 is desirable, indicating near-identical photons.

1.3.1 Quantum Dots

Quantum dots – nanoscale semiconductor particles – play a crucial role in QPICs. In a QD, the charge carriers occupy only a restricted set of energy levels, similar to electrons in an atom; therefore, QDs are sometimes referred to as ”artificial atoms”. However, the great advantage of QDs is that they are embedded in a solid material, which foregoes the need for trapping.

Epitaxial growth of self-assembled quantum dots

In a heterostructure, by combining two semiconductor materials with different energy bandgaps, a potential well for the carries can be made in the conduction band (CB) and valence band (VB) [30]. Figure 1.4 (a) shows the confinement potential in the heterostructure of gallium arsenide (GaAs) and indium arsenide (InAs). By absorbing a photon, either with the same energy as the bandgap (resonant excitation, red arrow in the figure) or with a higher energy (above-band excitation, gray arrow in the figure), an electron can be excited from the valence band and to the conduction band, and leaving a hole in the valence band. Subsequently, the electron relaxes down to the valence band while emmitting a single photon. The spectrum in Figure 1.4 (b) illustrates typical QD transitions excited by an above-band optical excitation, where the discrete nature can be observed. The pink area in the figure 1.4 (a) depicts the potential well forming the QD surrounded by GaAs bulk. During growth, at the interface between GaAs and InAs, an unwanted wetting layer is formed (WL). This should be ideally avoided, because the presence of the wetting layer leads to a less deep potential well. When all three dimensions are reduced, a quantum dot can be created. In this case of 3D confinement in a QD, the density of the states will be a delta-function, similar to the behavior of an atom [31].

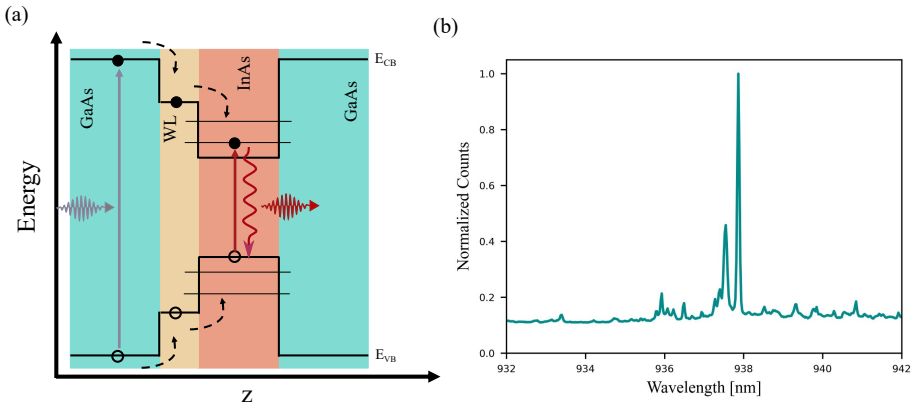


Figure 1.4: (a) The heterogeneous structure of a GaAs/InAs quantum dot. The difference in bandgaps make a potential well in conduction band (CB) and valance band (VB). The undesired wetting layer (WL) has been shown in yellow. (b) Emission spectrum from an above-band excited InAs/GaAs QD.

Molecular beam epitaxy (MBE) is an advanced material growth technique for building ordered layers of high-quality material from beams of different elements [32]. Using an MBE system, monolayers of lattice-mismatched semiconductor materials can be deposited on top of each other under highly controlled condition in vacuum

[33]. In the Stranski-Krastanov (SK) method [34], the lattice-mismatch between layers with two different materials can create strain, which leads to the random formation of self-assembled 3D islands, called quantum dots. In the wafers used in this thesis, self-assembled QDs are formed as a result of the epitaxial growth of InAs on top of GaAs with a lattice-mismatch of 7%. In figure 1.5 (a), a schematic illustration of an InAs quantum dot grown in a GaAs membrane is presented. The dots grown with this technique have dimensions 20-40 nm diameter and 4-7 nm height. As a final step, the dots are capped with GaAs to form 3D confinement and limit the oxidation effects from the surface states. In this thesis, all GaAs samples are grown by Dr. Arne Ludwig and colleagues at the University of Bochum, Germany. Figure 1.5(b) sketches the layer stack of the typical heterostructures studied in this thesis, showing the self-assembled QDs (red dots). It consists of a 160 nm GaAs membrane with self-assembled QDs on top of an AlGaAs sacrificial layer. The morphology of a self-assembled InAs/GaAs QD is shown in the scanning tunneling microscope (STM) image in figure 1.5 (c). A top-view atomic force microscope (AFM) image of an uncapped InAs QD layer is shown in figure 1.5 (d).

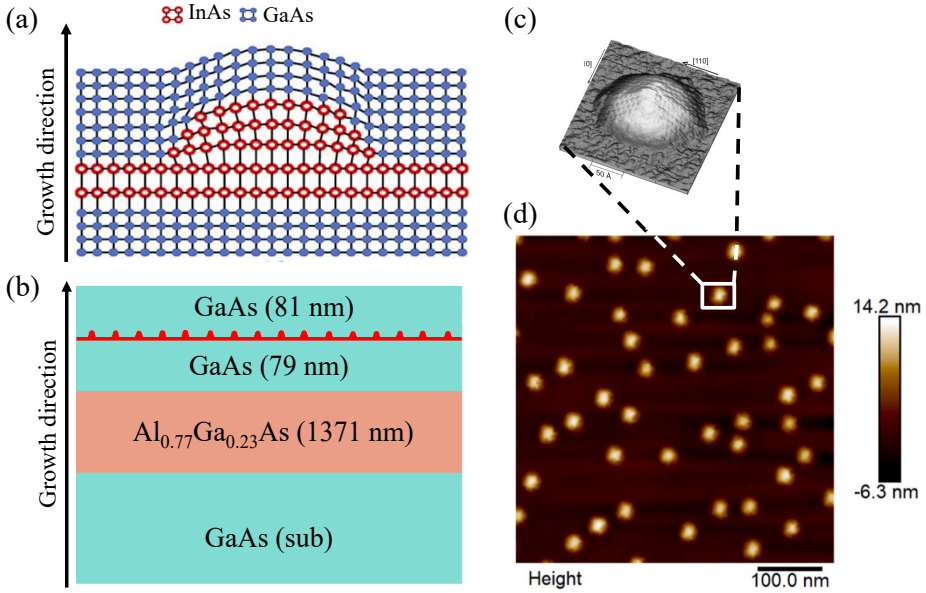


Figure 1.5: (a) Schematic illustration of InAs QDs embedded in a GaAs membrane (adopted from [35]). (b) Schematic of a heterostructure GaAs membrane with embedded QDs (red dots) grown by molecular beam epitaxy (MBE). (c) Scanning tunneling microscope image of an uncapped InAs quantum dot (top view) [36]. (d) Atomic force microscope image of self-assembled InAs quantum dots [37].

1.3.2 Quantum dot single photon sources

Quantum dot nanodevices play an undeniable role in quantum photonics, enabling high-performance devices like on-chip phase-shifters [38], routers [39], switches [40, 41], modulators [42], lasers [43–45], and on-demand single-photon sources [26, 46–49]. Among all the various materials and platforms, III-V group materials, especially GaAs with embedded self-assembled QDs, stand out for offering indispensable quantum functionalities such as single-photon generation, manipulation, and detection, all integrated in one single chip [50]. A key aspect of GaAs membrane technology is the suppression of out-of-plane photon leakage, which enables near-deterministic single-photon generation [51]. This results from the high refractive index contrast between GaAs (n = 3.5) and air. Therefore, the realization of a GaAs-based quantum photonic integrated circuit (QPIC) is currently implemented with suspended waveguides [52]. To date, there has been excellent progress in the development of suspended waveguide GaAs technology [53, 54]. Combining QD single-photon emitters with photonic nanostructures, such as photonic crystal waveguides and cavities, is a promising method for creating efficient and controlled single-photon generation and emission [55, 56]. Photonic crystal cavities can enhance single-photon sources by increasing the collection efficiency of single photons and producing indistinguishable photons. The near-unity coupling efficiency of such an emitter to a photonic crystal waveguide has been achieved by the Niels Bohr Institute (NBI) [51]. However, such approaches, even if commercialized [57], still require rather complex setups to generate photons, i.e., cryostats suitable for fluorescence microscopy. This limits the wide-spread use and scalability of such sources. To get out of the lab, there is a clear need to make such single-photon sources compatible with mature and scalable packaging approaches.

1.4 Hybrid integrated quantum photonic circuits

Quantum photonic integrated circuits contain several main building blocks for generating, manipulating, and detecting light, which underpin different applications. These central requirements consist of high-quality single-photon sources [26], ultralow-loss waveguides, low-loss passive components such as beam splitters and filters [58], photonic elements that can be actively controlled like optical modulators [59], high-speed optical switches [60], and efficient single-photon detectors [61]. Each of these functionalities with its best performance has been shown in a specific material platform. Therefore, different material platforms seem to be required. Namely, materials that have the capability to produce light, materials that provide low-loss waveguiding, materials that can perform fast switching, materials that can detect light, and even some nonlinear materials. The variety of desired building blocks, each essential for a

special task, implies that the existing photonic platforms based on one single material system, such as III–V, silicon nitride (Si_3N_4), lithium niobate ($LiNbO_3$), and etc., may be inadequate.

Hybrid integration for quantum photonics refers to combining different material platforms with different fabrication technologies to take advantage of different technologies [62]. Figure 1.6 provides a schematic of a hybrid quantum photonic integrated circuit with different components for the generation, manipulation, and detection of non-classical light [63]. The lower row shows each component in more detail. Quantum single-photon emitters (III-V based) generate light and couple it into low-loss photonic waveguides (Si-based). Directional couplers, phase shifters, and ring-resonators can be employed for the linear and nonlinear control of photons. Finally, the presence of on-chip spectral filters and detectors can lead to efficient reading of single-photons without the need for lossy photon extraction from the chip.

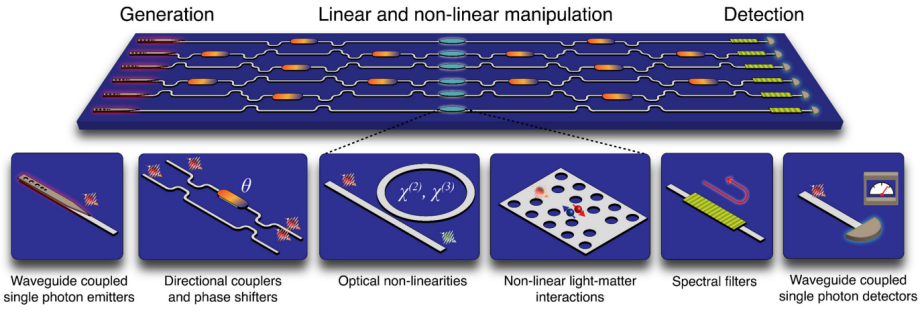


Figure 1.6: Schematic of a hybrid quantum photonic integrated circuit with different optical components based on different platforms [50]. Lower row: individual components in more details.

A lot of work has been done in the field of integrating quantum nanostructures like III–V QD single-photon sources [64], quantum lasers [43, 65], single-photon detectors [66–68], and quantum memories [69, 70] with different photonic platforms, including silicon nitride (Si_3N_4) [71], silicon on insulator (SOI) [72, 73], and lithium niobate ($LiNbO_3$) [74, 75]. By hybrid integration, one can take advantage of attractive properties in each photonic platform, which can lead to circumventing the limitations of different platforms. For example, Silicon Photonics offers wafer-based manufacturing and enables the integration of a variety of low-loss optical structures comprising switches, modulators, detectors, and filters. However, there is a significant exception here, light sources. Because of their indirect bandgap, the realization of an efficient light source is a challenge in silicon-based platforms. To date, photons can be generated outside the chip and brought to it using different available external coupling methods [47], or

they can be generated internally using the nonlinearity of waveguide materials [76]. However, these approaches currently cannot satisfy the demanding requirements of complex quantum information processing [77]. On the other hand, high-performance optical sources have been realized in III-V semiconductors. A promising alternative is the integration of efficient quantum emitters into silicon photonics integrated circuits. Therefore, for the realization of advanced photonic systems-on-chip, there is a need for the integration of III-V light sources directly on silicon PICs to take advantage of both high-quality single photon emission provided by QDs in GaAs and mature SOI platforms. Therefore, a heterogeneous CMOS-compatible quantum PIC can be constructed.

1.5 Heterogeneous III-V on silicon integration

The realization of scalable quantum technology for quantum information processing will likely require the integration of single-photon emitters with advanced functionalities for low-loss routing and switching provided by silicon nitride photonic integrated circuits. Many possible techniques have been developed for this integration [78] namely epitaxial growth of III-V layers (GaAs for example) on Si substrate [79], flip-chip bonding [80], pick-and-place assembly [81], micro-transfer printing [82, 83], and wafer bonding [84, 85]. Here, we describe the main technologies for this hybrid integration and briefly discuss the advantages and disadvantages of each approach.

Epitaxial growth of III-V layers

This method is based on growing quantum materials (like InAs or GaAs) directly on a photonic platform (Si wafer for example). Hybrid heterostructures enable the use of both quantum emitters and photonic circuits in a single chip. This can typically be achieved using technologies like molecular beam epitaxy (MBE) [86] or metal-organic vapor deposition (MOCVD) [87]. III-V QD single-photon-sources [88, 88] and lasers [89–91] monolithically grown on Si have been successfully demonstrated in recent years. Figure 1.7 (a) describes the epitaxial growth of GaAs on si using a graphene buffer layer [92]. Growing such heterostructures is not always favorable; discrepancies in material properties between Si and III-V lead to defects and reduce the performance of the resulting device. To address this issue, a wide variety of strain-compensation techniques have been developed [93]. However, compared with III-V devices on a native substrate, the quality of III-V layers epitaxially grown on Si remains unsatisfactory for deployment on PICs or ICs.

Flip-chip and pick-and-place assembly

In this study, the III-V components are typically fabricated on their native substrates using standard fabrication techniques for III-V platforms. Then, the prefabricated device can be either flipped or picked-and-placed one by one on a pre-processed Si wafer. Different III-V components like single-photon sources and lasers have been reported to be integrated on Si using pick-and-place assembly [64, 81, 94] and flip-chip technique[80, 95]. In this method a machine vision is a crucial requirement for the precise alignment of the III-V device to the target location on Si substrate. Transparent stamps are usually used in this method, which allows the user to monitor the alignment with an optical microscope. An adhesive layer is typically used to achieve bonding for this integration. Figure 1.7 (b) illustrates the concept of pick-and-place assembly. An array of pre-fabricated III-V optical devices on a target glass cover is picked, moved, and placed on a Si host substrate using a needle [96]. Although this method has some advantages, such as the use of standard fabrication for III-V and the opportunity to pre-characterize every single device before integration, the complexity of the alignment itself, makes it an expensive approach for the integration. The alignment accuracy is limited by the optical diffraction limit of visible light, which is approximately a few hundred nanometers. Moreover, in this method III-V devices are integrated one by one, which decreases the yield and success rate of this process and impacts production efficiency and cost-effectiveness.

Micro transfer printing

In this method, high-quality III-V devices can be fabricated and characterized on their original III-V substrate, and then they can be selectively removed from their source wafer and transferred simultaneously in parallel to a new target wafer. Successful transfer printing of different III-V components on a foreign platform like Si, has been demonstrated [82, 97, 98]. For transfer printing, the ability to undercut-etch the III-V components to remove them from their native wafer is required. Here, to print III-V nanodevices on the new substrate, a thin adhesive intermediate layer may be used. Figure 1.7 (c) depicts parallel microtransfer printing of III-V coupons on a silicon platform.

Unlike flip-chip and pick-and-place assembly, the parallel transfer of devices in micro-transfer printing reduces the number of packaging steps, which leads to significant simplification and cost savings. However, expensive complicated equipment is still employed for the precise alignment of the III-V components to the target wafer. The micro-transfer printing technique will be studied in greater detail later in this thesis, in chapter 6.

Wafer bonding

Another well-known method for integrating dissimilar material platforms is wafer bonding. This method involves transferring the entire unpatterned III-V membrane onto the target wafer. In this method, in the first step, the two III-V and Si wafers are bonded together, either by interfacial bonds (direct) or by using an intermediate adhesive layer, followed by removal of the III-V substrate. The concept of wafer bonding is shown in figure 1.7 (d). The transferred membrane will be processed to fabricate the integrated devices. The devices can then be precisely fabricated by lithographic alignment between the III–V and SOI structures.

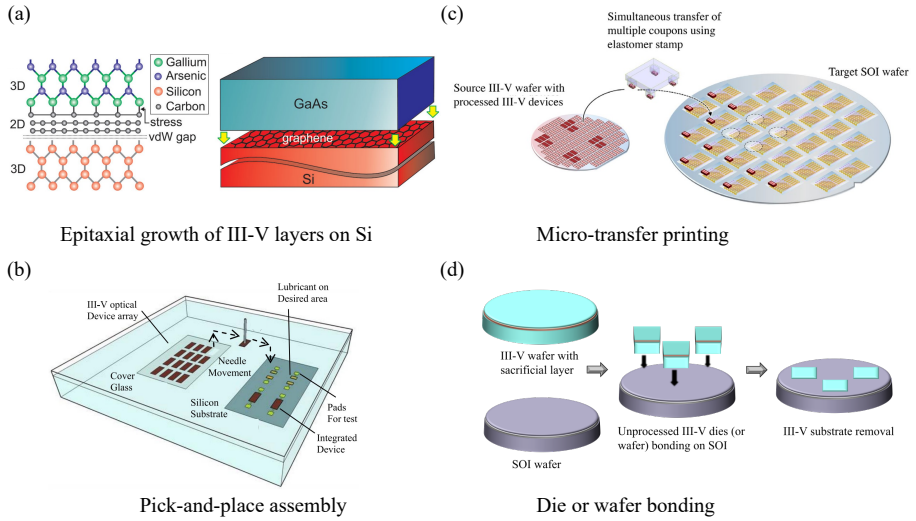


Figure 1.7: Main approaches for III-V-on-Si hybrid integration. (a) Atomic geometry and schematic view of the epitaxial growth of GaAs on Si using a graphene buffer layer (adopted from [92]. (b) Transferring an array of III-V optical devices to a Si host substrate using the pick-and-place assembly technique (adopted from [96]). (c) Simultaneous micro-transfer printing of multiple III-V pre-fabricated devices to Si (adopted from [99]). (d) III-V wafer with a sacrificial layer (to be removed for the lift-off removal of the III-V substrat) bonded on a Si-based wafer. After substrate removal, the transferred III-V membrane is processed to fabricate optical devices.

There are many examples of III-V devices integrated on Si-based platforms employing direct (or surface activated) [100, 101] and adhesive [102] bonding technologies. Both approaches are schematically outlined in figure 1.8. Figure 1.8 (a) shows surface-activated bonding, in which the wafer top surface, after cleaning, is treated either by plasma activation or by sputtering of different atoms. Then, the two surfaces come together for bonding; usually, high-temperature annealing is required at this step. Finally, the III-V backside substrate is typically removed by wet etching or by lift-off

using the sacrificial layer. For the adhesive bonding depicted in figure 1.8 (b), after cleaning the top surfaces, a thin layer of adhesive polymer is spin-coated. Finally, after bonding, the substrate is removed.

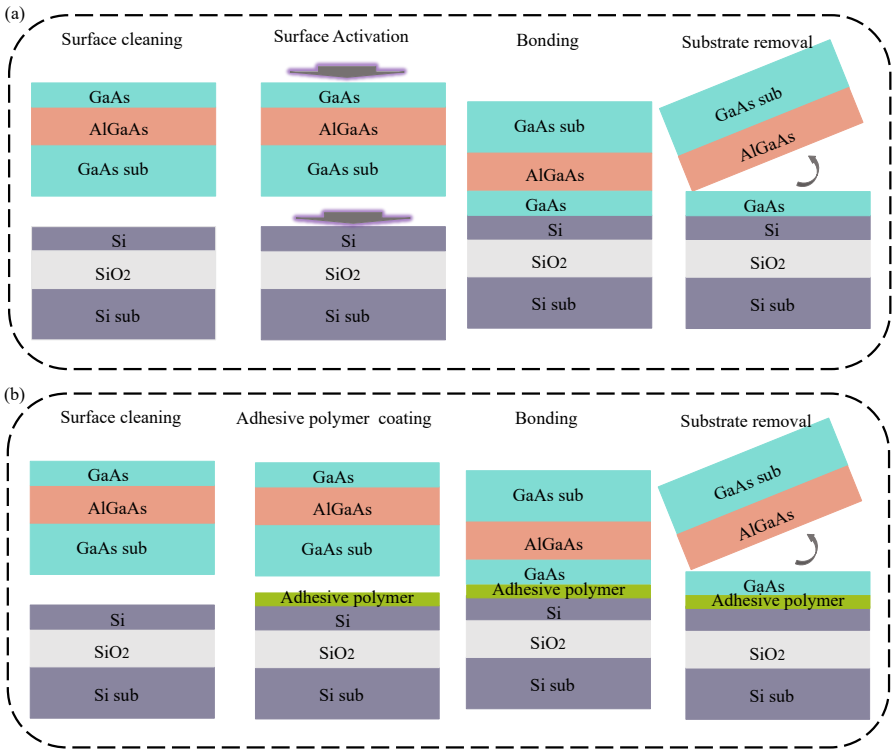


Figure 1.8: Outline of (a) surface activated direct bonding and (b) adhesive bonding.

Divinylsiloxane-benzocyclobutene (DVS-BCB) and Microresist GmbH (mr-DWL) are the most popular materials for adhesive bonding. A thin layer of the adhesive polymer is applied to at least one of the two mating wafers (or dies), followed by polymer annealing or ultraviolet light to strengthen the bonding. The great advantage of adhesive bonding over direct bonding is its lower temperature condition, which makes it suitable for photonic circuit integration and CMOS integrated devices. Another major advantage is that the adhesive polymer is typically soft and deformable; therefore, it can easily flow and compensate for the probable microvoids. On the other hand, as the thickness of this layer is adjustable, a sufficiently thick adhesive layer can be used to planarize the surface. In the wafer bonding technique, a III-V wafer including the QD layer near the top surface is flipped and bonded to a target photonic wafer. Therefore,

the two high-quality surfaces can be interfaced with a thin bonding layer between them. This enables us to configure a variety of comlicated photonic and electronic structures using nano-lithography techniques. The most favorable feature is to couple the quantum emitters emission to the underlying photonic circuits. The wafer bonding technique offers a scalable, cost-effective method for heterogeneous integration, as it does not require any complicated equipment for the alignment between the III-V device and the structure on the target wafer. Moreover, it allows for design flexibility. Because the III-V components will be fabricated directly on the hybrid III-V-on-Si substrate, more complicated components can be fabricated. However, because the bonding procedure is very sensitive to contamination and surficial defects, there are also some cons such as process complexity and yield and reliability challenges.We will return to the wafer bonding method in more detail in the next chapter.

1.6 Integration of single-photon sources on PICs (state-of-the-art)

Currently, there is excellent progress in developing suspended GaAs single-photon sources with high purity and indistinguishability [51], which, however, requires more advanced designs and fabrication methods to avoid collapsing the waveguides on the substrate (e.g. by using thin tethers or supporting ribs [103, 104]). Transferring the GaAs membrane on a low-index substrate offers a promising alternative as it maintains high photon-emitter coupling efficiency without compromising device complexity [17]. The realization of advanced photonic systems-on-chip requires the integration of III-V light sources directly on silicon photonics integrated circuits to take advantage of both efficient III-V sources and mature SOI platforms [65].

Recently, the integration of single photon sources on different PIC platforms has been explored. Employing flip-chip bonding, the detection of non-classical light integrated to Si and Aluminum nitride (AlN) has been shown [105]. Integration of single-photon sources to Si_3N_4 waveguides using pick-and-place assembly has been widely studied [64, 72]. Using this method, the emission of QD triggered single-photons into an ultra low loss Si_3N_4 waveguide has been reported in [64], second-order correlation measurements show multiphoton emission probability as low as $g^2(0)) < 0.1$. Integration of III-V waveguides with embedded InAs/InP QDs, which act like a telecom-wavelength single-photon emitter, onto a silicon waveguide, using pick-and-place technique has been studied in [72]. The coupling of the emitted single-photons into the underneath Si waveguide could be achieved by tapering down the III-V nanobeam waveguide. By sending a 785-nm pulsed laser, $g^2(0)) = 0.25$ has been measured, which is below the classical limit of 0.5.

A lot of investigation for the transfer printing of InAs/GaAs quantum dot single photon

source into silicon-based waveguides [98] and Si_3N_4 waveguides [106] has been published. An InAs/GaAs QD single photon sources has been trasfer-printed into a silicon waveguide in [98]. The coupling of single photons generated from the QD integrated on chip into the silicon waveguide has been experimentally measured, with $g^2(0)) = 0.3$. In [106] pre-selected nanowires-based QD emitters with directional emission has been transferred onto Si_3N_4 waveguides, where the coupling efficiency of 24% from the emitter to waveguide has been measured. High single-photon Fock-state purity has been ensured by measuring $g^2(0)) = 0.07 \pm 0.07$. Another method for heterogeneous integration of III-V single-photon emitters to si-based PICs, that has received much attention recently, is wafer bonding. In [107], using bonding technique, GaAs devices containing positioned QDs are fabricated on top of a SiO_2 box with embedded Si_3N_4 waveguides. Using mode transformers, deterministic single photons, emitted from a single QD in the GaAs nanowaveguide, has been coupled directly into a Si_3N_4 waveguide. with p-shell excitation using a contineous wave free space laser tuned at 904nm, $g^2(0)) = 0.11$ has been demonstrated. In another investigation in [108], after bonding GaAs membrane on top of the Si_3N_4 chip, GaAs micro-ringresonator and bus waveguides could be fabricated on top of the Si_3N_4 waveguides with sub-50 nm alignmen accuracy, defined strictly by e-beam lithography. The measured $g^2(0)) = 0.28 \pm 0.01$, indicateds that the cavity-coupled QD acts as a single-photon source.

1.7 Objectives and overview

This thesis introduces a method for the integration of a whole unprocessed GaAs membrane with embedded self-assembled quantum dots (QDs) on a silicon(Si)/silicon-dioxide(SiO_2) chip based on die-to-die bonding. Post-fabrication of the nanostructures on the transferred GaAs membrane provides a precise alignment to the underneath circuit, without the need for advanced high-resolution equipment for bonding. The objective of this thesis is to fabricate GaAs waveguide circuits on this hybrid substrate and perform optical characterizations. The overall goal is to propose a suitable and cost-efficient method for the fabrication and integration of quantum emitters with different platforms, such as the SOI.

Structure of the thesis

Chapter 1 served to give a brief overview of the photonic integrated circuits and the need for integration of optical sources like quantum dot single photon sources. The second part then dealed with introducing the most common methods for heterogeneous integration. Finally, there was a look at QD nanophotonic devices integrated with silicon-based platforms that is the foundation of this thesis (state-of-the-art). *Chapter 2*

provides a detailed description of the fabrication steps used for III-V on Si die-to-die bonding, and the utilized fabrication techniques of quantum nanophotonic devices in the hybrid GaAs-on-Si substrate. *Chapter 3* describes the experimental setup employed for the optical characterizations of the fabricated photonic nanostructures in this thesis. *Chapter 4* presents the optical characterization and the measurement results of the concentric waveguides and nanobeam waveguides fabricated on the hybrid GaAs-on-Si substrate. *Chapter 5* introduces a novel additive method for GaAs nanostructures fabricated aligned to the underlying Si_3N_4 waveguides. The coupling between material layers has been investigated by slowly tapering the width of the GaAs waveguide. In the last part, Light transmission measurements have been studied. *Chapter 6* discusses micro-transfer printing, which is another approach for integrating III-V materials on Si-based platforms. GaAs nanobeam waveguides micro-transfer printed on top of low-loss Si_3N_4 waveguides, in collaboration with Ghent university. Optical transmission and coupling efficiency have been investigated. *Chapter 7* summarizes the work carried out in this thesis, and an outlook toward future work for the realization of integrating single photon sources with metal contacts on Si-based platforms.

CHAPTER 2

Fabrication of heterogeneously integrated single-photon emitters

In this chapter, a detailed overview of the fabrication steps required to fabricate quantum photonic nano-devices on a hybrid III-V/Si substrate will be given. First, we discuss the transfer of the GaAs thin membrane with embedded quantum dots on a Si-based substrate via adhesive bonding. Next, we investigate the removal of the backside GaAs substrate in a series of wet etching in different acids. Subsequently, a description of the fabrication techniques of quantum nanophotonic devices on the transferred GaAs membranes is provided. Finally, we have characterized the quality of the fabricated devices using a set of scanning electron microscope (SEM) and atomic force microscope (AFM) scans on different parts of the chip.

In the heterogeneous integration of semiconductor devices using adhesive bonding method, one of the most challenging aspects is the choice of the material as the adhesive layer. To survive the fabrication process, the material in the adhesive layer needs to have a good wet and dry etch stability. Moreover, high thermal stability is required, when performing optical measurements. The adhesive layer must be capable of withstanding around 300 K temperature change when cooled down. In this study, we have used a cryo-compatible and transparent photo-resist polymer (Microresist mr-DWL 5) as the adhesive bonding layer. Some parts in this chapter are reproduced from [27].

2.1 General layout of the III-V on Si nano-devices

A schematic cross-section of the main steps required for the fabrication of the III–V-on-silicon waveguide structure using the adhesive bonding technique is depicted in figure 2.1. Here, we briefly describe the entire procedure, which will be discussed in more detail later in this chapter. The procedure starts by bonding the two Si and GaAs dies together. The bonding step consists of careful cleaning of the two wafers, finding the practical thickness for the adhesive layer and spin-coating it on one of the dies, joining the surfaces of the two dies, and baking the bonded dies under pressure to strengthen the bonding. Here, we used a thin layer ($\approx$ 160 nm) of diluted mr-DWL (Microresist Gmbh) resist (1:3 with $\gamma - But yrolactone$) on the SiO_2 sample as the adhesive polymer. Once we have the two dies bonded together, to be able to process the GaAs active layer and fabricate the III-V nano-structures, the thick GaAs backside substrate, which is on top now, needs to be removed along with the AlGaAs sacrificial layer. The GaAs substrate and the AlGaAs layer have been removed via a series of wet etching steps in different acids. Finally, when the GaAs membrane with embedded QDs has been successfully transferred onto the SiO_2 die, the fabrication of the III-V nanostructures begins. This consists of several series of e-beam lithography followed by reactive-ion-etching (RIE). Each step is studied in more detail in the following sections of this chapter.

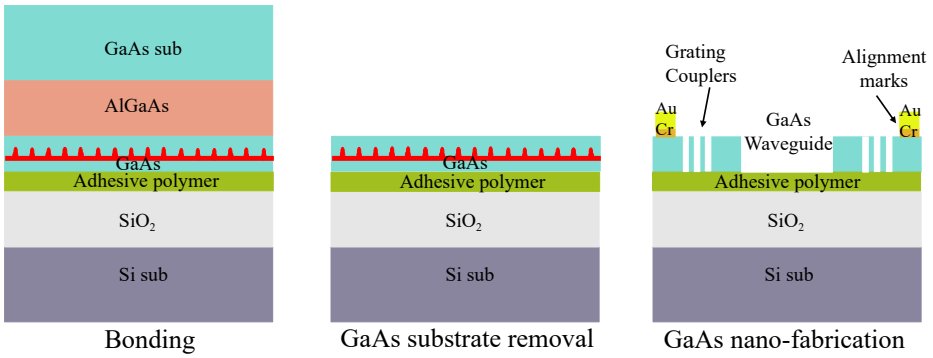


Figure 2.1: Schematic illustration of the required main steps for the fabrication of III-V-on-Si nanostructures.

2.2 Adhesive Bonding

Wafer bonding is a popular method for integrating III-V and Si-based wafers. In this method, an unpatterned III-V die or wafer is bonded to a Si-based chip (which can have some embedded circuits and waveguides), either by interfacial bonds (direct) or

using a polymer between the two dies, which acts as a glue (adhesive). The bonded dies will be further processed to fabricate the desired III-V component, usually a laser or a single-photon emitter, integrated on a Si-based ship [100]. Direct bonding mainly relies on van der Waals bonds between the atomically flat surfaces of III-V and Si dies to adhere them without the need for any intermediate layer. For direct bonding, precise surface preparation is required, which involves several steps of chemical cleaning and surface planarization and activation to ensure strong and reliable bonds [109]. Although direct wafer bonding offers high bond strength, it is very demanding in terms of surface preparation. Moreover, it requires high-temperature annealing, which is undesirable in many applications. Adhesive wafer bonding, on the other hand, is a promising alternative approach that uses an intermediate adhesive layer (usually a polymer) as the bonding agent. Compared with direct bonding, adhesive bonding offers some significant advantages and will be used in this work. Surface cleaning and preparation is still essential for adhesive bonding, but it is less demanding than the direct approach because the intermediate adhesive layer can compensate for some of the surface imperfections. Another advantage of adhesive bonding is its lower temperature conditions during fabrication, which makes it suitable for applications in photonic integrated circuits (PICs) and together with CMOS integrated devices. Moverover, adhesive bonding method for heterogeneous integration is not very material dependant. Transferring GaAs membrane with embedded QDs on a silica layer, paves the way for its integration also with a variety of other powerful material systems, such as lithium niobate thin films [74, 110] and low-loss silicon nitride waveguides [106, 111, 112].

2.2.1 Preparation of the samples

Successful bonding requires meticulous surface cleaning to avoid any nanoscale dirt that can prevent uniform adhesion between surfaces. In this work, the III-V wafer is grown by MBE on a 630 µm-thick GaAs substrate. It contains a 1371 nm-thick $Al_{0.75}Ga_{0.25}$ As sacrificial layer and a 160 nm-thick GaAs membrane with a layer of self-assembled QDs in the center, as shown in figure 1.5 (b), where we cleaved it in $\sim 8 \times 8$ mm^2 dies. All GaAs wafers used in this thesis are grown by Dr. Arne Ludwig and colleagues at the University of Bochum, Germany. The target wafer is a Si substrate with a thermally-grown 1000 nm-thick SiO_2 layer cleaved in $\sim 10 \times 10$ mm^2 dies. SiO_2 is a versatile material compatible with many material systems such as silicon nitride and lithium niobate. Hence, the integration of GaAs waveguide circuits on a SiO_2 layer is a very important step that can pave the way to scalable quantum PICs. To clean the dies, the protective resist on their surface is removed by sonication in acetone and isopropyl

alcohol (IPA), respectively, followed by sonication in millipore (MQ) water. Finally, nitrogen (N_2) blow drying followed by dehydration bake for 5 min at 185 °C on hotplate.

2.2.2 Bonding

An optically-transparent cryo-compatible polymer (mr-DWL 5, from Microresist GmbH) is used as the intermediate adhesive layer for ensuring uniform bonding between the two surfaces. The adhesive is diluted in a $\gamma - Butyrolactone : mr - DWL(1:3)$ solution prior to spin-coating on the SiO_2 surface, resulting in a 160 nm-thick layer. Now, both dies can be brought into contact by flipping the GaAs die and placing it upside down on the $\gamma - Butyrolactone : mr - DWL(1:3)$ coated SiO_2 die, figure 2.3 (a). As the SiO_2 die is slightly larger, this placement can be manually centered without much difficulty. To strengthen the bonding, the polymer is placed on a hotplate at 60 °C while applying gentle pressure ($\sim$ 7.5 N/cm^2) from the top and baked by gradually increasing the temperature to 140 °C for approximately 45 min. Afterwards, the sample is removed from the hotplate to slowly cool down and finalize the bonding process. Now, we have a SiO_2 sample bonded to a GaAs die, as shown in figure 2.2 (a). Figure 2.2 (b) shows an SEM image of the bonded sample, from an angled view, where a thin mr-DWL bonding layer between the SiO_2 and the GaAs wafer can be observed.

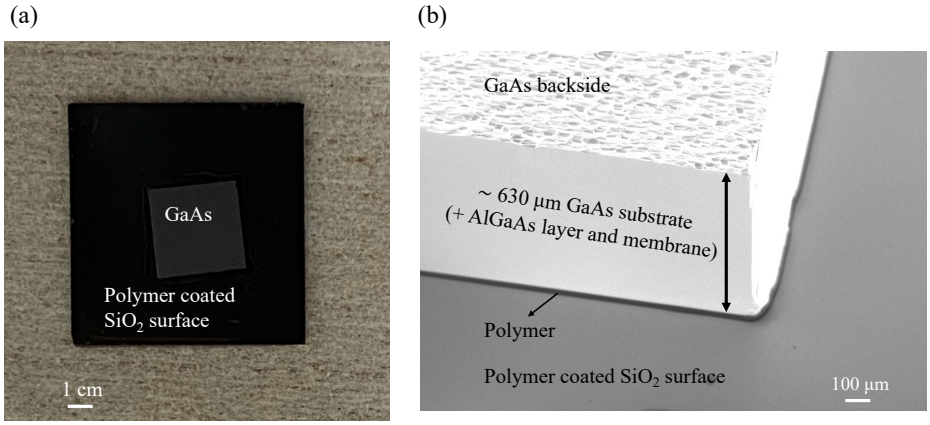


Figure 2.2: (a) Top view photograph of GaAs die bonded on an SiO_2 sample, . (b) An angled view SEM image of the bonded sample, showing the thin polymer layer in between the two bonded dies.

2.2.3 Substrate removal (wet etching)

After completing the bonding, to fabricate GaAs-based nanodevices on this hybrid substrate, the backside GaAs substrate and the AlGaAs sacrificial layer must be removed.

There are different possible ways available to remove the backside GaAs substrate. Mechanical grinding to remove the GaAs substrate or make it thinner is not very favorable because it is a toxic material and there is the risk of contamination. Another approach is to epitaxially lift-off the backside substrate by designing an appropriate mask to etch the $Al_{0.75}Ga_{0.25}As$ sacrificial layer. This method is not working for this sample because of the low concentration of aluminum in the $Al_{0.75}Ga_{0.25}As$ layer. In this work, backside GaAs substrate removal is performed by a series of wet etching processes in different acids, an overview of which is presented in figure 2.3 (b-d). First, the 630 µm-thick GaAs substrate, which is now located on top, is chemically etched in two steps [113]. A fast and non-selective wet etching process in a nitric acid solution ($1HNO_3$:$4H_2O_2$:$1H_2O$), followed by a slower etch in an ammonia-based solution ($1NH_4OH$:$19H_2O_2$), which is selective to AlGaAs. Then, the remaining AlGaAs sacrificial layer, which acted as an etch-stop layer in the previous etching step, is removed in cold hydrochloric acid. Figure 2.3, schematically illustrates the bonding and etching process flow.

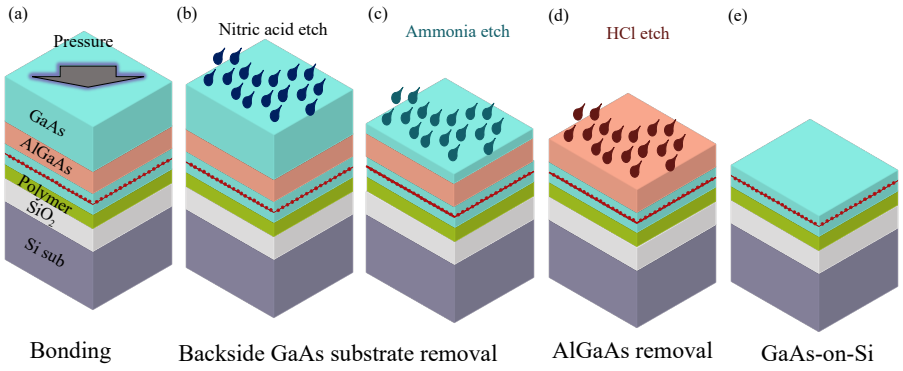


Figure 2.3: Schematic illustration of the required steps for transferring the GaAs membrane with embedded QDs on top of an SiO_2 chip. (a) Bonding step, interfacing the two dies with an adhesive layer in between and under pressure. (b) First wet etching process, which thins down the GaAs substrate. (c) Second selective wet etching process, which completely removes the backside substrate. (d) Sacrificial layer removal. (a) The GaAs membrane transferred on an an SiO_2 chip.

- **Nitric acid etch**
  The major part of the 630 µm-thick GaAs substrate is removed in a solution of $1HNO_3$:$4H_2O_2$:$1H_2O$. This etch solution has an average etching rate of ~ 5 $\mu m/min$ at room temperature [114] and etches GaAs relatively quickly compared with other candidates such as citric acid peroxide. Here, we need to consider that etching GaAs in this solution for a long time generates non-uniformity

across the sample, typically around 30 µm. As the etchant is not selective, it is important to manually stop the etching process, while we are still sure more 30 µm of the GaAs substrate is left. In this work we etched the bonded sample in this nitric acid-based solution for 115 min, which etches around 570 µm of the whole 630 µm-thick GaAs substrate. Therefore, we are sure there is still ~ 50 µm GaAs left (also double-checked by SEM), figure 2.3 (b). After completing the nitric acid-based etching and before going to the ammonia solution, it is essential to rinse the sample thoroughly. Otherwise, the reaction between the nitric acid residue and the ammonia-based etchant that follows, gives rise to the formation of "grass" on the sample, which is impossible to remove. A typical image of this, taken by optical microscope is presented in figure 2.4 (a). So, after removal from the nitric solution, we rinsed the sample in two separate beakers of MQ water, each one for at least 4 min.

- **Ammonia etch**
  To remove the ~ 50 µm remainder of the GaAs substrate a good selectivity to the etch stop layer (in our case the $Al_{0.75}Ga_{0.25}As$ layer) is required. We removed it in an etch solution of $1NH_4OH{:}19H_2O_2$, while stirring the solution for the entire time. This ammonia-based solution is selective to $Al_{0.75}Ga_{0.25}As$ with a high accuracy, and the etching rate is around 3 µm/*min*, but it slows down over time. Therefore, we use this solution to etch only the last 50 µm of the GaAs. Because the etch rate varies over time, we cannot rely on timing. To determine when the etching process is completed, we rely on the color change. The GaAs usually looks shiny gray during the etch process, however, the appearance of an approximately reddish color indicates that the $Al_{0.75}Ga_{0.25}As$ layer has been reached, figure 2.3 (c). Typically, this discoloration starts from one corner of the sample and gradually over time spreads over the whole sample. When the gray area is completely changed into a colorful area, the sample is kept in the solution for a few more minutes to ensure that no GaAs residue is left (typically it takes around 30 min). After completing this step, we clean the sample by rinsing it in two separate beakers of MQ water, each for 4 min. During etching, the total GaAs chip size laterally shrinks. This shows that the acid is etching the GaAs not only from the top surface, but it also etches it from the side walls. An optical microscope image of the bonded sample after removing the backside substrate is presented in figure 2.4 (b), where the GaAs chip has been shrunk approximately 1 cm from each side. One way to protect the sidewalls during the etching process, is to apply a protective layer around the edges of the GaAs chip before starting to etch. One good candidate would be a wax called "CrystalBond509". This wax has

a strong adhesion to the edges and exhibits high chemical resistance, moreover, after completing the etching process, it can be easily dissolved in acetone. We did not use this technique in the work presented in this thesis, as sample shrinkage was not the main issue at this step of the project, but it will be used in the future works.

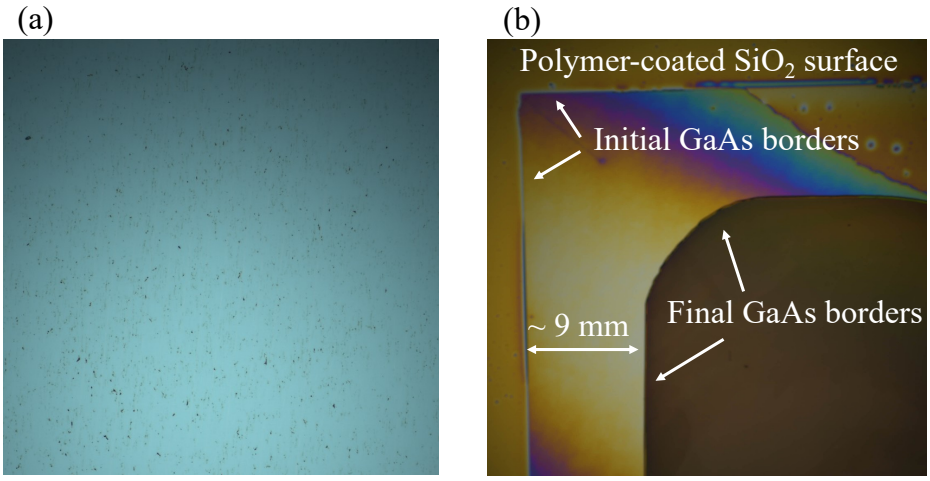


Figure 2.4: (a) Unwanted grass formation as a result of the chemical reaction between the nitricacid-based residue and the ammonia-based etch solution. (b) Microscope image of the bonded sample after substrate removal. The bonded GaAs die shrinks in the acid, approximately 1 cm in each side.

- **Etch-stop layer removal**
  When the GaAs backside substrate is completely removed, we begin removing the 1371 nm-thick $Al_{0.75}Ga_{0.25}As$ sacrificial layer, which was acting as the etch-stop layer in the previous step. It is selectively removed by immersing it in cold hydrochloric acid (HCl 2 °C) to avoid damaging the underlying SiO_2 layer, figure 2.3 (d). During this step, the surface starts to get shiny gray again, which means that the GaAs membrane has been reached, figure 2.3 (e). As the final step, we clean the surface in MQ water.

Having the GaAs membrane successfully transferred on the SiO_2, now we can start the fabrication process of the photonic nanostructures on this hybrid substrate.

2.3 Nano-fabrication of quantum photonic devices

The fabrication of quantum photonic nano-devices on a silicon-based substrate is an important step forward towards a fully scalable and hybrid QPIC technology. Suc-

cessful III-V membrane transfer on a silica layer using adhesive bonding, is a very promising method for integration of quantum light sources, like single-photon sources and quantum lasers, on a different host substrate like Si_3N_4 and $LiNbO_3$. To achieve this, there are several important main steps and requirements. One essential requirement is having high-quality MBE grown III-V material with embedded QDs, which in this thesis is provided by our collaborators in University of Bochum, Germany. In addition to bonding and backside substrate removal, which are explained in the previous sections, a set of reliable nanofabrication techniques is required. The devices implemented in this project are fabricated on a GaAs membrane with embedded self-assembled QDs, transferred on an SiO_2 layer using an adhesive bonding technique, for which the layout of the layer structure is illustrated in figure 2.3 (e). Photonic nanostructures are fabricated on the membrane following the same procedure used for suspended GaAs waveguides, as described in [52].
After successful transferring of the membrane, the complete process flow for the fabrication of nanostructures implemented in this project consists of three main steps: definition of alignment markers, shallow etching of the grating couplers, and deep etching and definition of GaAs waveguides. To complete each of these steps, a series of standard nanofabrication techniques are required. Electron-beam lithography for patterning the nano structures, metal deposition deposition for the definition of alignment marks, and dry etching of the patterns. These fabrication techniques used to fabricate nanostructures in this thesis, are explained in the following in this chapter. Before starting the fabrication procedure, we need to design a mask that consists all of our required structures, like alignment marks, waveguides and photonic crystals. In this chapter we are investigating fabrication of quantum nanostructures on a bulk silica layer, while in chapter 5 we introduce a method to fabricate GaAs nanostructures aligned to the underlying Si_3N_4 waveguides. The mask and the required steps are different for these two different fabricated samples. Here the deailed steps for fabricating on bulk silica layer is discussed.

2.3.1 Mask design

The first step in fabricating nanostructures is to carefully design the lithographic mask, considering separate layers for each of the steps stated above. MATLAB written codes are utilized to draw different circuit masks. Figure 2.5 (a) shows an image of the full mask layout implemented in this work, where the series of cross marks at the four edges of the mask are to be used for alignment in each step. Figures 2.5 (b-d) are zooming out some of the structures in the mask. Figure 2.5 (b) illustrates some concentric waveguides, which are designed to be completely the same and the only

difference is in their length, so they can be used to determine the propagation loss per unit length in this hybrid GaAs-on-SiO_2 substrate. The waveguides are designed to support the propagation of a single guided transverse electric (TE) mode. A photonic crystal waveguide has been shown in figure 2.5 (c), to test the ability of this fabrication method to define very small features like photonic crystals. Figure 2.5 (d) depicts a nanobeam waveguide with input and output grating couplers, where we tried to find and excite QDs in this type of waveguides.

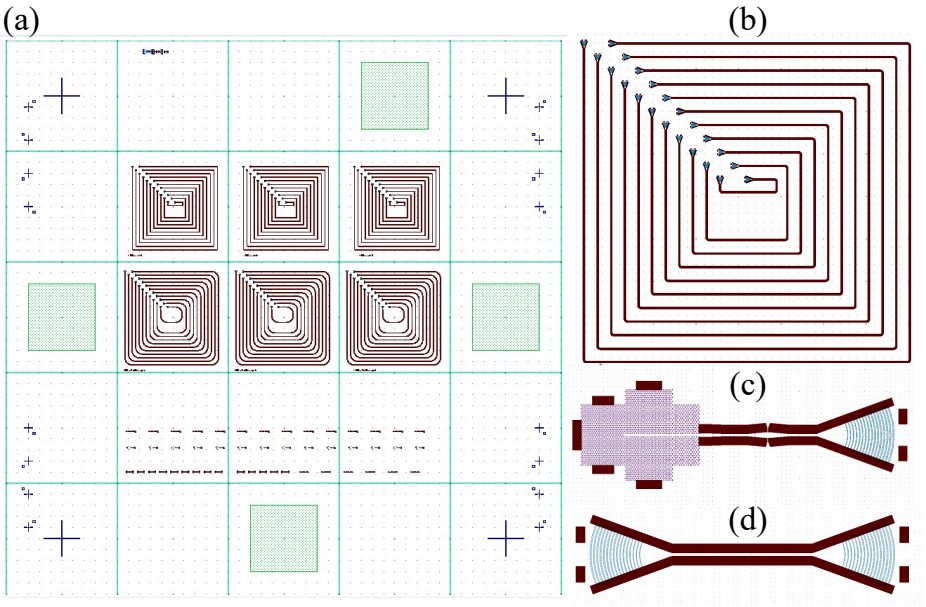


Figure 2.5: The full mask layout implemented in this work, contaning alignment marks, monitoring squares, concentric waveguides, photonic crystal waveguides, and nano beam waveguides. (b) Several concentric waveguides with different lengths to measure the waveguide loss by lithographic cut-back method. (c) Photonic crystal waveguides with one output focusing grating coupler. (d) Short nanobeam waveguides with two input/output focusing grating couplers.

Before starting fabrication in the cleanroom and the first exposure step, we need to prepare an exposure file based on this mask with a series of corrections to appropriately adjust the exposure conditions, such as the exposure time and dose. There are some possible sources of errors, like stitching and proximity effect, that we should try to minimize to obtain the ideal pattern out of the designed mask after the exposure process. Stitching errors arise from moving the stage during e-beam writing. We designed the layout accordingly and minimized the stitching field position error by trying to completely fit each individual structure in one writing field (green checkers in figure 2.5 (a)). The proximity effect results from the additional exposure due to backscattering

of the e-beam, which broadens the effective exposure area and increases the feature sizes compared with the mask. To minimize this effect, we apply a proximity effect correction. In this project, we calibrated the exposure dose using Beamfox Proximity, a detailed description of which can be found in [115].

2.3.2 Electron-beam lithography

Electron beam lithography (EBL) is a high-resolution nanofabrication technique (down to nm-scale) that is used to transfer the designed patterns from the mask to the sample surface. For EBL, the sample needs to be coated with a layer of resist material, which is sensitive to electrons. During EBL, a beam of electrons interacts with the resist layer on top of the sample and chemically changes it. Electron-resists are categorized into two groups of positive resists and negative resists. After e-beam exposure, the sample must be developed to reveal the patterned structures. In positive electron resists, the polymer exposed to electrons becomes more soluble and is removed during development. For negative electron resists, the opposite is true, meaning that the polymer in the exposed areas cross-links and remains after development. In this work we use the Elionix ELS-F125 e-beam lithography tool with an acceleration voltage of $V_{acc} = 125\,\text{keV}$, enabling the exposure of smaller feature sizes. After spin-coating the appropriate e-beam resist and having the mask files ready, the sample is loaded into the loading chamber of the Elionix ELS-F125 and will be transferred to the main chamber manually and using a rod. Then, using a computer, we can set all the settings and start e-beam exposure. Following exposure, an appropriate development be performed according to the resist used. Then, the sample is ready to serve as a mask for further processing in the next steps

2.3.3 Metal deposition

Metal deposition refers to the use of various techniques to deposit a thin layer of metal onto a substrate. Here we use the electron beam evaporation technique to form a thin layer of metal on the sample surface and then define the alignment marks. In electron beam evaporation, the metal deposition process occurs in a vacuum chamber. An electron gun, consisting a filament that emits electrons and an anode that accelerates the emitted electrons is used to generate a beam of highly focused electrons. There are different metal sources in a solid form, like crucibles, present in the chamber, towards which the electron beam is directed. The high-energy electron beam strikes the metal source, causing it to evaporate and release metal atoms in form of vapor. Using a holder, the surface to be coated is placed in the path of the evaporated metal vapors. The metal atoms, when hitting the surface, condense and form a thin layer. The deposition rate

and thickness can be adjusted by controlling the intensity of the electron beams and the duration of the process. In this work, in the first fabrication step after transferring the GaAs membrane on top of an SiO_2 chip (figure 2.6 (a)), we use a lift-off technique to define alignment marks. To do so, we first spin-coat the sample with a layer of a positive e-beam resist, ZEP520A (Zeon Europe GmbH), and pattern the marks using EBL, figure 2.6 (b,c). After room-temperature development (figure 2.6 (d)), the sample is ready to be mounted in the vacuum chamber of the metal evaporator. In the evaporator, we set a program to deposit 10 nm chromium (Cr) and 170 nm gold (Au), respectively (figure 2.6 (e)). These two metals have been chosen because apart from having good adhesion, they are compatible with the chemicals used in our fabrication process. Then, the sample is left in a 1,3-Dioxolane (I-III Diox) solution for 10 min, causing the resist to dissolve and lift off the metal in the unpatterned regions, figure 2.6 (f). Figure 2.6 (g) and (h) show a schematic cross-sectional view and a top-view optical microscope image of the sample with metal marks.

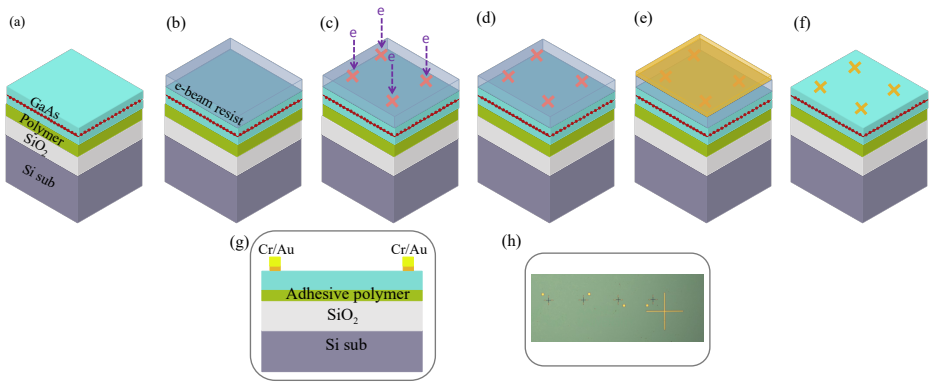


Figure 2.6: Schematic process flow for the fabrication of the alignment marks. (a) GaAs membrane transferred on a silica chip. (b) E-beam resist spin-coating. (c) E-beam lithography. (d) Room temperature development and O_2 plasma etching. (e) Metal deposition, depositing Cr/Au : 10 nm/170 nm. (f) Lift-off. (g) Schematic cross-section of the sample at this step. (h) Optical microscope image of the sample after defining alignment marks.

2.3.4 Dry Etching

Dry etching is one of the important semiconductor fabrication processes, that involves a combination of physical and chemical mechanisms to remove material from a substrate, in a patterned form. The two primary types of dry etching techniques are reactive ion etching (RIE) and inductively coupled plasma etching (ICP). Unlike wet etching, which relies on chemical reactions in a liquid solution, dry etching involves reactive gasses and plasma to isotropically etch vertical features and remove material. In this

work, to avoid excessive plasma damage to the underlying bonding resist, GaAs is etched by a slow and controlled reactive ion etching (RIE) in a BCl_3/Ar chemistry, using an Oxford Plasmalab 100 system. The dry etching process occurs in a vacuum chamber, where there is chemical interactions between the coming accelerated ions and the substrate surface, forming volatile compounds. Meanwhile, the sample is also physically bombarded with high-energy ionized reactive gas, which sputters away the reaction by-products. These result result in high-anisotropic and high-resolution etching of small vertical features with a good control over the etch depth. The four green squares in the mask (figure 2.5 (a)) are for the laser monitoring of the etch-depth during the etching process, according to calculations based on layer indices. A good accuracy of the etch-depth control using this method, has been confirmed by mechanical profile measurements (KLA Tencor Pro-filometer). Here, we use RIE to etch the transferred GaAs membrane after patterning, with two different etching depths. The process flow is mentioned below.

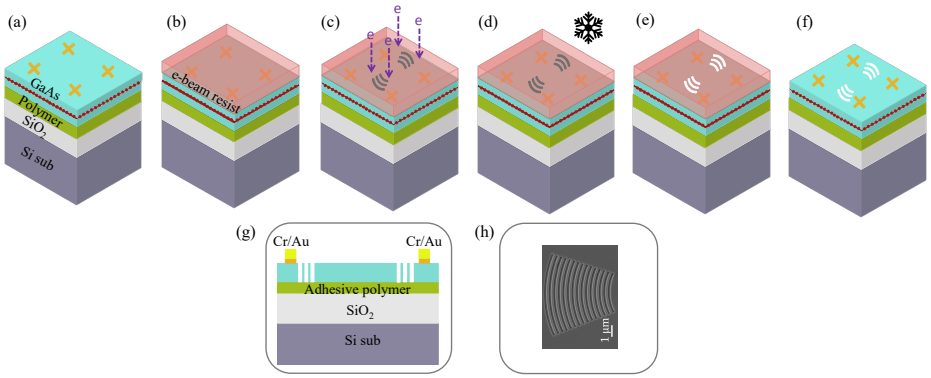


Figure 2.7: Schematic process flow for the fabrication of the shallow-etched gratings. (a) Sample with alignment marks from the previous step. (b) E-beam resist spin-coating. (c) e-beam lithography with respect to the alignment marks. (d) Cold temperature development. (e) Shallow etching of the gratings via RIE. (F) Removing the resist. (g) Schematic cross-section of the sample at this step. (h) Scanning electron microscope (SEM) image of the shallow-etched gratings.

The sample with metal alignment marks defined in the previous step (figure 2.7 (a)), is spin-coated with a positive e-beam resist CSAR 9 % followed by soft baking on a 185 °C-hot-plate for 1 min, figure 2.7 (b). Now, having the sample and the exposure mask ready, we do EBL of the grating couplers (figure 2.7 (c)), followed by cold development in −5 °C IPA for 20 s (figure 2.7 (d)). Now, we load the sample in the RIE machine loading chamber and guide it to the main chamber using a rod. We make sure to set the monitoring laser on the monitoring square on the sample, and satrt the etching process. In this work, during RIE the patterned sample is bombared with a mixed plasma of Cl_2

and BCl_3 gases diluted in argon, more details on the optimized RIE process used in this work can be found in [115]. To write grating couplers, we stop the etching procedure when about 90 nm of the GaAs membrane is etched, according to [116], figure 2.7 (e). As the final step in writing grating couplers, the resist is removed 80 °C N-Methyl-2-pyrrolidone (NMP) solution for 10 min, followed by rinse with IPA and N_2 blow dry (figure 2.7 (f)). Figure 2.7 (g) show the schematic cross-sectional view of the sample with metal marks and etched grating couplers. A top-view optical Scanning-electron microscope (SEM) image of the gratings is depicted in figure 2.7 (h).

To define GaAs waveguides, a similar process flow to the process explained above needs to be taken. The sample is again spin-coated with the positive e-beam resist (CSAR 9%), figure 2.8 (b). EBL with respect to the alignment marks (figure 2.8 (c)), followed by cold temperature development, figure 2.8 (d). The main difference from the previous step is in the RIE etching depth. To define GaAs waveguides, we etch through the whole membrane (a little more than 160 nm to be sure the whole membrane is gone at the waveguide area), figure 2.8(e). Finally, the resist is removed in hot-NMP, figure 2.8 (f). A schematic cross-sectional view of the final sample and an SEM image of the nanobeam waveguides fabricated on this hybrid GaAs-on-SiO_2 is presented in figure 2.7 (g) and (h), respectively. At this stage, the GaAs nanostructures could be successfully fabricated on the GaAs membrane adhesively bonded to a 10×10 mm^2-SiO_2 chip. To fit the sample inside our cryostat chamber for low-temperature measurements, as the very final step, we need to further cleave the final sample in smaller chips with 4×4 mm^2 dimensions.

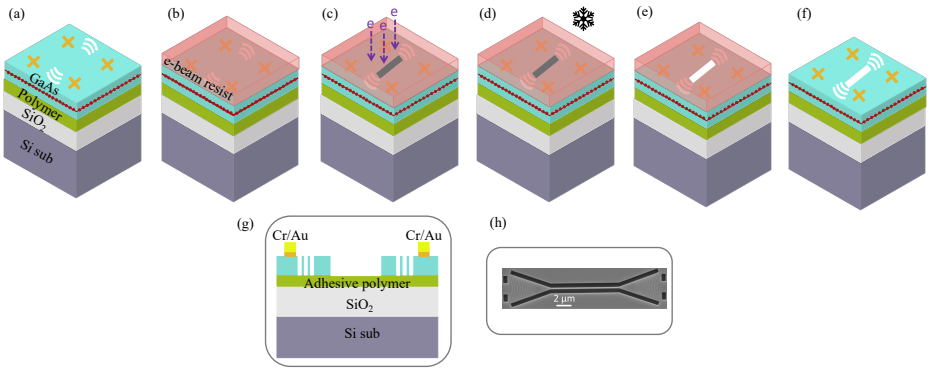


Figure 2.8: Schematic process flow for the fabrication of the GaAs waveguides. (a) Sample with alignment marks and the shallow-etched gratings from the previous step. (b) E-beam resist spin-coating. (c) e-beam lithography with respect to the alignment marks. (d) Cold temperature development. (e) Etching of the patterned area through the entire GaAs membrane. (F) Removing the resist. (g) Schematic cross-section of the sample at this step. (h) Scanning electron microscope (SEM) image of the nanobeam waveguides with two input/output grating couplers

2.4 Fabrication Results

In this chapter, we studied the fabrication process flow and the detailed steps to fabricate several designs of GaAs nanodevices, such as grating couplers, short nanobeam waveguides, concentric waveguides, and small features like photonic crystals on the hybrid GaAs-on-SiO_2 substrate. Figure 2.9 (a) illustrates the optical microscope image of the chip after final cleaving to fit in our cryostat chamber. Scanning electron microscope image have been taken on various parts of the chip to evaluate the quality of the outcome of this fabrication process. SEM images of the concentric waveguides (figure 2.9 (b)) and photonic crystal waveguides (figure 2.9 (c)) with zooming out of the grating couplers and photonic crystals (figure 2.9 (d) and (e), respectively) are presented. Moreover, we also performed atomic force microscope (AFM) scans to inspect the precise details of the structures and their etch depth. Figure 2.10 (a) and (b) present 3D topography images of the fabricated photonic crystals and the shallow-etched grating couplers, respectively, which are from the smallest features in the mask.

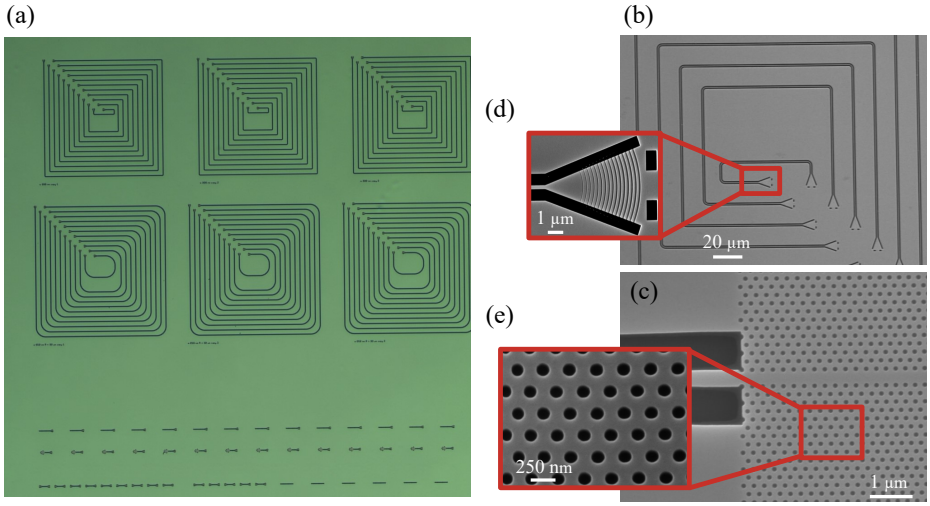


Figure 2.9: (a) Optical microscope image of the fabricated sample. Several different nano-devices have been fabricated on a hybrid GaAs-on-SiO_2 substrate. (b) SEM image of the concentric waveguides. (c) SEM image of the photonic crystal waveguides. (d) SEM image of the shallow-etched grating couplers. (e) SEM image of the photonic crystals.

We also analyzed the quality of the bending area in the concentric waveguides to ensure that they are not damaged or deformed during the fabrication process, figure 2.10 (c). In shallow-etched grating couplers, as can be observed in figure 2.10 (b), the etch depth reduces slightly on one side due to the RIE lag upon the gradual reduction

of the grating pitch, which reduces back-reflection and improves the collection spot shape [116]. To have a closer look, we scanned the shallow etched grating along its axis (red dashed-line in figure 2.10 (b)), and the etching depth is reported in figure 2.10 (d). The etch-depth scan in figure 2.10 (d) confirms that the shallow-etched gratings meet the desired size and etch depth previously reported for bulk GaAs nanofabrication, indicating that the presence of a different substrate does not visibly influence the lithography and dry etching steps. Moreover, from the AFM analysis on different parts of the sample, we observed that the surface root mean square (rms) roughness is 1.2 nm, which is comparable with previously reported values in GaAs after the removal of AlGaAs etch-stop layers [117].

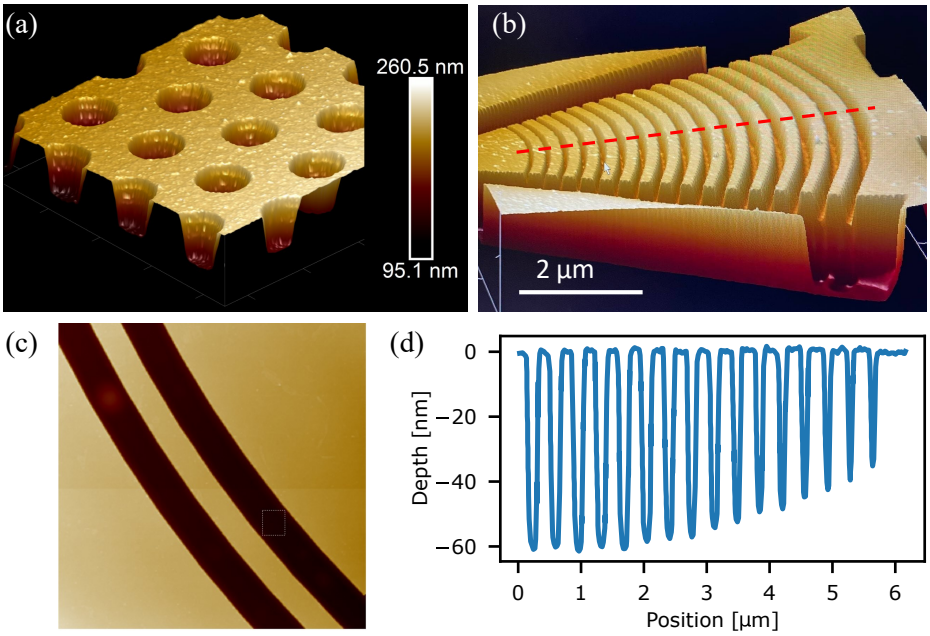


Figure 2.10: Sample AFM check. (a) 3D AFM image of the photonic crystals, showing that the small features could be successfully patterned and etched. (b) 3D AFM image of the shallow-etched grating couplers, showing a gradual decrease in the etch depth. (c) AFM image of the bending area in the concentric waveguides, confirming that they are fabricated as desired. (d) Etch depth measurement along the red dashed line in (c).

* * *

In conclusion, in this chapter, we reviewed nanofabrication techniques for manufacturing quantum photonic nanodevices in GaAs membranes with embedded QDs heterogeneously integrated on a silica layer. The optical characterization of this fabricated sample is presented in chapter 4 of this thesis. Yet, with approximately the same

fabrication process, GaAs tapered waveguides have been fabricated on top of some silicon nitride waveguides embedded in a silica box and coupled to it, which will be investigated in the following chapters.

Chapter 3

Experimental setup

In the previous chapter, we presented a detailed overview of the process flow for the fabrication of GaAs waveguides with embedded QDs heterogeneously integrated on a silica layer. To evaluate the optical performance of the fabricated devices, such as optical propagation loss and single-photon emission, it is essential to supplement the fabricated chip with an efficient and stable optical measurement setup. The optical experimental setup is as important as the nanophotonic device fabrication quality. Optimization of the measurement setup and finding ways to avoid losses and any additional noise, are crucial in the characterization of nanodevices. In this chapter, we describe the experimental setup employed for optical characterizations in this thesis.

3.1 Experimental setup

When working with QDs, it is important to suppress phonon noise by operating in a cold (< 10K) environment [118]. Therefore, for the optical characterizations in this thesis, we need a cryogenic system together with a stable vacuum chamber to hold the sample and some free-space optics to guide the input and output light. To do so, we used a liquid helium flow cryostat to cool the sample. This section is organized such that we start by presenting different input lasers, followed by introducing the cryostat, which is used to provide the cryogenic condition. Then, a detailed description of the optical setup implemented to direct and couple the light in and out of the chip. Finally, we provide an overview of the filtering and detection equipment.

3.1.1 Excitation laser

We primarily employed two types of lasers for the optical measurements in this thesis, as illustrated in the upper left corner of the figure 3.1. One is a supercontinuum laser source (SuperK EXTREME), as the input light for broadband characterizations, such as optical transmission and propagation loss measurements in concentric waveguides. The other is a pulsed laser diode (PLD), which emits short laser pulses. The PLD with 40 MHz repetition rate at 776 nm,is used as the input for the excitation of the QD and single-photon emission in the above-band excitation scheme, which is explained later in this chapter.

3.1.2 Liquid helium flow cryostat

To cool down the sample for precise optical measurements, we used a cryostat that uses liquid helium (He) as the cryogenic coolant. The sample is attached to a printed circuit board (PCB) and mounted on top of nanopositioners (XY) placed in the flow cryostat chamber (Microstat HireS II, Oxford Instruments), as seen in figure 3.1. The He-transfer tube, schematically illustrated in the lower right corner of the figure, is used to deliver liquid He to a heat exchanger close to the sample mount. The cryostat circulates the liquid He to cool and stabilize the temperature down to < 10K in just a few hours, which is cold enough to perform most of the QD characterization. To control the temperature of the sample, we used a temperature controller. This, together with a thermometer and a heater mounted on the heat exchanger, enables monitoring and balancing the cooling power of the cryostat and the temperature of the sample.

3.1.3 Optical setup

Figure 3.1 shows the experimental setup used for the optical characterizations in this work. The sample is placed on top of nanopositioners, enabling us to perform measurements from device to device by moving the stage around with respect to a fixed objective. Using a He-flow cryostat, a cryogenic condition is prepared for the sample to damp phonon noise while performing measurements. A closer look at the input and output paths is presented below.

As mentioned above, we used two different input lasers for different measurements in this thesis: supercontinuum and PLD. For each measurement, the appropriate excitation laser is coupled to an input fiber coupler, which collimates the laser with different beam diameters. The input beam is guided to the optical breadboard and propagates in the setup following the input path. Laser polarization is controlled by passing through a half-wave plate ($\lambda/2$) and a polarization beam splitter (PBS). Then, it reaches a 50:50 beam splitter (BS) whose reflection port is coupled to a power meter (PM) to monitor

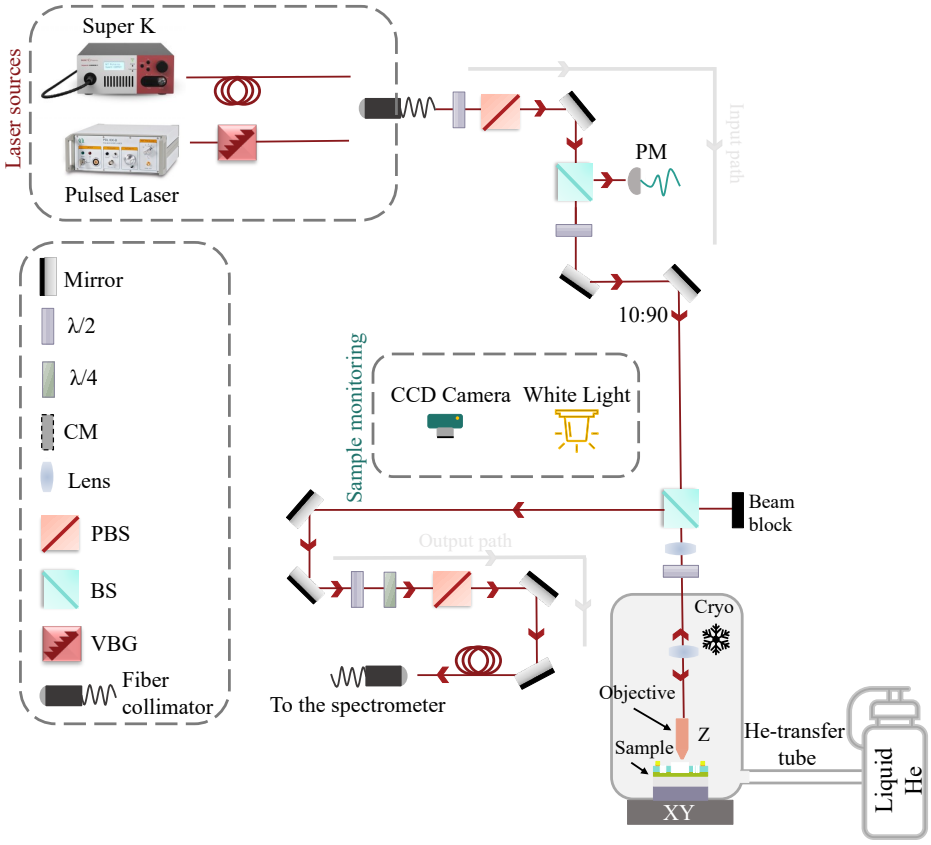


Figure 3.1: Schematic of the optical measurement setup. Upper-left, framed area showing the two possible input lasers that are sent, following the input path, through the optical components onto the sample. The sample is placed on XY nanopositioners in a chamber connected to the He-flow cryostat. The output signal from the sample propagates following the output path. For more details, see the main text. The dashed box on the left is a legend of the most used optical components.

the input power for reference. After passing through an additional half-wave plate, light is guided in the cryostat via a 10:90 beam splitter and is focused on the sample surface using an objective. Meanwhile, using the sample monitoring section in the figure, i.e., the CCD camera and white light, we can illuminate and image the sample whenever required. Using the imaging section, we align the input beam to the shallow etched grating and optimize the beam and its alignment to optical elements to obtain the best coupling into the nanodevices at our operating wavelength, around 950 nm.

The output from the shallow etched grating is coupled out of the cryo chamber through the same microscope objective, passing two lenses, and transmitted at the 10:90

beam splitter. Then, it propagated following the output path shown in figure 3.1. The output path contains a set of waveplates ($\lambda/2$ and $\lambda/4$) to control the light polarization and optimize the collection efficiency. Then, the beam reaches the polarization beam splitter, and after passing the two output mirrors, which are used to collimate light into the output fiber, it can be guided to the spectrometer (Oxford Instruments) for analysis. To monitor the device and for the alignment process, we used a white light source together with a CCD (charge-coupled device) camera, that are placed on the collection path to illuminate and image the sample.

3.2 Quantum dot excitation

In the previous sections, we discussed the general experimental setup used for the transmission measurements. However, experiments for QD excitation and single-photon emission require additional considerations, as explained below.

3.2.1 Quantum dot excitation schemes

In this thesis, we fabricated nanodevices on a GaAs membrane with embedded InAs QDs heterogeneously integrated on a silica substrate. Here, we discuss different available excitation schemes for the excitation of QDs and formation of excitons (electron-hole pairs). The three-dimensional confinement in the QDs results in discrete energy levels for excitons. Leading to the emission of only one photon per excitation, similar to atoms. In optical excitation, when the QD interacts with a photon with sufficient energy and absorbs it, an electron within the QD can be promoted from its ground state (valance band) to a higher energy level (conduction band), as schematically shown in figure 1.4 (a). The electron subsequently recombines with the hole via spontaneous emission, while emitting a photon with an energy (and hence wavelength) equal to the energy difference between CB and VB. Here we describe two main optical excitation schemes, which refer to the different energies at which excitons are created.
In resonant excitation, the absorbed photon has the same energy as the energy difference in the well, figure 3.2 (a). Here, unlike the above-band excitation, excitons are formed directly in the QD. Therefore, it is ideal for generating highly indistinguishable photons. As can be seen in figure 3.2 (c), there is only one prominent photon emission line, and the background from other transitions is prevented. In the resonant excitation of a QD, stark-tuning of the QD is desired, which means tuning the emission energy of the QD by applying a voltage [119]. However, electrical control is not possible in our work because we have transferred an undoped GaAs membrane, on which we cannot make metal contacts. Moreover, in this method, the excitation laser has the same frequency as the emitted single-photon, which makes it challenging to suppress it efficiently.

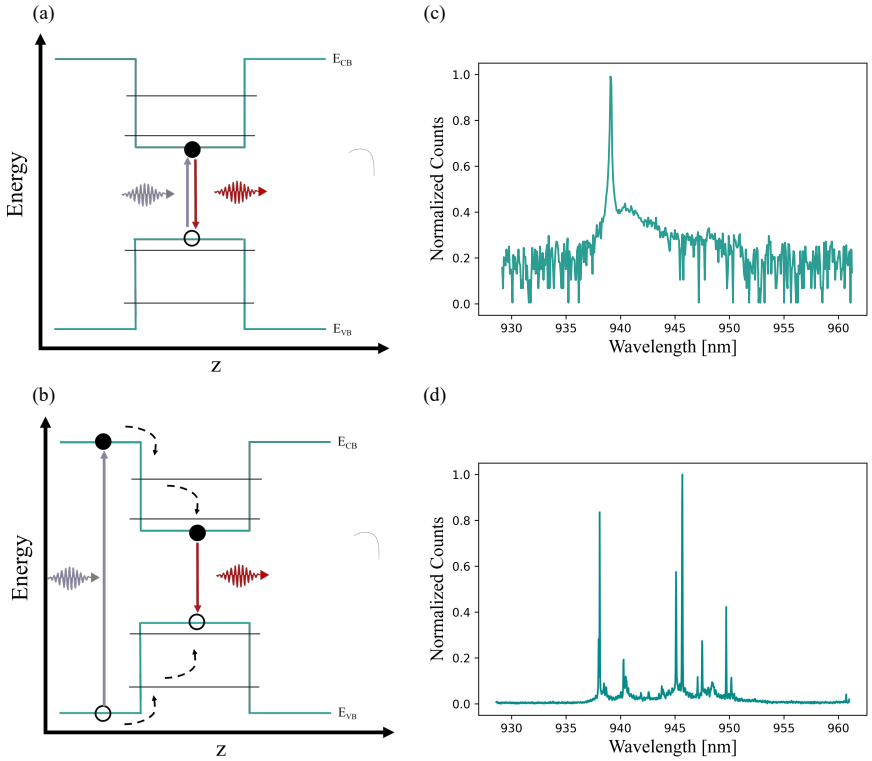


Figure 3.2: Two different schemes for QD excitation. Illustration of the process for creating excitons in QD using (a) resonant excitation, (b) above-band excitation. The corresponding spectra are shown in (c) measured by Ying Wang on a doped sample, (d) measured in this project.

Alternatively, the above-band excitation is also possible, when the input is a laser with an energy higher than the bandgap energy of GaAs, as shown in figure 3.2 (b). Here, after excitation, which occurs in bulk material, the excitons undergo relaxation simultaneously. Some excitons are then captured by the QDs and relax to the lowest unoccupied QD energy level. In this method, in each excitation, several different QDs will be excited, which leads to many transitions with different frequencies, figure 3.2 (d). In the above-band excitation, the energy difference between the excitation laser and the emitted photons, makes it easy to filter out the excitation laser and only see the emissions from QDs in the spectrum. However, with this excitation method, it is not possible to selectively excite one specific QD. Moreover, the relaxation process introduces some additional noise, which makes this excitation method undesirable when it comes to having indistinguishable photons.

In this work, to characterize the quality of the QDs after heterogeneous integration, we excited QDs and observed single-photon emission using the above-band excitation scheme, as presented in the next chapter.

3.2.2 Filtering equipment

We employ filters to suppress all spectral contributions that do not originate from an individual QD transition. Typically, these contributions could be from the excitation laser background, transitions in other nearby QDs, the phonon sideband, or the second dipole emission. Figure 3.3 (a) shows the grating filter used to extinguish the extra spectral contributions in this project. As shown in the figure, when the broad laser pulses reach this filter, it gets diffracted and different frequency components reflect off the grating at slightly different angles. With a larger beam diameter, we can ensure a higher spatial resolution between the different components. Hence, we use a beam expander, comprising a pair of lenses, before bringing the light to the grating. The diffracted beam is focused down to the spatially distributed spots of diffraction-limited size, using a large focus lens. Finally, the collimated beam is fiber-coupled into a NA_{fiber} = 0.13 fiber, with the rejection of undesired wavelength components. The filter is characterized when shone by a broad laser (Super K). The bandwidth of this setup for the grating filter is measured to be $\sim$ 0.2 nm, according to the transmitted spectrum presented in figure 3.3 (b).

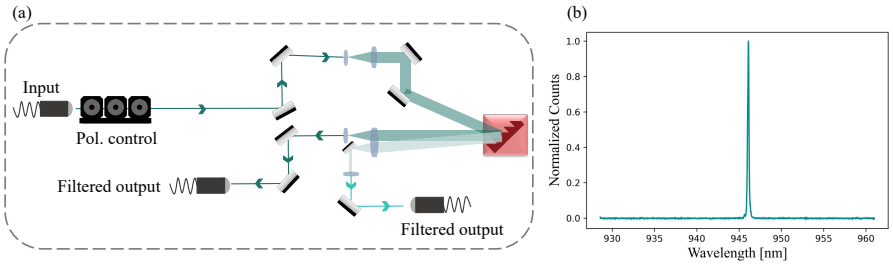


Figure 3.3: Grating filter. (a) Sketch of the grating filter setup, used to filter out the extra spectral contributions from the QD emission line. (b) Filter characterization by transmission scan through the filter.

3.2.3 Hanbury-Brown and Twiss setup

An important figure of merit when evaluating a single-photon emitter is its purity. Ideally, for such a two-level system, there is no chance to have concurrent emission events at the same time, which is known as anti-bunching and happens together with measuring $g^{(2)}(\tau = 0) = 0$, where τ is the time difference between two clicks, meaning

a completely pure single-photon source. On the other hand, $g^{(2)}(\tau = 0) = 1$ implies uncorrelated or classical behavior, where photons arrive independently of eachother. In this project, to measure the purity and characterize the single-photon nature of the light emitted by the QD, we have carried auto-correlation measurements. To do so, we designed a Hanbury Brown-Twiss (HBT) setup and added it to the optical setup presented in figure 3.1. The optical setup for this measurement is schematically illustrated in figure 3.4 (a), where the single photons emitted from the QD are incident to the grating filter (described in figure 3.3), to pick our desired emission line. The filtered signal is subsequently split by a 50:50 fiber beam-splitter, and the outputs are connected to two fiber-coupled avalanche photodiodes (APDs). The output from APDs is sent to a time-tagging module (PicoHarp 300), which measures the time delay between events where both detectors click, i.e., coincidence detection events. Figure 3.4 (b) shows the result of an auto-correlation experiment as a function of the delay between two detectors (τ) reported in [116]. The observed anti-bunching dip at zero time delay, confirms the presence of relatively pure single-photons.

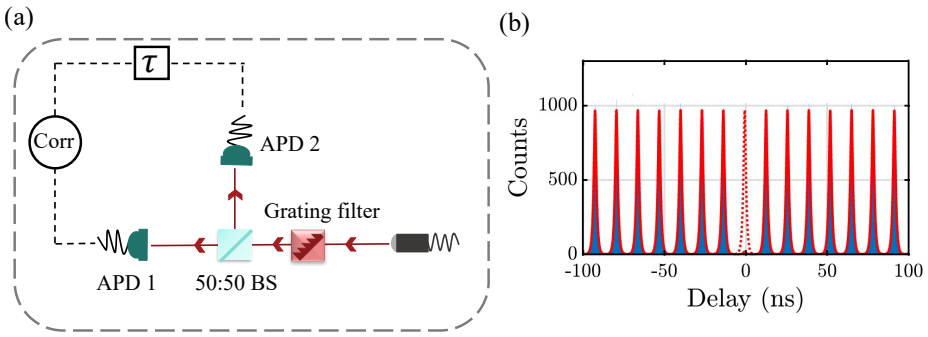


Figure 3.4: (a) Schematic of the experimental setup for measuring the auto-correlation. According to HBT setups, emitted photons are detected with APDs after passing through the 50:50 beam splitter (BS). (b) Typical result for auto-correlation measurement using this setup. The anti-bunching dip at zero time delay can be seen, adopted from [116].

3.3 Setup efficiency

For quantum information applications, achieving high count rates is crucial. Therefore, the efficiency of our experimental setup plays an important role in characterizing single-photon emissions from QDs. Here, we study the efficiency of all components in the out-coupling path to account for all losses experienced by single-photons. A CW diode laser (CTL) locked at 950 nm, which is the operational wavelength of our InAs QDs, is sent through each of the optical components in the collection path to measure

Table 3.1: Efficiencies of the different components in the collection path of the optical setup

Single optical component	η_{opt}	98±1%
Objective	η_{obj}	82±0.2
Beam Splitter	η_{BS}	95±2
Polarization Beam Splitter	η_{PBS}	98±0.5
Fiber Connector	η_{fiber}	59±2

their transmission efficiency, and the results are reported in the table below. We neglect the losses from the lenses and the entrance window because they are too low to be measured accurately. The efficiency for optical elements (waveplates, mirrors, and polarizers) is measured to be very similar, with less than a percent variation. Hence, for simplicity, we merged them in the table as η_{opt}.

Table 3.1 summarizes the efficiencies of the different components employed in the collection path of figure 3.1. Accordingly, we can calculate the efficiency of the output path in the setup (shown in figure 3.1). The optical elements in this path are; the objective, two lenses, the entrance window of the cryostat, a waveplate, a lens, a beam-slitter, two mirrors, two waveplates, a polarization beam-slitter, two mirrors, and a fiber coupler. Which leads the total efficiency to be:

$$\eta_{collect-path} = \eta_{obj}\eta_{opt}\eta_{BS}{\eta_{opt}}^4\eta_{PBS}{\eta_{opt}}^2\eta_{fiber} = (39 \pm 3)\% \tag{3.1}$$

For single-photon measurements, the output beam is sent to a grating filter. The grating diffraction inside the filter, limits the efficiency to $\sim$ 65%. Together with optical components involved in this filtering setup, the total efficiency is experimentally measured to be $\sim$ 40%. Finally, we have the APDs, for which the efficiency at our operation wavelength is measured to be as low as 30%.

* * *

In summary, in this chapter, we described the optical setup used for the characterization of the fabricated sample in this thesis. We also introduced two main schemes for QD excitation and discussed the additional requirements for single-photon measurements. Finally, we had a look at the efficiency of our experimental setup.

CHAPTER 4

Characterization of the Heterogeneously integrated devices

To date, the realization of efficient single-photon sources based on suspended GaAs membranes with embedded self-assembled quantum dots has been demonstrated. However, today, the integration of single-photon emitters with low-loss substrates like SiO_2 has attracted significant interest in the field of quantum photonics. In chapter 2, we demonstrated the fabrication of GaAs waveguides with embedded QDs on a silica substrate, which is an important requirement for scaling up the number of integrated components needed for quantum information processing and realization of actual quantum photonic integrated circuits. In this chapter, we describe the characterization of the fabricated GaAs-on-Si waveguides using the experimental setup described in the previous chapter. Some parts in this chapter are reproduced from [27].

4.1 QD excitation in waveguide

The optical excitation of QDs in waveguides results in a strong light-matter interaction and the realization of scalable and deterministic single-photon sources, which was previously introduced in chapter 1 of this thesis and in [120]. Due to the high refractive index contrast between the GaAs waveguide ($n \approx 3.47$ at 940 nm at 10 K) and the surrounding medium (air and SiO_2 with $n \approx 1 and 1.46$, respectively), propagation modes are confined in the material due to total internal reflection (TIR). For a single-mode nanobeam waveguide with width and height of 300 nm and 160 nm, respectively, the QD will couple to the fundamental TE_{00} mode, as it is located in the middle layer

of the waveguide. Figure 4.1 (a) shows the mode profile in the waveguide in the COMSOL simulation, which yields an effective refractive index of n_{eff} = 2.45. Here, we excite the QDs by directly coupling the laser light through the waveguide modes in the nanostructure. A pair of highly efficient shallow etched grating couplers with a reported efficiency of > 65% [116] are fabricated for the in- and out- coupling of light (so-called excitation and collection grating couplers), as depicted in figure 4.1 (c).

4.2 Propagation loss in GaAs-on-Si waveguides

Propagation loss, also known as attenuation, refers to the reduction in the power of an optical signal while traveling in the waveguide. It is an important parameter in determining the efficiency of a platform. In this work, we measure the propagation loss in GaAs waveguides fabricated on a hybrid GaAs-on-Si substrate. The sample is characterized by gluing it on a PCB and mounting in the chamber connected to a liquid He-flow cryostat. We performed transmission measurements at both room temperature and low temperature using a supercontinuum (Super K) laser source. To estimate the propagation loss at this platform, we measured the transmission through a set of rectangular waveguides of various lengths, which are designed as concentric waveguides. The concentric waveguides are fabricated with the same number of 90-degree bends and grating couplers. This allows us to factor out the effect of bends and grating couplers, ensuring that the measured loss is only as a function of the waveguide length. Figure 4.1 (b) depicts a top-view SEM image of a set of nanobeam waveguides with different length, made as concentric waveguides. The inner waveguide has been magnified in figure 4.1 (c), which shows the excitation (input) and collection (output) shallow-etched grating couplers. The focusing grating couplers are designed to vertically guide the light in- and out-of-plane to be directed to the objective on top of the sample and then send into the free-space optical path and the single-mode fiber.

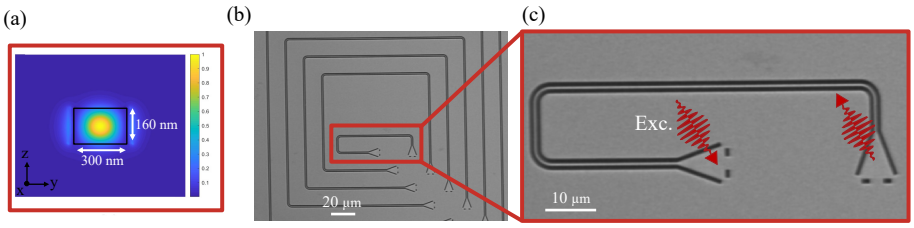


Figure 4.1: (a) SEM image of the nanobeam waveguides with different lengths, made as concentric waveguides. (b) Zoom out of the smallest waveguide, showing the excitation and collection geating couplers.

The Super K laser source, after propagating along the input path shown in Figure 3.1, is coupled through the excitation grating coupler. The transmitted light is collected and, following the output path in figure 3.1, is guided to the spectrometer for analysis. Figures 4.2 (a) and (b) depict the transmission spectra (normalized to the peak transmission) measured on the three inner waveguides at cryogenic (10 K) and room temperatures (295 K), respectively. We have smoothed out the small fringes, which are likely caused by the small reflectivity of the grating. To provide a better comparison, the transmission spectra of the shortest concentric waveguide (99 nm-long) at (10 K) and (295 K) are plotted together in figure 4.2 (c), which reveals two points. First, the larger absorption caused by the built-in electric field leads to a visible drop in the transmission at room temperature compared with that at low temperature. Second, the transmission peak of the grating coupler is red-shifted by $\sim$ 12 nm at room temperature because of the thermo-optic effect. The bell-shaped transmission curves and peak wavelengths of the GaAs waveguides fabricated heterogeneously on a Si substrate are in good agreement with the grating bandwidth of suspended waveguides [116]. By repeating the transmission measurements on the set of concentric waveguides of different lengths, assuming an identical response from each grating, the intensity drop is fitted to a linear absorption model, following the procedure outlined in [121], and the propagation loss and respective uncertainties are extracted at different wavelengths.

To compare the performance of the waveguides in these two platforms, i.e., suspended GaAs and GaAs-on-Si, we plotted the measured propagation loss for these two types of waveguides as a function of wavelength in figure 4.2 (d), where the error bars represent the standard deviation of the best fit parameters. At the transmission peak wavelength of the grating at cryogenic and room temperature, i.e., 933 nm and 945 nm, a loss of $(-11.6 \pm 1.0)$and (-26.0 ± 4.3) dB/mm are obtained, respectively. At longer wavelengths (> 933 nm) the loss drops to (-6.9 ± 0.7) dB/mm, which is in a good agreement with the propagation loss measured on conventional suspended waveguides and previously reported in [116, 121]. As shown in figure 4.2 (d), for both temperatures, the loss is strongly wavelength-dependent, with the higher loss occurring at shorter wavelengths. Such behavior is typical and in qualitative agreement with Franz-Keldysh electroabsorption, and has been previously observed to occur up to $\sim$ 200 meV inside the GaAs bandgap in the presence of strong electric fields [121]. Electroabsorption is normally not observed in undoped suspended GaAs waveguides, where the loss is nearly wavelength-independent in the 920–950 nm range. This is also confirmed by the plotted data for the propagation loss in the undoped suspendedGaAs waveguides fabricated in the GaAs monolithic platform (the data plotted in green in 4.2 (d)). Therefore, we suspect that the polymer, which is used as the adhesive layer for the bonding, and the underlying SiO_2 substrate have been charged due to the EBL exposure [122] at

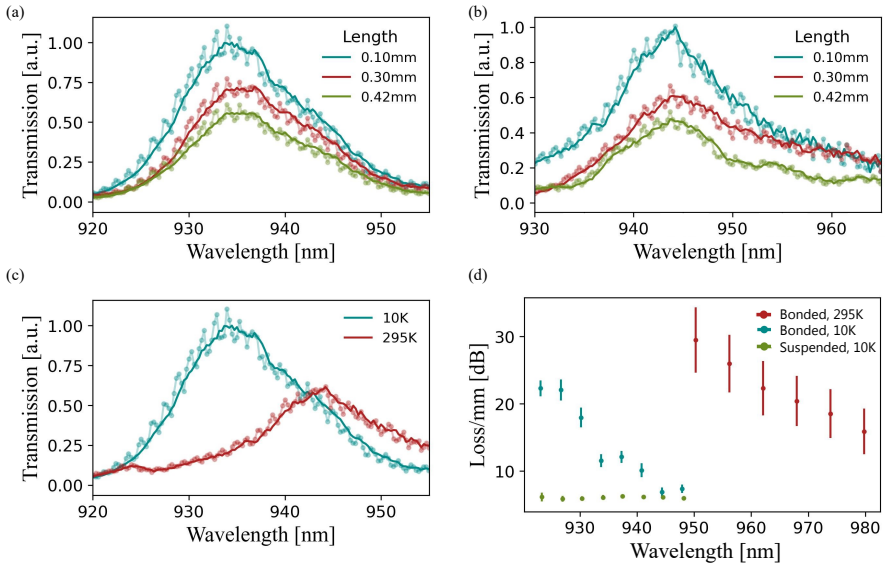


Figure 4.2: Transmission measurements. Normalized transmission spectra of the three inner concentric waveguides at (a) cryogenic and (b) room temperature. (c) Transmission spectra for the shortest concentric waveguide (L= 99 nm), at room (in red) and low temperature (in cyan). The weak interference fringes are caused by back-reflections at the grating couplers. showing the shift in the peak frequency. (d)) Propagation loss per mm (in dB) at room temperature (in orange), at cryogenic temperature (in cyan), and for the previously fabricated suspended waveguides at cryogenic temperature (in green) versus wavelength. Error bars are estimated from the fit procedure.

300–600 μC/cm^2 and cause a > 100 kV/cm uniform electric field in the proximity of the waveguides. Here, two dominant loss mechanisms limit the waveguide propagation efficiency: electroabsorption due to the charging during EBL and waveguide surface roughness. The residues produced during the etching of the waveguides can give rise to the surface and sidewall roughness, leading to unwanted scattering and higher propagation loss. This loss originates from the waveguide and is independant from the measurement mechanism. Surface passivation has been successfully reported to improve surface quality and to decrease this type of loss.

4.3 Characterization of single-photon generation

In order to optically characterize the quality of the QDs after bonding on a Si substrate, we performed photoluminescence (PL) measurements at cryogenic temperatures. We excite the QDs in the nanobeam waveguide with an above-band pulsed laser at 776 nm with 40 MHz repetition rate. Photons with an energy higher than the QD bandgap

energy are incident on the quantum dot. Following the interaction of a QD in the waveguide and the above-band input pulses, the QD absorbs the high-energy photon, which leads which leads to the formation of electron and hole bounded state, i.e., excitons, as depicted in figure 3.2 (a). The promoted electron is unstable in the excited state, so it relaxes by recombining with the hole, while emitting a photon with the energy corresponding to the energy difference between the excited state and the ground state of the QD. When the QDs are embedded in a waveguide, the light-mater interaction will be enhanced, which results in a more efficient light extraction. In waveguide-assisted QD excitation, single-photons are emitted at the location of the QD coupled to the waveguides fundamental mode, which helps to confine and direct the propagation of the photons. Figure 4.4, schematically illustrates a QD within a nanobeam waveguide, which is excited by a PDL. The photons are emitted in both directions and propagate along the waveguide, which leads to a significant decrease in the number of photons collected. Photonic crystal waveguides can also be used to direct spontaneously emitted photons and couple them in one direction to the single guided mode.

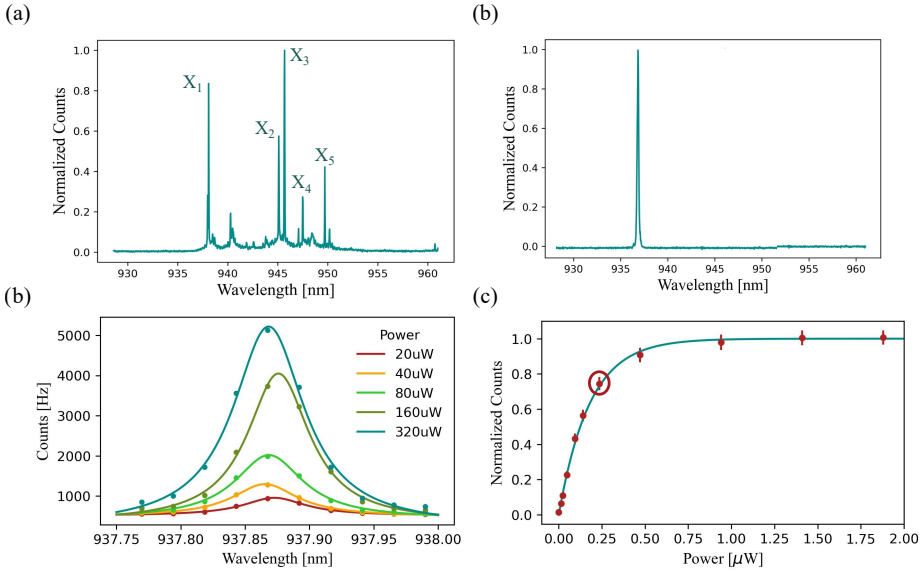


Figure 4.3: QD emission characterization. (a) Spectrally resolved emission from a quantum dot in response to the above-band excitation. (b) The filtered emission line X_1 in the emission spectra of (a). (c) Filtered emission intensity as a function of input power sweep (numbers for power are measured before coupling to the optical breadboard input fiber). (d) Normalized single photon counts as a function of excitation power, showing saturation (cyan line is a fit to the data). The numbers for power are measured at the sample. The circle shows the power level for the HBT measurement.

The focusing output grating coupler is designed at the end of the waveguide to enable vertical out-coupling of the emitted photons. The spectrum of the QD emission in response to the above-band excitation is presented in figure 4.3 (a). The density of QDs is relatively high in this sample, which results in multiple excitonic transitions leading to several emission lines (marked with X_n in the figure) in the above-band excitation scheme. To investigate the nature of the emitted signals, we performed further detailed optical characterization of the fabricated sample. We set the grating filter with ~ 0.2 nm bandwidth to pass the emission line X_1, i.e., 937.86 nm. As shown in figure 4.3 (b), extra spectral contributions that are not from our desired QD have been filtered out, which makes the signal ready for subsequent characterizations. The recorded emission intensity for the filtered emission line (i.e., the peak X_1 in figure 4.3 (a)) as a function of different excitation powers is displayed in figure 4.3 (c). Increasing the excitation power results in a saturation behavior in the number of emitted photons, confirming that this emission is from the neutral exciton, figure 4.3 (d). The saturation power can be extracted by fitting this data (red dots) with $I = I_{\text{max}}\,(1 - \exp(-P/P_{\text{sat}}))$ (solid cyan line in figure 4.3 (b)), where I is the number of counts, I_{max} is the maximum counts, P is the applied power at the sample, and P_{sat} is the power at which the emission saturates. Accordingly, a saturation power of $P_{\text{sat}} = 0.18\,\mu\text{W}$ is extracted at $I = 0.63 I_{\text{max}}$. The maximum number of total counts observed in the photodetectors is ~ 10 kHz.

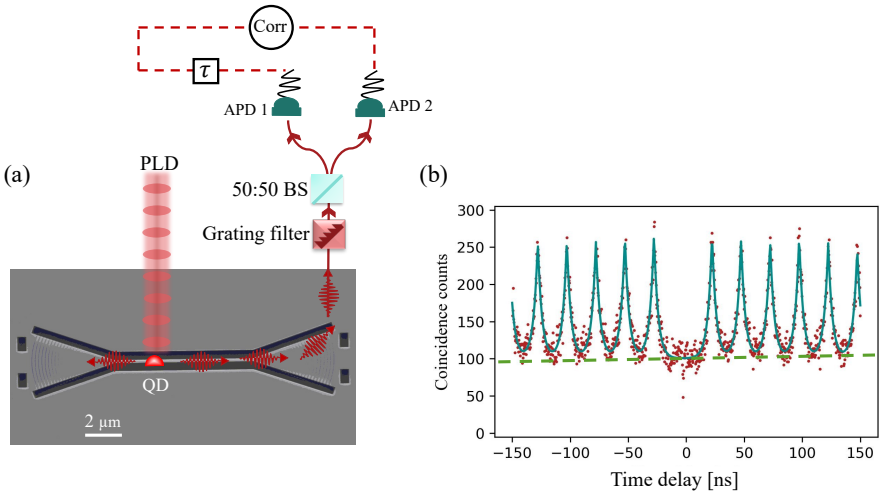


Figure 4.4: (a) Schematic illustration of single photon emission from a QD excited by a PLD. An output grating filter couples the emitted photons vertically to a HBT setup, which is made of a grating filter, a beam splitter, and APDs to measure second-order correlation between the coming photons. (b) The auto-correlation histogram from the Hanbury Brown and Twiss experiment as a function of the delay between the two APDs for the filtered emission line shown in 4.3 (b). The green dashed line indicates the background level.

To characterize the single-photon nature of the filtered signal of figure 4.3 (a), which is mainly from the emission of our desired QD, we experimentally quantified the second-order intensity correlation through a Hanbury Brown Twiss (HBT) experiment. According to the HBT measurement setup, which is schematically illustrated in figure 4.4 (a), the filtered signal is incident to a 50:50 beam splitter with two avalanche photodiodes (APDs) at each of its output ports. The detectors output is sent to a time-tagging module, which records the correlation events between the two detectors. As explained in the previuos chapter, the HBT experiment can be used to determine the purity of the emitted single-photons. If the input is a single-photon, there will not be simultaneous clicks in both detectors, due to the quantized nature of photons. The correlation of the detected photons in APDs can provide the measurement of $g^{(2)}(\tau)$, where the τ is the time interval between photon arrivals. Analyzing the correlation between detection events can reveal whether we have a single-photon emitter and the purity of the emitted single photons. Figure 4.4 (b) presents the result of this auto-correlation function, where the coincidence rate is plotted as a function of the coincidence time delay between the two APDs (τ) for the QD under study. The correlation histogram $g^{(2)}(\tau)$ is reported in figure 4.4 (b), which is measured at $P = 1.3P_{\text{sat}}$ (the power specified by the circle in figure 4.3 (d)). Here, we excite the QD using a PLD with 40 MHz repetition rate, which results in correlation peaks with $\sim$ 25 ns interval. The exponential decay of the correlation peaks is proportional to the QD radiative decay rate. The suppressed peak at zero time delay, i.e., $\tau = 0$ is observed, indicating anti-bunching behavior, which is the signature of the single-photon nature of the emission line from the QD. The above-band excitation allows for photon emission via multiple pathways and weakly excites other neighboring defects, giving rise to broad features in the emission spectra. Single-photon purity, which is a critical characteristic of single-photon emitters, is defined as the ratio between the suppressed central peak area and the neighboring peak area. A substantial number of counts, highlighted by the dashed green line in figure 4.4 (b), does not allow us to observe the peak at zero time delay and to extract the exact value of $G^2(0)$, but only to identify an upper bound to approximately 40%, that confirms the single-photon nature of the emitted light. To obtain a more precise estimate, a sample with a lower QD density and a narrower filtering apparatus is required.

4.4 Efficiency Breakdown

To identify the total efficiency, we need to consider all the possible losses that single-photons will encounter. When using a pulsed laser diode, ideally, every single laser pulse will result in emitting one single-photon. Hence, we can compare the laser repetition rate of 40 MHz to the measured single-photon rate to estimate the total

efficiency. In the first place, we have the losses in the experimental setup, which we completely analyzed in the previous chapter. As explained in section 3.3, the optical setup, including the objective in the cryostat, optical components, BS, PBS, and fiber connector, collectively introduces $(39 \pm 3)\%$ loss. In single photon generation and characterization, there are some extra possibilities for losses, which we will discuss in the following, and drive the total efficiency of our source.
As it is schematically shown in figure 4.4 (a), the single-photons emitted from the QD couple into the waveguide in both directions. When we collect the output signal from the grating coupler, we only collect half of the emitted photons ($\eta_{\text{directionality}} = 50\%$), which leads to a high loss in QD emission collection. Then, we have the propagation loss of the emitted photons in the optical path and coupling into the fiber, which is calculated in the previous chapter ($\eta_{\text{collect-path}} = 39\%$). Moreover, we employed a grating filter to extract the contribiution of other QDs sitting nearby in energy, so there is also the non-unity transmission efficiency of the grating filter ($\eta_{\text{filter}} = 40\%$). Therefore, we can calculate the total propagation and collection efficiency to be

$$\eta_{\text{collection-propagation}} = \eta_{\text{directionality}}\eta_{\text{collect-path}}\eta_{\text{filter}} = 7.8\% \tag{4.1}$$

Apart from all the setup and collection efficiency, the quantum efficiency of the QD also limits the total source efficiency. Different factors affect this quantum efficiency, including

- coupling efficiency of the QD emission into the waveguides optical mode (non-unity $\beta - factor$ due to coupling into non-guided modes).
- red- and blue- shifted emissions from the QDs central emission energy, due to interactions between the QD and its surrounding lattice vibrations, known as phonons (broad phonon sideband), which are filled out by the grating filter.
- Spin-flip and coupling to the dark exciton state, which is less likely to be involved in photon emission.
- Exciting the wrong dipole, which might lead to the emission of photons that do not meet the requirements for single-photon sources, e.g., multi-photon emission.

Taking into account all these mentioned contributions, it ended up with measuring the source efficiency of $\eta_{\text{source}} = 84\%$, by our colleagues on a similar self-assembeled QD (for detailed info check [26]). Finally, the total efficiency of the single-photon emitter is estimated to be

$$\eta_{\text{total}} = \eta_{\text{collection-propagation}}\eta_{\text{source}} = 6.5\% \tag{4.2}$$

Table 4.1: Summary of representative demonstrations with Integrated single-photon emitter on a Photonic Chip

Ref	Integration method	Emitter	Photonic chip	Alignment	$g^2(\tau)$
[98]	Transfer printing	InAs QDs in GaAs	SOI	optical microscopy	0.3
[72]	Pick-and-place	InAs QDs in InP	SiO_2	SEM	0.33
[64]	Pick-and-place	InAs QDs in GaAs	Si_3N_4	optical microscopy	0.07
[107]	Wafer bonding	InAs QDs in GaAs	Si_3N_4	e-beam lithography	0.11
[123]	Wafer bonding	InAs QDs in InP	SiO_2	e-beam lithography	0.2
This work	Wafer bonding	InAs QDs in GaAs	SiO_2	e-beam lithography	< 0.4

Considering the 40 MHz laser repetition rate, we arrive at an expected single-photon rate of 2.6 MHz for this efficiency. This doesnt agree with the measure single-photon rate of 10 kHz. The reason is that in our sample with a QD density, by the above-band excitation, we excited lots of emitters. Therefore, a small fraction of the 40 MHz will be used by the particular emission line we selected.

4.5 The state-of-the-art of heterogeneously integrated QD single-photon sources

As discussed in the introduction chapter, the hybrid integration of quantum dot single-photon sources on photonic integrated circuits (PICs) allows us to combine the important benefits of different technologies, for a wide range of applications. To date, there are several different methods for directly integrating bright quantum emitters on PICs, to create an efficient and versatile quantum photonic system.

To conclude this chapter, we summarize the current state-of-the-art for hybrid integration of QD emitters on PICs, based on different techniques for integration. Figure 4.5 illustrates some typical methods for the integration of QD single-photon sources, on different photonic integrated circuits. Figure 4.5 (a) and (b) show the pick-and-place technique to integrate III-V layers with embedded QD on a Si-based chip, [64, 72]. In Figure 4.5 (c) and (d), the two main steps for the micro-transfer printing of QD single-photon sources on an SOI chip are illustrated [98]. The schematical layer stack for the QD single-photon emitter heterogeneously integrated on an SiO_2 layer using the adhesive bonding method is presented in figure 4.5 (e), [123]. In conclusion, table 4.1 summarizes the key information of some state-of-the-art techniques for heterogeneous integration of QD-based single-photon sources on a low-loss platform. A comparison with the devices used in this work is also provided.

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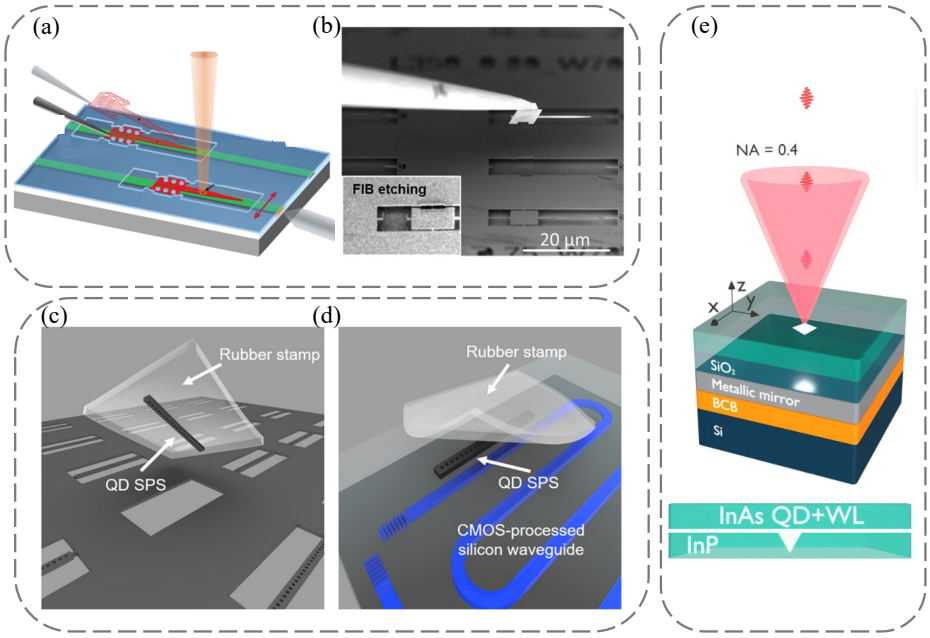

Figure 4.5: Different methods for heterogeneous integration SPS on PICs. (a) Schematic and (b) SEM image of the pick-and-place technique for hybrid integration of QD sources on a Si-based platform [64, 72]. (c) Removing the III-V waveguides with embedded QD from its native substrate and (d) printing it to the Si-based host substrate [98]. (e) Heterogeneous integration of QD single photon sources on an SiO_2 layer, using bonding method with a layer of BCB (benzocyclobutene) as the adhesive layer [123].

To sum up, we presented the characterization results for the fabricated GaAs waveguides with embedded QD, heterogeneously integrated on a SiO_2 layer. The measured propagation loss in this hybrid GaAs-on-Si platform is in good agreement with the propagation loss reported for the traditional suspended waveguides, which confirms that the method presented here enables the developing GaAs-based waveguide circuits with single-photon emitters without degradation of performance. Moreover, we used a pulsed laser for the above-band excitation of the QDs, where the single-photon emission demonstrates that the embedded QDs are not spoiled during the fabrication process. We also give an overview of the total efficiency of our setup, which can still be optimized, e.g, by using an efficient filter to extinguish unwanted spectral contributions (like etalon filter), or by using SNSPDs instead of APDs for single-photon detection. As a final conclusion for this chapter, we summarized some of the popular techniques for the integration of SPSs on PICs and compared them to the work presented in this thesis.

CHAPTER 5

Integration of GaAs waveguides with Si_3N_4 waveguides

As discussed in previous chapters, epitaxially grown III-V semiconductor quantum dots (like InAs/GaAs) provide strong light-mater interaction, which makes them a leading platform for the deterministic generation of high-quality single-photons in terms of brightness, purity, and indistinguishability. However, because of their relatively high loss, GaAs waveguides are not very desirable for large-scale photonic quantum technology. On the other hand, silicon photonics is known as an unrivaled platform in terms of low optical loss and compatibility with standard silicon processing techniques (CMOS-compatible). Therefore, by integrating GaAs single-photon sources with low-loss materials such as silicon nitride (Si_3N_4), the strengths of each material system can be combined to create a hybrid platform with improved performance and functionality.

Here, we integrated a GaAs membrane with embedded QDs on a chip with Si_3N_4 photonic circuits. By aligning to the underlying Si_3N_4 waveguides embedded in a thick SiO_2 layer, we designed and fabricated GaAs waveguides. The light is adiabatically coupled between the GaAs and Si_3N_4 waveguide layers by slowly tapering the GaAs waveguide. This chapter first explains the design and simulation of the adiabatic tapers. Subsequently, the fabrication of GaAs waveguides aligned with Si_3N_4 waveguides is discussed. Finally, we determined the optimized width for the GaAs taper tip and characterized the coupling efficiency between the two waveguide layers.

5.1 General layout of the coupling between the GaAs and Si_3N_4 waveguides

Optical light coupling between the GaAs waveguide layer and the underlying Si_3N_4 waveguide layer is realized using a taper-based spot-size converter structure. In the heterogeneous GaAs-on-SiO_2 platform studied in this work, the optical mode is completely confined in the GaAs waveguide. By gently tapering the width of the GaAs waveguide, we change the effective index of refraction, therefore, the optical mode can be gradually transformed to eventually reside in the underlying Si_3N_4 waveguide. Figure 5.1 shows the 3D schematic view of the tapering structure for coupling light between the GaAs and Si_3N_4 waveguide layers. In the first tapering section, the GaAs waveguide width rapidly tapers down to a width where the optical mode is still confined in GaAs. Then, the second tapering section begins by further tapering the waveguide to the final tip width with a very gentle slope, during which the light is adiabatically pushed down to the Si_3N_4 waveguide layer. When the GaAs waveguide dimensions vary slowly along the propagation direction, no power exchange occurs between its fundamental mode and the higher order modes, indicating that the tapering is adiabatic. In the next section, we discuss the simulation and design of the tapering parameters in more detail.

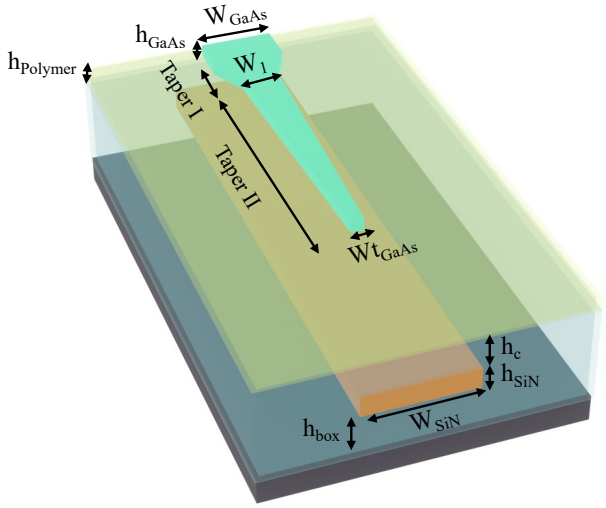

Figure 5.1: 3D schematic view of the taper-based spot-size converter structure designed for coupling light between the GaAs and Si_3N_4 waveguide layers.

5.2 Optimization of the coupling section

To find the optimized parameters for the coupling of light between GaAs and Si_3N_4 layers, we used finite-difference time-domain (FDTD) Lumerical simulations, performed by our collaborators at Aarhus University. The details and device geometry of the adiabatic taper section are shown in figure 5.2. The Si_3N_4 waveguide is embedded in a SiO_2 layer with a thickness of h_1=8 µm and is separated from the chip surface by a distance denoted as h_c. SiO_2 cladding is a common technique to reduce surface scattering loss in waveguides, as it creates a low-index layer surrounding the core of the waveguides, which are made of a higher-index material. When the light is propagating within the core of the waveguide, it experiences total internal reflection (TIR) at the core-cladding interface, which confines the light in the waveguide and reduces the surface scattering loss. The distance between the GaAs taper and Si_3N_4 waveguide, i.e. the thickness of the SiO_2 cladding layer (h_c), should be sufficiently large to avoid surface scattering losses but still provide efficient coupling. Figure 5.3 (a) presents the simulated transmission parameter (S_{12}) of the TE_{00} from the GaAs waveguide to the TE_{00} of the Si_3N_4 waveguide for three values of h_c. If the cladding layer is not sufficiently large, it may not provide adequate TIR, causing the guided mode to leak into the surrounding medium and increase the propagation loss in the waveguide. In this study, we used h_c=500 nm, to achieve a low-reflection, highly efficient power transfer between the two waveguide layers. The mode transformer geometry shown in figure 5.1 consists of two parts. The first part (Taper I) rapidly decreases the GaAs width from the normal waveguide width of W_{GaAs}=300 nm to W_1=170 nm. In the second part (Taper II), the actual GaAs-to-Si_3N_4 coupling occurs by gradually tapering the GaAs waveguide to the final tip width (W_{tip}). To achieve adiabatic coupling, we considered a long coupling length of 100 µm for the second tapering region.

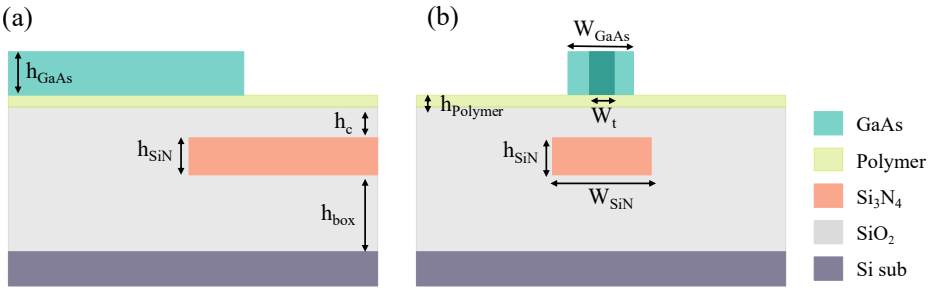

Figure 5.2: Cross-sectional (a) lateral view, (b) front view of the coupler.

The thicknesses of the GaAs and Si_3N_4 waveguides are taken from the available wafer stack used for fabrication, h_{GaAs}=160 nm and h_{SiN}=100 nm, respectively. The widths of the GaAs and Si_3N_4 waveguides are chosen to support a single transverse-electric (TE) mode, W_{GaAs}=300 nm and W_{SiN}=1 µm, respectively. Figure 5.3 (b) shows the simulation results for the transmission coefficient versus the taper length for the first tapering region. The figure shows that considering L_{T1}=3 µm, we have a very efficient taper, where almost no light is lost in this region.

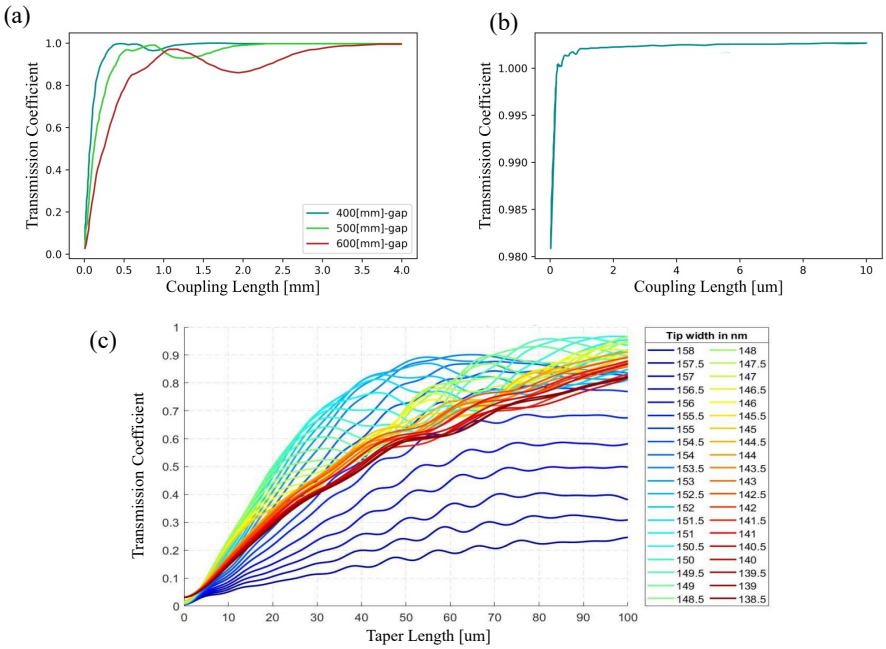

Figure 5.3: Simulation results for the optimization of the spotsize converter coupling section, courtesy of Mircea Balauroiu, Aarhus University. (a) Influence of the gap size between GaAs and Si_3N_4 waveguide layers on the transmission coefficient. (b) Transmission coefficient versus GaAs tapering length for the first tapering region (from W_{GaAs} down to W_1). (c) Transmission coefficient of different widths for the GaAs taper tips (W_{tip}). The transmission coefficient goes slightly higher than 1, which is due to normalization errors in the numerical code.

In the second part of the coupling structure, the GaAs waveguide is tapered from W_1=170 nm to W_{tip}, while the Si_3N_4 waveguide remains geometrically constant. The coupling efficiency strongly depends on the width of the GaAs taper tip and the length of the tapering region. Hence, we found the optimized value by sweeping the tip width versus tapering length, Figure 5.3 (c). The GaAs waveguide is tapered from W_1 to a narrow waveguide tip of W_{tip} in [158–138] nm. With respect to the taper length, there is a trade-off between having a tolerant structure with higher efficiency and

the device footprint and fabrication accuracy. We note that if the slope of tapering is very low, the variations might not be detected by the EBL tool during fabrication; therefore, we consider L_{T2}=100 µm, to be long enough to have an efficient coupling. The red lines in the figure are more stable than the lighter toned ones, however, they require a longer coupling length. On the other hand, the cyan lines couple with a very high efficiency in a length under 100 µm, but they are more unstable than the red lines. Because the fabrication of the tapers is one of the most critical steps during processing, some variations in the taper width may occur. In the real world, waveguides cannot be fabricated with an accuracy of 0.5 nm. Therefore, in our real chip, we will make an array of the waveguides with W_{tip} around 130 nm, i.e., a sweep of this value as well as ±10 nm and ±20 nm has been made to correct for the fabrication error. Figure 5.4, illustrates the electric field distributions during this tapering. At the start of this taper, the light resides mostly in the GaAs waveguide, figure 5.4 (a). By adiabatically tapering the GaAs waveguide along the propagation direction, power is efficiently transferred from the GaAs to the Si_3N_4 waveguide layer, 5.4 (b). Finally, the tapering length is chosen to transfer the entire light in the Si_3N_4 waveguide layer, figure 5.4 (c).

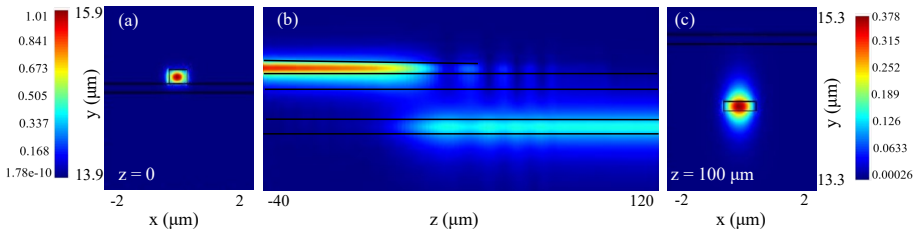

Figure 5.4: Electric field distribution (a) for the fundamental TE mode of the GaAs waveguide, (b) across the mode-transformer cross-section: the power is efficiently transferred from the top GaAs to the bottom Si_3N_4 guide, and (c) fundamental TE mode of the Si_3N_4 waveguide at the end of the mode transform. EME (Eigen Mode Expansion) simulations performed by our collaborators at Aarhus University.

5.3 Fabrication of the GaAs waveguides aligned to Si_3N_4 waveguides

In chapter 2, we provided a detailed overview of the fabrication process flow for integrating GaAs waveguides with embedded QDs on a bulk SiO_2 substrate. Here, we demonstrate the fabrication of GaAs waveguides with a taper-based spot-size converter, aligned to Si_3N_4 waveguides embedded in a thick SiO_2 layer. First, we discuss the mask and the required structures to be fabricated to characterize the coupling efficiency. Then, there is a fabrication overview, highlighting the differences in the fabrication process when integrating GaAs waveguides on a chip with embedded Si_3N_4 circuit, compared to the case of fabricating on bulk SiO_2 on Si substrate. At the end, there will

be a characterization of the fabricated structures and light coupling between the two waveguide layers.

5.3.1 Mask design

In designing the lithographic mask, we consider different types of devices with adiabatic taper to estimate the transitional loss between the GaAs and Si_3N_4 waveguide layers. As demonstrated in the previous section, by slowly tapering the width of the GaAs waveguide, light is squeezed out and captured by the underlying Si_3N_4 waveguide. To be able to measure in our optical setup, we need the light to be coupled back in our GaAs waveguide. To achieve this, we use another GaAs inverse-tapered waveguide on top of the Si_3N_4 waveguide. Because of its higher refractive index, when the width of the GaAs waveguide is increased, the light will be gradually coupled back to the GaAs waveguide on top.

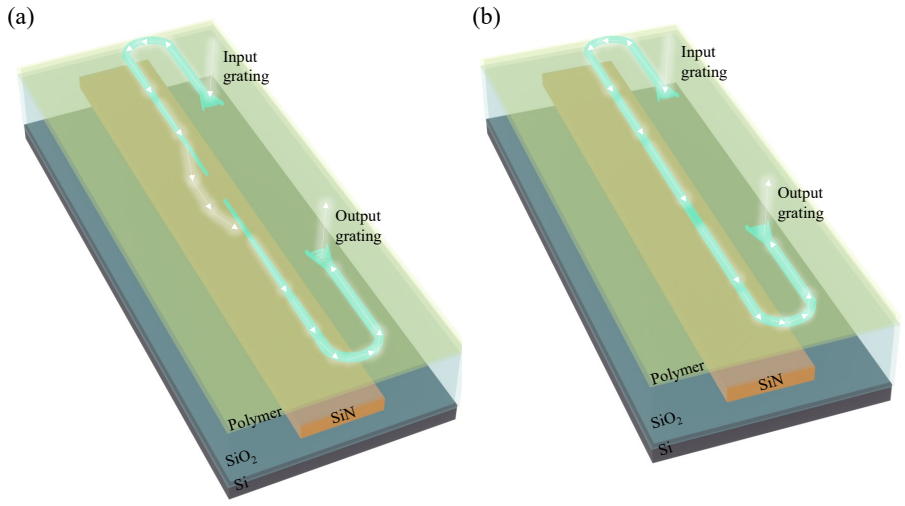

Figure 5.5: 3D schematic view of the GaAs waveguides integrated on a SiO_2 layer with embedded Si_3N_4 waveguides, (a) with tapered coupler (device) and (b) without tapered coupler (reference-devices). White arrows indicate the expected path for light propagation.

We have also considered two types of structures to be used as references. First, the so-called "reference-devices", are standard GaAs waveguides with the same shape and size as the understudy devices, but without tapering and coupling to the underlying Si_3N_4 waveguide. This structure can be used as a reference for transmission in a GaAs waveguide, where we do not have coupling loss. However, we have a higher propagation loss as the light stays more in the GaAs layer. The second type involves

fabricating one of our devices on an area without any Si_3N_4 waveguide underneath. We call these types of structures as "uncoupled-devices", using which we can check whether the light is really coupled to the underlying Si_3N_4 waveguide. In uncoupled-devices, there will not be any Si_3N_4 waveguide in which the light can propagate; therefore, we expect no signal to be transmitted and collected in the output grating. Otherwise, this doubt will arise that some of the light is actually taking a different path, without being coupled in the underlying Si_3N_4 waveguide, which we would have to consider and correct when estimating the coupling efficiency between the two waveguide layers.

Figure 5.5, shows the 3D schematic view of the integrated GaAs waveguides bonded on a substrate with embedded Si_3N_4 waveguides, using an adhesive polymer layer. The GaAs waveguides with adiabatic taper couplers aligned to the underlying Si_3N_4 waveguide and the reference-device without the tapering region to squeeze the light out are presented in figure 5.5 (a) and (b), respectively. The inter-taper distance, i.e., h_i = $h_{polymer}$ + h_c, should allow for sufficiently deep embedding of the Si_3N_4 to avoid surface scattering losses and should be shallow enough to avoid multi-millimeter coupling. To characterize the sample in our cryostat setup, we need the input and output grating couplers to be less than 100 µm apart, which is the size of our camera vision. By making bending waveguides, we can have both gratings in our area of vision, which makes it easy to align the input and output signals. As mentioned above, to correct for the fabrication error in the mask, we consider an array of waveguides with a sweep in their final tip width around 130 nm. To maintain a consistent overall geometry, the tapers of each device all have the same length of 100 µm and taper from an initial width (W_1) to the same width minus 40 µm (W_{tip}), to have the same tapering slope. This gives us five types of devices, their only difference being the GaAs taper tip width, with a spacing of 10 nm from 150 nm to 110 nm.

We created a gap between the tips of the GaAs waveguides, where the light is expected to propagate in the Si_3N_4 waveguide. In our standard devices, this gap is considered to be 37 µm. But, to study the effect of the gap between GaAs waveguide tips, we have also designed some devices with a longer and shorter gap, called "long-gap" and "short-gap", with gap lengths of 57 µm or 17 µm, respectively. We expect that this gap size does not affect the transmission efficiency, otherwise, we can conclude that a part of the light is scattered at the location of the first tip and is absorbed by the tip in front. To avoid this error, we designed the input and output grating couplers to be cross-polarized. The designed mask for reference-devices without tapering in GaAs is presented in figure 5.6 (a), where we expect the light to remain in the GaAs waveguide layer. Figure 5.6 (b) illustrates one of our devices aligned on top of the underlying Si_3N_4 waveguide. The GaAs taper tip and a part of the gap between the tips is zoomed out in figure 5.6 (c). The yellow area in the figure 5.6 (c) shows the area

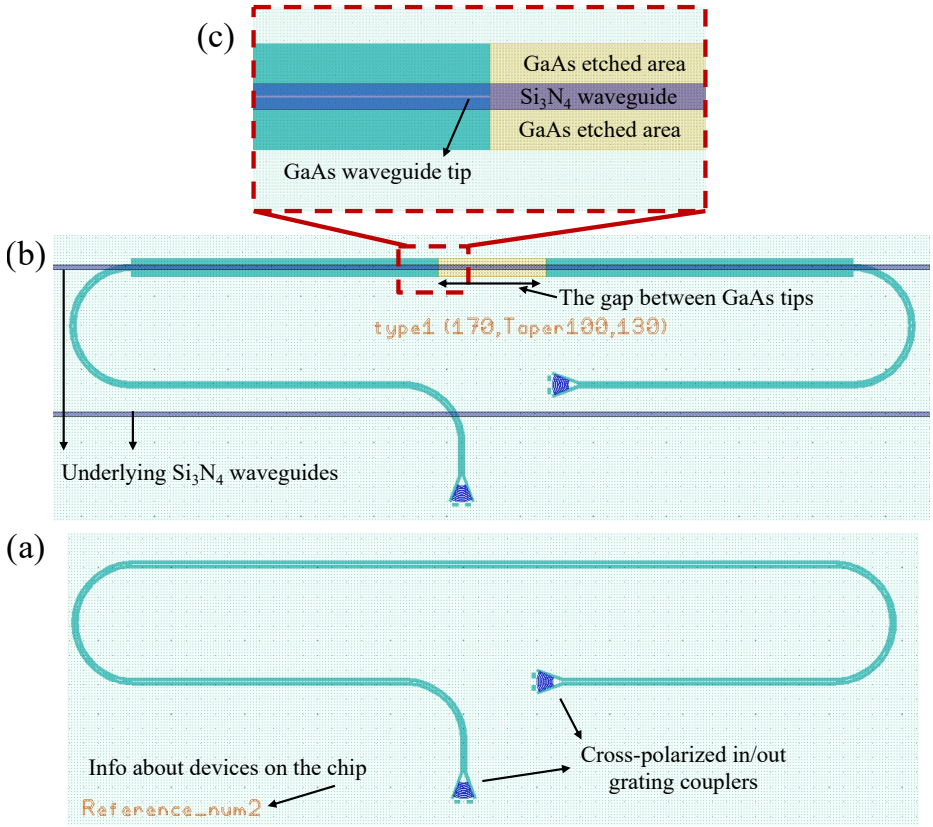

Figure 5.6: Mask design for (a) reference-device with cross-polarized in/out grating couplers, (b) GaAs waveguide with tapered tip for coupling to the underneath Si_3N_4 waveguide layer. (c) Zoom out of the tapered tip, showing the tip and underlying Si_3N_4 waveguide, to which the device is aligned.

around the gap between the GaAs taper tips. In this region, where the light is expected to propagate in the underlying Si_3N_4 waveguide, the GaAs material is designed to be removed, preventing the power from returning to the top layer. We have also included some information about each device on the chip to distinguish them while performing measurements. As the final design of the mask, we also included a set of concentric waveguides of different lengths to estimate the propagation loss in this platform, similar to the previous chapters. The concentric waveguides are located in a position where there is no Si_3N_4 waveguide underneath; therefore, they will give us the propagation loss in GaAs, independent of the underlying Si_3N_4 waveguide layer.

5.3.2 Fabrication of embedded Si_3N_4 waveguides

The chip with embedded Si_3N_4 waveguides is designed by our collaborators at Aarhus University and is fabricated by Lionix. The chip contains 3 arrays of 5 mm-long Si_3N_4 straight waveguides with different widths (1 µm, 1.5 µm, 2 µm), where there are 10 waveguides in each array with 25 µm gap between the waveguides. There are also 32 mm-long spirals with different widths (1 µm, 1.5 µm, 2 µm), which provides an opportunity to measure the propagation loss in Si_3N_4 waveguides. Figure 5.7, depicts the chip design for Si_3N_4 waveguides, where there is a symmetry around the middle.

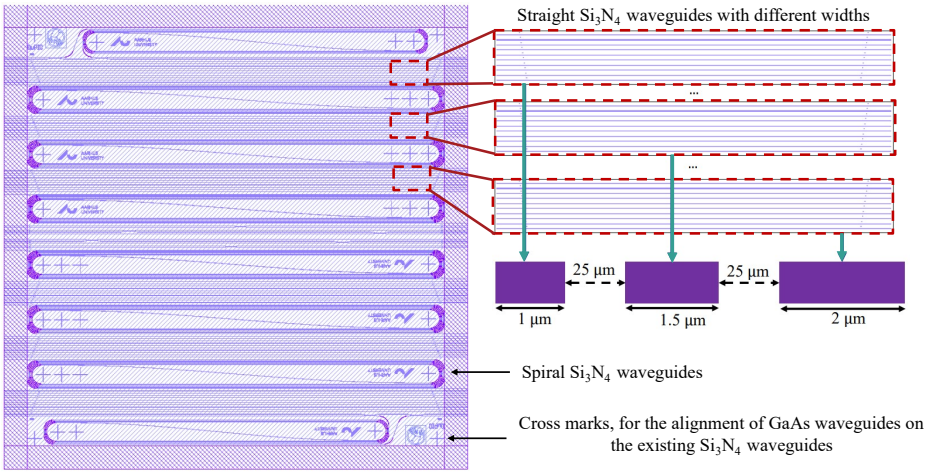

Figure 5.7: Mask design for Si_3N_4 waveguides embedded in an SiO_2 layer, showing sets of waveguides with different widths, spirals, and alignment marks.

The chip is fabricated by Lionix through a dedicated wafer run. The fabrication process flow, presented in figure 5.8, starts with the deposition of the 8 µm SiO_2 layer on the Si substrate using the wet oxidation technique. A layer of 100 nm-thick Si_3N_4 is deposited by low-pressure chemical vapor deposition (LPCVD), followed by the deposition of another SiO_2 layer by LPCVD. The waveguides are defined by optical projection lithography and dry etching, followed by deposition of a 500 nm SiO_2 cladding layer. Finally, after chemical mechanical polishing (CMP) of the top surface, the 4-inch wafer is diced into 10×10 mm^2 chips, which are to be used as the host substrate for the integration of GaAs waveguides in our clean room.

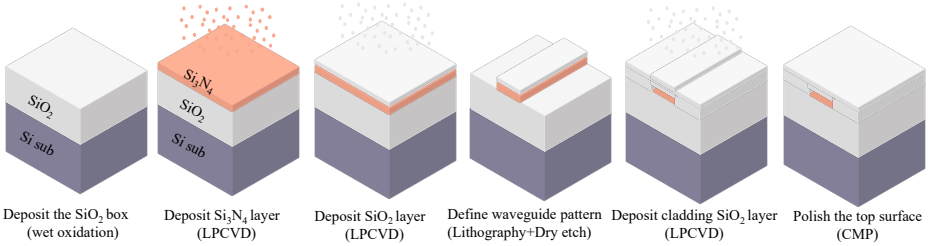

Figure 5.8: Lionix fabrication process flow for chips with embedded Si_3N_4 waveguides. The GaAs waveguides will be heterogeneously fabricated and aligned to these Si_3N_4 waveguides.

5.3.3 Bonding and fabrication of GaAs waveguides

The process flow for bonding the GaAs chip on top of one of the chips with embedded Si_3N_4 waveguides, removing the GaAs backside substrate, and the definition of the GaAs waveguides is similar to the procedure explained in chapter 2. However, having underlying waveguides and aligning to them requires some additional important considerations that we will address here. After checking the Si-based chips received from Lionix in SEM, we observed that, despite the CMP of the sample surface, there are still some bumps at the surface, which correspond to the embedded Si_3N_4 waveguides. Figure 5.9 (a) shows a cross-sectional SEM image of the Si-based chip. As shown in the schematic view of figure 5.9 (b), this caused the surface not to be perfectly planar anymore, and prevents successful bonding with the same parameters as the bonding on bulk SiO_2 sample. Hence, one solution could be to increase the thickness of the polymer, which is used as the adhesive layer for bonding, to compensate for these bumps and planarize the sample surface. Changing the thickness of the polymer layer can be achieved by changing its dilution proportion. Here, we used a solution of Butyrolactone:mr-DWL (1:1), which results in a 260 nm-thick polymer layer, for the bonding GaAs die on top of the chip with embedded Si_3N_4 waveguides from Lionix. Another point in the SEM image of the chip with Si_3N_4 waveguides, is that the cladding SiO_2 layer, which was designed to be 500 nm, is $\sim$ 220 nm. These two errors can compensate for each other since the refractive index of the polymer layer is similar to that of SiO_2 ($n_{polymer}$=1.58, n_{SiO2}=1.46), the thicker polymer layer can also be considered as a spacer between the two GaAs and Si_3N_4 waveguide layers.

After completing the bonding and removing the backside GaAs substrate following the procedure explained in chaper 2, we can begin the definition of GaAs waveguides. The second challenge is aligning the GaAs waveguides to the underlying Si_3N_4 waveguides, which should be done during EBL. Because of their close refractive index, the marks in Si_3N_4 are difficult to see in the vision of an e-beam machine. A very unclear

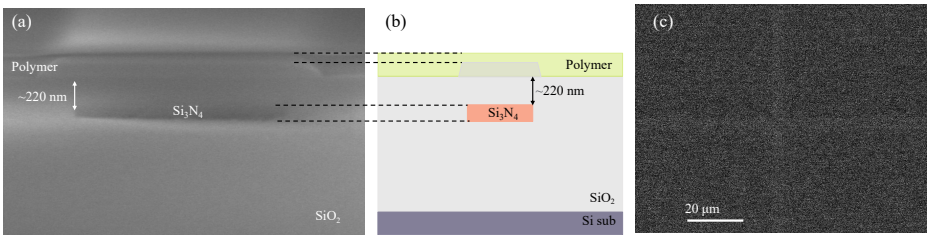

Figure 5.9: (a) Cross-sectional SEM image of the samples received from Lionix, with the spin-coated polymer on top. The gap size is less than desired, and the surface is not perfectly planar. (b) Schematic of (a). (c) Scanning electron microscope image of the Si_3N_4 alignment mark embedded in SiO_2 acquired in the EBL tool.

image of the marks is observable, figure 5.9 (c), on which we used manual alignment to define our metal marks exactly on top of the embedded marks. After defining metal marks on the transferred GaAs membrane, we can follow our normal fabrication process flow, i.e., a series for EBL followed by RIE, to define shallow-etch gratings and deep-etched waveguides.

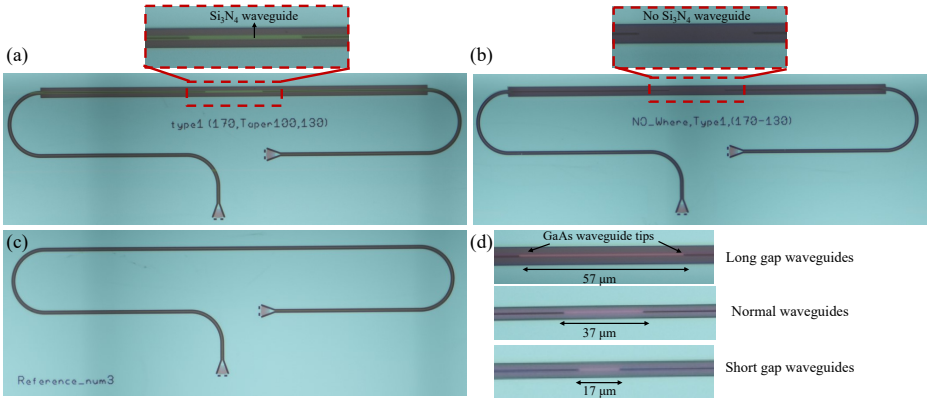

Figure 5.10: Optical microscope image of the different GaAs structures fabricated on the chip. (a) Devices with tapering in the GaAs waveguide, zoom: the underlying Si_3N_4 waveguide is observable in the optical microscope. (b) uncoupled-devices, which is completely similar to (a) but without any Si_3N_4 waveguide underneath. (c) reference-devices without tapering. (d) Devices with different gaps between the GaAs waveguide taper tip.

An optical microscope image of the different structures fabricated in this chip is presented in figure 5.10. Because the alignment is based on the EBL system, an alignment accuracy of $\sim$ 10 nm is achieved, which is much better than that of other similar methods for this heterogeneous integration. For example, the alignment accuracy of high-throughput transfer printing (between 500 nmand 1 µm) is not good enough to

ensure good coupling. As shown in the figure, the GaAs waveguide tip is aligned to the underlying Si_3N_4 waveguide with high accuracy. Figure 5.10 (a) shows an optical microscope image of one of the fabricated devices, which are GaAs waveguides with cross-polarized in/out grating couplers and two tapering tips aligned to the underlying Si_3N_4 waveguide. There are several similar structures available on the chip, with the same gap size of 37 µm between GaAs tips, whose only difference is in their tip width. The two references used to check the correctness of the coupling mechanism, i.e., uncoupled-devices and reference-devices, are illustrated in figure 5.10 (b) and (c). As can be seen in the zoomed area in the uncoupled-device, compared to that of the normal device presented in (a), the GaAs waveguide tip is not aligned to any underlying Si_3N_4 waveguide. In the reference-device of figure 5.10 (c), there is no tapering in the GaAs waveguide, which means that light will remain in this layer. We have also provided a microscope image of the devices with different gap sizes between the GaAs tips, figure 5.10 (d). In the final step, the chip is cleaved into 10×10 mm^2, to fit our optical measurement setup.

5.4 Optical characterization

The optical transmission and coupling efficiency is characterized by gluing the sample on a PCB and mounting it in a chamber connected to a liquid He-flow cryostat. We carried out the transmission measurements in the optical setup shown in figure 3.1, and at low temperature (10 K), employing a supercontinuum (Super K) laser source. We begin the measurements by characterizing the transmitted light in the set of concentric waveguides. Figure 5.11 (a) presents the transmission spectra for the four inner concentric waveguides. As can be seen in the figure, the spectra has three peaks, whose relative prominence varies. Assuming that the layer stack causes some internal reflection and interference in the design, which can be modeled as a low-Q cavity in the device, we will try to determine the approximate size of the cavity that generates this effect. Considering a cavity in the device that suppresses the non-resonant modes, the spectral range between the peaks should follow:

$$\Delta\lambda_{FSR} = \frac{\lambda^2}{n_g L} \tag{5.1}$$

Where L is the distance traveled by light in one round trip around the cavity with length l, L=2l. Assuming a small dispersion in our waveguides, we consider the group index to be $n_g \approx n_{SiO2} = 2.5$, according to the COMSOL simulations of the design. So:

$$L \approx \frac{\lambda^2}{n_g \Delta\lambda_{FSR}} \tag{5.2}$$

Looking at the spectra of figure 5.11 (a), we have three peaks that are 35 nm apart, meaning $\Delta\lambda_{FSR} = 35\,\text{nm}$, Which gives $L \approx 17.1\,\mu\text{m}$ for $\lambda = 935\,\text{nm}$. Accordingly, we find the cavity length to be $l = L/2 \approx 8.5\,\mu\text{m}$, which can be the spacing between the two GaAs and the Si substrate, confirming that our first assumption was correct that these peaks can be the effect of the internal reflections coming from the layer stack.

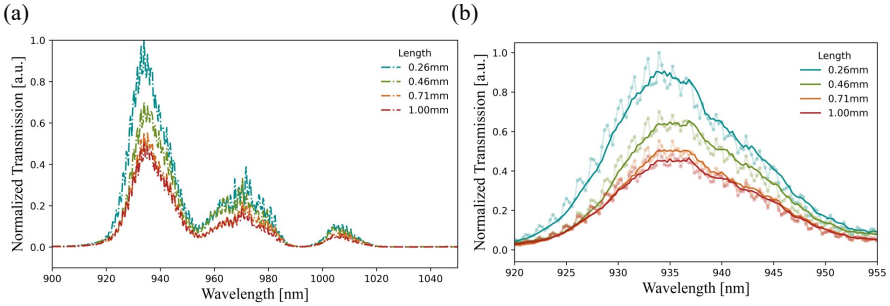

Figure 5.11: Transmission measurements in concentric waveguides. (a) Normalized Transmission spectra for the four inner concentric waveguides at cryogenic temperature. (b) The first peak in (a), which is our wavelength of interest.

To determine the propagation loss, we focused on our desired wavelength range around the first peak, as plotted in figure 5.11 (b). Figure 5.11 (c) shows the transmission, in logarithmic scale, as a function of the waveguide length. For the peak wavelength of 935 nm, a loss per unit length of $(6.9 \pm 0.7) dB/mm$ is obtained, which is compatible with previously reported results in chapter 4. For the wavelengths away from the central peak (i.e., at 925 nm and 945 nm), the loss per unit length is estimated to be $(7.7 \pm 3) dB/mm$ and $(5.7 \pm 0.9) dB/mm$, respectively. A visible wavelength-dependence is observed, with more pronounced absorption at shorter wavelength, which seems to originate from electro-absorption effect due to substrate charging during e-beam lithography [121].

5.4.1 Coupling efficiency

To estimate the coupling efficiency of the GaAs tapered waveguides, we will need a model for how the transition works. To do this, we also fabricated some reference-devices without any tapering in the GaAs waveguide, and therefore without any coupling to the underlying Si_3N_4 waveguide layer. Having the spectra for the light

transmission in the reference-devices and comparing them with the spectra of the actual devices with tapered tips allows us to account for the effect of the grating couplers and propagation losses in the GaAs waveguide and estimate the coupling efficiency. In the devices, the light travels some of its path in the low-loss Si_3N_4 waveguide instead of experiencing the higher losses in GaAs, hence, technically, it would be possible for a device to outperform the reference. Figure 5.12 (a) shows the normalized transmission spectra through two of the reference-devices (in gray). To see how the devices work, we also plotted the transmission through one of the devices with the GaAs waveguide tip width of 110 nm. The lower intensity of the transmission in actual devices compared to the reference-devices was predictable because of the GaAs-to-Si_3N_4 waveguide coupling loss. To ensure that the light behaves as predicted, i.e., it is actually coupling in and propagating a part of its path in the underlying Si_3N_4 waveguide, we fabricated some structures called uncoupled-devices (shown in figure 5.10 (b)), which are identical to the actual devices except that they are etched in locations where no Si_3N_4 waveguide is present underneath. Hence, in uncoupled-devices, we expect to have no light at the output grating coupler, which is confirmed by the measurements plotted in figure 5.12 (b).

Another source of error could be that the light might be scattered at the location of the GaAs waveguide taper tip and be captured by the other tip in front, without traveling in/out of the Si_3N_4 waveguide. To investigate this phenomenon, we considered some devices with shorter and longer gaps between the GaAs waveguide tips (17 µm and 57 µm) compared with the gap in our actual devices (37 µm), shown in 5.10 (d). If this was the case, we would expect to have a remarkable higher transmission for devices with a shorter gap compared with devices with a longer gap. Figure 5.12 (c) presents the normalized transmission spectra measured for the short- and long- gap devices. As can be seen in the figure, the transmitted intensity is similar, indicating that the scattering phenomena is not introducing a visible impact on the device performance, thanks to the cross-polarized in/out grating couplers. After checking the effect of all possible errors, we will need to model how the light propagates in the devices. As calculated in section 5.4, the propagation loss in our bonded GaAs waveguides is $(6.9 \pm 0.7) dB/mm$ in this chip. The loss in the Si_3N_4 waveguides should be on the order of at most $0.1 dB/cm$ or $0.01 dB/mm$ [124], which is low enough that we can assume to be insignificant in our calculations. Therefore, the maximal transmission through the actual devices with the tip width of W_{tip} ($T_{Dev,W_{tip}}$) relative to the average transmission among reference-devices (T_{Ref}) can be estimated solely from the path in the Si_3N_4 layer. Knowing the taper length and the gap length between the tips to be 100 µm and 37 µm, respectively, and assuming that light coupling mainly occurs at the beginning of the taper at the earliest and at the end of it at the latest, allows us to estimate

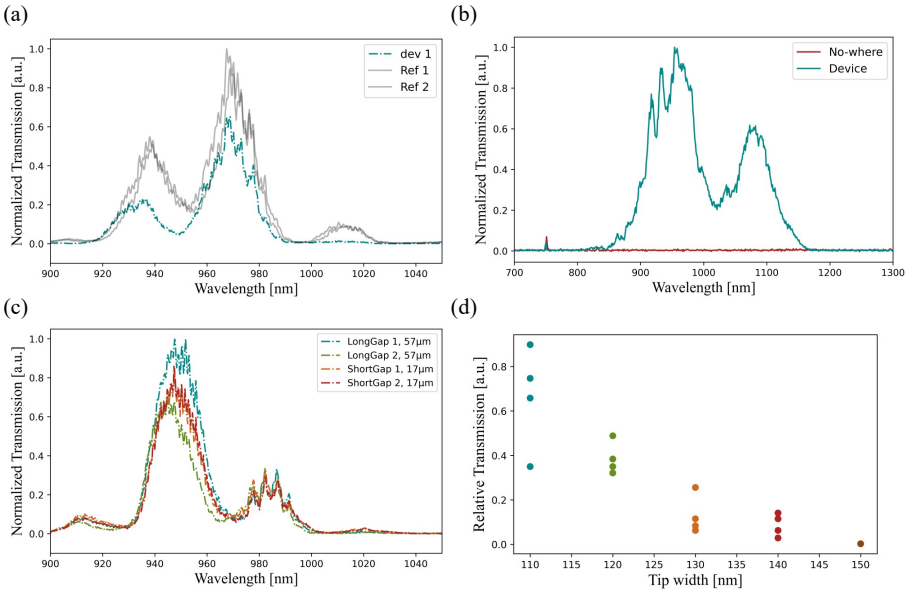

Figure 5.12: Transmission measurements through different structures on the chip. (a) Normalized transmission spectra through two of the reference-devices (without coupling to the underlying Si_3N_4 waveguide) and one of the devices (with coupling to the underlying Si_3N_4 waveguide). (b) Comparison of the transmission spectra for the actual devices and uncoupled-devices. No light is transmitted in the devices without having Si_3N_4 waveguide underneath. (c) Normalized transmission spectra for devices with short- and long-gap, to investigate the effect of the gap size between GaAs tips. (d) The ratio between transmission intensities in devices with different tip width and reference-devices ($T_{Dev,W_{tip}}/average(T_{Ref})$).

the upper and lower bounds of the extra loss incurred by the reference-devices as: $loss_{GaAs} = (0.26 - 1.64)dB$, however, according to simulations, we imagine that the adiabatic transition occurs closer to the tips and so should be in the low end of this estimate. If we want to mathematically express our description of the transmission through the reference-devices and the actual devices, we will have:

$$T_{Ref} = T_{grating,in} \cdot T_{propag,ref} \cdot T_{grating,out} \tag{5.3}$$

$$T_{Dev,W_{tip}} = T_{grating,in} \cdot T^2_{Taper,W_{tip}} \cdot T_{propag,dev} \cdot T_{grating,out} \tag{5.4}$$

With $T_{grating,in/out}$ being the grating coupling efficiency of light in/out of the device, $T_{Taper,W_{tip}}$ being the transmission of a taper with a tip width of W_{tip}, $T_{propag,ref}$ and $T_{propag,dev}$ are then representing propagation in the GaAs waveguides for the reference-

Table 5.1: The maximal and minimal estimates of the coupling efficiency based on the maximal and minimal transmission measured for each tip width. We consider a 10% error bar for the reported data, due to fluctuations in the transmission curves.

Taper tip [nm]	$MaxT_{Taper}$	$MinT_{Taper}$
110	0.92	0.57
120	0.69	0.55
130	0.49	0.24
140	0.36	0.17
150	0.05	0.05

devices and actual devices, respectively. Assuming a symmetrical tapering efficiency, leads to:

$$T_{Taper,W_{tip}} \approx \sqrt{\frac{T_{Dev,W_{tip}} \cdot T_{propag,ref}}{T_{Ref} \cdot T_{propag,dev}}} = \sqrt{\frac{T_{Dev,W_{tip}}}{T_{Ref}} \cdot 10^{\frac{-loss_{GaAs}}{10}}} \tag{5.5}$$

Where $loss_{GaAs}$ is the estimated loss in dB, avoided in actual devices compared to reference-devices. Therefore, to estimate the efficiency of the transmission through the taper in each device, we will need to measure the ratio of transmissions between the actual device and the average transmission among reference-devices, i.e., $T_{Dev,W_{tip}}/T_{Ref}$ from the transmission spectra for each device. As explained in the previous sections, we have different types of devices with a sweep in the width of their GaAs waveguide taper tips (W_{tip}), for which we have measured the transmission. Figure 5.12 (d) shows the relative transmission for each device versus the tip width in the device. Several numbers for some widths are because we had several devices with the same W_{tip} available in the chip, and we performed measurements on all of them. Different transmission intensities for different devices with the same GaAs waveguide tip width result from unwanted different alignments of the tip with the underlying Si_3N_4 waveguide or different optical alignments during measurements. Having the relative transmission, we can use equation 5.5 to estimate the coupling efficiency for each type of device. Considering the avoided GaAs loss to be closer to its lower limit, i.e., $loss_{GaAs} = 0.26dB$, we can calculate the maximum and minimum coupling efficiency for each tip width and find the optimized taper tip for future measurements. Table 5.1 summarizes the results for the description above.

In conclusion, all data sets agree that smaller taper widths in GaAs waveguides behave better in terms of transmission and coupling efficiency. The most efficient width for

the GaAs taper is 110 nm, based on the measurements. However, this trend will most likely stop for a minimal tip width, at which the effective index of refraction is very low for the light to stay in the GaAs layer and the adiabatic transition is less likely to occur.

* * *

In this chapter, we demonstrate the fabrication of GaAs waveguides aligned to Si_3N_4 waveguides embedded in a silica layer. After discussing the simulation results for designing the GaAs taper coupler, we presented the fabrication method based on the adhesive bonding of the two chips. Finally, we measured the propagation loss in this hybrid platform and investigated the light coupling between these two waveguide layers, which is a significant step toward fully scalable and hybrid QPIC technology. The efficiency measurements presented in this chapter are only one part of the story. The next step in this project would be QD excitation and single-photon emission, which require high efficiency and count rate.

Chapter 6

Micro-transfer printing of GaAs waveguides

Micro-transfer printing (uTP) is an innovative and versatile technology in the field of heterogeneous integration. In this technique, microscale components (so-called coupons) are selectively picked from their native substrate (source substrate) and printed in parallel to a new platform (target substrate). Simultaneous transfer of multiple coupons onto the target substrate can be achieved by using stamps with an array of multiple posts, making it a high-throughput process. Figure 6.1 shows the parallel micro-transfer printing of multiple coupons from two different platforms to a silicon target wafer.

In micro-transfer printing, coupons are released from their native substrate through undercut etching. Using an elastomeric stamp, manufactured by casting polydimethylsiloxane (PDMS), these coupons are picked up and transferred to a prefabricated target wafer. This process is described in more detail in the following sections. The biggest advantage of the micro-transfer printing method in heterogeneous integration is that the requirements for selectivity are greatly reduced, since its a back-end compatible process. In this method, components from different platforms, such as III-V and lithium niobate, can be combined on a single silicon photonic platform, ultimately paving the way for larger-scale quantum information processing. Unlike the adhesive bonding method, micro-transfer printing provides the possibility of prefabricating components and testing them before they are transferred. Although micro-transfer printing requires advanced tools for alignment, which makes it more expensive than the adhesive bonding method, it still introduces a relatively large misalignment. The official transfer

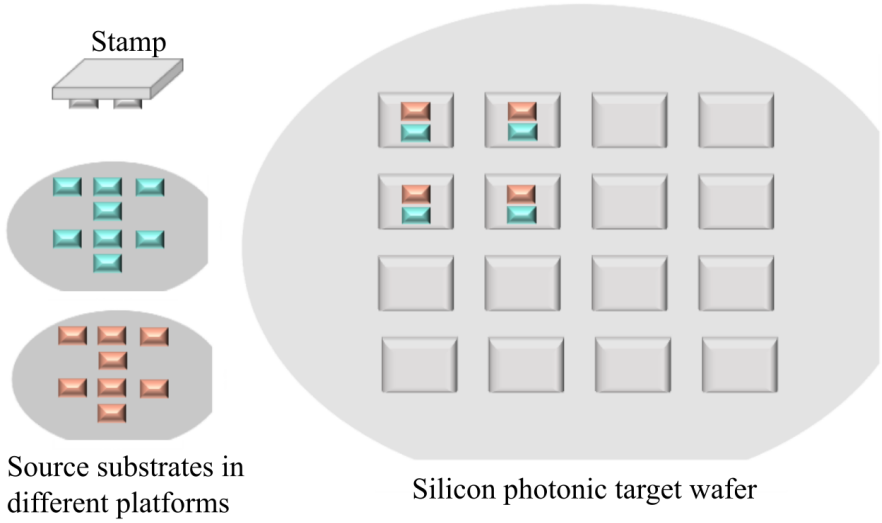

Figure 6.1: Mico-transfer printing of multiple coupons from different source substrates to a silicon photonic target wafer. The patterned stamp with multiple posts ensures the high-throughput.

printer tool used in this project claims an alignment accuracy on the order of 1 µm. The devices are designed to be tolerant to this misalignment, which involves designing longer mode coupler structures.

In this chapter, we propose the use of micro-transfer printing as an alternative approach for heterogeneous integration of GaAs waveguides on a silicon photonic platform, which is done in collaboration with Ghent University. First, we provide an overview of the fabrication of components on the GaAs source wafer. Then, there is a detailed description of the micro-transfer printing of the fabricated components on a Si-based target wafer. Finally, the quality of the micro-transfer printing, and the coupling efficiency of the waveguides is characterized.

6.1 Transfer printing of GaAs waveguides with embedded quantum dots

The components to be transferred are fabricated on an undoped GaAs wafer with a layer of embedded InAs QDs, whose layer stack is shown in figure 1.5 (b). The goal is to micro-transfer print standalone GaAs single-mode waveguides with the width and height of 300 nm and 160 nm, respectively. Here, the dimensions are much smaller than those for commonly micro-transfer printed devices, such as III-V lasers and photodiodes [125–127], which makes the process more delicate and challenging. Double-sided tapered GaAs nanobeam waveguides, with the dimensions shown in

figure 6.2 (a) are designed to be printed on top of Si_3N_4 waveguides. The tapering section in the GaAs waveguide, behaves like a mode-transfer, to couple the light between the GaAs and Si_3N_4 waveguide layers. The linear mode couplers in GaAs are designed to be tolerant to misalignment, based on finite-difference time-domain (FDTD) and eigen-mode-expansion (EME) Lumerical simulations done by our collaborators at Ghent University. Figure 6.2 (c) presents the simulation results for the coupling efficiency as a function of the misalignment between the GaAs and Si_3N_4 waveguides (δ in figure 6.2 (b)), including a rough estimate of the propagation losses. In the optimization of the linear taper coupler, there is a trade-off between the coupling efficiency and the propagation loss over its length. The 300 nm-width GaAs waveguide is designed to taper down to 200 nm in a short length of 5 µm, while the light is still confined in the GaAs waveguide layer. For the GaAs waveguide width of $\approx$ 150 nm, due to the index matching between the two waveguide layers, the light starts to couple between the two waveguides. Therefore, to have an adiabatic mode transfer, we taper the GaAs waveguide from the width of 200 nm to 115 nm with a gentel slope and in a length of 35 µm . For the GaAs width less than 115 nm, the light is compeletely confined in the Si_3N_4 waveguide. However, we further taper the GaAs waveguide to a final width of 60 nm in a short length of 5 µm, to minimize the possible reflections at the taper tip. As can be seen in the figure 6.2 (c), the designed linear taper coupler is relatively tolerant to misalignment.

After designing the main GaAs waveguides and the tapered couplers, we also added some pads around them. These extra GaAs pads can be used for the fabrication of metal contacts for future works with doped GaAs wafers. Moreover, they can improve our vision of where the nanobeam waveguides are located during micro-transfer printing. Although picking, transferring, and printing could be successfully done without these frames, they make the coupons even more stiff and lower their risk of collaps. The GaAs waveguides are patterned using e-beam lithography followed by RIE, as explained in chapter 2 of this thesis. Figure 6.3 (a) shows an optical microscope image of the double-sided tapered GaAs nanobeam waveguide. The SEM image of the taper tip is presented in figure 6.3 (b), showing that the 60 nm-tip could be successfully fabricated, while the imperfect sidewalls might cause scattering, which affects the coupling efficiency. The same nanobeam waveguide of figure (a) is fabricated with GaAs pads connected to it using tethers (which are copies of the tethers in the monolithical suspended GaAs waveguides), as shown in the microscope and SEM images of figures 6.3 (c) and (d), respectively.

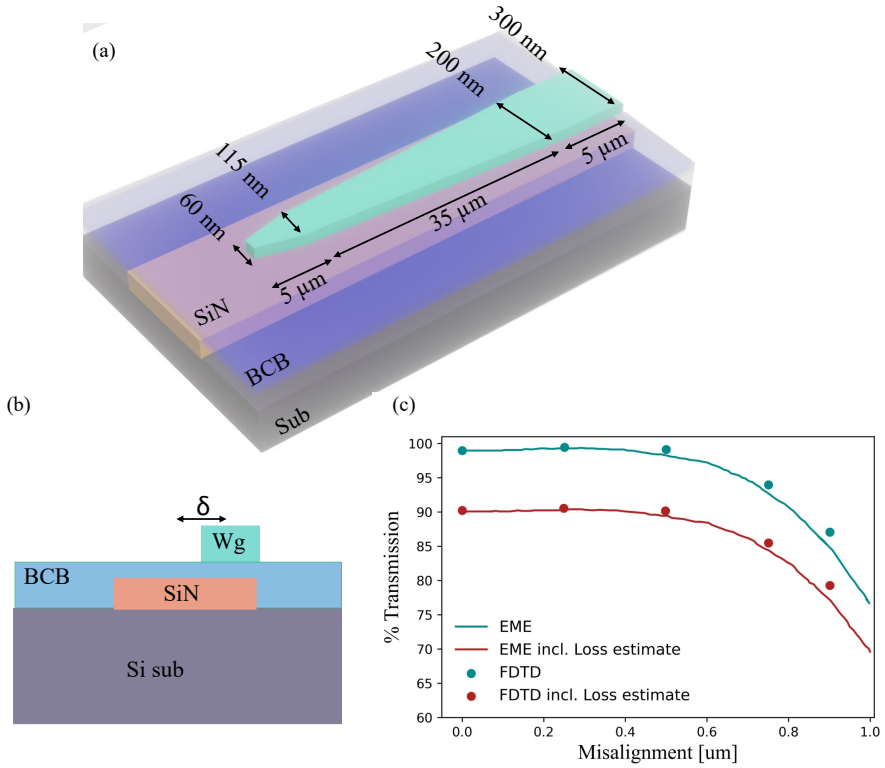

Figure 6.2: (a) 3D schematic of the linear taper structure for coupling the light between the GaAs and Si_3N_4 waveguide layers. (b) cross-sectional view of the structure, showing the possible missalignment between the two heteogeneously integrated waveguides. Simulation results for the coupling between the two waveguide layers as a function of misalignment, including a rough estimate for the propagation losses. Simulation courtesy of Jasper De Witte, Ghent University.

6.1.1 Transfer-printing process

The concept of micro-transfer printing of the prefabricated GaAs waveguides from their native substrate to a Si-based target substrate is illustrated in figure 6.4. This process involves several key steps, as described below.

- **Preparation of the source and target substrates:** The process begins with the pre-fabrication of GaAs components on their native substrate. The double-sided tapered GaAs nanobeam waveguides are fabricated in our cleanroom as explained in the previous section, and the wafer is taken to the cleanroom in Ghent University for further processing in collaboration with our collaborators. The target wafer contains arrays of Si_3N_4 waveguides patterned in a 300 nm-thick

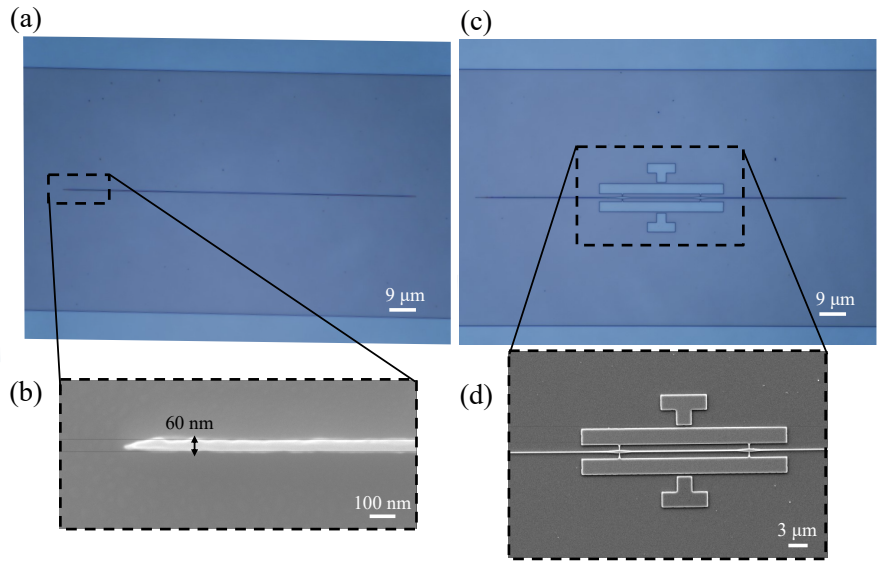

Figure 6.3: Fabricated waveguides on the GaAs source substrate. (a) Optical microscope image of the double-sided tapered waveguide. (b) SEM image of the taper tip. (c) Optical microscope image of the waveguide with pads. (d) SEM image of (a), showing the tethers connecting the waveguide to the pads.

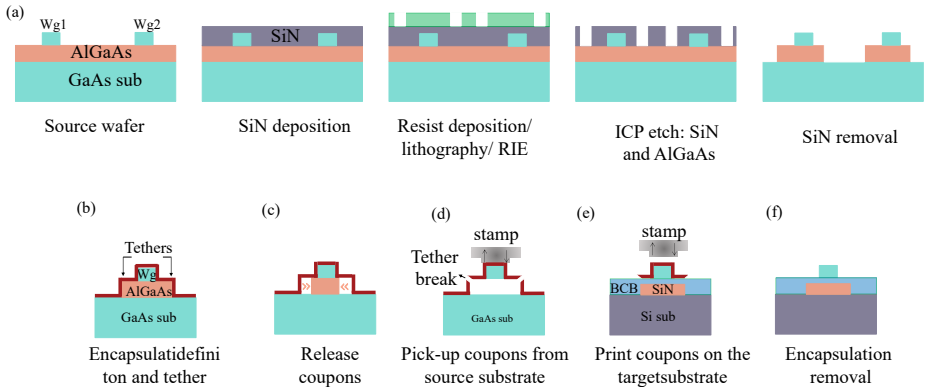

Figure 6.4: Schematic overview of the required steps in micro-transfer printing. (a) processing steps for coupon definition. (b) Encapsulation of the coupons with photoresist. (c) Underetch removal of the release layer. (d) Pick up the coupon with the stamp, while breaking the tethers. (e) Print the coupon aligned to the Si_3N_4 waveguide in the target substrate. (f) Removal of the encapsulation layer.

LPCVD Si_3N_4 layer via e-beam lithography followed by RIE. Before loading in the micro-transfer printer, the target wafer is spin-coated with a 50 nm-thick

BCB bonding layer. The thickness of the bonding layer can be controlled by dilution in mesitylene [128].

- **Coupon patterning on the source wafer:** Figure 6.4 (a) schematically illustrates the process flow for the coupon definition in the source substrate. To define GaAs waveguides as separate coupons ready for micro-transfer printing, the whole wafer (or chip) is protected by deposition of 500 nm silicon nitride hard mask layer using PECVD (plasma enhanced chemical vapor deposition). This is followed by the spin coating and patterning of the photoresist (AZ5214). Subsequently, we pattern the silicon nitride hard mask via RIE etching and removing the resist. Finally, we make openings to the substrate by ICP etching of the AlGaAs layer and defined the waveguides as separated coupons to be transferred.

- **Encapsulation:** The entire coupon is encapsulated with a layer of 3.2 µm-thick photoresist (TI35E from MicroChemicals), and tethers are formed to hold up the coupon, as shown in figure 6.4 (b). Photoresist encapsulation has two main functions in this approach; it is HCl-resistance and protects the coupons during release etch, moreover, it forms anchor pads and tethers the coupons to these anchors. The tethers, which interconnect the coupons and anchors, can have different size and topography depending on the size of the coupons. Several designs were tested in this work by our collaborators at Ghent University to optimize the tethers to have the best yield.

- **Release etch:** The used GaAs wafer contains a 1371 nm-thick AlGaAs layer, which acts as the release layer. Diluted hydrochloric acid HCl:H_2O (1:1) is used at low temperature (5 °C) to selectively etch away the release layer, which takes approximately 160 min. Generally, HF is used to remove the AlGaAs release layer, however, we found that the photoresist better survives this underetch process when using diluted HCl. After removing the release layer, the coupons are held by the tethers anchored to the substrate, as shown in figure 6.4 (c).

Once the coupons have been suspended, the actual transferring can take place. To pick up the coupons from the source substrate and print them on the target substrate, there are three coordinate systems; the stamp, the source substrate, and the target substrate. Figure 6.5 depicts the micro-transfer printing tool used in this study, highlighting the holders for the three key elements, i.e., stamp, source substrate, and target substrate. Micro-transfer printing relies on the rate-dependent adhesion strength between the coupon and the elastomer stamp (here polydimethylsiloxane, PDMS). According to its viscoelastic properties, PDMS is much stiffer and acts as an elastic material, when

stress is applied in a quick manner. Conversely, when the stress changes very slowly, it becomes viscous [128]. The same effect is used in micro-transfer printing for adhesion between the stamp and coupon surface. The PDMS stamp exhibits high adhesion to the coupon when it is pulled away quickly, where it can also break the tethers and pick up the coupon. The adhesion will be low when it is retracted slowly during the printing process.

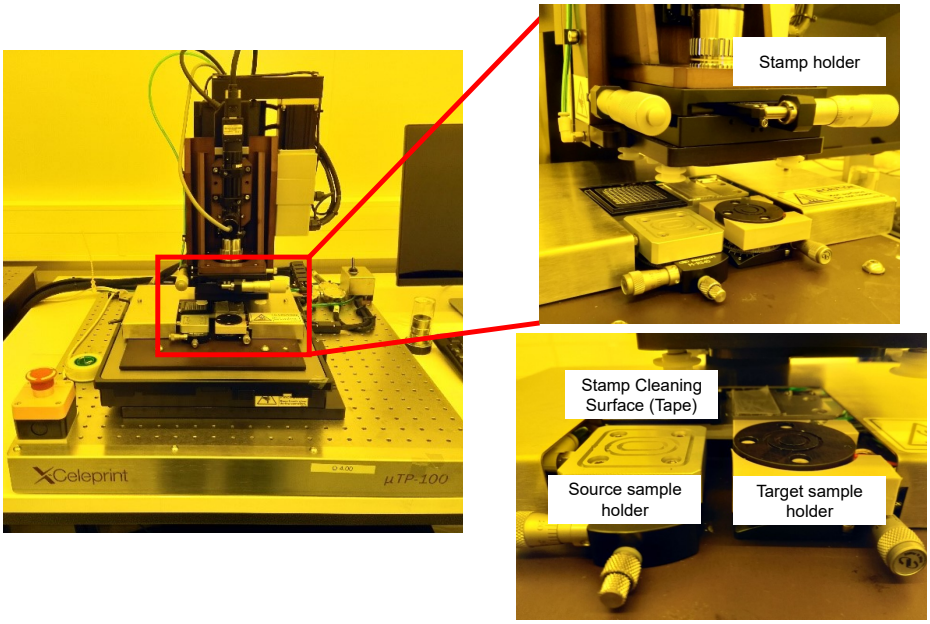

Figure 6.5: Micro-transfer printing tool used in this project. Showing the three coordinates systems; the stamp holder, the source sample holder, and the target sample holder.

- **Pick up the coupons:** The stamp is lowered until 100 µm above the coupon to complete the alignment between the stamp and the source substrate coordinate system. Then, it is further lowered slowly until it touches the coupon. As shown in figure 6.4 (d), by retracting the stamp rapidly from the coupon, the tethers break and the coupon sticks to the stamp as it moves upward.
- **Printing the coupons:** Using a mechanical motion, the coupon, which is now adhered to the stamp post, can be transferred to the desired Si_3N_4 waveguide in the target substrate. The stamp, together with the coupon stuck to it, are lowered until 100 µm above the target substrate. The stamp coordinate system can be aligned with the target coordinate system using a visual pattern recognition

system. Once the alignment is complete, the stamp moves further downward to touch the target substrate. Then, a shear force helps peel the coupon off the stamp during its upward movement. The printing step is schematically illustrated in figure 6.4 (e).

- **Post-printing treatment:** After printing the GaAs components on the target Si-based substrate, the first step is to remove the photoresist encapsulation via 60 min oxygen plasma. We avoid rinsing it in acetone to minimize the risk of delaminating the coupons. Subsequently, to strengthen the bonding, the BCB bonding layer is cured up to 280 °C in a duration of two hours.

6.2 Discussion

Micro-transfer printing of standalone double-sided tapered GaAs waveguides on Si_3N_4 waveguides was successfully performed in this project. The GaAs waveguide is printed with a lateral accuracy better than 750 nm. Figure 6.6 (b) shows the microscope image of a Si_3N_4 waveguide together with its grating coupler, on which the GaAs waveguide is transferred. Optical microscope images of the GaAs waveguides printed aligned to Si_3N_4 waveguides is presented in figures 6.6 (c) and (d). The quality of the GaAs taper tip after micro-transfer printing is illustrated in the SEM image of figure 6.6 (e)

This project aims the integration of efficient single-photon sources demonstrated in the suspended GaAs platform on low-loss Si_3N_4 waveguides, to realize a low-loss quantum photonic processor with on-chip single-photon sources. As schematically shown in figure 6.6 (f), the pump laser is sent through Si_3N_4 waveguide and couples to the GaAs waveguide on top, via the coupler region. The light incidents the embedded QD in the GaAs waveguide and interacts with it, leading to single-photon emission. The emitted photons couple back to the Si_3N_4 waveguide, where they can propagate with lower loss compared to the GaAs waveguide. At this step of the project, we focus on developing a reliable process for micro-transfer printing of such small coupons and coupling the light between the two waveguide layers. The excitation of the QD and single-photon emission will be the next step, out of the scope of this thesis. Room temperature transmission measurement is performed by sending the supercontinuum laser at 950 nm. The light is propagating following the path in figure 6.6 (f), couping to the GaAs waveguide, propagating in the 120 µm-long GaAs waveguide, and coupling back to the Si_3N_4 waveguide. Where we measured the overall loss of $\approx$ 3 dB per device, which includes propagation loss as well as in- and out-coupling losses.

* * *

In conclusion, in this chapter, we proposed micro-transfer printing technique as an alternative method to adhesive bonding for heterogeneous integration of GaAs double-sided

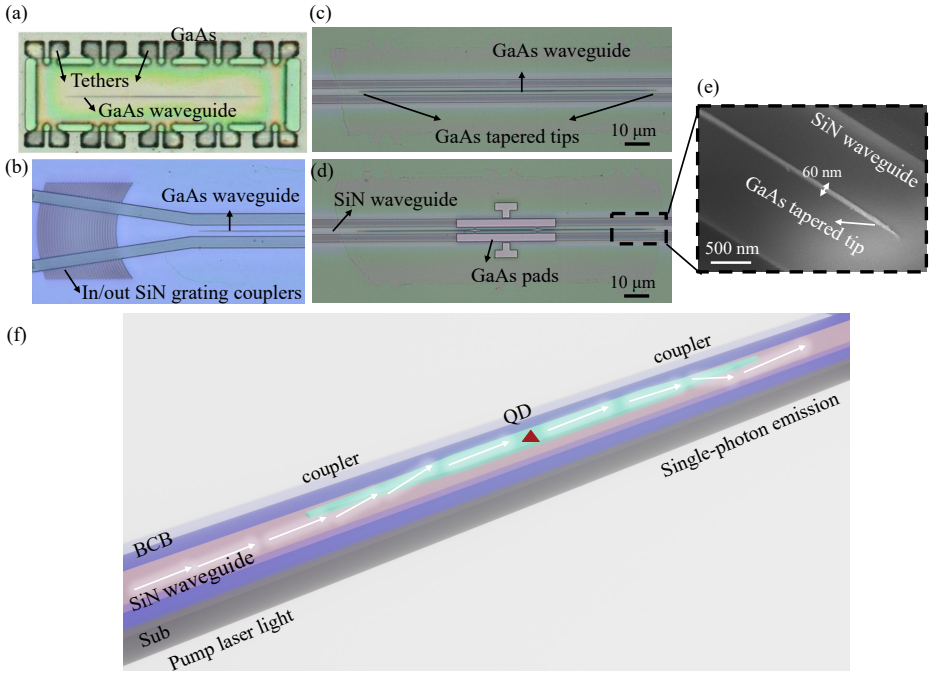

Figure 6.6: Micro-transfer printing results. (a) Optical microscope image of the underetched coupon on the source substrate, ready for micro-transfer printing, adopted from [129]. (b) Optical microscope image of the Si_3N_4 waveguide and its in/out grating coupler in the target substrate, on which the GaAs waveguide is printed. Optical microscope image of the transfer printed GaAs waveguides (c) without and (d) with pads, aligned to the Si_3N_4 waveguides. The alignment accuracy is better than 750 nm. (e) SEM image of the GaAs tapered tip after micro-transfer printing. (f) 3D schematic view of the GaAs double-sided tapered nanobeam waveguide with embedded QD, transfer printed on the Si_3N_4 waveguide, showing the path expected for the light to propagate (white arrows). Microscope images courtesy of Jasper De Witte, Ghent University.

tapered nanobeam waveguides with embedded QDs, on low-loss Si_3N_4 waveguides. This work is done in collaboration with Ghent University, where I spent my external stay as a PhD student. In this project, we transfer printed small standalone nanobeam waveguides for the first time. By designing the tapered couplers, we coupled light between the two waveguide layers and measured an overall loss of 3 dB per device, that includes propagation loss as well as the in- and out-coupling losses. The next steps for this project will be the integration of GaAs waveguides with metal contacts on Si_3N_4 waveguides and QD excitation.

CHAPTER 7

Conclusion ans outlook

7.1 Conclusion and outlook

In this thesis, we investigated the heterogeneous integration of GaAs waveguides with embedded self-assembled InAs QDs on silicon photonic circuits, which is an important step toward the realization of a fully integrated quantum photonic system capable of performing complex functionalities. An overview of the key outcomes of this thesis is presented below:

- We developed a method to transfer a GaAs membrane with embedded QDs onto a silica substrate using the adhesive bonding method. On this hybrid platform, GaAs nanobeam waveguides and small features, such as photonic crystals and grating couplers could be successfully fabricated via a series of e-beam lithography followed by RIE. The quality of the fabrication process is validated by a set of AFM and SEM scans. The optical measurements at both room and cryogenic temperatures showed that the propagation loss in this hybrid GaAs-on-Si platform presented here is compatible with the loss measured for the traditional suspended waveguides. We excited the QDs in the above-band excitation scheme, where the anti-bunching dip in the HBT measurement confirms the single-photon nature of the emitted signal. Therefore, GaAs-based waveguide circuits with single-photon emitters could be heterogeneously integrated on a si-based platform without degradation of performance, compared to traditional suspended waveguides.
- The heterogeneous integration of GaAs waveguides on top of Si_3N_4 waveguides embedded in a silica box is presented. We proposed a new method for the

alignment of the GaAs waveguides to the underlying Si_3N_4 waveguides with e-beam vision, resulting in a high alignment accuracy as good as 10 nm. To couple the light between the two waveguide layers, we designed adiabatic tapered coupler in GaAs waveguide, with a sweep in the tapered tip. According to optical measurements, we had higher transmission intensity for smaller taper tips. Howerver, we are aware that this trend will stop soon, because for very small tips, we will lose the adiabatic performance of the tapered coupler. We estimated an upper and lower limit for the coupling efficiency of each device type.

- As an alternative method for adhesive bonding, we proposed micro-transfer printing technique for heterogeneous integration of GaAs waveguides on Si_3N_4 waveguides. In this study, we designed double-sided tapered GaAs nanobeam waveguides with embedded QDs, which are tolerant to misalignment, and fabricated them on an undoped GaAs wafer. In collaboration with Ghent University, we could transfer print small standalone nanobeam waveguides for the first time, with an alignment accuracy better than 750 nm. We measured light transmission with a mean overall loss of 3 dB per device, including in- and out-coupling and propagation losses of the 120 µm-long waveguide device.

7.2 Outlook

The successful fabrication of single-photon emitters on a hybrid GaAs-on-Si substrate has been demonstrated in this thesis. However, in the HBT experiment, the low number of counts and relatively high dark counts do not allow us to observe the peak at zero time delay and to extract the exact value of $g^2(0)$. Therefore, the setup efficiency needs to be improved. We can replace the grating filter used in this project with an etalon filter, a temperature-tunable Fabry-Perot filter made of silica, which has a higher efficiency and smaller bandwidth. Moreover, the APDs in the HBT measurement can be replaced with SNSPDs (superconducting single photon detectors), which offer higher efficiency, better timing resolution, and more importantly very few dark counts.

7.2.1 Heterogeneous integration of electrically contacted QDs in p-i-n junctions

Another important characteristic of single-photon emitters is their indistinguishability, which we could not characterize in this thesis due to transferring undoped GaAs membrane. Future work will investigate the transfer of p-i-n heterostructure GaAs membranes, which enables fabrication of electrically-gated p-i-n junctions. Transferring a p-i-n heterostructure membrane allows the fabrication of electrical contacts

to apply voltage, offering the opportunity to stark-tune the emission frequency of the QD. Fabrication of devices with high-quality diode behavior is crucial for realizing indistinguishable single-photon sources, as it can minimize the decoherence resulting from charge noise, by controlling the charge surroundings of the QDs.

In adhesive bonding, the unprocessed p-i-n heterostructure GaAs wafer can be bonded to the Si-based chip. After removing the backside substrate, the p- and n-metal contacts will be fabricated via two separate series of e-beam lithography, RIE, and metal deposition.

In micro-transfer printing, in the doped GaAs wafer as the source substrate, the p-i-n diode can be fabricated on the pads around the waveguide. The waveguide with its p- and n-metal contacts can be transferred to the target wafer. After transfer printing, new bridge contacts will be defined on top of the transferred p-i-n diode in GaAs. Figure 7.1 depicts the mask designed for transfer printing of the GaAs waveguides with p-i-n diodes, and the bridge contacts to be added after transfer printing.

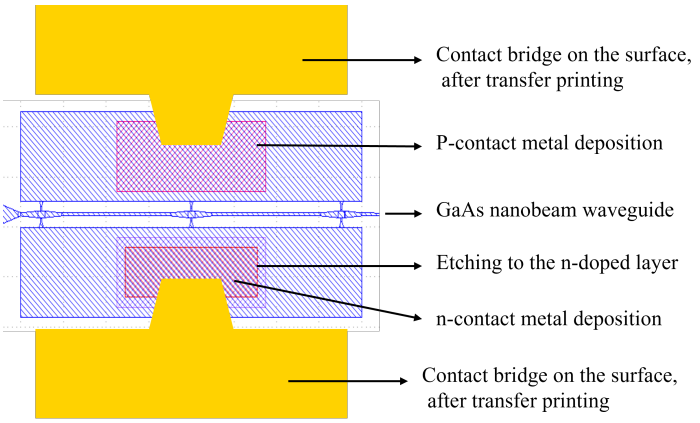

Figure 7.1: Mask designed for the transfer printing of GaAs waveguides together with p- and n- metal contacts. The yellow region, shows the bridge contact, defined with metal deposition, after transfer printing.

Appendix

.1 Layer structure of the wafer

Material Thickness (nm)	Doping (cm^{-3})	
GaAs	81	intrinsic
InAs QDs		
GaAs	79	intrinsic
$Al_{0.77}Ga_{0.23}As$	1371	intrinsic
GaAs	substrate	Undoped

.2 Optimized recipe for processing GaAs devices

.2.1 Recipe for adhesive bonding of the GaAs and Si-based chips

Si-based chip preparation

1. Pre-clean the 10 mm×10 mm chip: immerse in Acetone, Isopropanol (IPA), and millipore water (MQ) (each for 2 min@37 kHz and 80 % power). Blow dry by Nitrogen (N_2) gas.
2. Dehydrate: bake at 185 °C for 5 min on a hot plate.
3. Surface Preparation with O_2 Plasma: perform O_2 plasma on dried sample for 1 min (50 W RF, 3 mbar).

GaAs chip preparation

1. Cleave a chip of ≈ 8 mm×8 mm from the undoped GaAs wafer with embedded self-assembled QDs.
2. Pre-clean the 8 mm×8 mm chip: immerse in Acetone, Isopropanol (IPA), and millipore water (MQ) (each for 2 min). Blow dry by Nitrogen (N_2) gas.
3. Dehydrate: bake at 185 °C for 5 min on a hot plate.
4. Resist spin-coat: spin-coat $\gamma - Butyrolactone : mr - DWL(1:3)$ at 3000 (rpm) for1 min. The spin coating speed should be modified each time the diluted solution is made, since it depends on how old the resist is and how accurate it is diluted. Adjusting the appropriate dilution and spinning speed should result in the resist thickness ~ 160 nm afer baking (220 nm before baking).

5. Bonding: right after spin-coating of the resist on the Si-based chip, the GaAs chip is flipped and placed at the center of it. A manual alignment is sufficient at this step. Possible small rotation might occur while mating the two surfaces, which should not make any problem.

6. Resist soft and hard baking: place the bonded chips on a 60 °C pre-heated programmable hot plate, and run the program for a ramped hard baking of the mr-DWL resist. A small 0.5kg weight is placed on top of the bonded chips to apply a pressure equivalent to . The baking program is: 2 min at 60 °C, 10 sec at 75 °C, 2 min at 60 °C, 4 min at 90 °C, 2 min at 100 °C, 5 min at 120 °C, 5 min at 130 °C, 20 min at 140 °C, while the hot-plate ramps up the temperature between each step.

7. Sample cool down: after hard baking, the sample remains at room temperature to cool down before continuing.

Wet etching of the GaAs backside substrate

1. Fast non-selective etch of GaAs in a nitric acid-based solution : immerse the bonded sample in a solution of $1HNO_3$:$4H_2O_2$:$1H_2O$ for 115 min. This solution is not selective and has an etching rate of $\sim 5\,\mu m/min$, so $\sim 565\,\mu m$ of the $\sim 630\,\mu m$-thick GaAs substrate will be etched. At this step, the surface looks shiny gray, ensuring that there is still some GaAs left.

2. Rinse in MQ water: rinse the sample in two seperate beakers of MQ water, at least 4 min in each, followed by gentle blow dry with (N_2) gas.

3. Etching of the AlGaAs layer in cold HCl: immerse the sample in a 2 °C HCl, until the sample looks shiny gray again. It approximately takes 15 min. Rinse in MQ water same as the previous steps and gentle blow dry with (N_2) gas.

4. Check in optical microscope to evaluate the quality of the transferred membrane.

.2.2 Recipe for patterning nanostructures

Definition of the align marks

1. Dehydrate: bake the bonded sample from the previous step at 185 °C for 5 min on a hot plate, to completely dehydrate it.

2. Resist spin-coat: spin-coat CSAR 13 at 2200 (rpm) for1 min. Followed by 1 min soft bake at 185 °C. Expected thickness: 550 nm.

3. Electron beam lithography: e-beam exposure using Elionix ELS-F125, with: current 10 nA, dose 250 μC/cm^2, pitch 8.

4. Resist development: immerse the exposed sample in n-Amylacetate for 60s at room temperature, rinse in IPA for 10s, blow dry using N_2. Finally, descum in O_2 plasma (100W, 1 minute) to remove organic residues from the exposed/developed regions. O_2 plasma also activates the surface to be ready for the metal deposition.

5. Metal deposition: Using an e-beam evaporator tool and in a vaccum chamber at or below 1×10^{-7}, deposit a 10 nm layer of Cr, to improve the adhesion. Immediately and without breaking vacuum, deposit 170 nm layer of Au.

6. Resist lift-off: Soak the sample in 1,3-Dioxolane (I-III Diox) for 10 min, blow in the solution with pipet until all metal layers are removed. Rinse in IPA followed by blow dry with (N_2) gas.

Patterning Shallow Etch Gratings (SEGs)

1. Sample preparation and resist spin-coat: dehydrate the sample at 185 °C for 5 min. Spin-coat CSAR 9 at 4000 (rpm) for1 min. Followed by 1 min soft bake at 185 °C. Expected thickness: 200 nm.

2. Electron beam lithography: e-beam exposure using Elionix ELS-F125, with: current 10 nA, dose 350 μC/cm^2, pitch 8.

3. Resist cold development: immerse the exposed sample in −5 °C n-Amylacetate for 40s at room temperature, rinse in −5 °C IPA for 20s, blow dry using N_2.

4. RIE etching: using a small drop of Fomblin oil, mount the sample to the Si wafer carrier, and load in the RIE tool. By pre-conditioning, set the chamber temperature and pressure to be 15 °C and 10 m Torr, respectively. Perform a standard BCl_3 (5 sccm)/Ar (10 sccm), targetting the etch depth of 70-80 nm.

5. Resist strip: soak the sample in 70 °C NMP for 10 min, followed by room temperature NMP for 2 min. Finally rinse in IPA and blow dry using N_2.

6. Check the etch depth by profilometer.

Patterning photonic crystals and waveguides

1. Sample preparation and resist spin-coat: dehydrate the sample at 185 °C for 5 min. Spin-coat t ZEP 520A at 2200 (rpm) for1 min. Followed by 5 min soft bake at 185 °C. Expected thickness: 550 nm.

2. Electron beam lithography: e-beam exposure using Elionix ELS-F125, with: current 1 nA, dose 350 μC/cm^2, pitch 4.
3. Resist cold development: immerse the exposed sample in $-5\,^{\circ}$C n-Amylacetate for 40s at room temperature, rinse in $-5\,^{\circ}$C IPA for 20s, blow dry using N_2.
4. RIE etching: similar process as the previous step, but for a longer time to deeply etch the whole 160 nm GaAS.
5. Resist strip: soak the sample in 70 °C NMP for 10 min, followed by room temperature NMP for 2 min. Finally rinse in IPA and blow dry using N_2.
6. Check the etch depth by profilometer.

Final sample cleaving

1. After compeleting the fabrication process, cleave the smaple to $\approx$ 4 mm×4 mm, to fit in the flow-cryo chamber for optical measurements.

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