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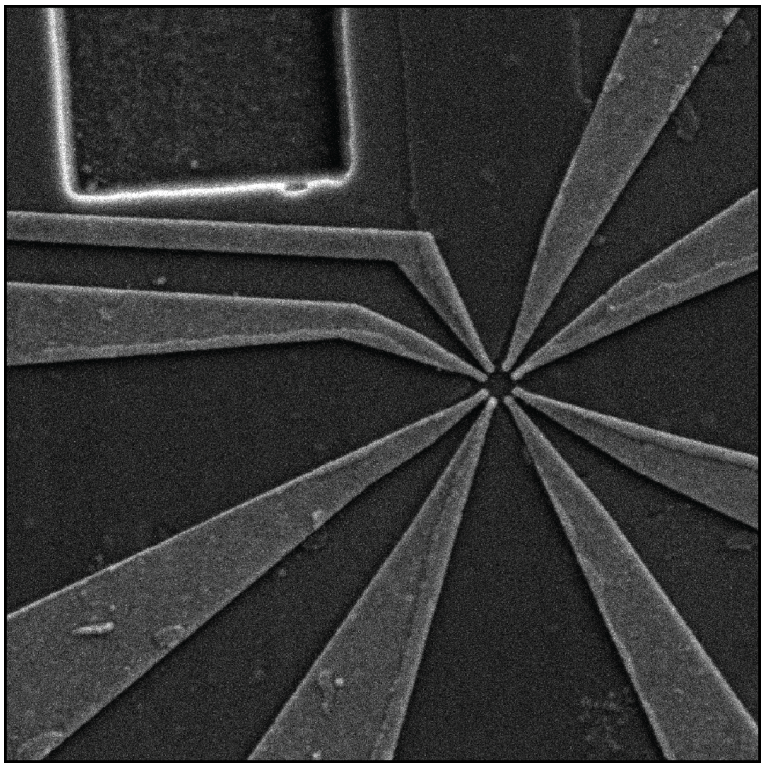

Master thesis

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Multi Terminal Josephson Junctions

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Abstract

Topological phases of matter are interesting because they are theorized to be usable for storing quantum information. This project set out to investigate a theory by Riwar *et al* [1] that an artificial topologically non-trivial material could be made by modulating the superconducting phases in a system made of a weak link connected to at least four superconductors. For some scattering matrices the Andreev bound state spectrum would undergo topological transitions through Weyl points. The system could be significantly simplified while maintaining topological transitions by reducing the number of conducting channels in each terminal to one.

This project set out fabricate devices that fill the criteria of Riwar *et al*. In an effort to build upon an understanding of the simplest case, the project focused on 4-terminal devices. These 4-terminal devices could be realized on a semiconductor substrate with a high mobility 2DEG below the surface with a layer epitaxial aluminum on top. The 4-terminal devices were formed through a series of fabrication steps including electron beam lithography, wet etching, atomic layer deposition and metal evaporation. This thesis will first give a detailed explanation on how the the devices were fabricated. The later parts of the thesis explain how measurements were carried out on the devices and what could be learned from those measurements.

While Andreev bound states were observed in source-drain bias spectra, there was no measurable response to phase modulation. This is thought to be the results of defects made during the semiconductor growth breaking the phase coherence of the aluminum on top. Although the project did not reach the goal of creating a device that could host Weyl points, a lot of knowledge was acquired on how the conductance in a 4-terminal systems with quantum point contacts behave. Ideas for improving the design and in general to move closer to an artificial topological matter is suggested in the conclusion.

1 Introduction

Science has often been directed by the environment surrounding humans. Most research is either to understand or to improve some aspect of the human experience. In modern times the human experience is closely tied to the electronic tools that are used. Computers provide a means of communications, entertainment, and for many people even a work space.
Semiconductor and superconductor physics research has long been motivated by the electronics industry. Since the first transistor was made, mankind has hungered for smaller or faster electronics. This quest for better electronics was described in 1965 by Gordon Moore [2] with him theorizing that the number of integrated circuits on a single chip would double every two years. This would go on to be known as Moore's law. For over 50 years Moore's law has been the benchmark of the industry and a large part of solid state physics has been devoted to making circuits smaller or more energy efficient.

In recent years, the development of quantum information technology has started to gain momentum. The idea that instead of classical bits, information is held by quantum states known as qubits was proposed in 1995 by B. Schumacher [3]. Quantum information would take advantage of quantum entanglement and the fact that the quantum state does not have to be "0" or "1" but can also be a superposition of the two. A lot of the mass appeal of quantum computers stem from Shor's algorithm [4], which can be used to break commonly used RSA encryption. The algorithm relies on entanglement and superposition of states to factor a prime number into two other prime numbers, a problem which is "hard" (it scales exponentially with the number of bits) on a classical computer. In comparison this problem is "easy" (scaling polynomially) on a quantum computer. Although Shor's algorithm is probably the best known feature of a quantum computer, several other proposed algorithms have been proposed like Grover's algorithm for searching a database [5].

With the growing interest in quantum computer several different ideas for platforms have been suggested. These platforms used a variety of materials from ions in a lattice [6, 7] using lasers, to platforms more using the same kind of semiconductor materials of classical computers in the form of spin qubits [8–10] or superconducting charge qubits [11,12]. A big problem for applied quantum mechanics is decoherence. The ideal world where a quantum state does not decohere does not exist. There will always be a coupling to the environment. It is clear that the state of a qubit needs to be stable for the entire operation. A class of particularly robust materials are topological materials.

Quantum states in a topological regime require a big change in order to be affected. These materials then allow for quantum states that are stable, but can still be changed by putting it into another topological state. Different schemes have been suggested to take advantage of topological states. One scheme is to use Majorana fermionic bound states at the edges of a topological superconductor [13, 14]. Another system that could host topological states are based on Josephson junctions with several terminals [1, 15, 16].

This project will focus on the fabrication of 4-terminal devices and attempt to experimentally find the topological states described by the theoretical work of Riwar *et al* [1]. The 4-terminal devices were made by wet-etching a pattern made by electron beam lithography. The used substrate was a stack of different semiconductors that form a 2-dimensional electron gas buried below the surface. The stack was capped with epitaxial aluminum, that could be etched away with high precision, forming a Josephson junction shared by 4 superconducting terminal. The devices were be cooled down in a cryo-free dilution refrigerator, reaching base temperatures of < 20 mK, before being measured using phase sensitive detection.

This thesis describes the work performed in this project over the course of several sections. Section 2 will give an introduction to the materials used and why they were used over other materials. It will also contain an introduction to some of the theoretical physics relevant for this project, including a how the topology of the system is expressed and how to measure it. Section 3 will first give a brief overview of the general concept of the fabrication methods and instruments used for fabricating the devices. It will go on to meticulously describe each fabrication step in the process, including the thought process behind some of the steps. It will finish by summarizing the fabrication recipe in a simplified form.
Section 6 will focus on the inner workings of a cryo-free dilution cryostat, including how it works, how to operate it and how to maintain it. The section also includes some of the ways the cryostat was modified to better suit the needs of the project. Section 7 will explain how the measurement were set up, describing which instruments were used and how they were connected, but also how to use the instruments to measure different effects. Section 8 will show the results of different measurements carried out during the project and interpret the data. Finally section 9 will summarize what can be concluded from this project and give an outlook to some of the possible ways to further investigate the presence of artificial topological phases in multi terminal Josephson junctions.

2 Background theory

In this section an introduction will be given to the fundamental physics relevant for this project. The first part will focus on superconductors and their physics. It will start on the unique properties of superconductors and then move on to more complex cases of what happens when superconductors and semiconductors interact with each other. The next part will be about quantum point contacts, what they are and why they are interesting in the scope of this project. Lastly, an overview will be given of the material that was used in this project, why it was chosen and what other alternatives were considered.

2.1 Superconductor basics

Superconductors have many properties of which not all will be covered in this thesis. One important property and the namesake of superconductors is perfect conductivity. The property that below some transition temperature T_C, there is zero resistance in the metal. This effect was theoretically modeled by Bardeen, Cooper and Schrieffer in 1957. They made a model (known as the BCS model) off electrons pairing up instead of repelling each other. These pairs are made from electrons with opposite momentum and spin, forming a bosonic particle known as a Cooper pair. The attraction can be understood by electrons attracting the positive ion cores, which then attract another electron. Under the right circumstances, the attraction is greater than the repulsion of the electrons leading to the formation of the Cooper pair. In conventionally used superconductors such as aluminum, niobium or lead, this interaction is mediated by phonons.

In order to describe all of the Cooper pairs that condensate to form the superconductor, it is useful to use a many-particle wavefunction.

$$\psi(\mathbf{r}) \equiv |\psi(\mathbf{r})|\mathbf{e}^{\mathbf{i}\varphi(\mathbf{r})} \tag{1}$$

Like other wavefunctions, it can be described with a spatial element and a phase is more relevant for this project. The wavefunction is periodic in the superconducting phase with a period of 2π. The phase of a superconductor can be altered by catching magnetic flux in a ring of superconducting material. The quantity required to change the phase by 2π is called a flux quantum Φ_0 and is independent of material.

$$\Phi_0 = \frac{h}{2e} = 2.06782810^{-15}\text{Wb} \tag{2}$$

By applying BCS theory[1], one can find that superconductors have quasi-particle excitations that can be describe with the following energy [17]:

$$E_{\mathbf{k}} = (\xi_{\mathbf{k}}^2 + |\Delta_{\mathbf{k}}^2|)^{1/2} \tag{3}$$

Where $\xi_{\mathbf{k}} = \epsilon_{\mathbf{k}} - \mu$ is the single particle energy relative to the fermi energy and $\Delta_{\mathbf{k}}$

[1]Full derivation can be found in Michael Tinkham's "Introduction to Superconductivity" citation [17]

is a minimum energy excitation. This minimum energy is commonly referred to as the superconducting gap, as there is no conducting states for single electrons with energy below that. One can find the density of states (DOS) for a superconductor by considering it a normal metal with a gap around the Fermi energy [18], meaning that

$$N_s(E)dE = N_n(\xi)d\xi \tag{4}$$

By only looking at the states close to the Fermi level, the density can be additionally simplified as $N_n(\xi) = N(0)$ is assumed.

$$\frac{N_s(E)}{N(0)} = \frac{d\xi}{dE} = \begin{cases} \frac{E}{(E^2-\Delta^2)^{1/2}} & (E > \Delta) \\ 0 & (E < \Delta) \end{cases} \tag{5}$$

The density of superconducting states is the highest close to the gap ($E^2 - \Delta^2 << 1$) and it converges towards unity further away from the gap. In experiments this gap can be seen for example in a source-drain bias spectroscopy measurement, which shows a current response proportional to the density of states.

2.2 Josephson effect

A highly relevant part of superconductor physics in general and especially for this project is the Josephson effect. In its essence the Josephson effect is what can cause a super current of Cooper pairs to still flow between two superconductors separated by a weak link. Brian Josephson made two predictions in 1962. The first prediction was that in the situation of two superconductors separated by a small insulating barrier a super current I_s would flow at zero applied voltage

$$I_s = I_c \sin(\Delta\varphi) \tag{6}$$

Where the supercurrent is equal to the maximum current the junction can support, denoted I_c, when the superconducting phase difference $\Delta\varphi$ is π. This equation is known as the DC Josephson effect.

The second prediction was that if one instead did apply a voltage, the phase difference between the two electrodes would start to evolve in time according to:

$$\frac{d(\Delta\varphi)}{dt} = \frac{2eV}{\hbar} \tag{7}$$

This evolution in phase difference, will if applied to equation (6) yield an alternating current with amplitude I_c and frequency $2eV/h$. This is known as the AC Josephson effect. The AC Josephson effect can be measured with such precision that it is used in metrology to calibrate standards for the Volt [19].

There are three typical cases of weak links [17]: Superconductor-insulator-superconductor (S-I-S) as originally proposed by Josephson, superconductor-normal metal-superconductor

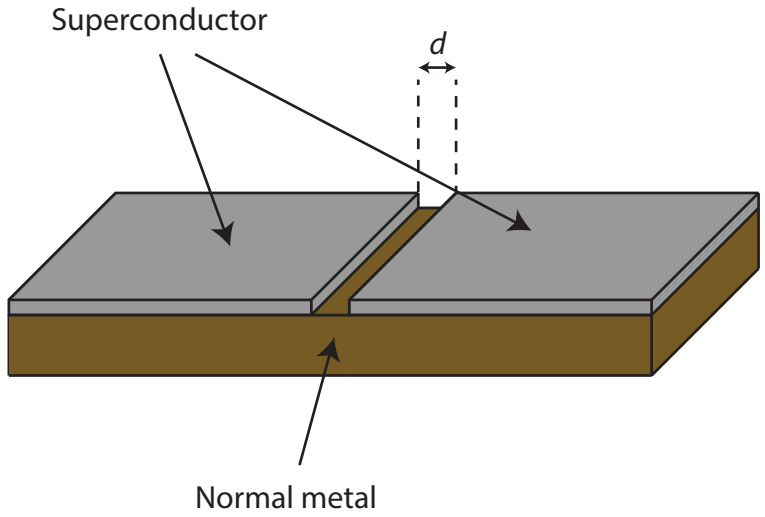

Figure 1: **Sketch of a S-N-S Josephson junction.** For there to be a Josephson junction, the separation of the two superconducting islands needs to be small enough for the condensate wave functions to overlap.

(S-N-S) and superconductor-constriction-superconductor where where the two superconducting electrodes are connected by a narrow constriction of superconducting material. In this project all Josephson junctions are of the S-N-S variety. A sketched example is shown in figure 1.

The Josephson effect can be understood as Cooper pairs leaking into the normal conductor. It is said that the normal conductor has been "proximitized". It is then these Cooper pairs that carry the super current. In a wave picture this can be understood as the condensate wavefunctions have a finite overlap within the Josephson junction.

2.3 Andreev reflection

Having an interface between a superconductor and normal metal gives rise to a physical phenomenon known as Andreev reflection. Imagine a S-N junction at equilibrium. In the normal part of the junction an electron near the Fermi level diffuse around with a momentum k until it reaches the S-N interface. Upon reaching the interface, it cannot go further as there are no available states in the superconductor for a single electron due to the gap Δ as explained in section 2.1. The superconductor could however accept the incoming electron and an additional electron with opposite momentum and spin thus forming a Cooper pair. To conserve momentum, the Fermi sea acquires a net momentum of k and the process can therefore instead be described as the original electron being reflected as a hole with momentum k and opposite spin, see figure 2.

In a S-N-S geometry, there are two such S-N interfaces. The hole formed from the first reflection can also undergo Andreev reflection at the other interface with an analogous result (effectively creating an electron with the same properties as the original electron). This gives rise to resonant modes of Andreev reflected particles appearing in the normal region between the two superconductors. These resonant

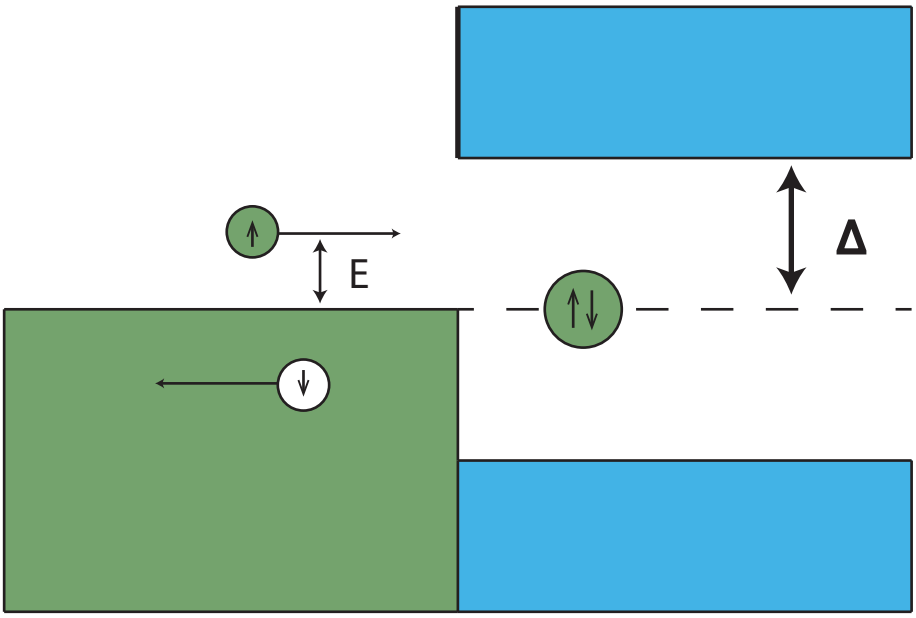

Figure 2: **Model of Andreev reflection in energyspace**. An electron can be considered reflected as a hole with opposite spin and momentum. Figure recreated from M. Kjaergaard's thesis [18]

modes are fermionic states that in an S-N-S geometry would appear inside the gap during a source-drain bias spectroscopy measurement.

2.4 4-terminal Josephson junctions

In 2015, it was posited by R. Riwar *et al* that a Josephson junction with four or more terminals could be regarded as an artificial topological material [1], meaning they can have non-trivial topological phases. The material is artificial in the sense that the Andreev Bound States (ABS), that are formed in the junction form a quasi band structure that mimic the band structures of a real material. The superconducting phase acts as the quasi momentum. These energy bands can with the right tuning have zero energy crossings, called Weyl points. A Weyl point alters the topological properties of the quasi band structure, acting as a monopole for the Berry connection. The material is said to be topologically protected, since the only way to induce a gap in the spectrum is to bring two Weyl points together or break momentum conservation [1].

The system can be modeled as n superconducting leads connected to a scattering region described by the matrix $\hat{S}$ by a number of ballistic channels. The bands in the energy spectrum of the bound states in the scattering region can be described by the equation [20]:

$$det[1 - e^{-2i\chi}\hat{S}e^{i\hat{\varphi}}\hat{S}^{*}e^{-i\hat{\varphi}}] = 0 \tag{8}$$

Where $\chi = arccos(E/\Delta)$ and $e^{i\varphi}$ is a diagonal matrix relating channels to the corresponding phase of a terminal. The ABS are periodic in all phases with a period

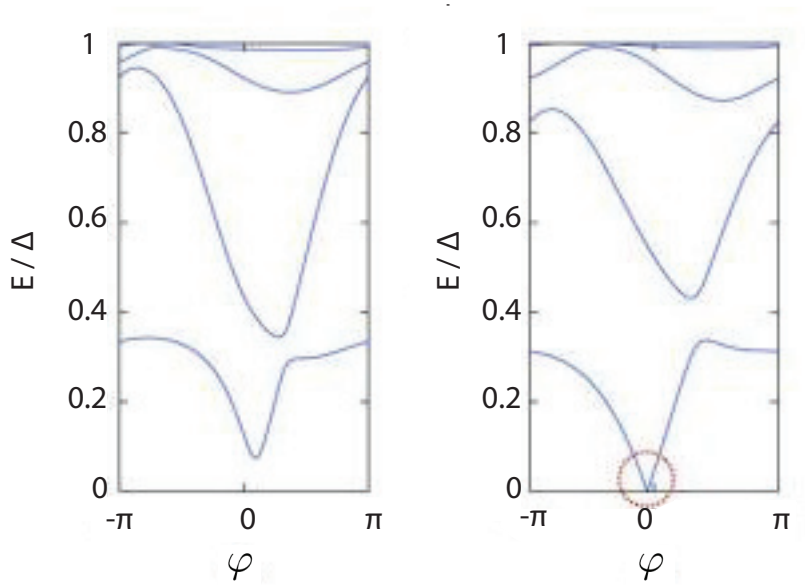

Figure 3: **Model of the quasi band structure formed in a 4-terminal Josephson junction.** Andreev bound state energies are periodic in 2π of the superconducting phase and can be described by a structure similar to a band diagram. **a** and **b** shows the energy of the Andreev bound states as a function of the superconducting phase of one of the terminals. In the case of **a** the other phases are not tuned as to have a Weyl point where in **b** a Weyl point is formed. Figure adapted from paper by R. Riwar [1]

of 2π and can therefore be regarded as a quasi band structure with the superconducting phases as quasi momenta. The total energy of the junction dependent on the occupancy of the band can defined by the equation [1]:

$$E = \sum_{k\sigma} (n_{k\sigma} - 1/2) E_k \tag{9}$$

Where $n_{k\sigma}$ is either 0 or 1 depending on occupancy of state k with spin σ. The zero-energy states can be described as the crossing of two singly-degenerate spin states. One with spin σ and energy E and one with opposite spin and energy. These zero-energy states can then be described by the two-by-two Weyl Hamiltonian

$$H_W = \sum_{i=x,y,z} h_i \hat{\tau}_i \tag{10}$$

Where $\hat{\tau}_i$ are the Pauli matrices and $h_i = \sum_\alpha \delta\varphi_\alpha M_{\alpha i}$. Weyl points occur for $h_i = 0$. Tuning the system to where $h_i = 0$ will require tuning of 3 different phases. Not all phases are independent however due to gauge invariance. Only 3 of the 4 superconductors have independent phases that can then be tuned to find the Weyl point. Weyl points are therefore, if they exist, points in the 3-dimensional phase-space, as illustrated in figure 4a. Since the total topological charge of a system must be zero and there is time reversal symmetry the Weyl points come in groups of four. In the case of only one channel connecting each of the superconducting terminals to the scattering region, approximately 5% of randomly generated matrices exhibited 4 Weyl points (and none with more) [1].

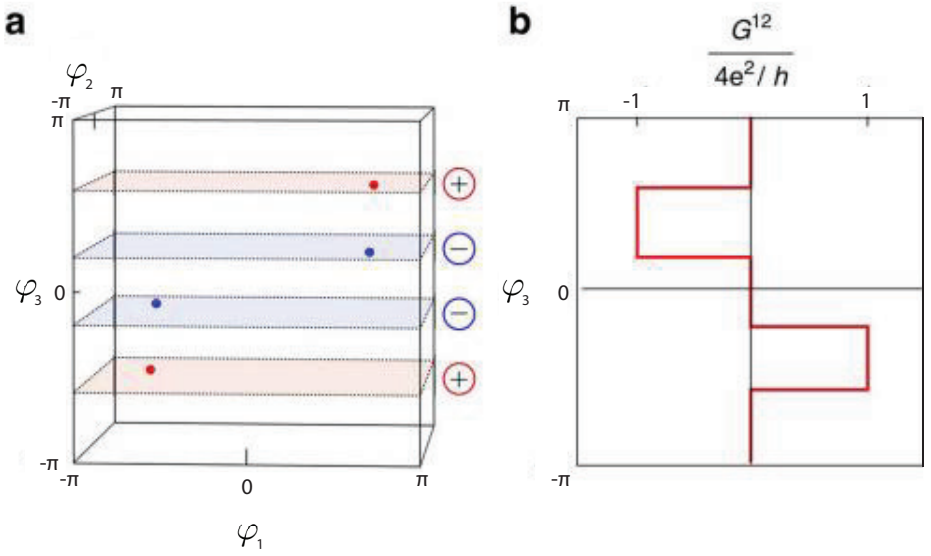

Figure 4: **Multi (>4) terminal Josephson junctions can exhibit non-trivial topological phases. a** Representation of 4 Weyl points in 3-dimensional phase-space in the simple case of every terminal in a 4-terminal junction having a single conducting channel. The different colors denote different topological charge. **b** Transconductance of the same junction as **a**, in units of the Chern number. Figure adapted from paper by R. Riwar [1].

The topology of a system can be described by Chern numbers. A Chern number can be found by integrating over the Berry curvature of the ABS [1]. The Berry curvature is defined as:

$$B_k^{\alpha\beta} \equiv -2Im\,\langle \frac{\partial\psi_{k\sigma}}{\partial\psi_\alpha} | \frac{\partial\psi_{k\sigma}}{\partial\psi_{beta}} \rangle \tag{11}$$

The Berry curvature for the entire system gives a result similar to the energy due to the Berry curvature not being dependent on spin [1].

$$B^{\alpha\beta} = \sum_{k\sigma} (n_{k\sigma} - \frac{1}{2}) B_k^{\alpha\beta} \tag{12}$$

The Chern number which only takes on integer values becomes:

$$C^{\alpha\beta} = \sum_{k\sigma} C_k^{\alpha\beta} (n_{k\sigma} - \frac{1}{2}) \quad , \quad C_k^{\alpha\beta} = \int_{-\pi}^{\pi}\int_{-\pi}^{\pi} d\psi_\alpha d\psi_\beta \; B_k^{\alpha\beta} \; / \, 2\pi \tag{13}$$

The Chern number describes the topological properties of the material. If the Chern number is zero the material is topologically trivial. The Chern number can be measured by measuring the transconductance through the junction. One could apply a small voltage on one terminal called β, letting $eV_\beta << \Delta$. Since this is below the gap, any conducting state can be assumed to be from the ABS and not the superconductors. The applied voltage gives rise to a current in terminal α. By applying two constant incommensurate voltages on two different terminals, one can sweep the phase-space due to the phase difference induced by the DC Josephson

effect while measuring the transconductance at terminal α. The transconductance is then proportional to the Chern number:

$$G^{\alpha\beta} = -\frac{4e^2}{h} C^{\alpha\beta} \tag{14}$$

This means that the topology of the material can be measured by measuring the transconductance and then translating that into a Chern number. An example is given figure 4b. It can also be seen that the transconductance is quantized in units of $\frac{4e^2}{h}$.

2.5 Implementation of 4-terminal devices

To construct the 4-terminal devices described in section 2.4 one needs 4 superconductors connected by a weak link with coherent transport properties. That is to say, the separation of the terminals need to be short compared to the mobility of the sample. The superconducting gap of the terminals need to be "hard", there should be no conducting states inside the gap. If the gap instead is "soft", it will be too hard to distinguish between ABS and some non-ideal conducting state inside the gap.

In order to see the topological behavior of the device, it must be possible to tune all but two of the phases, this can be done by connecting the terminals in a loop , creating a phase difference when a magnetic field is applied as investigated by Y. Aharanov and D. Bohm [21]. The acquired phase difference due to the Aharanov-Bohm effect can be calculated with the equation:

$$\Delta\varphi = \frac{q\Phi_B}{\hbar} \tag{15}$$

Where the charge of a Cooper pair (2e) returns the flux quantum Φ_0 as the magnetic flux Φ_B required to induce a phase difference of 2π. The magnetic field can either be induced globally in which case the loops would need to be of different sizes in order to tune the terminals to different values, but the field could also be induced locally by placing a strip line next to the loop, which due to the spatial separation would only generate a negligible field everywhere else.

In practical cases two additional things would be desirable. The first is one or more gates to control the scattering region. Not all scattering matrices yield topological states and having a way to tune the scattering region is more efficient than remaking all devices that only show topologically trivial states. This gating of the scattering region should be done asymmetrically as the goal is to change scattering parameters and not simply opening or depleting the region. The second thing one would want in a "practical" 4-terminal device are gates for the terminals. Quantum point contacts (explained below), can tune the terminals to only have 1 open channel each, significantly simplifying the system.

2.6 Quantum point contacts

Quantum Point Contact (QPC) is a term used to describe a conducting channel so narrow as to only allow a few or even a single mode. Throughout this section as

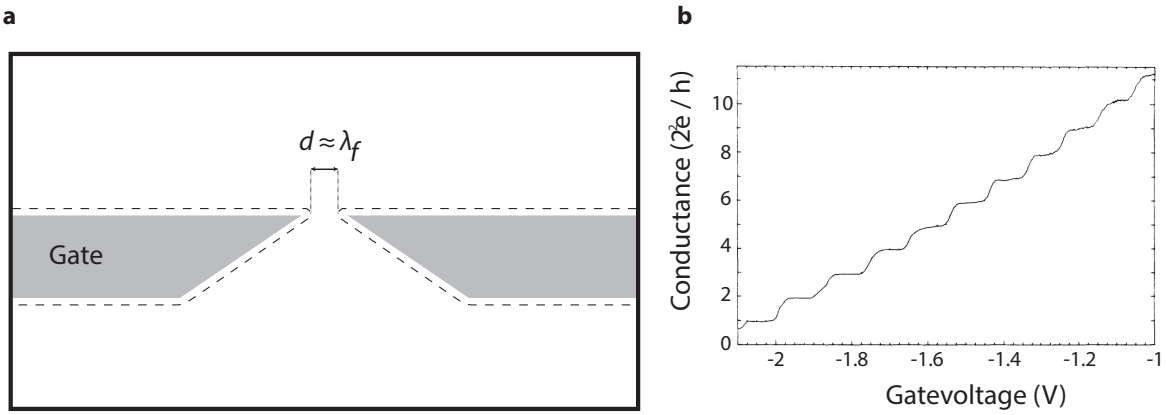

Figure 5: **Quantum point contacts show quantization of conductance.a** Schematic of a quantum point contact. The dashed line is a sketch of depleted region when a negative voltage is applied on the gate. **b** Conductance through the quantum point contact is quantized in steps of $2e^2/h$. Subfigure b adapted from paper by B. J. van Wees [22].

QPCs are explained, all transport will be assumed ballistic. The channel goes from having a continuum of states to a discrete number of modes when the width of the channel becomes comparable to the Fermi wavelength of the electrons [22]. In practice this is often realized by gating a semiconductor. This means that instead of the channel being restricted by the geometry of the material it is defined by applying a negative electric field. The field increases the energy required for the electrons to occupy the area beneath the gates and force them to go through the channel. An example of split gate QPC can be seen in figure 5a.

The channel in a QPC can be modeled as an ideal wire of some length L with an electron reservoir at either end of the wire. If the length of the channel is much longer than the cross sectional area, the current in the wire can be modeled as following [23]:

$$I = -g_s \frac{|e|}{h} \sum_n \int_{E_n}^{\infty} dE[f_L(E) - f_R(E)] \tag{16}$$

Where g_s is the spin degeneracy of the wire, 2 in the case of GaAs, and f_L and f_R are the Fermi-Dirac distributions for the left and right side respectively given by

$$f_i(E) = \frac{1}{e^{\frac{E-\mu_i}{k_B T}} + 1} \tag{17}$$

If the potential difference across the wire is small, meaning much smaller than the thermal energy, $f_L(E) - f_R(E)$ can be expanded

$$f_L(E) - f_R(E) = \frac{\partial f_L(E)}{\partial \mu_L}(\mu_L - \mu_R) = -\frac{\partial f_L(E)}{\partial E}|e|V_S D \tag{18}$$

Where V_{SD} is the source-drain voltage. This expansion can be inserted back into

equation 16 to yield

$$I = g_s \frac{e^2}{h} \sum_n f_L(E_n) V_{SD} \tag{19}$$

By looking at the ideal case where $T \to 0$, the conductance $G = \frac{I}{V_{SD}}$ can be simplified even more

$$G = g_s \frac{e^2}{h} N \tag{20}$$

Where N is the number of modes available in the channel. Each additional mode that is occupied increases the conductance in steps of $g_s \frac{e^2}{h}$. This constant is known as the conductance quantum. The number of channels N, can be approximated with the following relation $N \approx 2W/\lambda_f$ [23] where W is the width of the channel and λ_f is the Fermi wavelength. In 1988 experiments performed by multiple groups [22, 24] showed that the conductance through such QPCs as a function of gate voltage do indeed show plateaus at integer multiples of $2\frac{e^2}{h}$ on a GaAs substrate as in figure 5b. Adjusting the gate voltage either depletes the region less or more, effectively adjusting the width of the channel.

In a more realistic scenario of finite temperature, the thermal energy broadens out the the Fermi-Dirac distribution. The thermal broadening smoothens out the steps, making the less pronounced. If the spacing of the steps are comparable to $4k_BT$, the curve will smoothen out completely [25]. In reality the channel itself is also rarely ideal. When using gates to define the channel, the steps will most likely not be as regular. Impurities close to the QPC might get charged which will then affect the channel by it's own electric field. Applying a magnetic field has been shown to reduce noise in an unideal QPC [25].

2.7 Materials

Although different materials were used during this project, all of it was based on 2-Dimensional Electron Gases (2DEG) buried in a stack of III-V semiconductor heterostructure with a thin layer of epitaxial aluminum on top. The 2DEG material was grown out of house by M. Manfra in Purdue and shipped to Copenhagen. Growing a wafer of the 2DEG material consist of growing several layers of semiconductor material by the use of a molecular beam epitaxy instrument.
In figure 6 it can be seen that the 2DEG material consists of many layers of varying sizes. By altering the thickness or chemical composition of the layers slightly, the electronic bands of the material can be changed. Molecular beam epitaxy is a bottom-up method [23], meaning that the molecules are fired at the growth area and the molecules themselves diffuse into an energetically favorable formation to create the layered material. Shutters to different materials can be opened and closed to create the difference in chemical composition.

The epitaxial aluminum layer is grown *in situ*, meaning that the aluminum layer is grown without breaking vacuum. The *in situ* growth guarantees a pristine interface. In effect making a bigger part of superconducting wave function reside in the

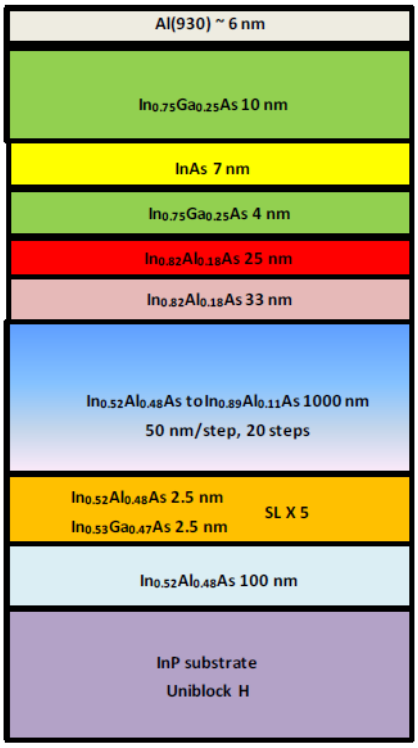

Figure 6: **Overview of the layers in one the 2DEG materials used for this project**. The material is built from several layers of semiconductor material with a superconductor on top. Figure adapted from summary sheet by M. Manfra. (see appendix)

2DEG. It makes the supercondcuting gap "harder", which is necessary to measure the bound states that have energy inside the gap.
The material is chemically rather robust, not showing appreciable degradation in atmosphere along with being resistant to organic solvents and water. Even though we found no indication of atmosphere damaging it, any material that was not in immediate use was stored in a inert (N_2) atmosphere. The inert atmosphere both kept it safe from prolonged exposure but also kept it clean from any contaminants. Physically the material is also quite robust, but continuous handling of samples frequently led to the edge starting to chip away.

2.8 Alternative materials

An alternative material to the 2DEG stack that was considered is nanowire crosses. These crosses provide an exciting alternative with different pros and cons.

In figure 7 an example of such a cross can be seen. The crosses are grown catalytically in a way that makes the two arms grown into and past each other, creating 4 arms in total. The cross is picked up by a microscopic needle so that it can be placed on the device substrate. The cross will have two legs where the original two arms originated, and it is highly improbable that the cross breaks off exactly at the top of the legs when picked up. To ensure that the cross is lying flat on the device substrate, it needs to be flipped such that the legs point directly up from the surface.

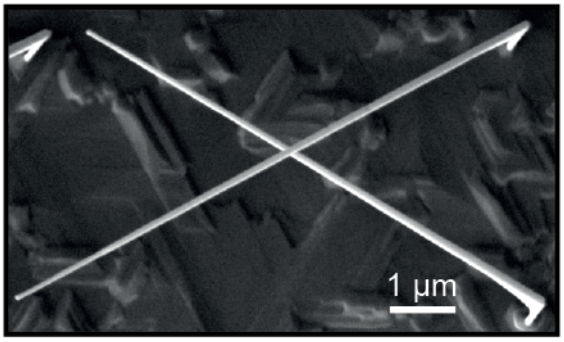

Figure 7: **SEM image of a nanowire cross before being picked from growth substrate**. Figure adapted from Filip Křížek's Ph.d. thesis [26].

When comparing the two different kinds of material several things were taken into account. The crosses can be grown with *in situ* epitaxial aluminum, meaning that the semiconductor/superconductor interface nominally is just as good. The junction in the nanowire crosses has the definite advantage of being defined not by lithography but by the growth itself. In the 4 terminal devices that was based on the 2-DEG material, the junction would ultimately have to be restricted by depleting the 2DEG underneath the QPCs. In the cross devices, the junction would always be perfectly defined and the QPCs could be used solely for restricting access to the terminal. The second advantage was that nanowire crosses were grown in-house. This is advantageous for numerous reasons; the quality is known, delivery is quick and options for feedback for the grower before next iteration are very good. Finally, the group as a whole was more experienced in working with nanowires and as such could save significant time on optimizing the fabrication process.

When the decision was made to use 2DEGs as material for the devices it is because the crosses also have disadvantages. Even though the crosses are grown in-house, they still have a low yield which means two things. First, it means that the number of devices per growth is low, requiring many growth for not that many devices. Since growth is a fairly long process, meaning that constantly waiting for new growth can significantly reduce the turnover of devices (both in a research aspect but also in an imagined industrial aspect). Secondly, it makes the process picking crosses from the growth substrate and depositing them on the chip much longer and more tedious. Each cross would be hidden among thousands of uncrossed nanowires.

Another disadvantage of the crosses is the quality of aluminum when creating the loop. While it is true that, as previously mentioned, the epitaxial interface should be of equal quality, connecting two arms of the cross in a loop would require depositing aluminum on top of the epitaxial layer. These two layers of aluminum would quite possibly not have a perfect interface which could lead to coherence problems in the loop. Making designs for the 2DEG would also be considerably easier. Nanowire cross designs would need to be carefully adjusted for every device even if it was a

device that one had made before. The adjustments would be necessary to accommodate things such as rotation or width change compared to the last time the device was made. 2DEG designs in comparison can be infinitely reused with no adjustment since the entire design is made relative to an empty plane. The last major consideration that was taken into account was the degrees of freedom. In the crosses, the terminals restricted by the number of arms in the cross. While technically possible to create a 6 armed nanowire cross, the already low yield would decreases drastically. Having more than the 6 arms would not be possible with the current materials, as they are hexagonally faceted. In comparison, the 2-DEG material could have an arbitrary number of terminals (although the junction size would have to increase with an increased number of terminals).

3 Fabrication

In this section an overview will be given of the fabrication processes used for this project. It is the intent that people unfamiliar with or new to the field can understand the basic principles of the instruments and processes used but will also offer insight into why specific steps were chosen over similar options.

The section starts off with a description of the techniques and instruments used in the fabrication. A general explanation and relevant advantages will be given for each of the techniques before continuing on to a description of the design process. Example of different designs and how they evolved over time, including reasons for those evolutions, will be given. A more rigorous walk-through of the fabrication recipe used during this project will be presented next. The walk-through will also contain thoughts on how the instruments were operated specifically during this project. Lastly, a simplified enumerated recipe will be given to summarize.

3.1 Atomic layer deposition

Atomic Layer Deposition (ALD) is a way to deposit a single atomic layer of material on a surface. ALD is a type of chemical vapor deposition technique. A common use of ALD is to create an insulating layer of oxide on a metal substrate. A vapor of metal compound is injected into the reaction chamber where the gas molecules react with the hot surface. The molecules adsorb to the surface creating a monolayer. By choosing gas reactants and temperature such that there is no homogeneous reaction, the process becomes self-limiting. The gas is then flushed from the chamber leaving only the adsorbed monolayer behind.

After the gas has been removed, water vapor can be inserted into the chamber. The water vapor then oxidizes the metal, creating a monolayer of oxide. The water vapor is then flushed from the reaction chamber. Since the metal precursor can also adsorb to the oxide these gasses are then alternated, building an oxide monolayer by monolayer. Since the monolayer has a well defined height, the totalt oxide height can easily be calculated by the counting the number of cycles that has been used.

This process is used to created a dielectric of a fixed thickness. This dielectric can be used to electrically insulate two parts of a design from one another, either to prevent a short or to create a gate by keeping a capacitive coupling. The good control of the thickness is what makes the ALD appealing when creating a gate, the dielectric needs to have a non-negligible resistance (which increases with thickness) and at the same time have a good capacitive coupling (which decreases with thickness). The control of the ALD not only makes it possible to find the sweet spot between being insulating and having coupling but it also makes it highly reproducible.

3.2 Electron beam lithography

Electron beam lithography (EBL) is a technique that allows one to draw extremely detailed patterns using an electron beam. First a resist is spun on the substrate. Two types of resists exist, positive and negative. A positive resist is something

that gets damaged by exposure to electrons, whereas a negative resist gets hardened by exposure. Different resists can be used but the most common is polymethyl methacrylate (PMMA) which is a positive resist.

Once a a resist has been spun on, the substrate can be exposed. This is done in an what at its core is a modified SEM. The SEM uses a focused electron beam to expose the resist in a designed pattern, changing the structural properties of the resist according to resist type.

The resolution depends on several things. One of them is the writefield size. To avoid excessive beam deflection the pattern is divided into writefields. A writefield is a section of the pattern that will be written without stage movement, this saves time because it reduces the time used on moving the stage. The writefield is placed concentric with the beam. To write away from the center of the writefield, the beam is instead deflected by a magnetic field, this also means resolution is inversely related to the distance to the center of the writefield. The relationship between resolution and distance means that the bigger the writefield, the worse the resolution. However during to bigger writefields covering a larger area you need fewer which means fewer stage movements which saves time.

Another aspect to consider is the number of dots. The EBL instrument assigns a number of dots to a writefield which gets some dose. This is equivalent to pixels in a digital image. Once again it is a matter of speed versus precision. By having a larger number of dots per writefield, the resolution increases, however this also slows down the exposure, if it is limited by the shutter speed. As a rule of thumb, the minimum feature size should contain 10 dots.

When the resist is exposed to the electron beam the electrons will generally pass through the resist and get scattered on the substrate. While the transparency of the resist is good in the sense that all the molecular layers gets exposed, it also means that adjacent resist gets unintentionally exposed. To counteract this effect known as the proximity effect, a correction is made. By either adjust dose manually or using an external software, a proximity effect correction can be calculated. This takes adjacent doses into account and based on a model estimates how big a dose is needed. This means that the center of a large area gets a much smaller dose than a finer feature. The end result is under perfect conditions that the entire pattern has been equally exposed.

After exposure, the resist needs to be developed. Development is done by dissolving the exposed (for a positive resist) or the unexposed (for a negative resist) with a weak organic solvent. The previously mentioned scattering, also affects how the profile of the exposed resist, and therefore the hole left by development, looks as can be seen in figure 8. The profile will leave a overhang of resist. This will prove to be advantageous during metal evaporation processes.

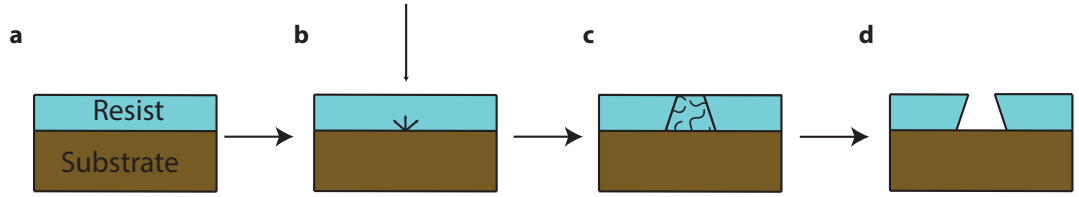

Figure 8: **Electron beam lithography and development process.** Due to the scattering of electrons on the substrate, the resist will be left overhanging the gap made by development.

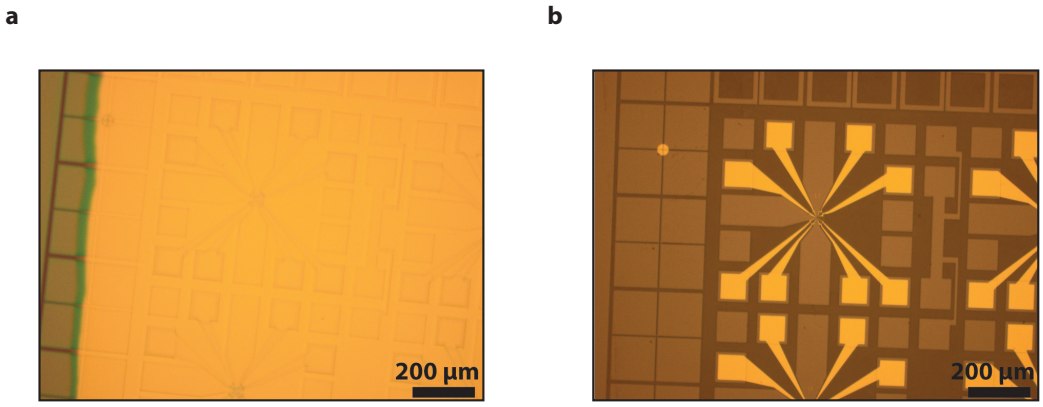

Figure 9: **Comparison of chip before and after lift-off. a** Aluminum foil has cast a shadow on the unpatterned part of the chip, increasing area that can be attacked by solvent. **b** Same chip as **a** after lift-off.

3.3 Metal evaporation

The easiest way to make small leads in an exact way is to combine EBL (3.2) with metal evaporation. To evaporate metal it needs to be heated. One way to do this is by using an electron beam to supply the required energy to evaporate. A filament is excited and electrons are emitted. These electrons can then by magnetic fields be channeled towards the metal. Once the metal starts to get bombarded by electrons, it will start to first heat and then later evaporate. The metal evaporation rate can be controlled by adjusting the current of the electron beam. The rate gets measured by a vibrating quartz crystal, the added mass of the metal will change the oscillations. The change in mass can by calibration be translated in to a thickness of the metal layer. Once the rate is the desired value and is stable a shutter is opened and the metal can be deposited on the sample.

The metal is only deposited parallel to the axis between the sample holder and the crucible where the metal is held. Due to the nature of the deposition, parts of the sample can be obscured by aluminum foil to prevent deposition in that region. Even in the case that the design has no part that disallows metal deposition, obscuring all parts that does not need it can be a good idea. After metal deposition on a patterned chip, the remaining metal needs to be lift off, meaning that the resist underneath it is dissolved. The cleaning agent needs uncovered PMMA to lift off the metal, and in general is faster the more PMMA is exposed to the solvent, see figure 9.

This technique can be combined with EBL to create structures out of metal. By patterning a chip with EBL and then evaporating gold onto it, will result in gold touching the substrate in the pattern and lying on the resist everywhere else. Using the lift-off process mentioned before, the gold is left in a precise pattern. In this way the size of gold wires are limited by the resolution of the EBL process which is very high.

While it would have been possible to deposit the superconductor using the same instrument, it was decided to define the super conducting structures by wet etching epitaxial aluminum instead. The epitaxial aluminum has a better interface with the semiconductor which means that the proximity effect is better.

3.4 Wet etching

As the name suggests, wet etching is the process of etching something with an liquid etchant. Wet etching therefore covers a lot of different processes, but throughout this project wet etching will always refer to acid in aqueous solution. An acid is prepared, this will require mixing and/or heating the acid, and the sample is submerged in the acid for a given time.

Wet etching is not a very refined process. It is hard to control and does not always offer a lot of reproducibility. This irreproducibility stems from the fact that fluid mechanics are very complex (and will not be covered in this thesis), which leads to one trying to replicate something they never had the full picture of. In general one could say that there are two methods to wet etching a sample, one is to keep it as still as possible and the other is to move it around as much as possible. The first thing, while easy to mechanically reproduce, potentially creates small regions in the fluid where the acid is depleted as a result of reacting with the sample. The other way constantly mixes the fluid and assuming a significantly higher volume of acid than sample, will always have the approximately same concentration of acid reacting with the sample. The second option is however much harder to mechanically replicate by hand, even with a robotic arm moving the sample around the same pattern would not yield the same result as the liquid is not prepared in the same microscopic state.

Wet etching has another feature, which is that is has both an isotropic etch rate. This means that even with a mask such as one created by EBL (see subsection 3.2), etching down also means etching to the side. The consequences of the lateral etch rate means that the distance between two islands separated by wet etching will always be limited by how deep the vertical etch goes. This phenomenon can be somewhat helped by the fact that many solid state materials are ordered in crystals where each face might react differently with the acid in question. As a result one could, in theory at least, find an acid that only etches vertically. Alternatively one can use an anisotropic dry etching such as reactive ion etching. Dry etching techniques are more expensive, time consuming and require significant investment into equipment,

The negative aspects of wet etching has been mentioned, but there also ways to mitigate these. The random nature of a wet etchant can be mitigated by increasing the etching time. The idea is that increasing the sample space over which the random motions are averaged will ultimately yield more reproducible results, this goes for both the fluid dynamics and movements of the sample. The lateral etch rate can be mitigated of course by finding an acid that has a low lateral etch rate compared to vertical for your material, but also in the design process. This will put some constraints on the design, but having thin pieces that can break if a specific region is slight over etched is risky.

4 Designs

Designing chips is an important part of fabricating devices. The designs are made in a Computer Assisted Drawing (CAD) program. The CAD file can then later through various software be converted into a file that can be read by the lithography system. Designing a chip is more than just drawing however. A lot of decisions that will affect the final quality of the devices have to be made during the design. A comparison between the CAD drawing, and the etched pattern derived from it can be seen in figure 10.

An obvious place to start are the dimensions of the chip. A seemingly simple, yet still important decision. A consideration is that larger chips can have more devices on. More devices are double edged sword. It means that more devices can be fabricated at the same time, which saves time and guarantee global parameters such as etch times are the same. It however also means that more devices are made without feedback, which can mean that several devices are destroyed at the same if one of those global parameter is bad. A consideration to take, is that in the end, only 48 bonds can be made to a daughterboard (explained in detail in section 5) no matter how many devices are on there. While it is possible to rip the bonds and rebond, there is always the risk of electrostatic discharge and the effects of repeatedly cooling down and warming the sample up is unknown.

When designing chips one is always trying to find the correct balance between what one wants to have and what the limitations of the instruments are. This will often lead to multiple iterations of the same device with one parameter being varied over the same chip. For example taking the 4 terminal device described earlier in section 2, one of the first things that was done was looking for the minimum junction size that could be made with high reproducibility. Ideally the junction would be small to guarantee coherent transport in the junction, but the size is limited by several factors. First there is the junction size itself, the junction is defined by etching away aluminum which means that the junction is limited to the resolution of both the EBL system and the wet etching of the aluminum of which the resolution of the EBL system is significantly higher. What proves to be even more significant in determining the size is the QPCs of each terminal. The QPCs are closer together than the terminals and they need a finite width and a finite separation to not break during liftoff (in the case of the former) and actually be separated by the liftoff (in the case of the latter). Of the different size we tested, the smallest viable one appeared to be 250 nm across the junction (superconducting terminal to opposing superconducting terminal).

Another thing to consider when designing the chip is that at the end of the fabrication each bond pad needs to be connected by a bond wire, which should ideally not cross. Initial designs had the devices arranged as square blocks in a 2 x 6 grid on the chip. While square blocks make it easy to place them next to each other, the design makes it hard to bond several devices. To help with this issue, the design later evolved into a geometry where each device was in a block that had all bond pads in only 3 directions and mirrored block next to it. This geometry means that a bonded device in one column can easily be bonded in a way where it will not

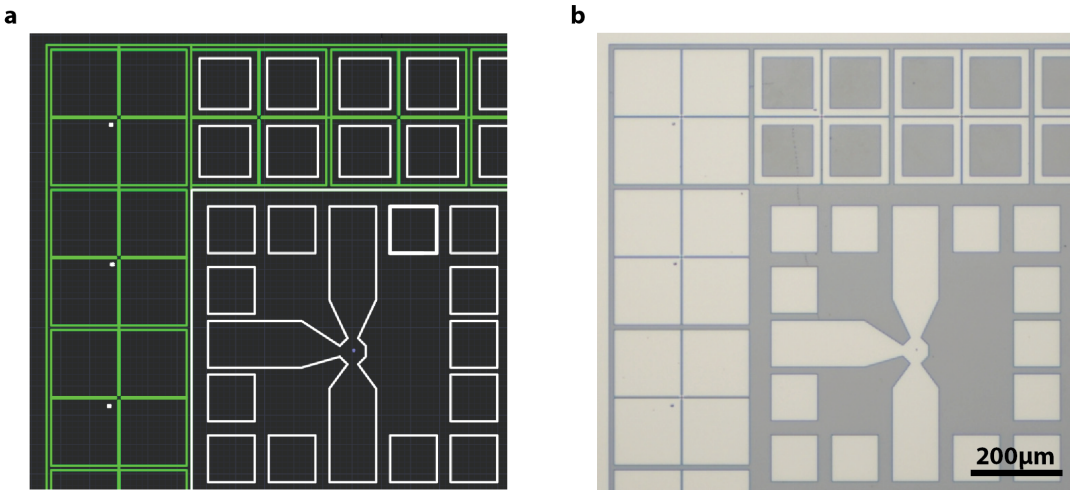

Figure 10: **A CAD drawing determines the pattern of the etch. a** A CAD drawing of the pattern in a mesa etch. **b** Micrograph of sample after etching.

interfere with any device in the other column. The disadvantage is that less devices can be fitted on to the same area.

Since many of the fabrication steps have the same cost, both in regards to time and materials spent, regardless of the area of the chip utilized, it is desirable to use as much of the space as possible. Due to this, much of the "waste space" between the blocks of bond pads are then used for test devices. These devices can then be bonded if there are bonds left after bonding the devices, or even get higher priority than "real devices". A case where it might be relevant to measure a test device before measuring something else would be the case of a Hall bar. A Hall bar can be rather big and low risk to fabricate and is then used to probe the intrinsic properties of the material. If the Hall bar does not show the correct mobility for the material, there is likely something wrong, either with the material, the bonds or the way the chip has been mounted. Other test devices include a series of device meant to test that each fabrication step was successful. This can be tested by checking that steps that should create an insulation (etching a gap between two bond pad) or a conductance (a gold gate should not be broken by crawling over a mesa edge) conducts accordingly. In these devices there are no fine features to observe and super conductivity does not matter, which means they can be measured in a so called "Board Station" at 4K. The Board Station is easier, cheaper and faster to operate than the dilution refrigerator explained in section 6.

The last kind of device that was typically included on the chips during this project were imaging devices. Imaging devices are devices for imaging in a scanning electron microscope to avoid potentially damaging devices by charging them up. The imaging devices were placed close to the alignment marks, far away form the actual devices. Imaging devices usually only mimic real devices where it is the most sensitive, which is usually the small features. For example for the 4-terminal devices the rest should be functional, if the junction is etched correctly and the QPCs had good alignment to the junction.

5 Fabrication process

A visual guide to the fabrications steps can be seen in figure 11, while a three dimensional figure of how the steps affect the appearance of the sample can be found in the end of this section in figure 13

5.1 Scribing and cleaving

The starting point of any fabrication concerning two dimensional electron gases is a wafer made from crystal growth. The growth of wafers was not a part of this project and as such will be not explained in detail here. A wafer is scribed, scratching the surface with a diamond tip, creating a grid of rectangular samples with the sizes of 5x7 mm. The force of the diamond tip is calibrated such that it does not break the sample apart, yet making definite fracture lines. After the scribing, the wafer is broken mechanically using a set of tweezers to apply force to the wafer. By aligning the scribed scratches with the edge of a cleaving block, the wafer should always break exactly along the scribed marks due to the crystal structure of the wafer. The following fabrication steps usually carried out on a single 5x7 mm sample at a size. This is done for mainly two reasons: using only a single sample at a time removes mixing up samples as a potential error source and a single sample has room for 12 devices and there is rarely a reason to make 24 devices before measuring.

5.2 Clean and spin resist (A4)

Before the sample can be used for anything it needs to be cleaned. Even just from atmospheric exposure, small dust particles will gather on the surface of the sample, but cleaving will generate a lot of particulate matter that sticks to the surface. Cleaning was done by ultrasonicating in dioxolane for 5 minutes at a frequency of 80 kHz at 80% power. The sample is then transferred to a beaker with fresh dioxolane and rest there for 20 minutes. The dioxolane is then rinsed of the sample by letting it rest in first acetone for 1 minute and then isopropanol for 1 minute. After rinsing in isopropanol the sample is blown dry by nitrogen.

The next step is spinning on resist which should be done immediately after cleaning the sample as to avoid any further dust to accumulate on the sample. Dust particles can seriously harm the resist layer by creating shadowed regions without resist. Spinning on resist is done by placing the sample in the spinner and activating the vacuum to lock the sample into place. A more stable layer of resist is achieved by using a technique called dynamic deposition. As the name implies the resist is deposited while the sample is rotating to let the resist settle before the spinner is rotating at maximum rotation. Dynamic deposition can be done by starting the spinner program before depositing resist and then pausing the program during its 5 second ramp time at which the system is rotating a 500 rpm. While rotating 7.5 μL of PMMA A4 is deposited on the center of the sample. After the deposition, the program is the resumed to go to its 4000 rpm for 45 seconds. When the resist has been spun on, it should be baked immediately for 3 minutes at 185 °C. After baking the resist can be visually inspected in a optical microscope to ensure the quality.

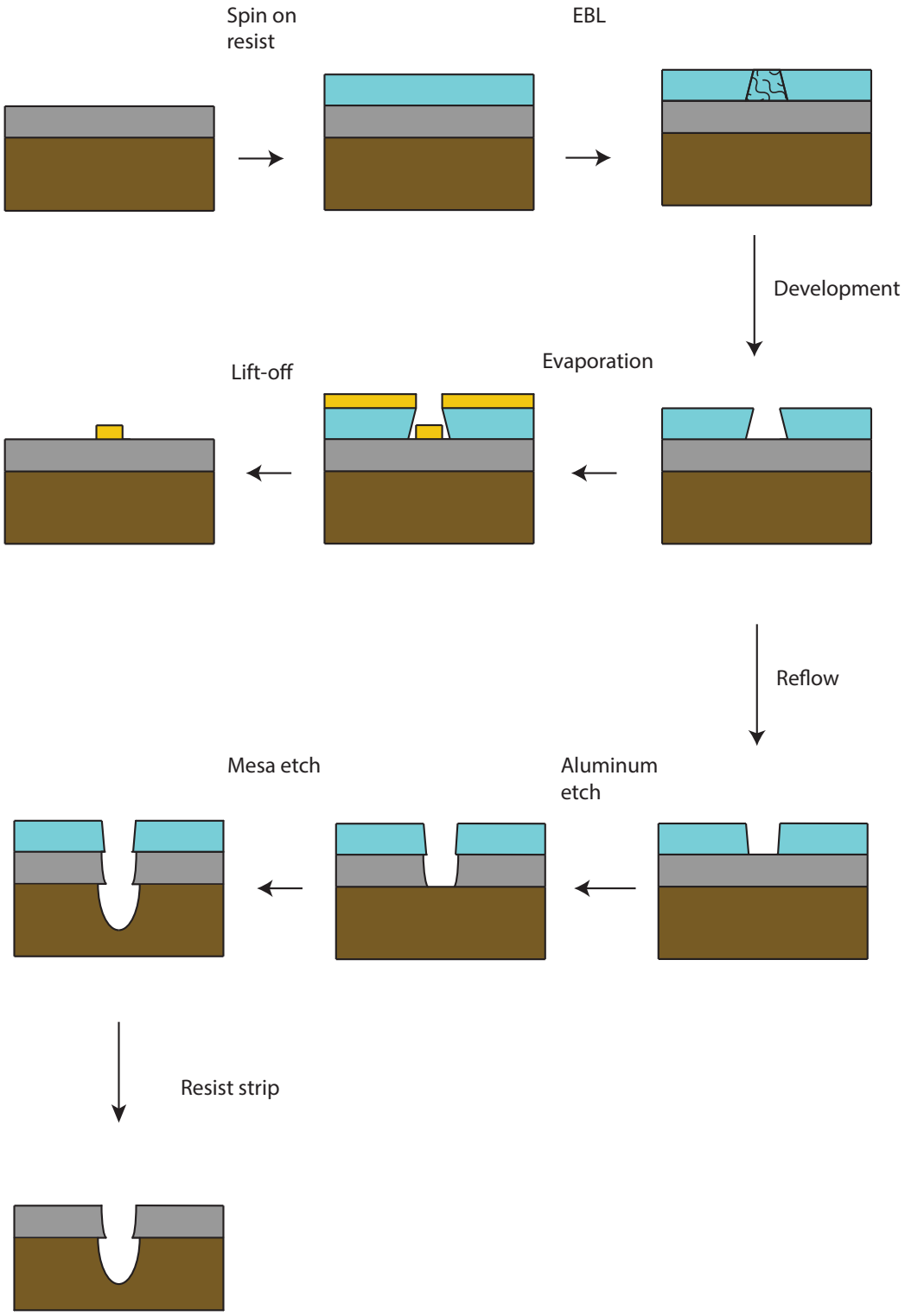

Figure 11: **Schematic overview of the fabrication process.** Fabrication is a iterative process where many steps are repeated several times. A detailed description of each step is given in the subsections of section 5

5.3 EBL: defining the mesa

The next step is defining etch windows in the resist by the use of EBL. While PMMA can degrade and the sample might as well be stored in an inert gas such as nitrogen (slowing degradation), time between spinning on resist and doing EBL is not critical and the resist can be prepared in advance, e.g. the day before. Theoretical information on how EBL works can be found in subsection 3.2 whereas this subsection will focus on the practicalities of the fabrication step.

The first thing to do when doing EBL is conditioning the beam. This is done before even loading the sample to give the system the maximum amount of time that it could reasonably have to settle. The desired beam and aperture settings are recalled and the beam is then moved a bit from the reference position of Elionix to focus on an area that has not been as exposed as much. Rough focus and stigmatism is then set at around 60000x magnification. After the beam has been roughly focused the aperture needs to be aligned, this is easiest done at lowest possible magnification with hight contrast settings. The beam is then zoomed in to around 60000-80000x magnification and refocused including stigmatism. During the fine focus the averaging can be increased to focus better. As the last step before loading the chip, the beam current is measured to calculate the dose time. This is preferred to trying to set the beam to the exact current that one wants it to be as it will save time.

The next step is loading the sample. First the sample holder needs to be retrieved from the main chamber. The load lock is evacuated before opening the gate to the main chamber, this is done to avoid pumping out the main chamber every sample exchange. The sample holder is then retrieved before the lock load is resealed and vented. The sample holder is blown with nitrogen to remove any particulate matter on it. The sample is then placed in the holder with clamps holding it in place. The sample needs to lie as flat as possible on the sample holder to minimize inclination during the exposure. Before loading the sample holder back into the main chamber it is once again blown with nitrogen to remove any dust. After having loaded while retrieving the rod, the rod is pushed back into the stage to make sure that it is not in a slightly wrong position from having followed the rod out, but completely at the back.

After the rod has been taken out of the main chamber completely and the gate has been closed the SEM computer needs to be told where to expose. First the beam is moved to the lower left corner of the chip. The beam is then moved 1 mm to the right and 1.5 mm up to center the design on the chip. The design is then placed at this location in the SEM software, since there is no alignment mark on the sample yet it will just place the lower left corner of the design at the position. The next step is to measure the sample inclination, it should be as flat as possible. The height is measured at 3 points by a laser and the inclination then calculated. While not as important at this step due to the sample not having anything on it, false readings can be avoided by visually inspecting the signal of the laser at each of the 3 points manually before initiating the measurement.

The last step is field correction. Field correction is an automated process where the Elionix draws crosses using the electron beam and then tries to find them again.This

is done to calibrate the beam deflection. This process usually converges to an accepted value within 1-3 tries, but it can take longer. Once the field correction is completed exposure can be started.

Exposure is separated into two parts. The first part is writing the inner etch windows at 150 μm writefield and 60,000 dots. The beam current is 500 pA with a dose of 600 μC/cm^2. After the inner exposure is finished, the beam settings for the outer mesa is recalled (600 μm writefield, 20,000 dots, 40 nA, 750 μC/cm^2 dose). Before continuing with the outer exposure the beam is allowed to settle for 10 minutes. The inner part is done first to make sure that the fine features are done with the highest precision. The second exposure is most likely not correctly conditioned and the accumulated stage drift will be higher.

5.4 Development

The exposed resist is developed by using Methyl Isobutyl Ketone (MIBK) in a 1:3 solution with IPA. The sample is developed in MIBK for 60 seconds followed by a 30 second rinse in IPA. The sample is then plasma ashed for 60 seconds to remove the last residues of resist in the etch windows.

5.5 Mesa etch

Before the actual the etching the sample is baked at 115 °C for 3 minutes to reflow the resist. The reflow process smoothes out the natural undercut in the resist. Neglecting to do the reflow can lead to the etch etching further out than wanted.

The purpose of the mesa etch is to isolate the structure that make up the device from the rest of the wafer by etching deep, about 200 nm, in the wafer. This way the 2DEG in the relevant areas is isolated from the the environment. The first step of the mesa etch is to etch away the top layer of aluminum. The chosen acid for this etch is Alumnium etchant type D from Transene. A heat bath is prepared with 3 beakers: 1 containing aluminum etchant type D and 2 containing MQ water. One of the water beakers are used exclusively to measure the temperature, which is reasonably assumed to be the same as the etchant. Once the temperature reaches 49 °C the sample is etched for 6 seconds while moving the sample around to keep the acid concentration approximately constant throughout the etch. The sample is then moved to the hot (non-measurement) MQ water and rinsed while moving the sample around for 30 seconds to stop the etching. Finally the sample is rinsed in cold MQ water

The rest of the mesa etch is done by a mixture of acids. The acid is mixed in the following order: 220 mL MQ water, 55 mL citric acid (1 M), 3 mL phosphoric acid (85% aqueous solution), 3 mL hydrogenperoxide (>30% aqueous solution). The acid should be stirred for a couple of minutes to mix the acid. After the acid is mixed the stirring speed is turned down and the sample is placed near the edge of the beaker. The movements in the liquid should not be violent enough to disturb the sample. The sample is then etched for 6 minutes during which it is moved around in the

beaker with a pair of tweezers to average the acid concentration of a bigger area. The etch is stopped by rinsing in MQ for 30 seconds.

5.6 Cleaning and new resist (A4) like 5

5.7 EBL: defining Al etched regions

For the most part this step is identical to 5 such as loading and unloading the sample. A crucial difference during this step is alignment. In the previous EBL step there was nothing on the sample and the pattern therefore just needed to be approximately centered on the sample. The Aluminum etch windows however need to be placed in an exact relationship with where the mesa etch windows were. To expose the correct regions the crosses defined in step 5 is used to align the sample. Since the crosses are merely etched into the sample and not as usual made out of gold on top of the sample the contrast is low. Turning the lights down/off can make it easier to make out the crosses. Likewise averaging over a longer time can also make it easier to see the crosses.

Like the inner mesa, this EBL step contains fine features and therefore needs high resolution. Beam settings used are 150 μm writefield, 60,000 dots, 500 pA beam current and 575 μC/cm^2 dose.

5.8 Aluminum etch

Before the etch, the resist is reflown like before the mesa etch 3 minutes at 115 °C. The etch itself is similar to the aluminum etch described in 5, however the sample is only etched for 5 seconds in the aluminum etchant type D instead.

5.9 Cleaning like step 5

Preferentially the sample should be move directly from the dioxolane to the ALD (see next step), to avoid contamination of the surface.

5.10 ALD

Before running the actual ALD program, the dead space between the precursor and the reaction chamber is pumped out. This is done by closing and the manual valve and then running a few cycles of the ALD until there is no trace of the precursor.

After the dead space has been pumped out, the sample can be loaded and the program started. The program should contain a waiting time of 10 hours before starting the actual precursor-water cycle. A total of 150 cycles were used, enough to make an oxide layer of 15 nm.

5.11 Cleaning and new resist (EL9 and A4)

Cleaning is done as in 5.

Resist is made with first a layer of 7.5 μL EL9 spun on with dynamic deposition in the same way as PMMA. A layer of PMMA A4 is then added on top of the EL9 completely like 5.

5.12 EBL: defining inner gold leads

Like step 5. The combination of the oxide and a low beam current makes the crosses very hard to see. Beam settings used are 150 μm writefield, 60,000 dots, 100 pA beam current and 608 μC/cm^2 dose.

5.13 Metal deposition

A thin strip of tinfoil is cut and put over the edges if the chip. It will aid the later liftoff of the resist since the dioxolane will have an easier time attacking the resist when it is not all covered with gold. First a layer of 5 nm titanium is deposited this acts as an intermediary between the substrate and golds and allows to gold stick much easier. On top of the titanium layer, a layer of 25 nm gold is added.

5.14 Liftoff, clean and new resist

Liftoff is done in dioxolane, until the gold is gone from the sample except for the pattern. Once the gold has started to lift off the process can be quickened by blowing air gently from a pipette. For the cleaning and spinning on of new resist, see 5.

5.15 EBL: defining outer gold leads

This exposure has a fine and a rough part like 5. The fine part will connect the inner gates with the outer leads and the rough part will then connect that to the bondpads which are also drawn in this step. The fine part uses beam settings of 150 μm writefield, 60,000 dots, 100 pA beam current and 608 μC/cm^2 dose. Beam settings used for the second exposure are 600 μm writefield, 20,000 dots, 20 nA beam current and 800 μC/cm^2 dose.

5.16 Metal deposition at a tilted angle

Since some of the outer gold leads will need to cross the mesa etch which should be around 200 nm high, the metal needs to be deposited at an angle to let the gold "crawl" up the step. Whenever metal deposition is done at an angle, the sample holder should be rotating as at any given time some of the steps will be shadowed. Initially titanium is evaporated at a rate of about 1 Å/s with a 5 degree angle until a layer of 10 nm has been deposited. Next gold is evaporated with a rate of about 2.5 Å/s with a 5 degree angle until a layer of 55 nm is reached. A new gold layer is evaporated at a rate of about 3 Å/s with 0 degree angle with an additional 140 nm gold (total gold layer 195 nm). Lastly a gold layer is deposited at a rate of 2.5 Å/s with a 10 degree angle for an additional 55 nm (total gold layer is 250 nm).

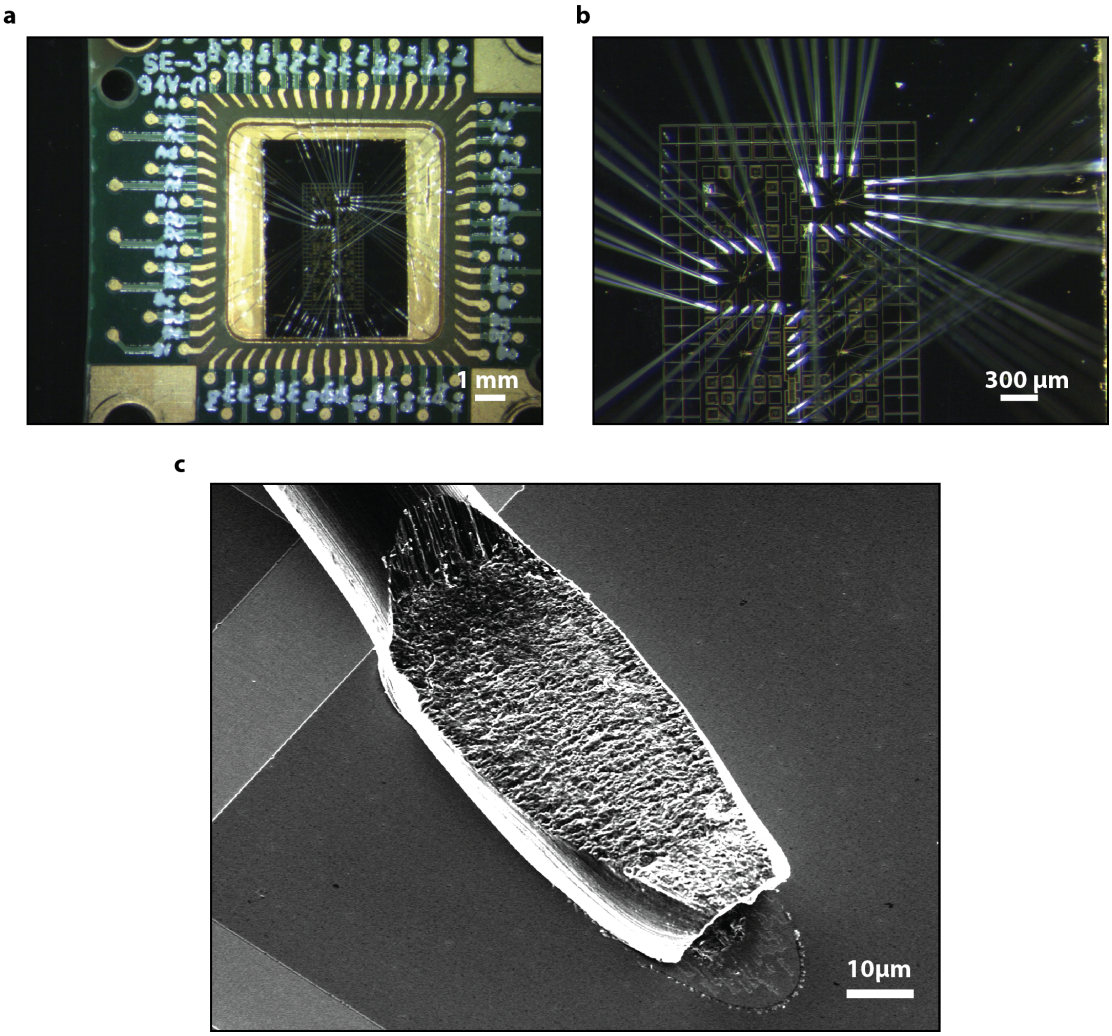

Figure 12: **Example of a bonded sample.** **a** A sample bonded to a daughterboard. Only a couple of devices on each sample can be bonded at the same time due to available connections on the daugtherboard. **b** Zooomed in dark field micrograph of the same sample. **c** SEM micrograph of a bondwire bonded to a bondpad.

5.17 Liftoff and clean like 5

5.18 Bonding

The chips needs to be bonded to a daughterboard before it can be measured. By applying a bit of PMMA to the daughterboard the sample can be glued on to the daugtherboard. PMMA is used instead of for example silverpaste as there is no backgate and PMMA has a weak adhesion to the sample. Being able to take the sample off the daugtherboard is desirable as any SEM imaging before measuring can result in globally damaging the hafnium oxide layer. An example of a bonded sample can be seen in figure 12.

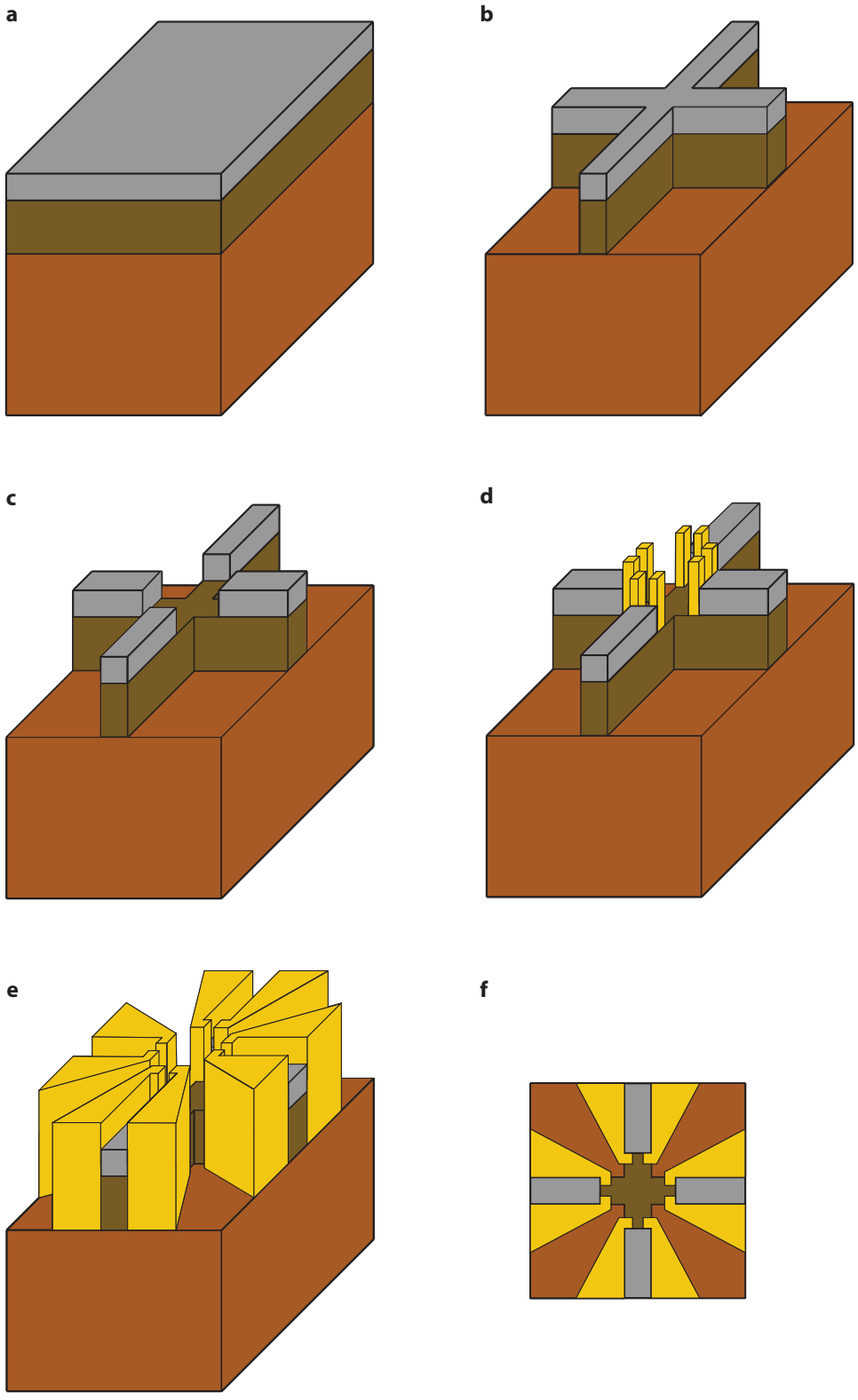

Figure 13: **Visual representation of the fabrication process.** Relative size of layers distorted to better see the aluminum layer.**a**chip pre-processing. **b** Mesa etch, defining coarse features. **c** aluminum etch defining the scattering region and the finer features. **d** A shallow layer of gold define the innermost part of the QPCs. **e** Finally thick layer of gold connect the shallow layer to a bondpad. **f** Top-down view of the device

6 Cryo-free dilution refrigerator

This section contains a thorough explanation of how a dilution cryostat works. Although some things will be generalized, this section will focus on a Oxford Instruments Triton Cryofree Dilution Refrigerator. All low temperature measurements taken during this project was measured inside a Triton cryostat. First a description of the general principles of dilution refrigeration will be given before some of the ways the Triton refrigerator was modified to suit the needs of this project are explained. In conclusion to this section information on cleaning the mixture and controlling the Helium circuits will be provided.

6.1 Overview of a Oxford Instruments Triton cryostat

The Triton cryostat is built up of several shields surrounding a series of plates connected by an insulating carbon composite material. A view inside the cryostat can be seen in figure 14. The plates will be at different temperatures decreasing as they go further down. During operation the top plate (PT1) will go down to about 75 K whereas the lowest plate (the mixing chamber plate) can go below 20 mK. On each of the plates different parts which serve different purposes are installed such that they are in thermal equilibrium with the plate.

There are total of 5 plates inside the cryostat. Each of the plates are monitored by one or more thermometers. A Cernox thermometer is used for higher temperatures but once the temperatures get low enough, the Cernox starts to be less precise and a Ruthenium oxide thermometer is used instead. The other things installed on the plates either pertain to the cooling of the cryostat (explained in detail in the sections below) or the electric measurements conducted on the sample inside the cryostat (explained in detail in section 7). Thermally contacted to the bottom of the mixing chamber plate is the coldfinger. The coldfinger connects the cryostat to a puck carrying the sample (explained in detail in section 7). A superconducting magnet is also screwed into the bottom of the thermally conductive radiation shield that is in thermal contact with the PT2 plate. The magnet encases the space where the puck will be inserted into the coldfinger.

To ensure the quality of the measurements, a lot of care is taken to avoid stray radiation. The plates inside are covered by radiation shields and then the outer vacuum can. Beyond the shields themselves, small pieces of electrical tape covers all open surfaces on the plates to form a Faraday cage. An extra layer of protection is added for the wires going from the filters (explained in section7) to the puck. This extra layer of protection consists of the radiation absorbing material Eccosorb, which is a black hard foam substance. One side is covered in a glue like substance that will make the material stick. Attempts to remove Eccosorb after having been glued on will most frequently result in the plate breaking apart, making it a long process that leaves a lot of residue. A comparison of the coldfinger before and after adding the Eccosorb can be seen in figure 15. To make it easier to remove, should it be so desired, two plates with the same dimensions were glued to each other preventing the Eccosorb from sticking to wires with fragile solder joints. Outside the coldfinger a similar thing is done to protect the wires until they reach a filter.

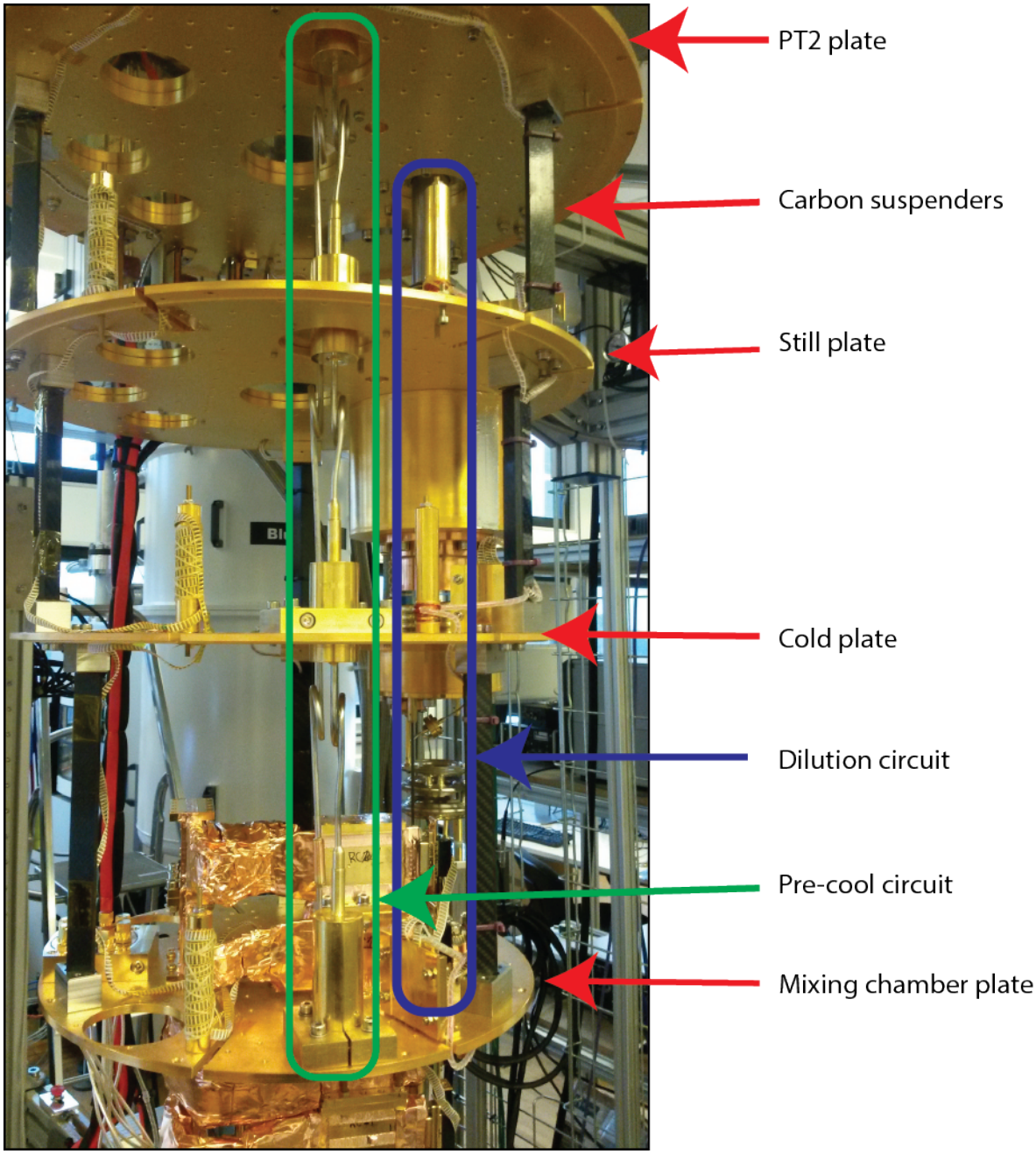

Figure 14: **Photograph of the cryostat without the shields.** Several objects of interest are pointed out. Uppermost plate is not visible from this angle. The magnet is taken off in this photograph in order to gain full access to the coldfinger.

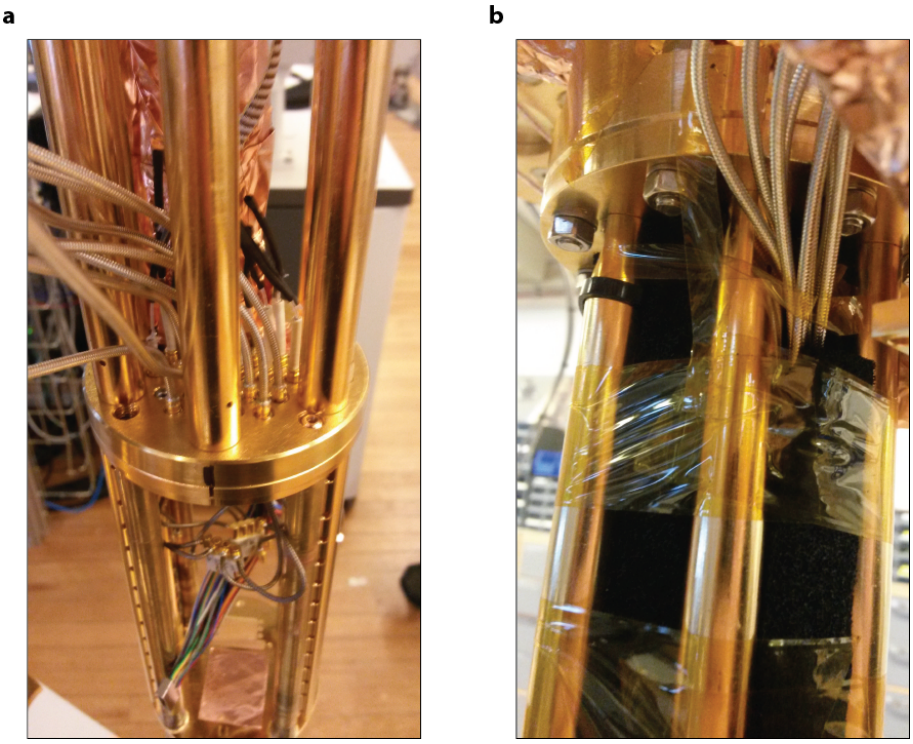

Figure 15: **Side by side comparison of the coldfinger before and after adding the Eccosorb** The purpose is to absorb stray radiation inducing noise in the DC lines are having been filtered.

Instead of sticking two plates to each other, the wires were covered in carbon tape which the Eccosorb was then glue to.

6.2 General principles of dilution refrigeration

To cool something means to reduce the internal energy of that thing. This can be done in a number of ways, of which simply letting the energy equalize by having the object that needs to be cooled in contact with a colder object (coolant) is most likely the most well known. Heat transfer from the cooled object to the coolant will gradually heat up the coolant, and new supply is therefore constantly needed to maintain as steep a heat gradient as possible. The easiest way to maintain a supply of cold coolant is to have the coolant flow from some source, past the object that needs to be cooled and then away. No natural coolant exists that would be able to cool down a cryostat below the critical temperature of normally used superconductors. There are however other ways to make things cold. An example of this, is the Joules-Thomson effect which can be used to make a gas cooler. The Joules-Thomson effect is an isenthalpic process that relies on letting a gas expand when going from a high pressure to a low pressure, this will below a certain temperature (known as the inversion temperature) cool the gas. The Joule-Thomson effect can therefore create a liquid with a temperature equal to boiling point. By the Joules-Thomson effect, one can make Helium into an approximately 4 K cold liquid

Liquid Helium forms the foundation of cooling the cryostat down, from the ini-

tial stages to temperatures below 20 mK. In the Triton cryostat the first stage of cooling is called pre-cool and will bring the system down to 20 K from the starting point (possible room temperature). The pre-cooling is cooled by a series of tubes called pulse tubes. The pulse tubes come from outside the cryostat, enter it and then return to a compressor to be cycled again. These tubes carry liquid Helium (which should be around 4 K) to a part of the tubes called the pulse tube cooler. The pulse tube cooler is located between the top most two plates and is thermally connected to both of them by a series of copper braids that keep it from being mechanically connected to either of them. Through simple heat exchange the pulse tube cooler will start to cool down the two plates it is in thermal contact with. There is a separate helium circuit that does not carry Helium-4 like the pulse tubes. Instead of Helium-4 (the most common isotope), one uses a mixture of Helium-4 and Helium-3 (hereafter referred to as simply "the mixture"). During the pre-cool the mixture is entirely in a gas state. While the pulse tubes are running, the mixture is circulated in a pre-cool loop which has a heat exchange with the pulse tubes. The now cooled mixture will then circulate, exchanging heat with the other plates inside the cryostat. Once the mixing chamber reaches a temperature of 20 K, the pre-cool loop is evacuated into a storage tank and the cooling can continue to the next step which is the condensing.

The pre-cooling process would be able to bring the cryostat to 4 k, if it ran continuously. This would in most circumstances have been cold enough, but the cryostat needs to be even colder for two reasons: the first is that lower temperatures are required to observe superconductivity in normally used superconductors and the second is that thermal energy introduces noise into the system. The colder temperatures the cryostat can reach, the less noise there will be in the measurements. The next step of cooling, the condensing, is able to get it below a crystal temperature of 20 mK, The crystal temperature is the temperature of the sample, and not the temperature of the conduction electrons which will have a temperature of around 100 mK at base temperature.

The condensing process starts by releasing the mixture into the dilution circuit. The mixture is then compressed and further cooled down until the mixture condensates in the mixing chamber. The two different isotopes of Helium in the mixure have different physical properties. Among these differences is a lower density and a lower boiling point. Once the temperature is sufficiently low this will create a phase barrier between the two isotopes with a Helium-3 dense phase on top and a Helium-4 dense phase at the bottom. The lower phase has a concentration of approximately 6.6% Helium-3. This phase barrier is the key to dilution refrigeration and is used to achieve the low temperatures. The bottom of the mixing chamber (consisting mostly of Helium-4) is connected to a volume above the mixing chamber. Helium-3 is preferentially evaporated into the volume, effectively dragging the Helium-3 across the phase boundary to refill the missing Helium-3. Helium-3 crossing the phase boundary and mixing with the Helium-4 has a energy cost, cooling the system. The volume above is constantly pumped out and compressed to condensate the helium-3 into the mixing chamber again.

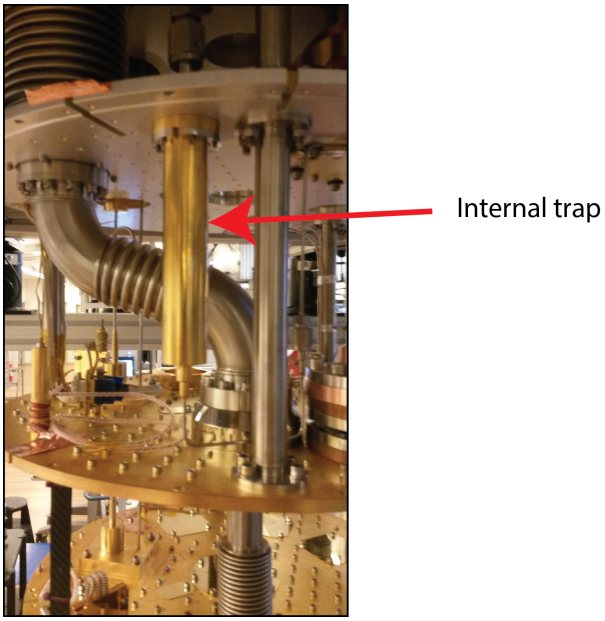

Figure 16: **Photograph of the internal cold trap.** Nearby heat sensitive components can be seen. For example the plastic covered wiring to the left of the trap.

6.3 Cold traps

Contaminants are a constant risk to experiments. Even if the cryostat was perfectly sealed such that no contaminants from the outside could enter, the surfaces inside the cryostat would still outgas. The lubricated O-ring might create a seal to the outside world, but if it itself is a contamination source one still risks contaminating the mixture. Any contamination of the mixture risks clogging the condenser lines, potentially causing critical failures in the system. To avoid this issue, cold traps are used to clean the mixture. The Triton cryostat used in this project had two internal and one external cold trap. "Internal" and "external" in this case means "inside" and "outside" the vacuum can. Both types of cold traps are part of the same closed circuit that the mixture is circulated in.

The external cold trap is a tube of active charcoal dipped into a dewar with liquid nitrogen. Contaminants in the mixture will either adsorb to the charcoal or freeze on the cold walls. The nitrogen will naturally start to evaporate from heat exchange with the environment this will of course cause the nitrogen level in the dewar to drop which means the cold trap itself needs to be refilled with liquid nitrogen often. If everything is sealed tight and operating correctly the traps should be able to run for up to 6 months without needing cleaning but at some point the cold trap needs to be cleaned. The first step of cleaning the traps is to collect all the mixture in the tank, this eliminates any risk of leaking the precious mixture. The valves leading to the cold trap are then closed and the cold trap disconnected from the Helium circuit. The cold trap is baked at 80°C while getting pumped out. The increased temperature will cause all adsorbed contaminants to evaporate and the pump will then remove them from the cold trap. Unless necessary, it is recommended to not clean the cold trap while the cryostat is cold.

The internal trap is located inside the cryostat and can only be cleaned by removing the vacuum can of the cryostat. Cleaning the internal trap is more inconvenient but follows the same general procedure. First the mixture is collected inside the tank, since this step is followed by a full warmup, additional care should be taken to retrieve all the mixture. Next step is to warm up the cryostat to room temperature. After the cryostat is warm, the outer shield can be taken off to expose the top plate where the internal trap is placed. Once again, the cold trap is isolated by closing off valves and the cold trap is pumped out. It is not possible to remove the internal cold trap (without significant effort) and as such it should be baked using other methods of heating such as a heat gun. The internal trap will be in the proximity of several other components some of which might not be able to withstand much heat, so it is important to be mindful of where one is heating. The trap itself is attached with solder joints and therefore can not get too hot either. An approximate temperature of 80 °C should be maintained.

6.4 Helium circuit control

The Triton cryostat relies on mostly automated processes for cooling it down. A command is issued that will automatically open the correct valves to let in the correct amount of the mixture. The computer controlling the cryostat will then readout the temperature of the thermometers inside and adjust the pressure accordingly to maximize the cooling power. The same script also shifts from pre-cooling to condensing when the system is at the right parameters. Although the cool down (and the warm up) can be done automatically, all valves can also be controlled manually in case one wants to do a non-standard operation or the automation simply fails. Some of the valves outside the cryostat that are not used during the normal operation, such as the two safety valves directly next to the tank, can only be controlled manually.

7 Measurement setup

In this section an introduction to the experimental setup will be given. The section will build upon the description of how wafers are processed into devices (section 3) and expand upon how to measure the properties of these devices at low temperature using a dilution cryostat which was explained in depth in the section 6. A detailed description will be given of how instruments outside of the cryostat such as a lock-in amplifier are connected to the sample inside the cryostat. This section will include elementary concepts as it is the intent that people new to the field can use this as a resource entering the field of low temperature electron transport.

7.1 Installing the sample inside the cryostat

As previously covered in the fabrication section 3, each sample is a 5x3 mm piece of III-V heterostructure wafer with epitaxial aluminum on top. It will have a number of devices on it that have been patterned using a combination of EBL, wet etching and gold evaporation. Each part of the device that needs to be connected to an external instruments (for example a gate) is then connected to a bondpad. These bondpads are structures on the order of 100 x 100 μm which allows a thin wire to be punched into it and get stuck there, forming an electrical connection from the chip to a bondpad off the chip known as a bond.

Once fabricated, connecting the sample to the outside world requires many interlocking pieces. First a sample will be electrically connected to a **daughterboard** which is a small 17 x 17 mm Printed Circuit Board (PCB) through a series of bonds. Bonding on the bondpads of the PCB is a similar process, but might require different bonding parameters than that of bonding on a chip. The daugtherboards used for this project allowed 48 DC lines and 12 channels bypassing the filters in the cryostat. These 12 lines can be used to carry high current for a flux bias line. The high current would cause a high heatload in the resistance and the filters, and the signal would not be as susceptible to stray noise due to the higher current. The limit in number of channels means that following the fabrication scheme detailed in this thesis and having all the devices work, will result in having to select at most two 4-terminal devices to bond. Considering what devices look promising from imaging it, should be considered a task in itself. The daugtherboard serves the function of being a small and easily transportable vessel to bond to, but cannot be connected directly to instruments outside the cryostat. Connection to the outside world is performed through the **motherboard**. Like the dautherboard, the motherboard is made out of PCB, however unlike the daugtherboard the motherboard has connection that can be adressed by macroscopic wires. In the case of this project, it has a nano D-sub connector for the normal conducting wires and SMP connectors for the superconducting wires.

The daugtherboard is screwed down on an **interposer** which itself is screwed into place on the motherboard. The motherboard and the dautherboard are connected through fuzz buttons, essentially conducting springs, inside the interposer. Although it can be removed if so needed, the motherboard is usually kept locked in place inside

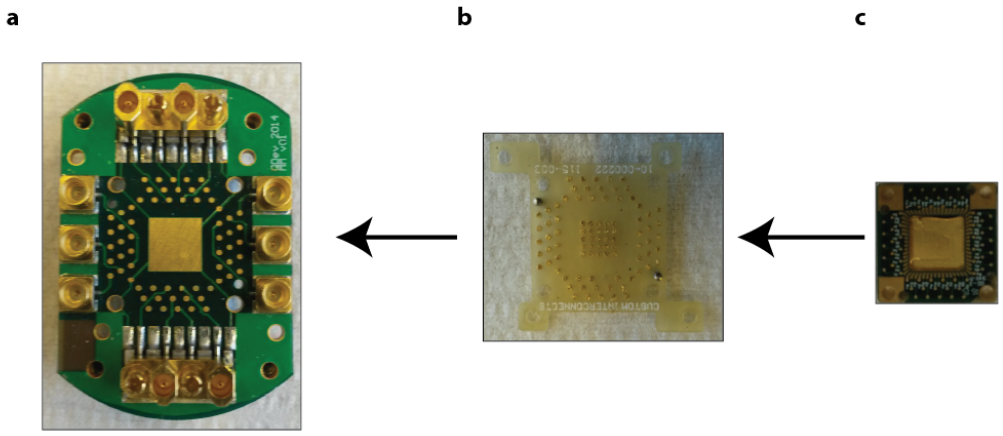

Figure 17: **Pictures of the parts hosting the sample inside the cryostat. a** shows a motherboard, on which an interposer (**b**) will be placed with a daugtherboard (**c**) on top of it. The sample (not shown) itself will be bonded to the daugtherboard.

the **puck**. The puck is a casing made out of gold plated copper with 4 rods from which the motherboard(s) are suspended. In either end, there are nano D-sub connectors supporting 51 DC lines and on the top end there are also SMP connectors. These connectors will be attached to the motherboard using a corresponding cable. In most setups the SMP connectors would be used for connecting high frequency lines, however in this project they were used to carry high current without a filter.

The puck is what will eventually be loaded inside the cryostat. Where the casing is in thermal contact with the coldfinger, the coldfinger is in thermal contact with the mixing chamber described in section 6. The casing in contact with the rods, the rods with the motherboard, the motherboard with the daughterboard and the daughterboard through the bondwires with the sample. In this way the sample will reach the temperature of the coldfinger once loaded. The connectors (both nano D-sub and SMP) on the top side will seamlessly slot into opposing gender connectors on the bottom of the cryostat while loading. The connectors on the bottom side is there to ground the DC lines so as to not blow up the device by electrostatic discharge. The pucks do not have SMP connectors on the bottom side, meaning that in order to ground the superconducting wires, one will have to bond from one of the normal conducting contacts on the daugtherboard PCB to one of the superconducting ones, further limiting the number of available wires.

Once the daugtherboard has been loaded onto the motherboard and the motherboard has been connected to both the top and the bottom of the puck, the casing is secured around the puck by screwing 4 screws in and the puck can then be loaded.

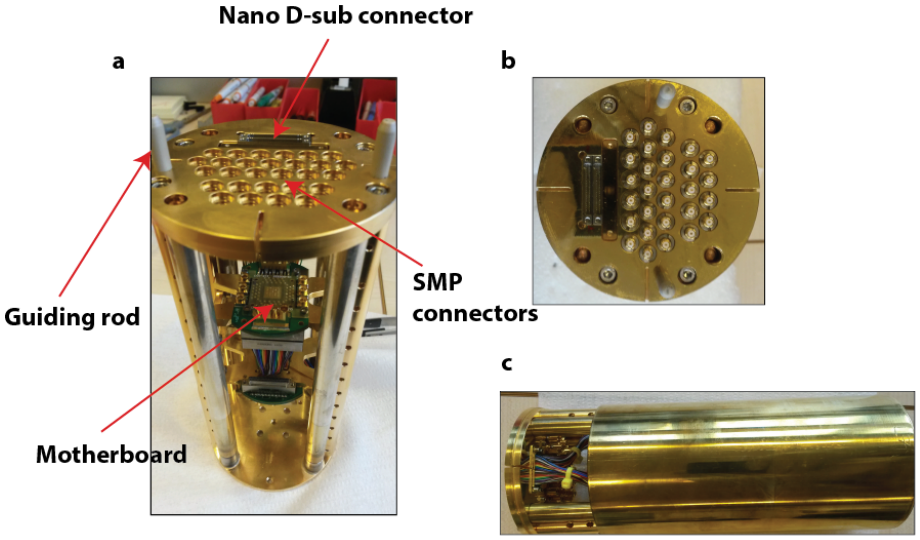

Figure 18: **Photograph of the puck. a** The inner part of the the puck can be seen with two motherboards screwed unto the four rods. textbfb A top view of the puck showing several SMP connectors ordered in two groups and two nano-D connectors. **c** A partially open puck to illustrate how the inner part fits into a shell.

The loading is done using a loading stick. The loading stick functions as a load lock and allows for changing the sample while not letting the cryostat heat up too much or lose pressure. Using the loading stick samples can be changed without disturbing the vacuum and with mixing chamber plate temperature only rising to around 70 K. This saves substantial time and energy once the samples have been changed and the puck is loaded again with the new sample inside. A sample change with the loading stick on average takes approximately 17 hours. Cooling down from room temperature (necessary for each sample change without the loading stick) take approximately 60 hours, additionally the cryostat would first need to heat up to room temperature, which takes on the order of three days. Guiding rods on the puck make sure that the puck will always, without fail, slot into the connectors on the coldfinger. Once the puck has been loaded using the loading stick, the stick is retracted and the cryostat is sealed before cooling down (see section 6).

7.2 Electrical connections from the puck to the laboratory equipment

The sample is not entirely cut off from the rest of the world as it is still electrically contacted through the bonds. Those bonds are how the sample is measured while inside the cryostat. This subsection describes the wiring inside the cryostat. Any alteration to the circuits described within requires at the minimum to break the vacuum and remove part of the outer vacuum can. A more detailed description of a how a cryo-free dilution refrigerator was given earlier in section 6.

The puck is connected directly to the coldfinger. Beyond supplying thermal contact to the mixing chamber plate, the coldest plate of the cryostat, the coldfinger also

connects the two nano-D and 12 SMP connectors to wires. The two types of wires do not take the same path to the outside world, as they have different requirements. First I will explain how the DC lines are connected to the instruments outside the cryostat, and then explain how the path of the superconducting wires is different.

Each nano-D connector has 48 connections. From the connector in the coldfinger these 48 wires are split into 2 set with 24 wires each called looms. The looms serve two purposes: to keep the wires tidy and to reduce noise from stray magnetic flux. To further protect these looms they are encased first a layer of Eccosorb, which absorbs radiation and then the outside of the Eccosorb is covered with copper forming a Faraday cage, the purpose of both part is to reduce any noise in the system. Encased in their protective shell, the looms will eventually reach a set of filters that will filter out noise. On the other side of the filters the looms are unprotected.

After passing through the filters, the looms will make their way up the cryostat passing the 5 stages described earlier in section 6 on the way up. Each stage has increasing temperature in ascending order. To make sure that the electrons reaching the sample has the desired temperature (around 100 mK) and to prevent the cryostat from heating up from heat dissipation, the looms are carefully thermalized on each stage. The thermalization is optimized with regard to the space by either pressing two plates together around the loom or by coiling the loom around a post. By having the loom be thermalized at each stage and not only at the last, a lot of the energy is dissipated at the upper, hotter plates which do not directly affect the temperature of the sample. After having reached the top plate of the cryostat, the wires then exit through a vacuum feed-through. The feed-through allow for an electrical connection to be made to the outside without breaking the vacuum. After having left the cryostat the wires continue in a shielded cable to a **breakout box**.

A breakout box is a box where the 24 wires in the cable "break out" into 24 individual wires. The breakout box acts as a sort base for the measurement. Each wire has a BNC connector and each connector can be set to one of three different configurations by a switch. "Ground", which ground the specified connectors. "Switched to", which allows whatever is connected to the BNC connector to connect to the sample. This can also be used to make a line floating if it is not connected to anything. The last setting, "Bias", is setting to bias which will connect the select connectors to an extra connector which by itself is not connected to any wire inside the cryostat.

Having discussed how the DC lines make their way up the cryostat and connect to the measurement equipment, it is now time to look at the superconducting lines. They start at the 12 SMP connectors at the coldfinger where they are gathered into a loom.

The main purpose of the superconducting wires in this project is to induce a magnetic flux from the flux bias line which will eventually go into the superconducting loop. Inducing sufficient flux to gather a full flux quantum requires a current on order of 100 μA due to the size constraints of the chip. Since the filters in the cryostat have a finite resistance (around 4 kΩ and the current would have to pass through each way), filtering the superconducting wires would induce more heat than the

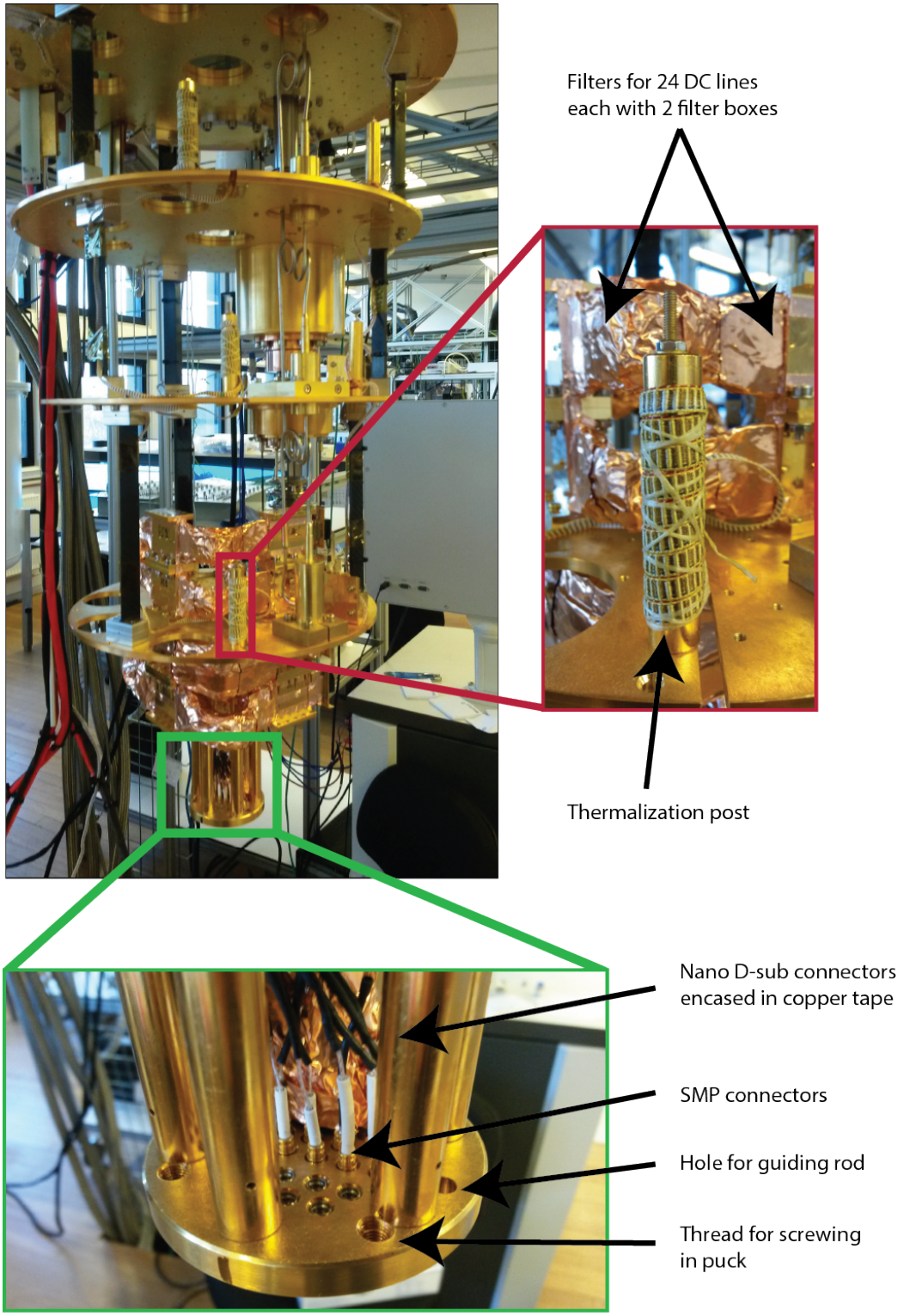

Figure 19: Schematic drawing of the wiring inside the cryostat. It can be seen how the wires go from the puck and out into the breakout box where each wire can be addressed individually by grounding it, switching it on and possibly connecting it to further instruments.

cooling power of the mixing chamber can keep up with. Since there is no way to increase the cooling power (or this would already be done), one will have to let the superconducting wires bypass the filters and live with the noise there might be.

After having bypassed the filters, the superconducting loom make its way up the cryostat much the same way as a normal conducting loom. Like the other looms, the superconducting loom gets thermalized at each stage. The loom is made out of a Niobium-Titanium alloy which has a critical temperature of around 9-13 K, which mean that the resistance above can cause the wire to heat up in the higher levels of the cryostat. At the top of the cryostat the wires exit through their own vacuum feed-through. Although one could guide the superconducting wires into a breakout box, in the measurement setup used for this project, the wires end shortly outside the cryostat in a rack with a BNC connector for each of the wires.

7.3 The filters in the cryostat

A series of filters are used to reduce noise during measurements. Each DC line would be filtered in six stages, over the course of two PCB filter boards. The first filter board, called the RF board, had three stages of RF filters. The three RF filters had cutoff frequencies of 80 MHz, 1450 MHz and 5000 MHz. The other board, called the RC board (see figure 20a, had a RF filter with a cutoff frequency of 80 Mhz and two RC stages with a cutoff frequency of around 15.6 kHz [18]. The effectiveness of the filters were tested by applying a 100μA signal through a chip that had intended shorts between bondpads, eliminating effects that could occur from measuring a sample. The gain as a function of the frequency of the signal can be seen in figure 20b. A circuit diagram of a RC filter can be seen in figure 20d. The cutoff frequency is defined by the equation:

$$f_c = \frac{1}{2\pi RC} \tag{21}$$

Each filter board filters 24 DC lines, resulting in two sets of filters being necessary to filter the 48 DC lines available on a daughterboard. 12 lines and their filter components run on one side of the board and the other twelve on the other side. At either end, a nano D-sub connector allows connection to and from the filterboard. Metal brackets are screwed in tight around the filterboard before being mounted on a plate in the cryostat. The metal brackets ensure thermal contact with the cryostat.

A DC line going into the cryostat after being thermalized at the different plates first reach the RF filterboard where it would be filtered in the three RF stages, then through a jumper cable reach the RC filterboard where it would be filtered three times more, first one RF filter and then two RC filters. After being filtered a total of six times, a short piece of cable connect the RC board to the nano D-sub connector on the coldfinger. Both the jumper cable and the cable from the RC board to coldfinger were protected in first a layer of eccosorb and then a layer of electrical tape. A photograph of the mounted filters can be seen in figure 20c

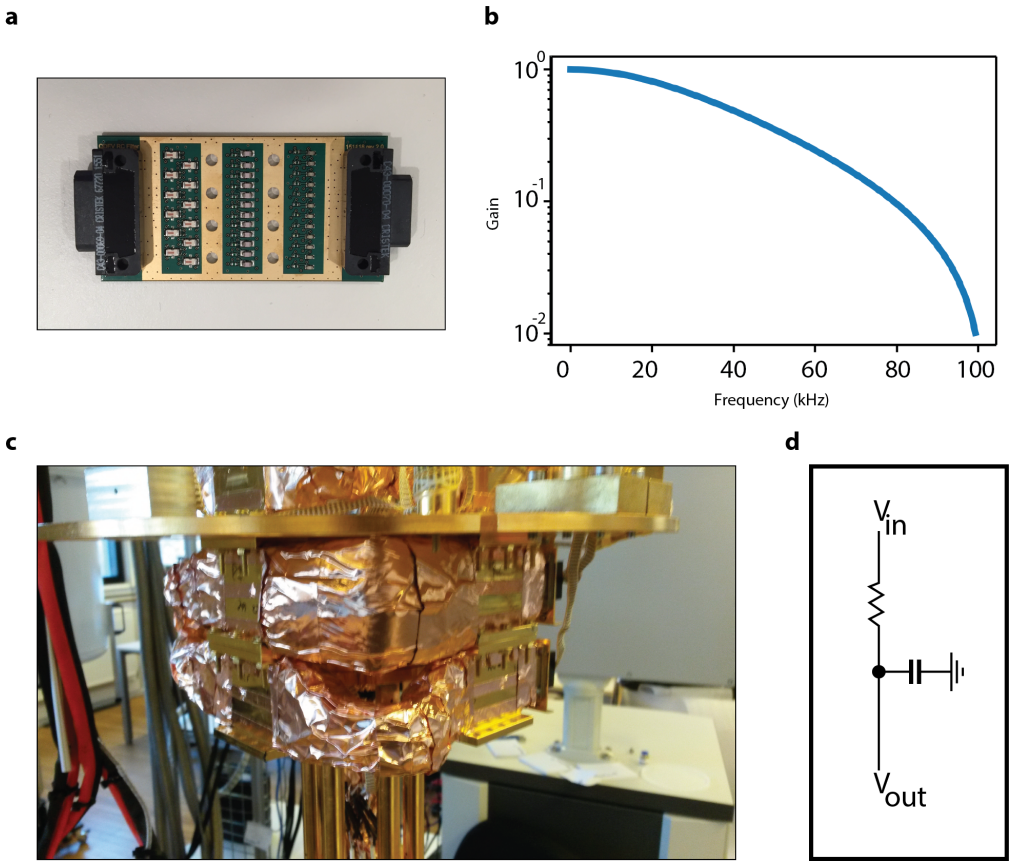

Figure 20: **Each DC line was filtered 6 times inside the cryostat.** **a** Photograph of a RC filterboard which contained 1 RF filter and 2 RC filters. The RF filterboard (not shown) was place before the RC filterboard with 3 RF filters. **b** Test of filter measured. **c** Photograph of filters installed on the mixing chamber plate. **d** Circuit diagram of a RC filter.

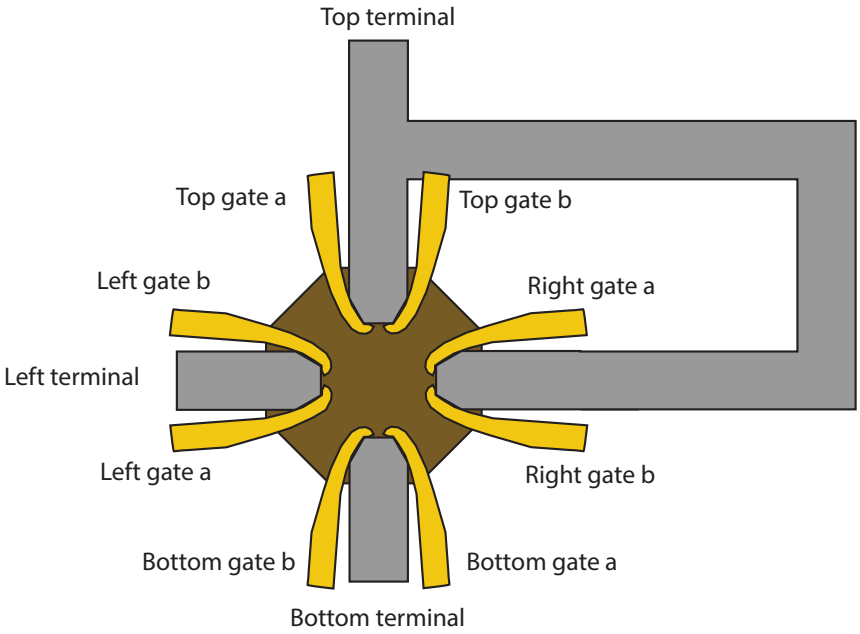

Figure 21: **Simplistic drawing of a 4-terminal josephson juction device.** All leads have been shortened for clarity. Grey is aluminum, yellow is gold and brown is the 2DEG

7.4 Setting up the measurements in the outside the cryostat

Now that is has been detailed how the sample is connected to the puck and how the puck is connected to a breakout box in the lab outside the cryostat, it can be understood how other instruments in the lab can be connected to the sample.

There are many different instruments one might want to connect to the sample. What they all have in common is the way to connect them to the sample inside the cryostat. The output or input channel of the instrument is connected to one of the BNC connectors on the breakout box and the corresponding switch can be switched on. To avoid damaging the device, the output of any given instrument should always be zero when connected to the device and only after being switched on should it be increased at a safe pace.

To get an idea of what instruments will be used for the measurements look at figure 21. The focal point of the project is the electron and hole states in the junction, so a current will need to pass through the junction to sample these. For this a technique known as phase sensitive detection will be used which requires a reference signal from a **lock-in amplifier** to be sourced at one terminal and for each of the drains to be connected to a lock-in amplifier. Phase sensitive detection is explained in detail below.

Lock-in amplifiers are not capable of outputting voltages in a range where the device does not blow up, so a **voltage divider** will be necessary as an intermediary between the lock-in amplifier and the device. By changing the input to a safe range, the output has been changed to a unmeasurable range and a **current amplifier** is now needed between the sample and the measurement lock-in amplifier.

Control of the conductance to and from each terminal is desirable and thus the QPCs will need a **voltage sources** to allow them to gate the 2DEG. In an ideal world the QPC will be symmetric and the two halves could be connected to the same voltage source, however the world is rarely ideal and 8 separate voltage source are therefore preferable
Lastly a flux bias line will require a **current source** to source a current high enough to induce a magnetic flux through the loop

The purpose of a lock-in amplifier is to amplify the signal compared to the noise. This is done by the lock-in making a reference signal which is uses to excite the sample. The output of the measurements is then fed back into the lock-in amplifier. The output signal might have noise from any number of sources, however most of this noise will not match the frequency of the reference signal. The instrument is then capable of eliminating all signals that do not match the reference, thereby canceling the noise. This technique is known as phase sensitive detection.

Phase sensitive detection relies on multiplying the reference signal with the signal from the measurements. The result of this multiplication is two AC signals, one with a phase equal to the difference in the two signals and one equal to the sum. [27]

$$V_{psd} = V_{sig}V_L\sin(\omega_r t + \theta_{sig})\sin(\omega_L t + \theta_{ref}) \tag{22}$$

$$V_{psd} = \frac{1}{2}V_{sig}V_L\cos([\omega_r - \omega_L]t + \theta_{sig} - \theta_{ref}) - \frac{1}{2}V_{sig}V_L\cos([\omega_r + \omega_L]t + \theta_{sig} + \theta_{ref}) \tag{23}$$

The AC signals can be filtered out to some degree using a standard low pass filter, which means that every signal will be filtered out except for the case where the difference is 0. In the case of zero difference, the signal becomes a DC signal proportional to the amplitude. Good quality lock-in measurements thus require a mixture of good filters and good choice of reference frequency. A good reference frequency is away from big bands of noise such as the band generated by standard 50 Hz electrical grid noise and the harmonics of this.

Phase sensitive detection can be either digital or analog. In the digital case the analog input signal will be converted to a digital signal before being multiplied by a digital reference signal. Digital lock-in amplifiers' dynamic reserve (tolerated noise to signal ratio) is only limited by the analog to digital conversion whereas in a analog amplifier it is limited to about 60 dB. The lock-in amplifiers used for this project were model SR830 from Stanford Research Systems

The next part will focus on how the measurements of the samples were set up. For a reference on the geometry of the sample see the simplified drawing in figure 21.

The first thing to measure in a sample is simply to test whether or not the device is operational. This is done by testing for leakage. Leakage occurs when there is an unintentional short in the circuit. In these kinds of devices, there are 2 primary ways the device can leak: mesa leakage and gate leakage. Mesa leakage occurs when the etch process described in section 3 was not deep enough (approximately

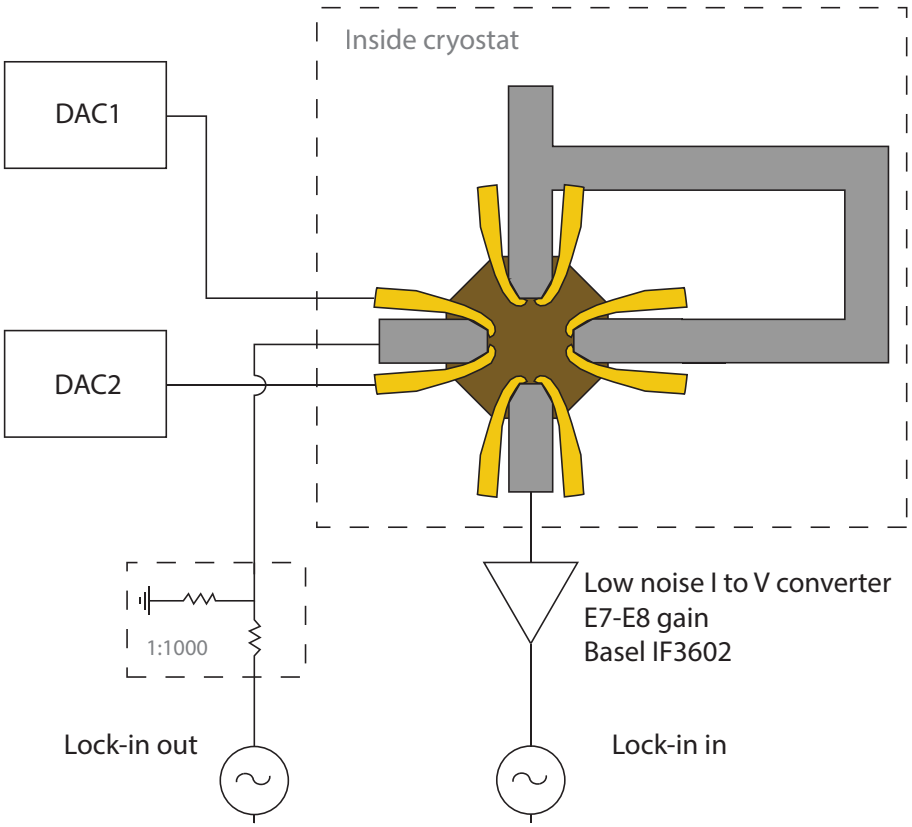

Figure 22: **Drawing of a gate-gate measurement setup**. An AC excitation is supplied by the lock-in which is then connected to the left terminal. If there is not gating, the current can pass through the 2DEG and into the bottom terminal where it will go into the lock-in again. As an increasingly negative voltage is supplied to the 2 gates of the QPC at the left terminal, the current will first diminish and then vanish entirely.

200 nm is required) to remove some conducting layer. The exact nature of this layer is as of yet unknown, however experiments show that a conducting layer can form if the etch is too shallow. The consequences of mesa leakage can be that current can pass through the entire substrate, all the way from one device to another device, easily crossing millimeters of distance. The gates might also leak through the protective hafniumoxide and into the aluminum or the 2DEG below. It can be hard to determine what exactly is the cause of the leakage since leakage from gate to the ohmics might also be a leakage current traveling through the mesa and into the 2DEG bondpad which is bonded below the gold on the gate contacts.

The next thing to test on a device is whether the gates are operational. This is done by connecting the sine output from the lock-in amplifier to first a voltage divider and then one of the terminals, say the left one. Another terminal for example the bottom one is then connected to an element which first amplifies the current, then converts it into a voltage signal and then direct the signal to the input of the lock-in. Each gate of a QPC is then connected to a voltage source. By sweeping the voltage on the QPC it can been seen when the conductance from terminal to terminal drops to zero and the QPC has been "pinched off". See figure 22 for an illustration of the measurement setup. This example was deliberately the simplest one. The more

advanced case is measuring the pinch off of the QPCs on a loop. Since there are now several QPCs blocking (or not blocking) access to the terminal, simply sweeping one of them will never actually pinch off the device, it might reduce conductance enough to give a clear picture of when the QPC is pinched off but reality is usually not as clear as that. Instead all the QPCs can be swept equally until the terminal is completely pinched off and then that pinch-off voltage can be used to close one QPC while the other is swept. In the ideal case of perfect alignment and everything being defined perfectly by lithography/etch/metal evaporation all QPCs would of course close at the same voltage, however that is rarely the case in the real world. After a relationship for the gates compared to the pinch-off of the QPC has been determined, this ratio of voltages can be then used to close the QPC in the following measurements

The QPC might not give the biggest conductance plateaus (see section 2.6) by closing the two gate symmetrically. For this reason it is a good idea to make a "gate-gate" by sweeping the two voltages against each and showing the conductance in a three dimensional plot.
To get an overview of the states in the system one makes a source-drain bias map. This is a three dimensional with the source-drain bias on one axis, a gate voltage on the other and conductance shown on a color scale. A terminal is chosen as the source where an AC excitation is supplied, however unlike the last example the AC signal is now mixed with a DC signal. The AC excitation remains with a constant amplitude and only the DC signal is swept during the source-drain bias sweep.

The last kind of typical measurement in this project is the flux sweep. The flux sweep picks a single line in the gate space from the source-drain bias sweep and then measures what happens to the conducting states if a magnetic flux is forced through the loop. The basic setup is similar to that of the previously mentioned source-drain bias sweep, however instead of sweeping a gate voltage, it is locked in place. Either a magnet or a flux bias loop can be used to induce a flux. The y-axis and z-axis (color scale) remain the same, and the x-axis is then the magnetic flux in units of the flux quantum through the loop. Any conductance carried by Andreev bound states would be affected by flux passing through and should undergo a full period in 1 flux quantum.

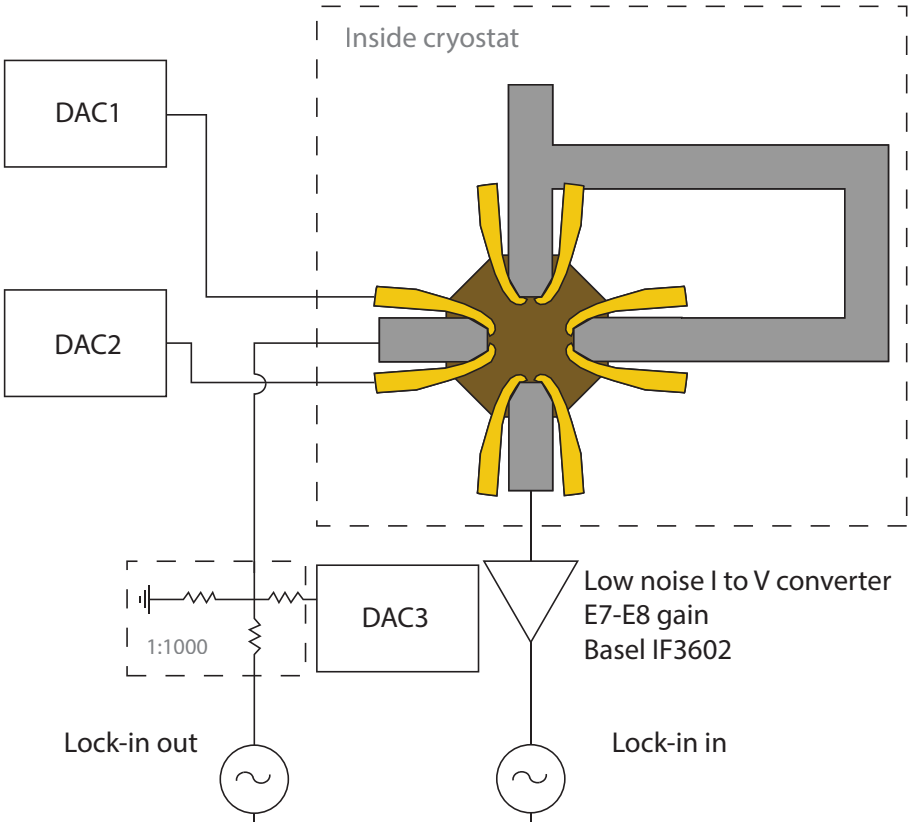

Figure 23: **Drawing of a gate-gate measurement setup.** Similar to the gate-gate sweep shown in figure 22, but now the AC signal from the lock-in amplifier is mixed with a DC signal from a voltage source.

8 Results

This section will contain results from the project. The results will be discussed at the same time, give possible explanations for the data observed. All measurements done on a system as the one shown in section 7.

The first thing to be measured in a new device as described previously in section 7 is to test for leakage currents. Everything but a single gate would be grounded and a sourcemeter would be connected to a single gate contact at a time. The sourcemeter sources a voltage and measures the current at the same time. The sourcemeter would then be used to slowly ramp the voltage from 0 down to -1 V while measuring the current. Ideally there would be no measurable current increase as in figure 24a, but a resistance of 10 GΩ was generally considered to still be viable to continue measurement (see for example figure 24b). A leaking gate on the other hand would have exponentially rising current with an applied voltage as in figure 24c. The compliance on the sourcemeter was set to the minimum of 10 nA meaning that the current could not go over that value. The compliance acts as a safety net, hopefully preventing damage to the device due to the current. Even with the compliance, the measurement would be stopped early if there was an obvious leakage current.

The next thing to be measured was the control of the QPC over a single terminal. An AC excitation was sourced to one terminal and the current was read out at the other terminals. The two gates of the split gate QPC were always swept symmetrically (equal voltage on both gates) initially. Most QPCs were able to pinch off the terminal although it would often not show signs of quantized conductance. While the system has four terminals, two of them are connected so if a voltage is sourced at one terminal it will be possible to measure at two drains. If the gate voltage at a drain QPC is swept, the measured conductance at that drain electrode should show quantized conductance like the one described in section 2. If however, the source QPC is swept instead, the drain electrodes should individually not show quantized conductance in steps of $2\,e^2/h$ as the two drains need to share the quantized current. Instead one would expect the sum of the conductances in the two electrodes to be quantized in steps of $2\,e^2/h$. This is consistent with measured results during this project, as can be seen in figure 25.

Due to broken symmetry of some kind, be it from a fabrication process or just intrinsic properties of the scattering region, the best way to close (and open) a split gate QPC might not be with symmetric voltages. Best in this case meaning biggest plateaus. This can be investigated by plotting the conductance as a function of the two voltages creating a gate-gate map. QPCs in the systems investigated in this project, show the same general trend in a gate-gate map. Both gates of the QPC need to reach a certain threshold value before the conductance is pinched off. This threshold appears to be approximately the same across the 8 gates on the same device. This threshold could be the gate gating the normally open 2DEG underneath it, blocking the current from flowing under the gate.

An overview of how the conductance through the QPCs was modeled can be seen

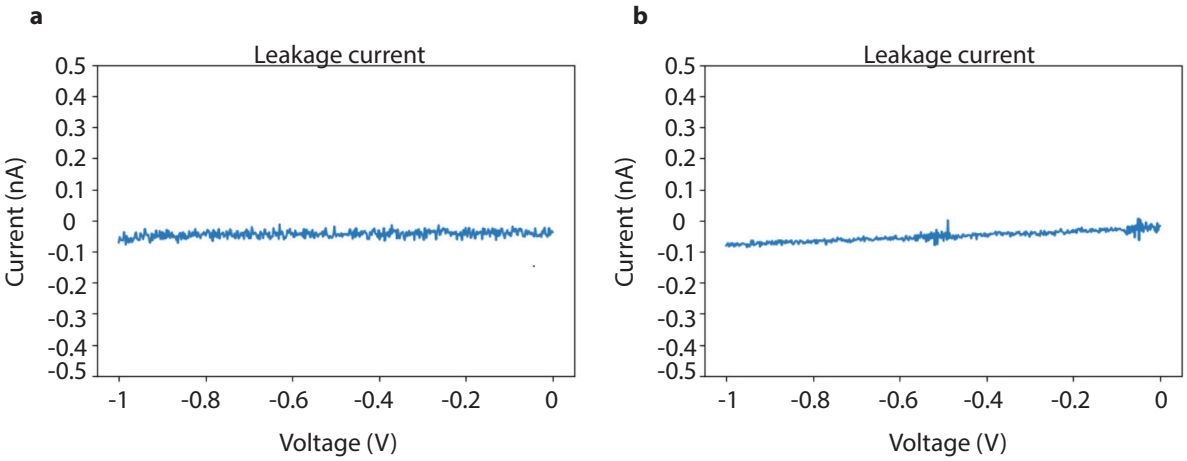

Figure 24: **Examples of leakage current measurements of working devices.** **a** Ideal measurement with no visible slope. **b** Measurement of a gate where the resistance is still high enough that the gate was considered working. Resistance is the 10 GΩ range. **c** A leaking gate results in an exponential increase in current with an applied voltage.

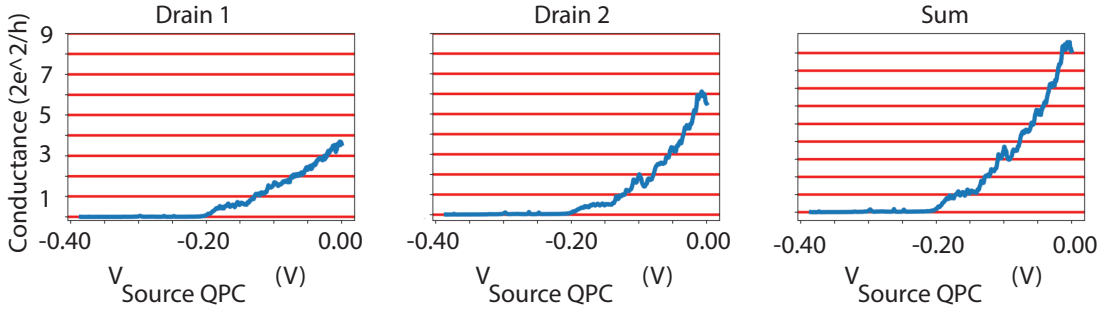

Figure 25: **Quantized conductance in a system with 3 drains.a** Conductance measured at the first drain. **b** Conductance measured at the second drain. **c** Sum of the two conductances show that the conductance through the source QPC is quantized and has a plateau at $2\,e^2/h$.

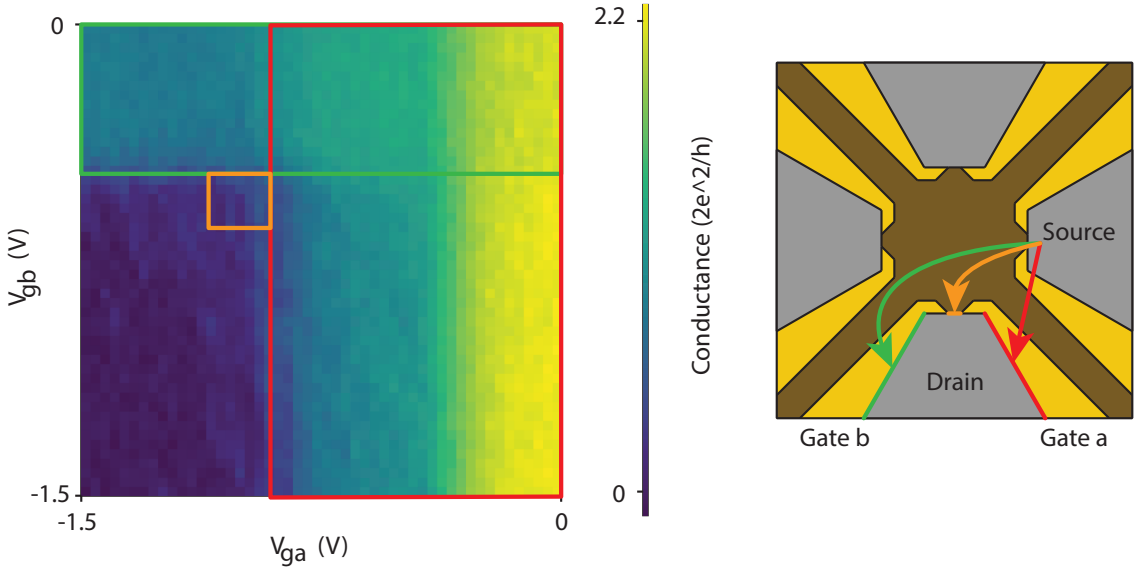

Figure 26: **Model of how conductance signatures corresponds to different current pathways.** The red path denotes the direct path of a terminal from the source to the drain. This path can be controlled solely by the gate on top of the path. The green path runs around the closest gate, but not necessarily through the QPC. The orange path runs through the QPC. The conductance signature of each path is marked with similar colored rectangle.

in figure 26. In most of the QPCs there were no plateau-like features present where they were expected (shown in the orange rectangle in figure 26). It is possible that separation between the split gates was too small, making it impossible to gate the 2DEG underneath the gates without also closing the QPCs. This would explain why there are no visible plateaus in the gate-gate map as they would effectively be overshadowed by the massive conductance of the electrons simply going under the gates. A solution to this would be increasing the separation between the gates, which would mean a more negative voltage on the gates would be required to constrict the channel. In the model, this would push the orange area further down and to the left while keeping the red and green areas the same. Alternatively the coupling to the 2DEG could be increased, for example by reducing the ALD layer, which would push the red and green area further to the right and up respectively. Reducing the ALD layer would however increase the likelihood of leakage.

Once the conductance response of manipulating the gates was established, the device would be put into a regime of low conductance and a source-drain bias spectrum was measured. The conductance is kept low to keep the system simple by only allowing a few channels to be open. for an S-N-S junction a gap is expected of the size 4 Δ which means the gap was approximately 0.2 meV in the measurement seen in figure 27. Definite traces of states inside the gap can be seen in figure 27.

Once a region is picked, the source-drain bias is then swept against the magnetic field with a fixed gate voltage configuration. The results of such a measurement can be seen in figure 28

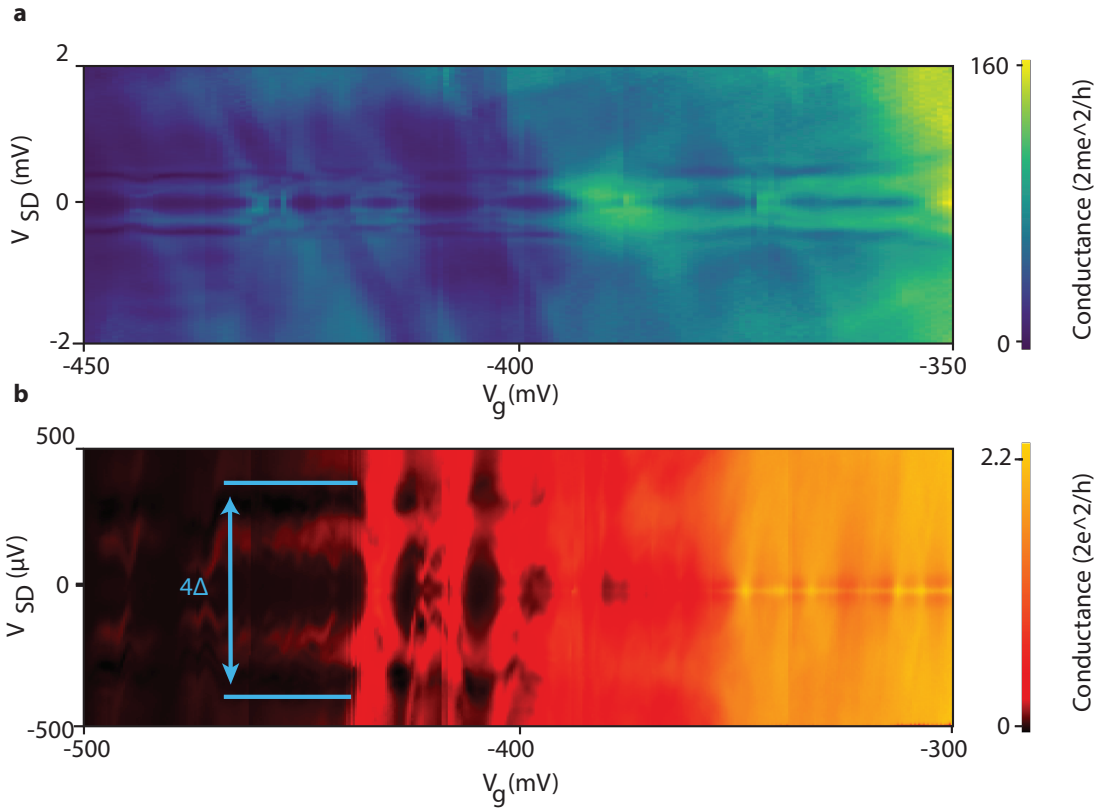

Figure 27: **Source-drain bias spectra as function of drain gates of a 4-terminal device.** **a** Source-drain bias spectrum with a DC source-drain bias of $\pm 2\,\mathrm{mV}$. The gap and continuum above and below is clearly visible. Diagonal features resembling a coulomb diamond can also be observed. **b** Source-drain bias spectrum with a DC source-drain bias of $\pm 0.5\,\mathrm{mV}$. The superconducting gap is marked with blue lines. There are clear signatures of conducting states within the gap.

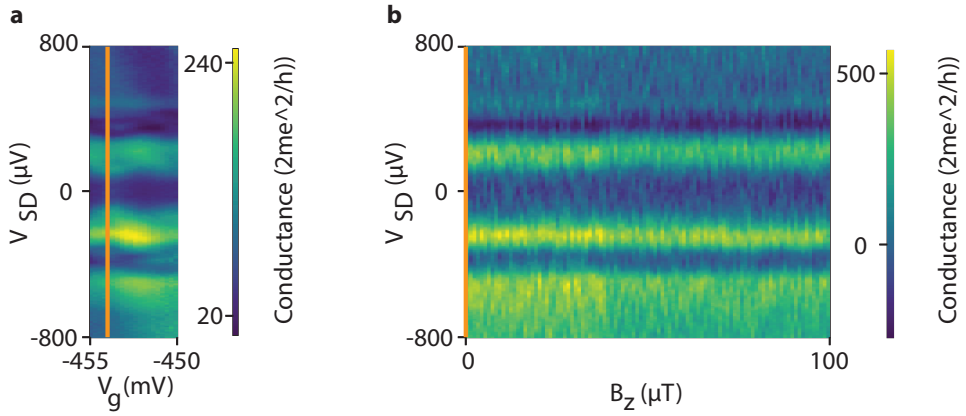

Figure 28: **Source-drain bias spectrum of a 4-terminal device.a** Section of a source-drain bias spectrum, with the gate configuration chosen for **b** marked with an orange line. Gate voltage is a symmetric voltage on both the source gates. 1 non-loop terminal completely closed. Loop (drain) gates completely open. **b** Source-drain bias against an applied perpendicular magnetic field on the same device with the same gate configuration as in **a**. The orange line corresponds to the orange line in **a**.

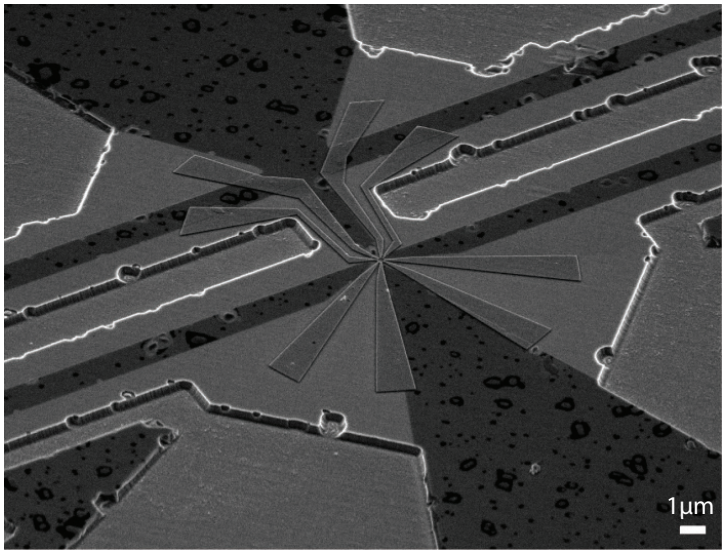

Figure 29: **Defects in 2DEG material cause damage in the aluminum layer.** Severe damage can be see in the aluminum layer. The observed phase decoherence in the system was contributed to these defects. Defects were present on all chips made from the wafer.

The source-drain signal is sourced at the non-loop terminal which is constricted into low conductance by a QPC located next to the superconductor. The two terminals on the loop are completely open whereas the last terminal is completely closed. In figure 28a, while sweeping a range of 100 μT no effect was observed in conductance, despite it being calculated that it should have a period of 83 μT, by measuring the size of the loop. The most likely scenario is that the loop was not phase coherent along the entire path.

It is possible that the lack of phase coherence in the loop stems from defects in the material. The M26 material, similar material to the one used for the measurement in figure 28, for unknown reasons had a large number of defects underneath the surface, damaging the aluminum at the top. The defects are also perceived to be the root of other problems, including instances of no supercurrent in the junction, even though the junction geometry was known to support supercurrent. The defects are also credited for several problems with the etching, causing a significant amount of devices to have broken loops. A tilted SEM micrograph of the defects can be seen in figure 29.

The surface of the aluminum which should be smooth is instead filled with defects. The defects result in both big and often damage to the aluminum. The defects appear to be spread evenly over the entire chip and though less extensively investigated, the other chips made from the same wafer seem to have the same problem. The defects seem to be present in even untreated pieces of the M26 wafer, and it is therefore highly likely that the defects originate from the growth.

In section 2.5 it was mentioned that a central gate would be necessary to control the scattering region which would be useful since only about 5% of randomly generated matrices have topological transitions. Initial attempts to fabricate 4-terminal de-

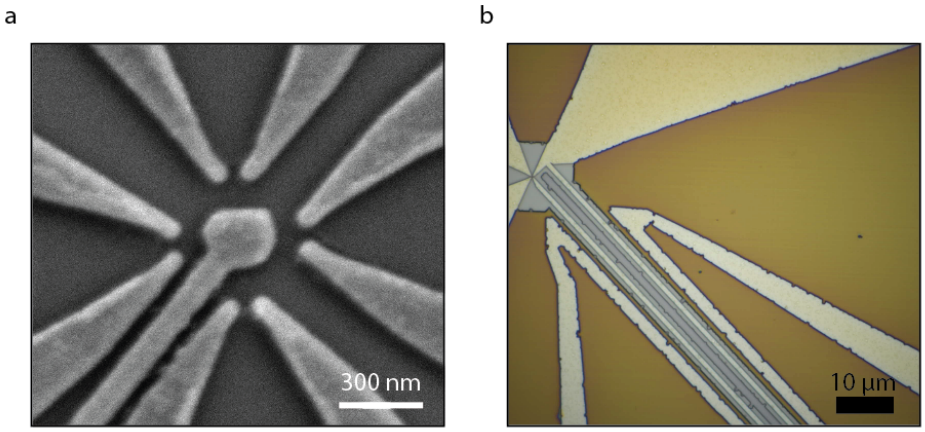

Figure 30: **Micrographs of devices fabricated, but not measured on. a** a SEM micrograph of a 4-terminal device with a central shape gate. Simpler devices were prioritized. **b** 4-terminal device with a flux bias line around a bigger loop to reduce the necessary current. The increased length compounded etch problems, leaving few devices with whole loops.

vices with a central shape gate were carried out, however there was no measurement conducted on these devices as the overall quality were lower than the devices without and it did not seem worth prioritizing while there was no good data of phase control, since the transitions would be impossible to detect without the phase control. An SEM micrograph of a design with a central shape gate coming in between the QPCs of two terminals can be seen in figure 30a. Another design was also able to complete lift off, were made with a five fold symmetry in the junction. Each terminal would take up one side of the pentagon with the gate coming in from the last side.

Several attempts were also made to create flux bias lines accompanying bigger loops like the one seen in figure 30b. Typically 80% or more of 4-terminal devices were made with flux bias lines in an effort to create a system where the phase could be controlled locally. The lengthscale required of both the the superconducting loop and the flux bias line made the the structures very susceptible to the aforementioned etch problems, often breaking the superconductor completely (clearly visible in an optical microscope). In a few case where the loop and flux bias lines looked complete, measurements were in an attempt to control the superconducting phase with the flux bias line. These attempts were ultimately unsuccessful despite sourcing a higher current than predicted necessary from COMSOL computer models. It is probable that it was phase coherence of the material and not the design itself that was the problem, but it is not possible to test without using a new material. What was observed which is useful to take into consideration when further developing devices, was an increased heatload. It was not possible during the project to locate where exactly the heatload was located, but it was noted that the SMP connectors on the puck (see section 7 were not made of superconducting material and would therefore have finite resistance. The heatload with the used design would raise the base temperature of the mixing chamber about 20mK with the current predicted by models to induce a flux quantum. It is possible that a loop could be made long enough within the size constraints of the chip to have access to the full phase range

without heating up the mixing chamber appreciatively .

Attempts were also made to create two flux bias loops on a single 4-terminal device, however none looked promising enough to be measured due to etch problems.

9 Conclusion and outlook

This section will present what could be concluded from this project. It will discuss how the problems that came up during the project can be addressed in further research. Finally it will give some thoughts on where the research into multi terminal Josephson junction artificial non-trivial topological phases could head.

It is too early to say whether a system with topological phases like the one described in Riwar *et al* [1] can be fabricated. It is possible with current fabrication technology to create a junction geometry believed to be able to support topologically non-trivial Andreev bound states on a 2DEG substrate with epitaxial aluminum, but measurements indicate that the material quality of the superconductor measured during this project is lacking. Although Andreev bound states were observed in a 4-terminal device, there was a distinct lack of phase modulation from applying a magnetic field. Although more flux than one flux quantum was applied, there was no visible change in conductance. This lack of phase modulation is believed to originate from defects in the material breaking the phase coherence of the superconductor. These defects are homogeneously distributed over the wafer and are believed to come from the growth in the MBE, however other groups working with the same grower report that the defect problem varies from growth to growth. It is therefore possible that simply acquiring a new substrate would solve the aluminum problems. Fabricating on a substrate with less defects is also expected to reduce the observed problems with the wet etching, increasing resolution and reproducibility.

Although not theorized to be a hindrance to induce topological phases, it is expected to be difficult to observe these phases with the current lack of QPC control exhibited in this project. With the model of the QPC behavior described in section 8, this obstacle could be overcome by increasing the separation of the two gates in the split gate QPC. Increasing the separation is not without complications. The current design of the QPCs has points of the split gate facing each other which are supposed to create a constriction. The constriction will be broadened (see figure 5) and not a point, but the channel is still wider further away from the intended constriction. Increasing the separation would also increase this effect in turn increasing the risk of creating a large enough area to form quantum dots between the terminals and the QPC due to over etching or misalignment.

Preliminary attempts to create a central shape gate to perturb the scattering region was carried out during the project, however no measurements were carried out due to having no clear picture of how the junction behaves without the central gate. Further optimization of fabricating the gate would be necessary to reliably find topological phases, as Riwar *et al* [1] predicts only about 5% of the scattering regions to be capable of hosting topologically non-trivial phases. Two different geometries were fabricated, both of which could possibly be used in more advanced systems.

Going forward with investigating multi terminal Josephson junctions, it is probable that a new 2DEG substrate with fewer defects could solve the primary problems due to the hypotheses outlined above. Continuing on a 2DEG substrate would allow for great flexibility in design. Allowing for a large number of terminals or for squeezing

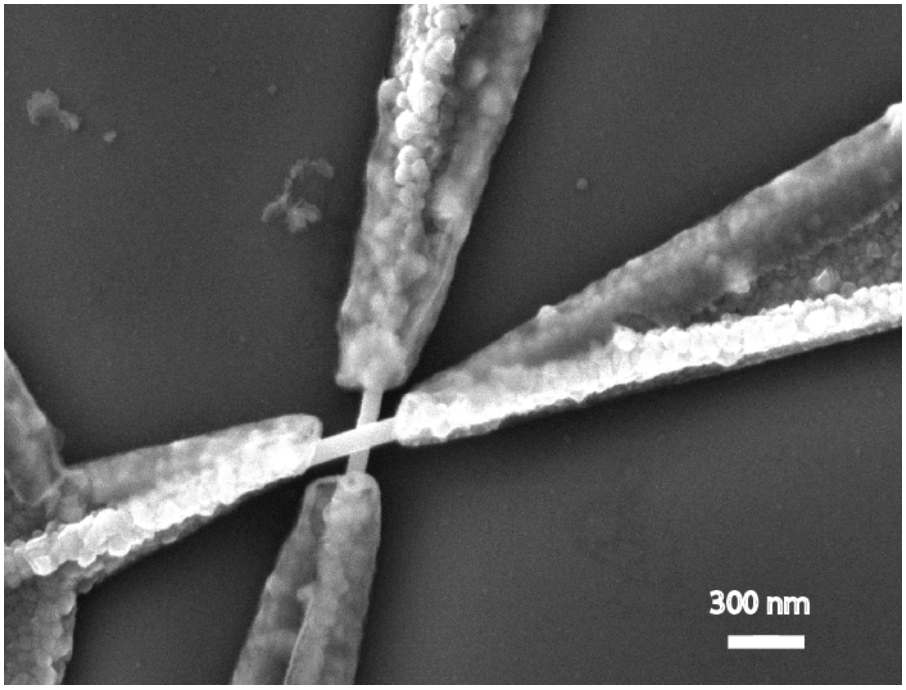

Figure 31: **Examples of the junction in an InAs nanowire cross device.** Nanowire cross devices has the advantage that the scattering region is defined by the growth and not by gates depleting the extents of the region.

terminals together to make room for a central gate.

Research could also be continued on a nanowire cross platform such as the one described in section 2. Since starting on the project, a new type of crosses have been fabricated. These new crosses made from indiumantimonide with epitaxial aluminum, have high yield and are easy to manipulate. The crosses have a junction that is defined by the growth and there is no chance of there being any accidental channels that avoid the scattering region, as those would have to go through vacuum. An example of a junction in a 4-terminal indiumarsenide nanowire cross is given in figure 31. The loops would instead need to be made by evaporated aluminum, which imposes it's own risk and rewards. The risk is that the interface between the old and the new aluminum is not phase coherent, however it also means that the aluminum which could be affected by defects in the growth of the nanowire is minimal.

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A Fabrication recipe

1. Clean: 5 minutes dioxolane ultrasonication, 15 minute dioxolane, 1 minute acetone, 1 minute IPA
2. Resist: 7.5 μL PMMA A4 for 45 seconds at 4000 rpm, bake for 3 minutes at 185
3. Exposure: Inner mesa: 60.000 dots 150 μm 500 pA 640 μC/cm2, beamsettling 10 minutes, outer mesa: 20.000 dots 600 μm 40 nA 750 μC/cm2
4. Develop: 60 seconds MIBK:IPA, 30 seconds IPA, 60 seconds plasma ashing
5. Etch: 120 second 115 °C reflow, aluminum etch: aluminum etchant D for 5 seconds while stirring at 49 °C, hot MQ water while stirring for 30 seconds, cold MQ water for 30 seconds, mesa etch: mix 220 mL MQ water, 55 mL citric acid, 3 mL phosphoric acid and 3 mL hydrogenperoxide, etch for 6 minutes while stirring, stop etch in MQ water for 40 seconds
6. Clean: 5 minutes dioxolane ultrasonication, 15 min dioxolane, 1 minute acetone, 1 minute IPA
7. Resist: 7.5 μL PMMA A4 for 45 seconds at 4000 rpm, bake for 3 minutes at 185 °C
8. Exposure: 60.000 dots 150 μm 500 pA 575 μC/cm2
9. Development: 60 seconds MIBK:IPA, 30 seconds IPA, 45 seconds plasma ashing
10. Etch: 120 seconds 115 °C reflow, aluminum etch: aluminum etchant D for 5 seconds while stirring at 49 °C, hot MQ water while stirring for 30 seconds, cold MQ water for 30 seconds
11. Clean: 5 minutes dioxolane ultrasonication, 15 min dioxolane, 1 minute acetone, 1 minute IPA
12. ALD: 10 hours pre-pumping followed by 150 cycles of hafnium oxide deposition at 90 °C
13. Clean: 5 minutes dioxolane ultrasonication, 15 min dioxolane, 1 minute acetone, 1 minute IPA
14. Resist: 7.5 μL EL9 for 45 seconds at 4000 rpm, bake for 3 minutes at 185 °C, 7.5 μL PMMA A4 for 45 seconds at 4000 rpm, bake for 3 minutes at 185 °C
15. Exposure: 60.000 dots 150 μm 100 pA 608 μC/cm2
16. Development: 60 seconds, MIBK:IPA, 30 seconds IPA, 60 seconds plasma ashing
17. Metal deposition: 5 nm titanium, 25 nm gold
18. Liftoff: Dioxolane 15 minutes to 12 hours

19. Clean: 5 minutes dioxolane ultrasonication, 15 min dioxolane, 1 minute acetone, 1 minute IPA

20. Resist: Resist: 7.5 μL EL9 for 45 seconds at 4000 rpm, bake for 3 minutes at 185 °C, 7.5 μL PMMA A4 for 45 seconds at 4000 rpm, bake for 3 minutes at 185 °C

21. Exposure: 60.000 dots 150 μm 100 pA 608 μC/cm2, switch beam to 44 nA and let settle for 10 minutes, 20.000 dots 600 μm 44 nA 800 μC/cm2

22. Development: 60 seconds, MIBK:IPA, 30 seconds IPA, 60 seconds plasma ashing

23. Evaporation: 10 nm titanium at 5 degrees, 40 nm gold at 5 degrees, 170 nm gold at 0 degrees, 40 nm gold at 10 degrees

24. Liftoff: Dioxolane 15 minutes to 12 hours

25. Clean: 5 minutes dioxolane ultrasonication, 15 min dioxolane, 1 minute acetone, 1 minute IPA

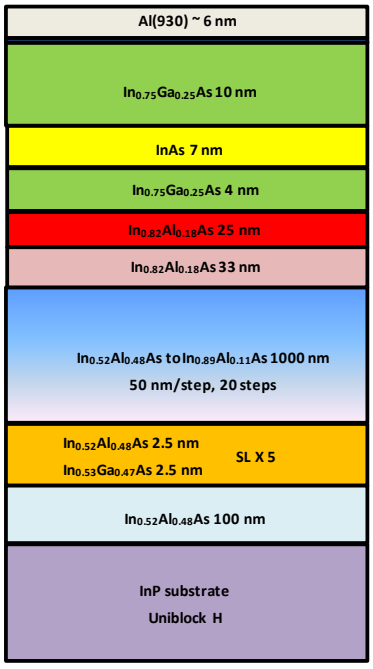
B Material summary from M. Manfra

M03-12-18.2

Summary

Wafer Context/Description: MZM structure with 7nm InAs QW in InGa(25%)As barriers

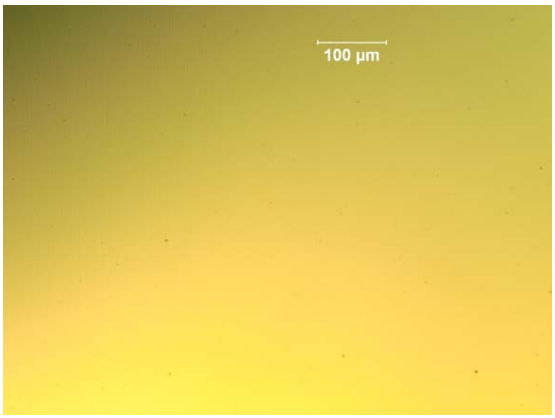
Layer Stack



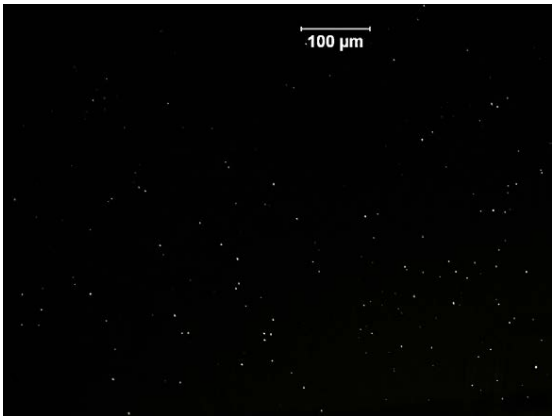
M03-12-18.2

Surface morphology

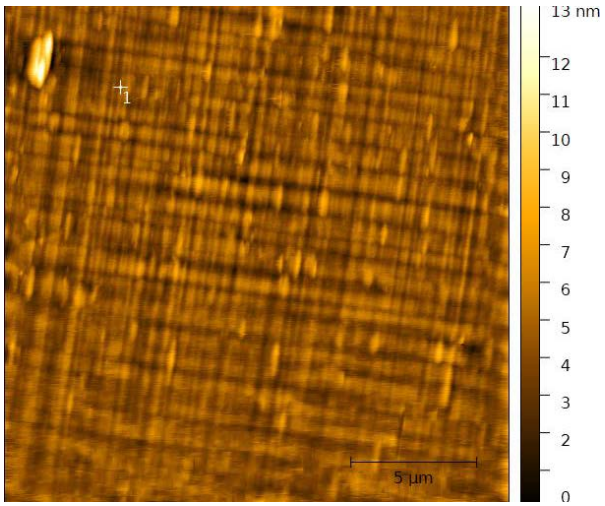
Optical micrograph



Dark field



AFM 20x20 µm²



RMS= 0.9 nm