CIRCUIT QUANTUM ELECTRODYNAMICS OF A TWO-DIMENSIONAL ELECTRON GAS BASED GATEMON QUBIT HOSTING A QUANTUM DOT

Master thesis

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Abstract

In this thesis i present Circuit Quantum Electrodynamics (cQED) and transport measurements of a semiconducting gate tunable transmon (gatemon) with a gate-controlled quantum dot formed in the Josephson junction. The "Dotmon" was fabricated in a Two-Dimensional Electron Gas (2DEG) heterostructure on an InP substrate, by using state of the art Electron Beam Lithography (EBL) techniques. We report successful in-situ switching between transport and cQED measurements using a secondary Josephson junction with a simple Field-effect-transistor (FET) type gate on the qubit island. Current-bias transport measurements show a controllable critical current (I_c) in the Dotmon device of 1-100nA, tuned by the dot-forming electrostatic gates of the device. We confirm several quantum dot associated resonances in the critical current, and correlate them directly with an enhancement of the qubit frequency (f_q) in two-tone spectroscopy measurements.

Coplanar waveguide (CPW) style resonators made of superconducting aluminium were designed, fabricated and measured to "fit" the control circuitry to the dotmon qubit. Specifically, the coupling from the resonator to the feedline, represented by the external quality factor (Q_e) of the feedline-resonator system, was "controllably designed" to go from $Q_e \approx 23.000$ to $Q_e \approx 3.000$. This allows for faster measurements of posssible low-lifetime qubits.

On-chip crossovers connecting the groundplane of the qubit chip across feedlines and resonators were designed, fabricated and measured for a cleaner microwave environment on the qubit chips. The crossovers were measured at room temperature in a DC probe station, and proven to connect the groundplane across a feedline with minimal resistance, with no leakage to the feedline. The crossovers were implemented in a resonator test chip to measure the effect of crossovers on RF properties of the resonators. The crossovers were shown to have no negative effect on a feedline, however no positive effect was measured in general transmission measurements. The resonance frequency (f_r) of resonators with implemented crossovers were decreased with approximately 1GHz, likely due to a capacitative coupling of crossover to resonator, increasing the overall capacitance of the resonator. The crossovers also had a marked effect on the internal and external quality factors ($Q_i,\ Q_i$) of the resonators, decreasing Q_i and increasing Q_e compared to resonators without crossovers. It was decided that crossovers could provide benefits when implemented on feedlines, but to avoid implementing them on resonators due to the negative effects.

Preface

This thesis represents my work conducted from 2020-2022 at the Center for Quantum Devices (Qdev) during my master's degree at the Niels Bohr Institute, University of Copenhagen.

I would like to thank my supervisor Charles M. Marcus for having me as a student for the last two years, and facilitating my work at Qdev. It has been a wonderful experience, I have worked in a fantastic lab with many fantastic researchers and students, and greatly appreciate it. I would like to thank the members of the Gatemon/cQED group that i have been a part of for this thesis: Anders Krinhøj, Oscar Erlandsson, Morten Kjaergaard, Jose Manuel Chavez-Garcia, Michaela Eichinger, Zhenhai Sun, Asbjørn Drachmann and Kian Gao. All of you have been welcoming and helpful, I am grateful for your assistance and company during my thesis. I would also like to thank Smitha Nair Themadath, Sangeeth Kallatt and Martin Bjergfelt for your help and input with fabrication and in the cleanroom, it was truly invaluable for my project.

I would also like to thank my family and friends for all your support, help and encouragements during my thesis. Lastly, i would also like to thank the limitless supply of great coffee in the Qdev lounge, much of this thesis would have been impossible without it.

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CHAPTER 1

Introduction

1.1 Quantum Computation

Quantum computation is an exciting and interesting frontier in physics, promising a myriad of real-world applications such as quantum information processing, quantum cryptography and quantum simulation[1]. The road to a fully realised quantum computer is filled with obstacles, the largest one being building a fault-tolerant and consistent quantum processor. A quantum processor is built on the quantum analog of the classical bit: the qubit. A qubit has to be made from a two-level system that can be put into a superposition of the two states, the 0 and the 1. Finding a suitable system to construct qubits is a huge field of research, in this thesis I focus on one particular proposal: the dotmon.

1.2 Superconducting Qubits

The focus of this thesis is the family of supercondunducting qubits, a promsing platform for for high-coherence scalable quantum computation[2][3]. This work explores a new addition to the family: The dotmon. To be able to describe the dotmon, we first have to understand the transmon. The transmon is, at the time of writing this thesis, being used in large quantum processors[4][5], at the frontier of quantum computing technology. We start with a close look at the transmon system

The transmon is a nickname for the "Transmission line shunted plasma oscillation qubit", first proposed by Koch et. al[6]. It is comprised of a superconducting island, coupled to a large shunt capacitor through a Josephson junction[7], that is then coupled to a transmission line through a superconducting resonator. The transmission line and superconducting resonator will be discussed in detail in a later chapter of this thesis (chapter 4), let us start by examining what defines the two-level system. It is useful to think of the system as an LC resonator circuit, with the capacitor being dominated by the large shunt capacitor, and the inductor being the Josephson junction. The system is described as a anharmonic quantum oscillator, with the anharmonicity being supplied by the non-linear element in the circuit: the Josephson junction, see Figure 1.1 from Krantz et. al[8]. A Josephson junction defined by a weak link between two superconducting electrodes/reservoirs. In the case of the transmon, the weak link is an insulating tunnel barrier separating the superconducting electrodes: a Super-Insulating-Super (SIS) junction.

Whilst much time can be spent discussing the details of the Josephson junction[9], I will only summarise a few important attributes here. A superconductor is a macroscopic quantum phase found in metals, hosting a dissipationless supercurrent when a voltage is applied on the metal. This dissipationless state is caused by electrons pairing up into cooper pairs, that form the superconducting condensate. The maximum current the superconducting phase can sustain before breaking down into a resistive state is called the critical current I_c. An amazing

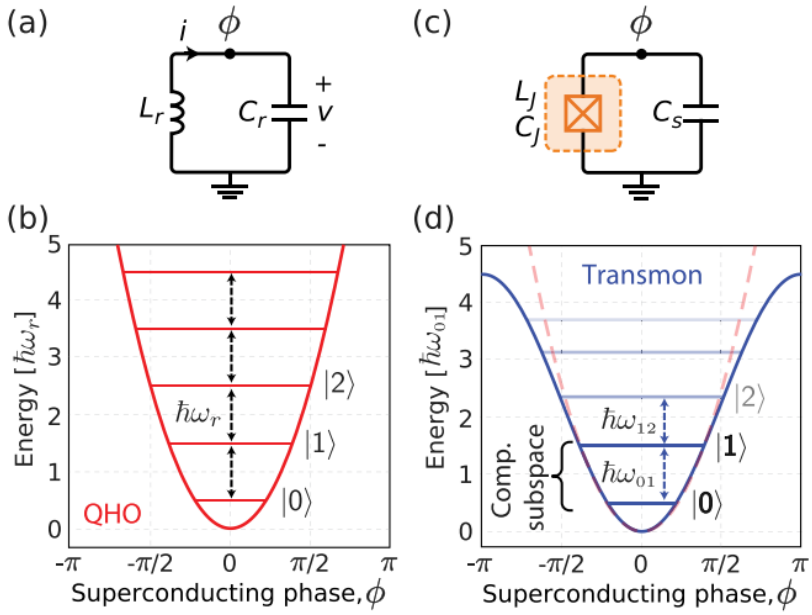

Figure 1.1: Figure from Krantz et al.[8] showing the energy spectrum of a harmonic quantum oscillator (b) and an anharmonic quantum oscillator (d), with their LC circuits shown in a) and b) respectively. The anharmonic oscillator is specifically modelled as a transmon, with a Josephson junction as the non-linear inductor. The junction has an associated inductance L_j and capacitance C_j. The Josephson junction is connected in parallel to a shunt capacitor, forming the transmon qubit.

property of the supercurrent is that it can run across a break in the conductor, a junction if you will, only picking up a phase in the current. This is exactly what happens in the Josephson junction, the current across a Josephson junction is as follows:

$$I_s = I_c \sin(\phi) \tag{1.1}$$

where $\phi = \phi_R - \phi_L$ is the difference in the quantum phase of the state on the right and left side of the junction. This is called the current-phase relation of the junction.

A remarkable fact of the transmon is its inherent resistance to charge noise. Since noise is the enemy of coherence[8], this feature is very desirable in a qubit. To show how the transmon is resitant to charge noise, let us start with the Hamiltonian of the system:

$$H = 4E_c(\hat{n} - \hat{n_g})^2 - E_j \cos(\hat{\phi}) \tag{1.2}$$

Here $E_c = \dfrac{e^2}{2C}$ is the charging energy of the shunt capacitor and $E_j = \dfrac{I_c\hbar}{2e}$ is the energy associated with the inductance of the Josephson junction. $\hat{n}$ is the cooper pair number operator, and $\hat{n_g}$ represents an offset charge on the qubit island. This Hamiltonian can be numerically solved, as was done by Koch. et. al, shown in figure 1.2. They discovered that a high ratio of E_j/E_c suppresses the charge dispersion of the system, shown by the flattening of the energy bands in figure 1.2.

However, there is a clear trade-off from increasing the E_j/E_c ratio: the anharmonicity suffers. We are in luck however, the charge dispersion flattens exponentially with increasing E_j/E_c, whilst the anharmonicity only falls off algebraically. This means that we can find a sweet spot where the anharmonicity is large enough for qubit operations, and the charge dispersion small enough to protect from charge noise.

Nevertheless, a couple of downsides are present in the transmon system: the transmon requires large shunt capacitors to achieve the large ratio of E_j/E_c, limiting the numbers of

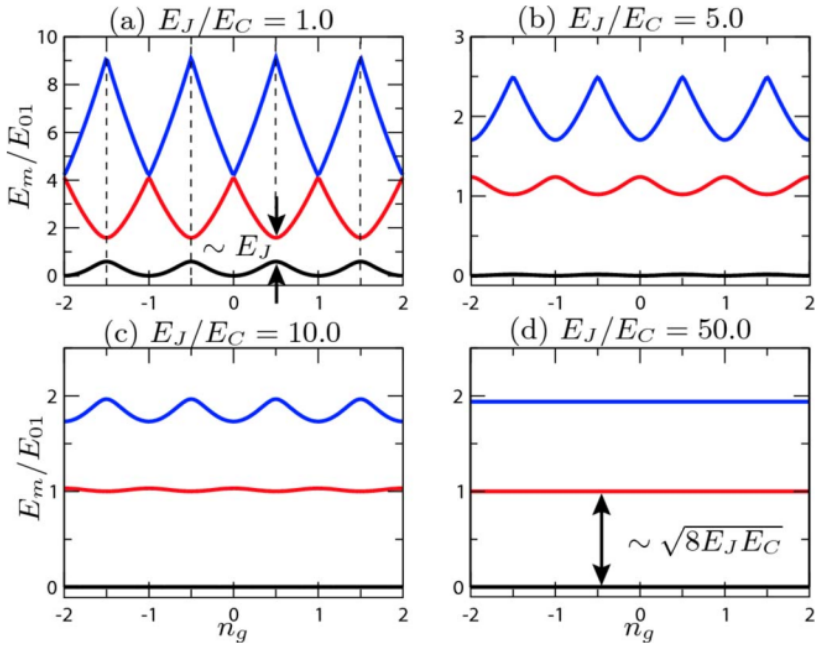

Figure 1.2: Energy spectrum of the Cooper pair box / transmon as a function of offset charge, for different values of E_j/E_c, from Koch et. al[6]

qubits on a chip. A single transmon is also fixed-frequency, meaning that there is no way to tune the frequency of the qubit without embedding the transmon in a Superconducting Quantum Interference Device (SQUID) configuration, or using troublesome flux bias lines.

1.3 The Gatemon

The counter to some of these issues come in the form of a new kind of qubit: the gatemon. It is a gate tunable transmon, achieved by replacing the insulating element in the Josephson junction with a semiconductor. This results in a Super-Semiconductor-Super(S-Sm-S) junction, where the charge carrier density of the semiconductor can be tuned by a field-effect transistor style electrostatic gate.

Another remarkable effect of the superconductor manifests itself in the S-Sm-S system, namely the proximity effect. When a semiconductor or normal metal is in contact with a superconductor, the superconducting cooper pairs leak into the semiconductor, effectively turning the semiconductor superconducting[9]. This allows the semiconductor to form a Josephson junction, however the CPR is slightly different from the sinusoidal CPR of the insulating junction[10]. It was discovered that the electrostatic gate could tune the critical current of the junction, thereby changing E_j. From Koch et. al. the transition energy can be approximated to $E_{01} = \sqrt{8E_jE_c}$, thus we can change the qubit frequency $\omega_q = E_{01}/\hbar$ with the electrostatic gate.

Cooper pairs are transported through the semiconducting region of the S-Sm-S system by a process known as Andreev reflection[11]. If the junction length is much smaller the the coherence length of the Cooper pairs, the junction will host Andreev bound states that can be thought of as carrying the supercurrent across the junction. We can adopt a Landau-Buttinger formalism for the transmission across the junction, with multiple Andreev transmission channels with an associated transmission T_i carrying the supercurrent. The Andreev bound state energies are given by[9]:

$$E_A = \pm\Delta\sqrt{1 - T_i \sin^2(\hat{\phi}/2)} \tag{1.3}$$

with Δ being the superconducting gap, and T_i being the individual transmission probability of the mode. Summing over all modes gets us the Josephson potential:

$$V(\hat{\phi}) = -\Delta\sum_i \sqrt{1 - T_i \sin^2(\hat{\phi}/2)} \tag{1.4}$$

The general Hamiltonian of the system is given by

$$H = 4E_c\hat{n}^2 + V(\hat{\phi}) \tag{1.5}$$

The transmon can be though of as a specific case of this general equation, with many channels with low transmission. A gatemon usually operates with a few channels of high transmission[10]. Gatemons have been realised using both Vapour-Liquid-Soild(VLS) nanowires[12], [13], two-dimensional Electron Gas (2DEG) heterostructures[14] and van der Waals graphene heterostructures[15].

1.4 The Dotmon

During nanowire gatemon experiments at the Center for Quantum device by Anders Kringhøj[16] [10], it was discovered that an accidental quantum dot in the semiconducting Josephson junction had remarkable effects on the charge dispersion of the gatemon[16]. A similar experiment has taken place in Delft[17]. Accidental quantum dots in a junction is a common occurrence near depletion, when the electrostatic gate has depleted most of the charge carries in the semiconductor. It was discovered that the quantum dot created a mode with transmission of unity, resulting in a flat charge dispersion. This can be seen in figure 1.3, from Kringhøj et. al.[16] The quantum dot is modeled as a resonant level with energy ε_r with tunneling rates Γ_1 and Γ_2 on and off the dot. The experiment is discussed in great detail in the PhD dissertation of Anders Kringhøj[10]

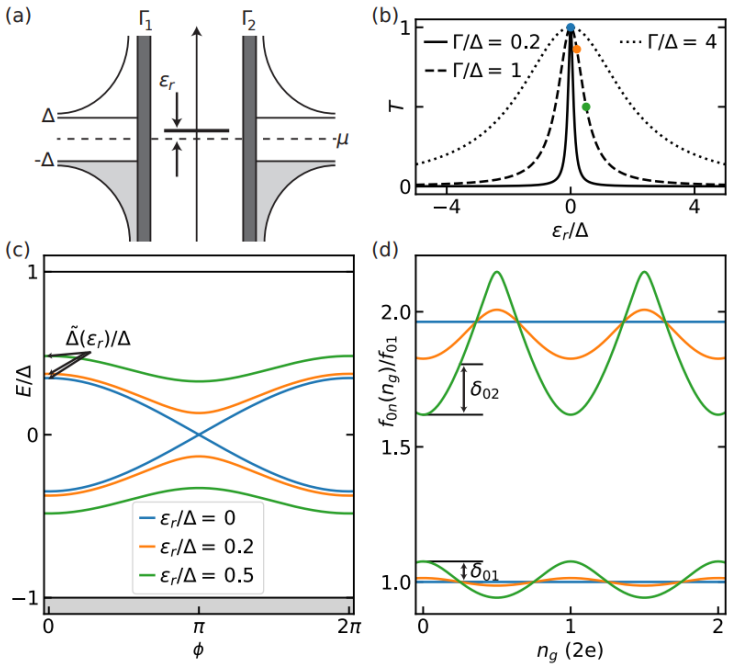

Figure 1.3: Figure from Kringhøj et. al.[16] showing the effect of a resonant level in the Josephson junction of a gatemon. The blue line shows the flat charge dispersion in d).

This experiment motivated the work of this thesis. The idea is to make the accidental dot in the gatemon purposeful and tunable, whilst changing the materials platform from a VLS nanowire to a 2DEG. This new qubit is nicknamed "The Dotmon". We hope to be able to tune the energy of the resonant level by a plunger gate, and the tunnel barriers with two pincer style quantum points contacts. Details on the design of the dotmon can be found in chapter 5.

CHAPTER 2

Fabrication and Measurement Setup

2.1 The Two-Dimensional Electron gas (2DEG)

A two-dimensional electron gas (2DEG) is used as the materials platform for our qubit devices. The 2DEG is formed by band gap engineering a layered heterostructure of III-V semiconductor materials, creating a quantum well in a designated area of the stack. Electrons are confined to move in the plane of this layer, which forms the 2DEG. Our system uses an InGaAs - InAs-InGaAs quantum well, where the quantum well lies in the InAs layer. Superconducting aluminium grown in-situ on the top of the 2DEG creates a highly transparent interface between the 2DEG and superconductor, creating a proximitised superconducting 2DEG[18]. The 2DEG stack is grown on an InP substrate, and a carefully engineered buffer layer separates the quantum well from the substrate. The wafer stack is shown in figure 2.1. The figure shows the whole wafer stack, as well as Schrodinger-Poisson simulations of the band gaps of the different materials, showing where probability density of the wavefunction of the electrons. An optical image of the wafer is also shown (supplied by the wafer growers).

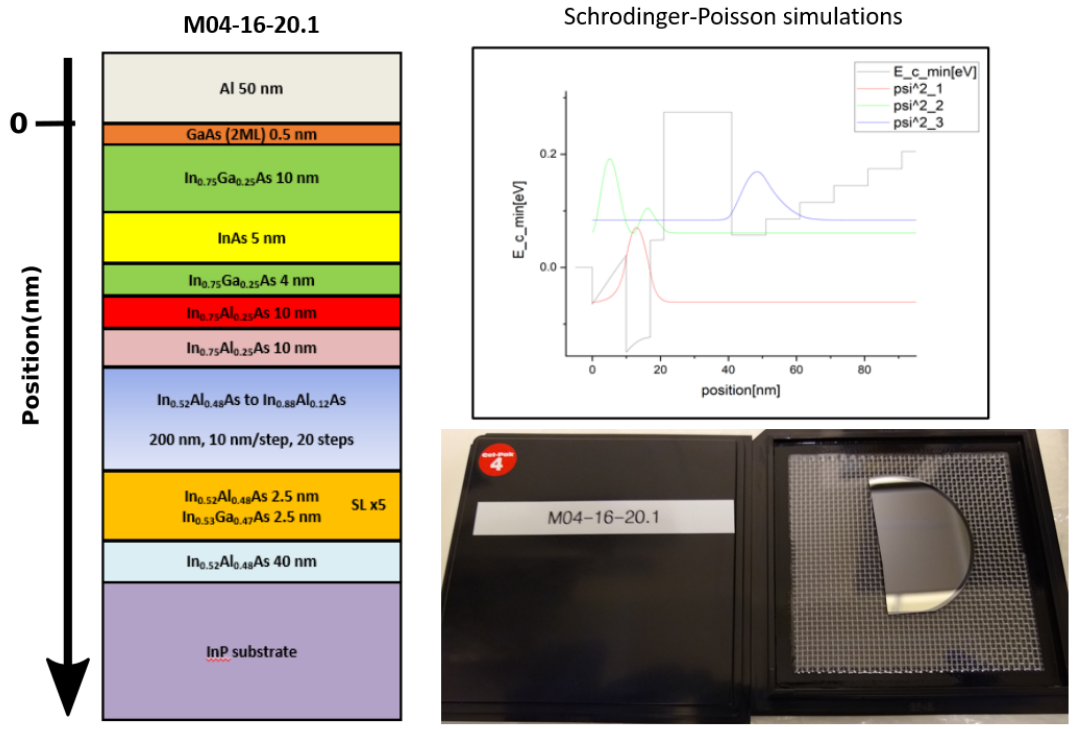

Figure 2.1: Illustration of the 2DEG wafer stack of M04-16-20.1. Schrodinger Poisson simulations are also shown, showing the probability density (wavefunction squared) of the electrons in the struture. The first harmonic is shown to lie in the InAs quantum well, as expected. An optical image of the wafer is also shown, inside a carrier box.

The 2DEG platform allows for streamlined fabrication of complex mesoscopic devices, making it an ideal platform for combining a gatemon with a tunable quantum dot.

2.2 Electron Beam Lithography

Electron Beam Lithography (EBL) is the primary fabrication method used in this thesis. EBL uses a concentrated beam of electrons to precisely pattern out nanoscale designs on a given material platform, in our case a III-V 2DEG heterostructure. The basic principle/workflow employed in this thesis is as follows:

- Design and prepare exposure files using CAD software and Exposure software
- Spin resist on sample
- Expose design using E-beam lithography system
- Develop exposed regions using MIBK:IPA(1:3)
- Perform desired operation (Chemical Wet Etch / Metal Evaporation / dielectric Atomic Layer Deposition (ALD))

This method can create a plethora of interesting devices and structures, including the dot-mon qubits, resonators and crossovers featured in this thesis. The specific recipes used for this thesis can be found in appendix A. These recipes have been developed on the foundation of former recipes used for device fabrication at the Center for Quantum Devices, with assistance from dedicated fabrication experts. EBL is a reproducible and accurate method of creating nanoscale devices, but it can be an arduous task to develop and perfect fabrication recipes. Much of the time spent on this thesis was spent on modifying and performing fabrication workflows for this exact experiment.

2.2.1 Wet Etching

A wet etch is a process where the sample is submerged in an etching liquid solution, then dried and cleaned. The semiconducting 2DEG Mesa and the superconducting aluminium forming the qubit island and Josephson junction is defined by two wet etch processes.

- The mesa etch forms a semiconducting region with a top layer of 50nm of epitaxial aluminium remaining to form the qubit island and Josephson junction. The mesa etch process requires first an aluminium etch to etch away unwanted epitaxial aluminium, before the main mesa etch. The aluminum etch uses transene type D, an agressive etchant that ethces through the 50nm of aluminum in roughly 10 seconds. The mesa etch uses a solution of water, citric acid, autophosphoric acid, and hydrogen peroxide to etch through the 2DEG heterostructure (see A.2 for details). The etch is quite controllable, etching through the 360-400nm 2DEG heterostructure (and slightly into the InP substrate) in 10 minutes.
- The junction etch forms the Josephson junction, and thereby also the two superconducting islands that end up defining the transmon qubit. It uses the same etchant, transene D , and etch time as the aluminium etch for the mesa etch, but requires a new lithographic mask.

2.2.2 Metal Evaporation

Metal evaporation is a reliable method to deposit nanometer scale thin films of metals on a sample. A substantial part of the final qubit chip is defined using a metal evaporation procedure. The ground plane of the chip, the superconducting transmission line, the superconducting resonators and the electrostatic gates are all made of evaporated Aluminum. The specific machine used is an AJA international E-beam evaporation system. In the process, the chip is mounted on a sample holder that can be transferred between a vacuum lock and the evaporation chamber. In the evaporation chamber, multitple crucibles containing different metals are placed at the bottom. The sample is loaded in the middle of the chamber, and rotated to face the metal crucibles. It is also possible to place the sample holder at an angle, and rotate the sample holder around an axis normal to the chip. This is useful for "climbing" large structures, for example climbing the 2DEG mesa with a gate. An electron beam is then directed at the crucible, heating the metal to the point of atoms escaping the surface. These atoms then fly up and cover the sample holder, as well as the chip, to form the metal film. A specific acceleration current is chosen for the ebeam, which supplies a specific heat to the crucible. This translates into a stable deposition rate, usually around 1 Ångstrom per second.

For the control layer of the qubit (transmission line, resonator and shunt capacitor) we use 100nm of evaporated aluminum. The inner electrostatic gates are made with 5nm of evaporated Ti (a sticking layer) and 45nm of evaporated aluminium. The outer electrostatic gates and superconducting contacts are made with 10nm evaporated Ti and 400nm evaporated Al. The superconducting contacts are used to connect different parts of the chip, formed by aluminium, i.e. the inner and outer electrostatic gates, or the ground plane across a transmission line. Aluminium forms a native oxide, we therefore requires a Kaufmann milling step to remove the oxide, before depositing the electrical contacts. Kaufmann milling uses ionised Argon atoms to remove thin layers of surface material from a sample.

2.2.3 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is an advanced method used to create atomic layer scale thin films on a sample. ALD is used as to create an insulating dielectric for multiple parts of the qubit chip. Most importantly, the dielectric layer separates the electrostatic gates from the superconducting aluminium that forms the qubit and control layer, and the semiconducting Josehpson junction. Atomic layer deposition uses multiple precursor materials, mixed as gas in a vacuum chamber at a specific temperature (80C in our case). The gasses interact with each other, forming a dielectric layer on the sample surface. The specific machine used for this project was a Cambridge ALD machine, capable of creating AlO2 and HfO2 films. For this device, we used 15nm HfO2 as the dielectric layer for both the electrostatic gates and the on-chip crossovers. A liftoff process was then employed to remove the globally deposited HfO2 from most of the chip, the HfO2 then only remains in the lithographically patterned areas.

2.3 Dilution Fridges and Electrical measurement setup

2.3.1 cQED Setup

All cQED and transport experiments presented in this thesis was carried out using a Oxford Instruments Triton cryo-free He3-He4 dilution cryostat, with an expansive measurement setup. Measurements of resonator and qubit devices are performed at the base temperature of the fridge: 50mK-70mK. A full schematic of the electrical measurement setup for cQED measurements is shown in figure 2.2, and a full schematic of the transport measurement setup is shown in figure 2.3.

The setup shown in figure 2.2 allows for 2 different measurement setups depending on the RF switch configuration, one based on a Vector Network Analyzer (VNA), and one on an Alazar readout circuit:

1. **(VNA+qubit) drive + VNA readout:** The VNA both generates the microwave signals going to the sample, and measures the signal coming back from the sample. This setup is used for characterising the RF properties of the device, mostly the resonators. All RF switches set to 2

2. **(qubit+cavity) drive + Alazar readout:** Used for two-tone spectroscopy and time domain measurements, the AWG shapes the "cavity" signal and drives the qubit, the Alazar readout circuit mixes the signal with the "local oscillator" signal and demodulates the signal (Heterodyne measurement). All RF switches set to 1

The RF switch allows for fast and easy switching back and forth between configurations, making measurements quicker and negating possible failure modes from changing cables and other setup configuration.

Going through the setup with the signal: The signal start from either the VNA or the Cavity signal generator, and is immediately mixed with the Qubit signal (coming from the C port in the RF switch) in a "Mini-circuits ZX10R-14-S+ Splitter" for the VNA or a similar splitter for the cavity signal. This signal is then run to the A port of the switch, and sent to the fridge. Going down the fridge, the signal is heavily attenuated before reaching the mixing chamber stage and the sample. The signal is transmitted through the sample, and sent back up through the fridge. Here the signal first goes through two "Quinstar CWJ1019-K414 Quantum Isolator"s and then goes through the "LNF-LNC4-8C 4-8GHz cryogenic low noise amplifier" (4k cryoamp for short). The signal then exits the fridge, and goes through a "Mini circuits ZX60-83LN-S+" room temperature amplifier before going into the B port of the RF switch. Here the signal is either sent back to the VNA (if in config 1) or sent to the Alazar readout circuit (if in config 2). The alazar circuit consist of a Marki Mixer M8-0420MS (IQ Mixer) where the signal is mixed with the local oscillator signal. From there, the signal goes through another amplifier and out into the Alazar digitizer card, where the signal is demodulated.

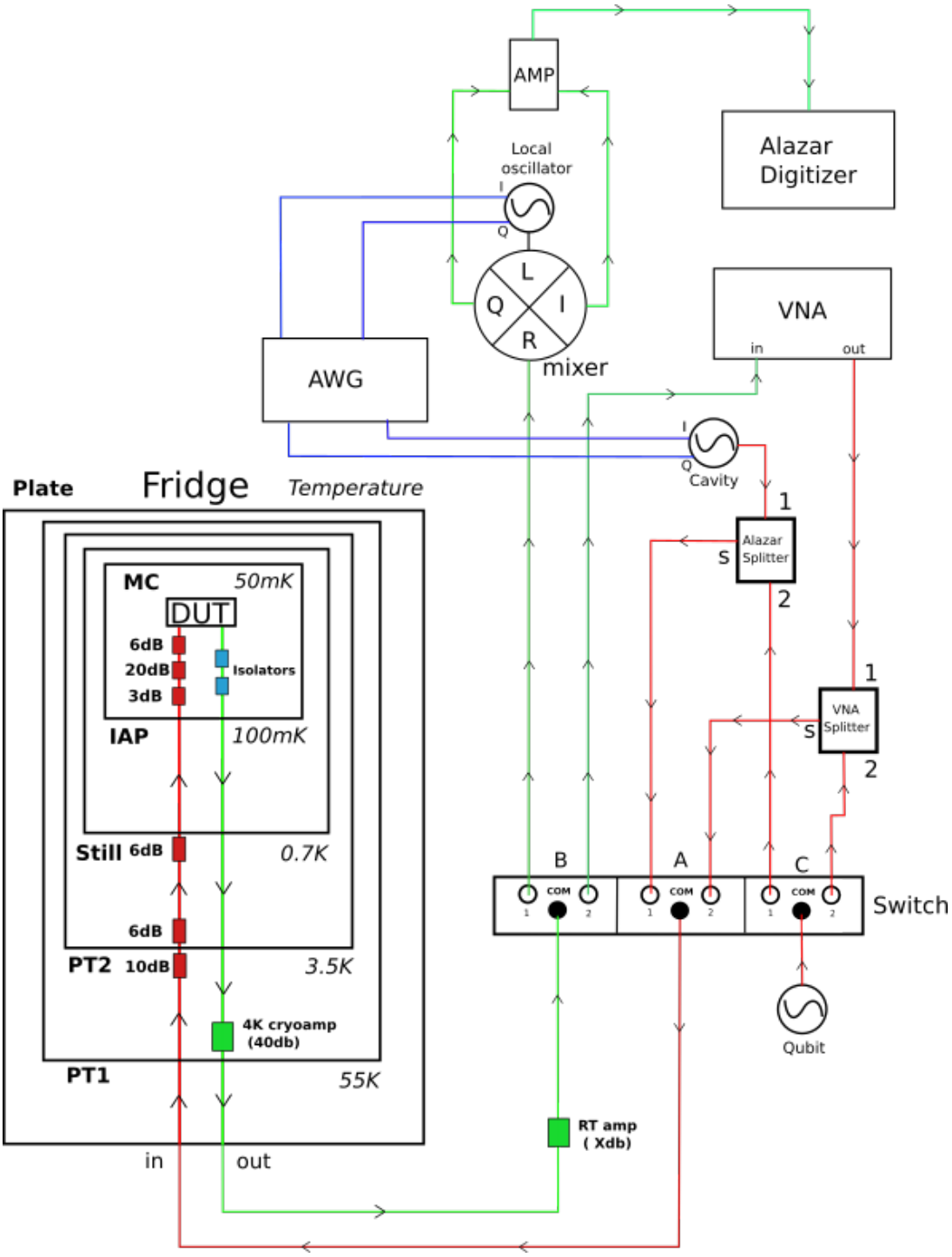

Figure 2.2: WIP - Illustration of the cQED measurement setup used for experiments in this thesis. All lines represent RF SMA cables, colours show if the signal is going to the sample, or coming from the sample. Red lines show the qubit drive cirquit, green lines show the qubit readout circuit. Blue lines represent the AWG circuit that shapes the waveforms of the signal generators. This setup allows for 2 seperate measurement configurations, controlled by the switch settings. One configuration is used for basic VNA charecterisation of the device (config 1), the other allows for two-tone spectroscopy and time domain measurements (config 2)

2.3.2 Transport Setup

The electrical setup used for measurement of transport through the qubit devices presented in this thesis is shown in figure 2.3. The design of the qubit device (see chapter 5) only allows for applying voltage or current through one terminal to the device, resulting in a slightly unusual measurement setup. The terminal connected to the device under test (DUT) is both used to apply a voltage excitation to the system, and also used to measure the current response. The DUT is connected to ground on one side, and the terminal on the other.

When performing transport measurement, we are used to thinking of either current biasing or voltage biasing the DUT. For this type of measurement, the definition is more blurry. The simplest definition of current and voltage bias is where the voltage is dropped in the system. If there is a large voltage drop across the DUT (and therefore a small current), we are voltage biasing. If most of the voltage is dropped elsewhere in the system (across a dedicated bias resistor, or in our case the line resistance), and there is a large current across the DUT, we are current biasing.

We make the simplification of saying that the voltage in our system is either dropped across our DUT, or elsewhere in the system associated with a line resistance $R_{Line} = 3.41k\Omega$. We measure the resistance across the device during measurement, and if the resistance across the device is smaller than the line resistance $dR < R_{line}$, we are in a pseudo current bias. If the resistance of the device is larger than the line resistance $d_R > R_{line}$ we are in a pseudo voltage bias. Our measurements will focus on monitoring the critical current of our device, which i would describe as a current bias. As of writing this thesis, tunneling spectroscopy in voltage bias has not been performed on the dotmon qubit devices.

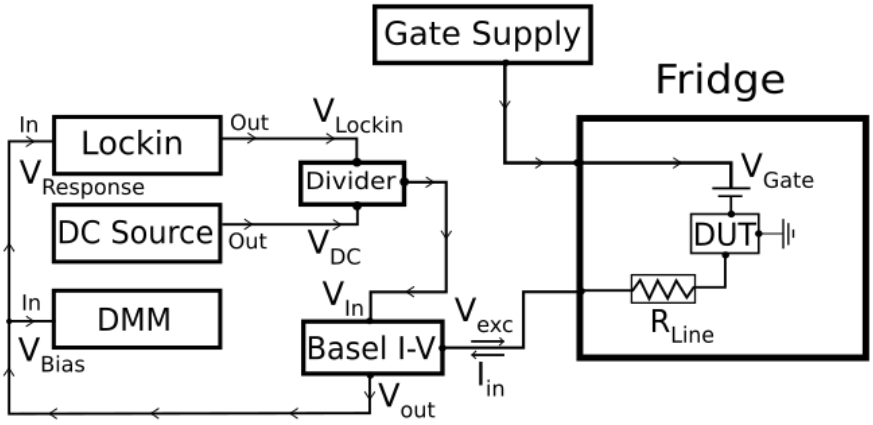

Figure 2.3: Illustration showing the transport measurement setup used for current bias measurements of the M15 Dotmon qubit. The qubit is represented by the Device Under Test (DUT), the setup is centered around the Basel I-V converter.

I will now describe how the measurement setup works. The measurement setup is centered around our "Physics Basel SP983c" I-V (current-to-voltage) converter (see image in figure 2.4, showing both the Basel and the voltage divider). The Basel unit can both apply a voltage excitation to the device, measure the current response and convert it to a voltage. It is important to convert it to a voltage, so the "Stanford Research SR830 DPS" lock-in amplifier can measure the signal. We start by applying a DC and AC voltage to the DUT. The lock-in amplifier

provides the AC excitation with a specific frequency and amplitude $V_{AC} = 0.1V$ (before division in divider), and a "Yokogawa GS200" DC source is used to provide the DC part of the signal V_{DC}. The AC and DC parts are combined in a voltage divider specifically designed to work with the Basel unit (see figure 2.4). The voltage divider reduces the AC signal with a factor $\beta_{AC} = 1e^{-5}$ and the DC signal with a factor $\beta_{DC} = 1e^{-3}$. The resulting signal V_{in} is fed into the "voltage in" port on the Basel, and the voltage excitation V_{exc} is applied to system. The voltage is then dropped both across the line resistance R_{line} and the DUT. The Basel then measures the current response I_{in} and converts it to a voltage V_{out}. The Basel amplifies the signal with a factor $\alpha_{basel} = 1e^{5}$ when converting from current to voltage. The voltage signal is then fed into a "Keithley 2400 SourceMeter" DMM to measure the resulting bias current V_bias, corresponding to the DC part of the signal, which can be converted back to a current I_{bias} using the conversion factor from the Basel α_{Basel}. The lock-in then measures the AC part of the voltage signal, corresponding to the differential current dI_{bias} when converted back into a current using α_{Basel}. We can then calculate the differential resistance using the following procedure:

$$I_{Bias} = \frac{V_{Bias}}{\alpha_{Basel}},\ dI_{bias} = \frac{V_{Response}}{\alpha_{Basel}} \tag{2.1}$$

$$dV_{Bias} = V_{Lockin} \cdot \beta_{AC} - R_{line} \cdot dI_{bias} \tag{2.2}$$

$$dR = \frac{dV_{bias}}{dI_{bias}} \tag{2.3}$$

We can also apply a voltage V_{Gate} to the electrostatic gates coupled capacitively to the DUT (specifically the Josephson junction) by using a DC voltage supply (for single gates a Keithely voltage supply, for multiple gates we use a DeCaDaC).

Measuring the differential resistance of our device is critical to observe the dot resonances we are hoping to create. See chapter 5 for detail on the qubit devices.

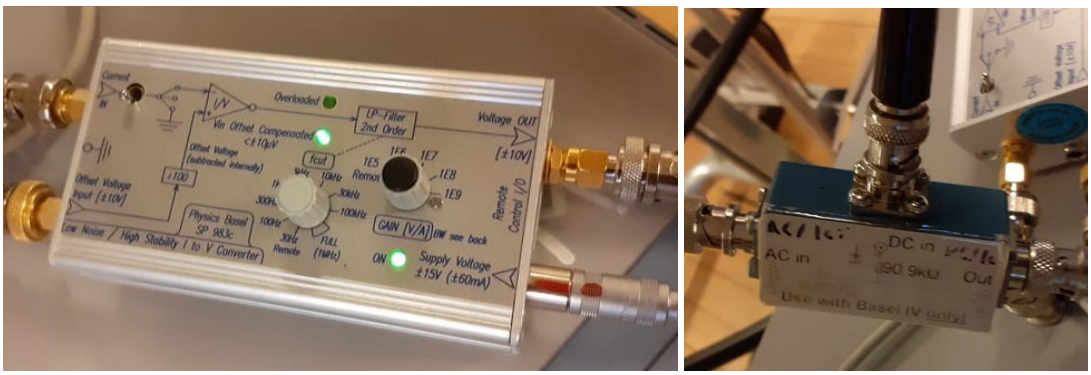

Figure 2.4: Image of the Basel I-V converter and the associated voltage divider. The input and output ports of both devices are shown, the Basel gain α_{Basel} is variable and set to $1e^{5}$ for our measurements. The voltage divider has a $9k\Omega$ resistor connected to the DC port, and a $9M\Omega$ resistor connected to the AC port. This results in an attenuation of $\beta_{DC} = 1e^{-3}$ and $\beta_{AC} = 1e^{-5}$, when connected to the Basel unit. The voltage divider is specifically designed to work with the Basel unit.

CHAPTER 3

Crossover Devices

3.1 DC Crossover Characterisation

An important part of a superconducting qubit chip is a well defined groundplane[19]. The qubit is essentially defined by the electric field of the chip, most notably around the superconducting island. If the ground plane is not properly defined, stray charge can build up on unintended islands on the chip, and stray currents might run over parts of the chip. This leads to parasitic modes that couple to the qubit-resonator system, acting as a loss channel. This ultimately affect the noise in microwave measurements and characterisation, and can also result in troublesome on-chip resonances creating a problematic background signal.

A specific example of this is found when using a transmission line for qubit control, a coplanar waveguide defined by a thin piece of superconducting aluminium in our case. As mentioned earlier in section 2.2, we define the control circuitry of the qubit chip by etching and/or depositing aluminium, depending on the specific fabrication step. A transmission line ideally goes from one edge of the chip to another, to allow easier access for bonding to designated bond pads at the end of the transmission line. The transmission line is formed by making trenches in the aluminium, separating the line from the groundplane. This often results in two ground planes being formed, one on each side of the transmission line, effectively splitting the intended groundplane in the middle. The two new ground planes are often connected at some point on the chip, usually near the edges, but this is not enough to keep both planes grounded. It is a simple case of needing more current paths: if a stray electron (or cooper pair) near the line wants to travel to ground, it needs a good infrastructure.

The first measure to remedy this issue is to make an electrical connection from the ground plane edges, to a well defined ground outside the chip. The chip is situated in a trench on a daughterboard for measurements, see figure 3.1, allowing electrical connections to gradually increase in size from a very small wirebond, to a small metal strip on the daughterboard, to an SMP cable, an SMA cable and finally a BNC cable. The daughterboards are designed with large metal pads near the chip trench, allowing for ground plane bonds to the chip. A lot of bonds are usually placed on the edge of the chip to the daughterboard, as many as the geometry allows. This helps to define the ground plane near the ground plane edge, but how do we make sure that the potential is uniform and zero near the middle of the chip, or near chip-carving features such as resonators, transmission lines and test structures?

A common solution is crossovers, also called jumpers or air-bridges in other literature. They are small structures, reminiscent of pedestrian highway bridges, that climbs over chip-carving features such as transmission lines and resonators. The crossovers connect the ground planes on either side of the chip-carving features, ensuring the formation of a singular well-defined groundplane on the chip. A crossover is constructed using a dielectric layer underneath a conductor. The dielectric layer separates the conductor of the crossover from the features

beneath it, ideally making sure that the groundplane does not short to the features.

My crossovers are made with two different layers of dielectric and 400nm thick evaporated aluminium as the conductor. The first layer of dielectric is a 15nm layer of ALD defined HfO2, the second is a layer of crosslinked PMMA resist. The PMMA resist is the same as used for the lithographic e-beam steps, but rendered chemically inert by exposing it with a ultra-high e-beam dose. This layer is mostly used to create a large separation between the conductor and the feature beneath. These fabrication steps use the same parameters as other parts of a full qubit chip (except the crosslinked resist), and is easy to implement in the qubit fabrication process flow. An important Kafumann milling step is required before depositing the aluminium for the crossovers, to remove the native oxide of the aluminium.

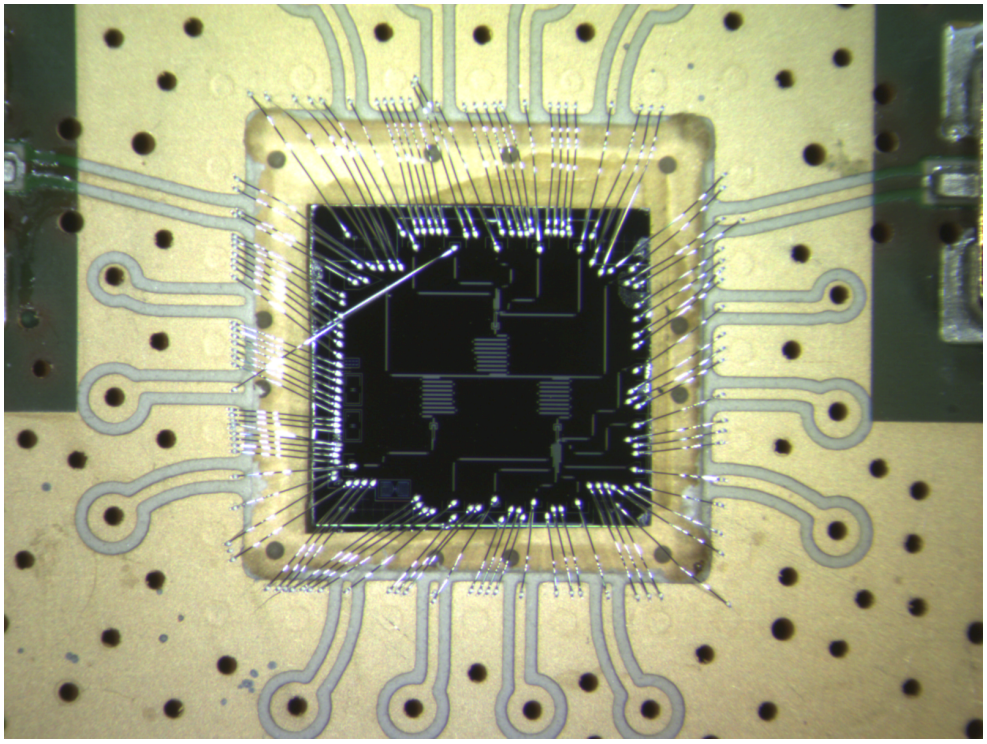

Figure 3.1: Optical image of qubit chip, described in detail in chapter 5, in a daughterboard trench immediately after bonding. The chip is 5mm by 4.6mm to give a sense of scale. The lines carved in the gold of the daughterboard are bonded to the bondpads on the chip, connecting to feedlines and gates. The rest of the bonds are groundplane edge-bonds going from the large ground on the motherboard to the groundplane on the qubit chip. The features visible on the chip are the feedline, the three qubit resonators, the gate lines, two test structures and the large qubit capacitors (if you look closely)

3.2 InP-H3 Crossovers

3.2.1 Design

The crossover test chip was made with a binary question in mind: does crossovers provide a connection between two aluminium islands, across an aluminium transmission line? There are two possible answers, either they do, or they do not. Two types of devices were designed: one to test a single crossover, and one to test five crossovers in series. The multiple-crossover device was created to get qualitative information on the yield of the process. The chip also included test structures, comprised of two aluminium islands shaped as the crossover bond-

pads, shorted with a small connecting segment. The chip also included two different kinds of crossovers: thin crossovers and wide crossover (see specific dimensions below). The thin crossovers were ones previously tested (locally), and determined not to work, and the wide ones provided a possibly more stable crossover.

Figure 3.2 shows the mock control layer created by depositing 100nm of aluminium, with the same geometric and e-beam parameters used in the qubit control layer. Large aluminium bondpads are usually used for wirebonding from a daughterboard to the chip, here they will be used for touching down with a thin needle probe in a DC probe station. The top and bottom bondpads are meant to mimick the ground plane of the qubit chip, they are separated by a distance of 5μm from the mock transmission line. The mock transmisison line is defined by a 10μm wire, connected to a bondpad in one end. The mock transmission line is connected to a bondpad to allow measurements of the leakage from the ground plane to the transmission line (not to test RF properties, another chip was made for this purpose, see section 4.4.

Figure 3.3 shows the two device variants on the chip. The simplest device (to the right), named α, has two bondpads forming the mock ground plane ($\alpha_{Ground,1}$, $\alpha_{Ground,2}$), and a single mock transmission line (α_{line}). One crossover connects $\alpha_{Ground,1}$ and $\alpha_{Ground,2}$. By applying a voltage V_{probe} between $\alpha_{Ground,1}$ and $\alpha_{Ground,2}$, and measuring the current $I_{Response}$, making us able to calculate the resistance of the current path R_{cross}. This resistance tells us if the current is flowing through the crossover metal, or somewhere else. It is possible for the current to flow through the substrate, which would show a high resistance. We expect a low resistance through the aluminium film. To measure the leakage from the crossover to the transmission line, we apply a voltage between $\alpha_{Ground,1}$ and $\alpha_{Ground,2}$, and measure the current from $\alpha_{Ground,1}$ to α_{line}. We then calculate the resistance R_{leak}, which tells us if a significant amount of current is leaking to the transmission line.

The more complicated device (to the left), device β, has a mock ground plane defined by $\beta_{Ground,1}$, $\beta_{Ground,2}$, and five transmission lines between them, $\beta_{Line,1}$, $\beta_{Line,2}$, $\beta_{Line,3}$, $\beta_{Line,4}$, $\beta_{Line,5}$. Between each line, a small Al island is located. 5 crossovers in series then connects $\beta_{Ground,1}$, $\beta_{Ground,2}$, crossing over the transmission lines to an aluminium island. This device allows us to test the yield of the crossover design, and give a qualitative picture of how well they function in series. The measurement is the same as device α, but the leakage measurement is iterated 5 times, one for each line.

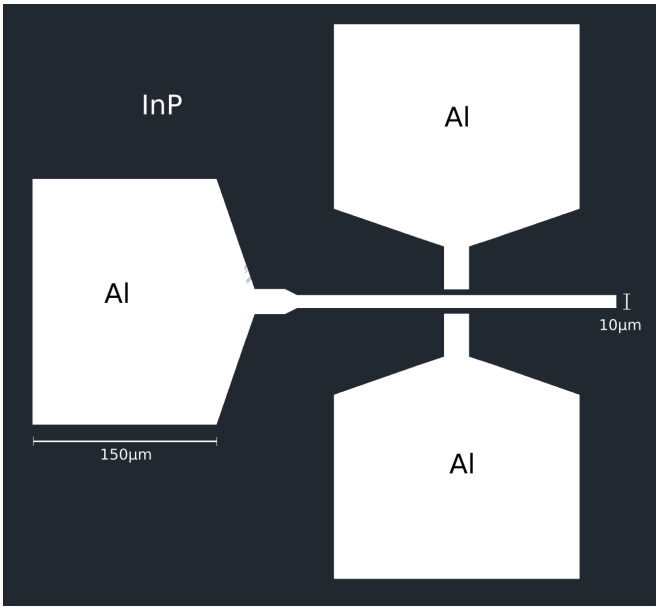

Figure 3.2: Illustration of crossover device design, without the crossover. Grey is the InP substrate, white is the deposited 100nm Al forming the mock control layer

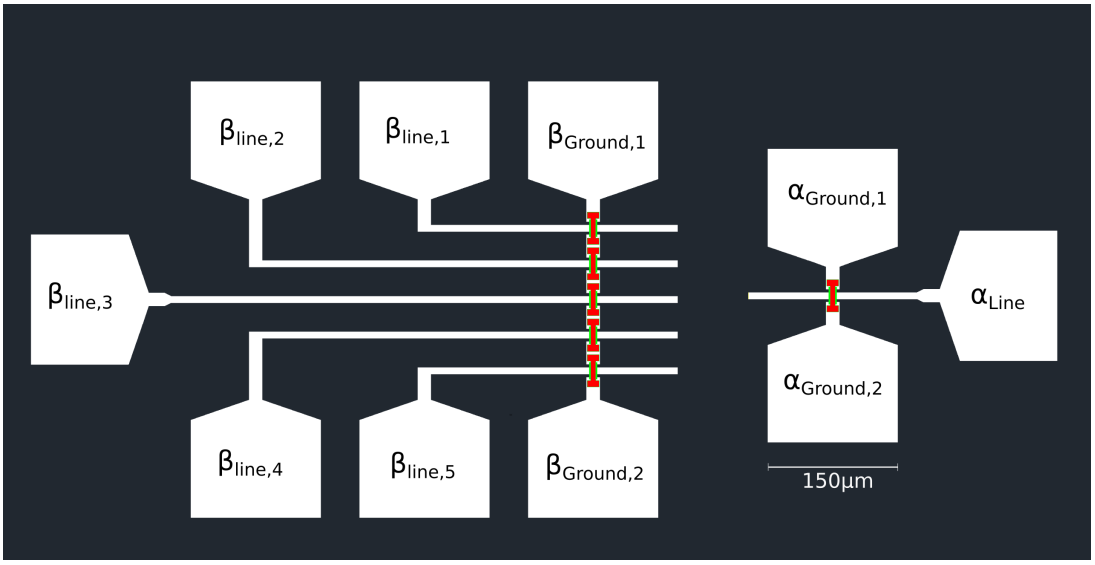

Figure 3.3: Illustration of crossover device design variants, with crossovers . Grey is the InP substrate, white is the deposited 100nm Al forming the mock control layer, red is the deposited 400nm Al contacts forming the crossover, green is the ALD and crosslinked resist forming the dielectric layer that seperates the crossovers from the control layer. Devices "α" and "β" are shown, with their bondpads labled by their function.

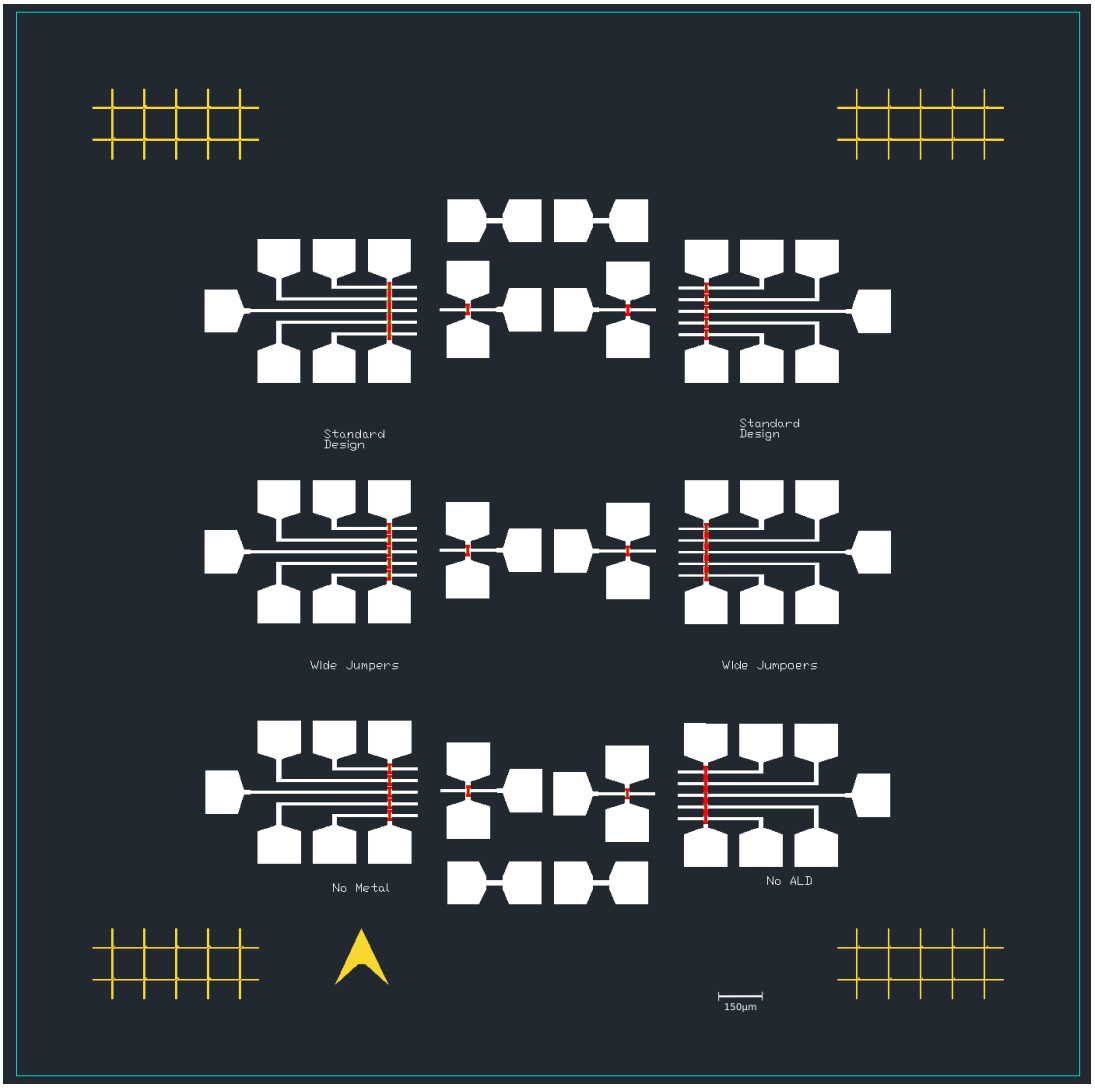

Figure 3.4: Illustration showing the entire crossover test chip design. The chip edge is shown with a blue line, the chip is 5x5mm. The yellow is gold alignment marks for E-beam lithography, and an orientation arrow. The variations on each device are written below it, including devices with regular crossovers, devices with wide crossovers, devices with no ALD and device without the crossovers (only dielectric layer). The Devices are mirrored in the middle, yielding pairs of the same device variations.

3.2.2 Fabrication

The crossover devices were fabricated on an InP wafer, matching the subrate in the qubit 2DEG wafers. The sample name is InP-H3-CrossoverTest. The fabrication steps were as follow:

1. *Scribe:* Scribe and Cleave InP wafer into 5x5mm chips (executed by process engineer on Autoscriber)
2. *Alignment Marks:* Spin PMMA A4 resist and E-beam expose alignment marks, develop with MIBK:IPA 1:3, ash with oxygen plasma
3. *Aligment Marks:* Evaporate 10nm Ti sticking layer, Evaporate 40nm Au layer, liftoff unwanted metal
4. *Control Layer:* Spin Bilayer EL9 and PMMA A4 resist, E-beam expose control layer, develop with MIBK:IPA 1:3, ash with oxygen plasma
5. *Control Layer:* Evaporate 100nm Al, liftoff unwanted metal
6. *ALD:* Spin PMMA A4 resist and E-beam expose ALD area, develop with MIBK:IPA 1:3, ash with oxygen plasma
7. *ALD:* Use ALD to grow 15nm HfO2, liftoff unwanted HfO2
8. *Crosslinked Resist:* Spin PMMA A4 resist and E-beam expose crosslinked resist (high E-beam dose), strip unwanted resist with acetone
9. *Crossovers:* Spin trilayer EL9 + EL9 + PMMA A4 resist and E-beam expose crossovers, develop with MIBK:IPA 1:3, ash with oxygen plasma
10. *Crossovers:* Kaufmann mill with Ar ions in AJA metal evaporator, removing native Al oxide on control layer for contacting crossovers
11. *Crossovers:* Evaporate 5nm Ti sticking layer, 50rpm stage rotation. Evaporate 50nm Al, 5deg stage tilt, 50rpm rotation. Evaporate 300nm Al, 0 deg tilt, 50 rpm rotation. Evaporate 50nm Al, 10deg tilt, 50rpm rotation.
12. *Crossovers:* liftoff unwanted crossover Al.

Detailed fabrication information can be found in the appendix A.1.

3.2.3 Fabrication Images

This section shows optical images of the final devices on InP-H3-CrossoverTest, (figure 3.5, 3.6 left) and a Scanning Electron Micrograph (SEM) of the crossovers (figure 3.6 right)

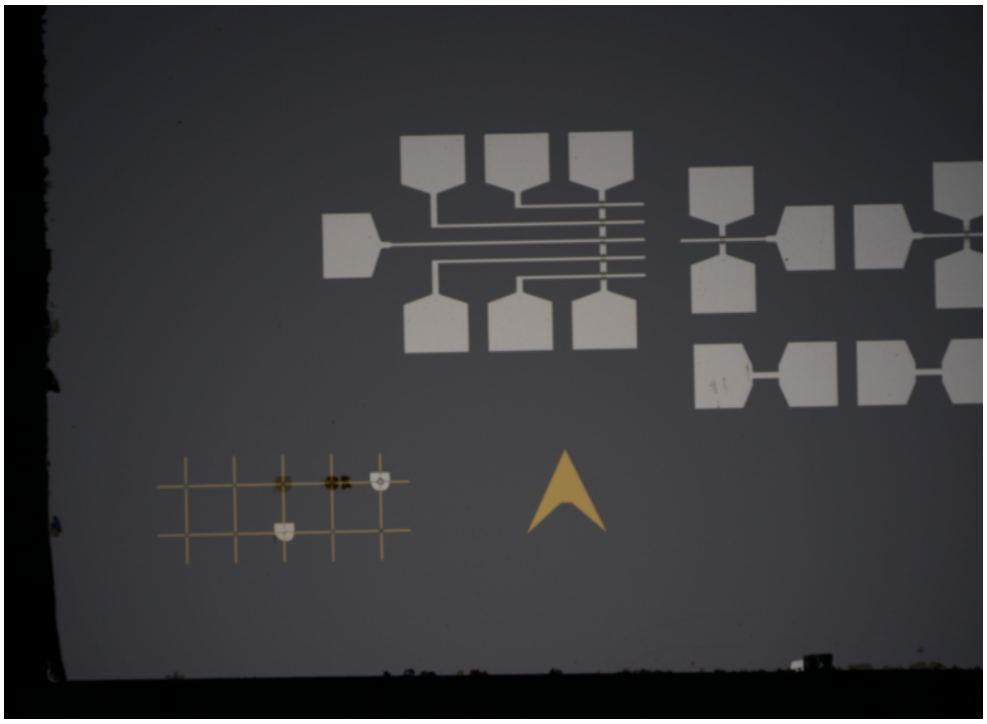

Figure 3.5: Optical image taken in the lower left corner of the finalized crossover chip. The grey is the InP subrate, the white is the control layer aluminium, the gold is alignment marks and an orientation arrow; made of gold.

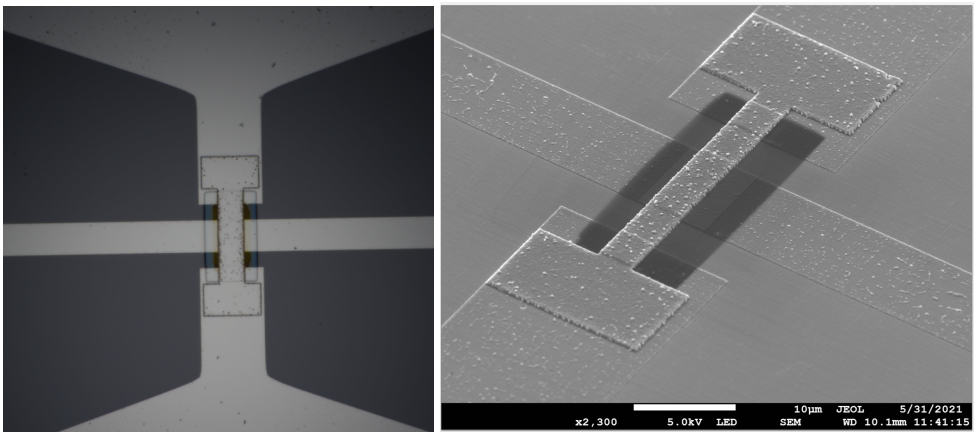

Figure 3.6: Left: Optical image of a wide crossover after fabrication. The crossover is situated in an α device. The brown part below the crossover is the ALD HfO2, the opaque film is crosslinked resist. Right: Scanning electron micrograph of a crossover on an α device. The crossover shown is the "regular" variant, not the "wide" variant shown in the optical images. The shaded part of the image is the crosslinked resist, the opaque layer beneath is the ALD HfO2. It is also clear to see the height difference betwen the 100nm control layer Al and the 400nm crossover Al.

Detailed fabrication images for each fabrication step can be found in the appendix

3.2.4 Measurements

This section shows the measurements of the test structures, device α and device β, in all their variations. The resistance of the devices was measured using an LCR-meter. The variations are as follow: "Test" devices, two bondpads connected by an aluminium bridge, used for resistance reference for other measurements. "Standard" devices, referring to the crossover and dielectric layer width (4 microns wide crossovers, 6 microns wide dielectric layer). "Wide" devices, referring again to crossover width, they are twice as wide as standard crossovers (8 microns wide crossovers, 10 microns wide dielectric layer). "No ALD" Devices, devices without the ALD HfO2 layer. "No Crossover", devices with only the dielectric layer.

We expect a low resistance on test devices, and a low resistance through all crossovers. The measurements for device α are shown in table 3.1, measurements for device β are shown in table 3.2. The resistance between unconnected Al pads on the chip was also measured: Between pads close together on the chip, the resistance was $300k\Omega$, between pads far away from each other it was $750k\Omega$. This is most likely the current finding a path through the InP substrate, resulting in a length-dependent resistance. Resistance was measured using a "keysight E4980A precision LCR meter", with an AC bias of 8V with a frequency of 1kHz.

Device α	Test	Standard	Wide	No ALD	No Crossover
α_{ground}	2.8Ω	2.3Ω	2.5Ω	No data	161kΩ
$\alpha_{ground,line}$		30kΩ,30kΩ	200kΩ	No Data	100kΩ

Table 3.1: Device α resitance measurements

Device β	Standard	Wide	No ALD	No Crossover
β_{ground}	6.0Ω	4.6Ω	6.2Ω	750kΩ
$\beta_{ground,line1}$	76kΩ	723kΩ	62kΩ	No Data
$\beta_{ground,line2}$	144kΩ	723kΩ	62kΩ	No Data
$\beta_{ground,line3}$	75kΩ	960kΩ	62kΩ	No Data
$\beta_{ground,line4}$	75kΩ	725kΩ	No Data	No Data
$\beta_{ground,line5}$	75kΩ	723kΩ	No Data	No Data

Table 3.2: Device β Resistance measurements

First, this clearly shows that the crossovers work: it is possible to connect the ground plane across a feedline using this design and recipe, and have a minimal leakage current.

This also shows that the wide crossovers perform better than standard. Their ground-ground resistance is roughly the same, but the leakage resistance is far greater with wide crossovers. We also clearly see that ALD drastically reduces the leakage resistance. This would suggest that the best type of crossovers are the wide ones, which have been implemented into further resonator tests, see section 4.4

CHAPTER 4

Resonator Devices

4.1 Resonator Quality Factor and Transmission Line Coupling

When designing superconducting Coplanar Waveguide (CPW) resonators for qubit purposes, it is important to have an understanding of the resonator and feedline system, and how it relates to measuring the qubits. I will spend some time going into detail on how we interpret the read-out data of a resonator, with a focus on the resonator quality factor. Let us start with a practical approach: How do we expect a resonator to show up in a transmission measurement, using a Vector Network Analzyer(VNA). The VNA measures the S-matrix of the system. Since we are interested in the transmission from the in to the out of the feedline, we focus on the S_{21} element of the S-matrix. This simply means that we compare the signals going from port 1 to port 2, corresponding to the feedline in and out respectively.

The S21 signal will be complex, following a Lorentzian model, which can be visualised either as the real and imaginary components of the signal, or the magnitude and phase of the signal[19]. McRae et. al[19] has a very nice simulated response of a 5Ghz resonator, that shows the expected behaviour of the S21 measurement, seen in figure 4.1

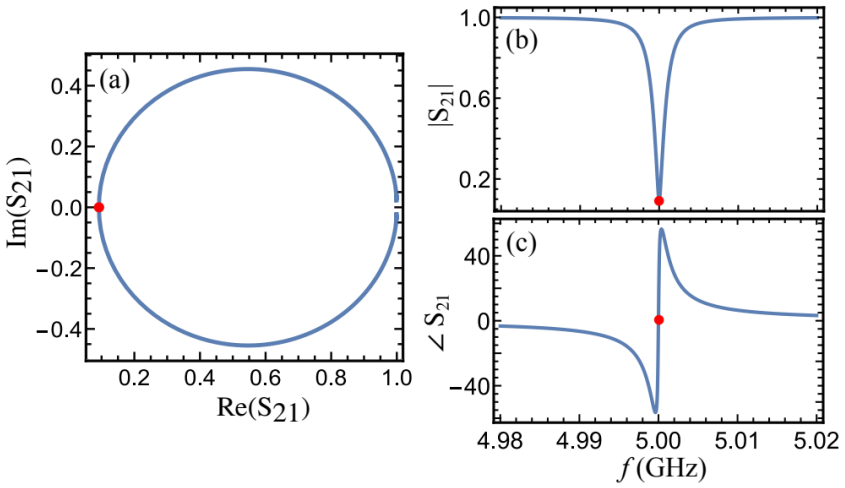

Figure 4.1: Figure from McRae et. al.[19], showing the Lorentzian response of a simulated 5GHz resonator, in an S21 measurement. The red dot indicates the resonance frequency of the resonator in each representation.

This Lorentzian behaviour as a function of frequency is described by the input impedance of the resonator[19]:

$$Z_{in} = (\frac{1}{R} + \frac{1}{i\omega L} + i\omega C)^{-1} \tag{4.1}$$

An important quantity that will be used extensively through this thesis is the quality factor Q of the resonator, defined as follows:

$$Q = \frac{2\pi f_0 W}{P_r} \tag{4.2}$$

Here, $f_0 = (2\pi\sqrt{LC})^{-1}$ is the resonance frequency of the resonator, W is the total time averaged power and $P_R = \frac{|V|^2}{2R}$ is the power loss associated with the resistor of an RCL resonator. In qualitative terms, the Q factor describes the relation between the power stored at resonance and the power loss of the system[19]. The Q factor can be extracted as a fit parameter from a Lorentzian fit to the S21 response of the resonator

The quality factor of a resonator coupled to a feedline has two important components: the internal quality factor Q_i and the external quality factor Q_e, given by the relation.

$$\frac{1}{Q} = \frac{1}{Q_i} + \frac{1}{Q_e} \tag{4.3}$$

The internal quality factor describes the rate that energy stored in the resonator escapes to parasitic effect, whilst the external quality factor describes the rate associated with energy escaping into the coupled system. When we couple a feedline to our resonators, Q_e describes the resonators coupling to the feedline, and is related to the resonator linewidth κ, by the following equation[20]

$$Q = \frac{f_r}{\kappa} \tag{4.4}$$

This expression can also be seen as a definition of the Q value, i find it more intuitive to use when thinking about resonators for our qubits. Notice that this equation uses the full Q value. For our experiment, the internal quality factor is not easy to change, therefore we modify the external quality factor when tweaking the system. The linewidth (and thereby the Q value) can also be related to the delay needed (τ_{rd}, rd= readout delay) when measuring, to avoid measuring the resonator transient:

$$\tau_{rd} = \frac{1}{2\pi\kappa} = \frac{Q}{2\pi f_r} \tag{4.5}$$

We need to readout in a time much shorter than the qubit lifetime, $\tau_{rd} << T_1$. If we expect a short qubit lifetime, we need a low Q, corresponding to a large coupling to the feedline. This also ties into the Purcell effect, and how it is important to balance out the need to readout quickly with isolating the qubit form the environment, explained well in Krantz et. al[8]. From Krantz we get an upper limit on the qubit liftetime, in the dispersive regime. We can reverse this to think of it as a limit on Q, imposed by the lifetime of the qubit:

$$T_1^{lim} = \frac{Q * \Delta^2}{\omega_r * g^2} \iff Q_{lim} = \frac{T_1 * \omega_r * g^2}{\Delta^2} \tag{4.6}$$

The S_{21} response of the resonator can also be expressed from the Q values, from Besedin et. al.[21]

$$S_{21} = ae^{i\alpha}e^{2\pi i f\tau}(1 - \frac{e^{i\phi}Q/Q_e}{1 + 2iQ(f/f_r - 1)}) \tag{4.7}$$

Here a, α, τ are parameters not directly related to the resonator, but rather the transmission through other components in the circuit. This makes it clear how it is possible to fit and calculate the Q values, given the S_{21} response of the resonator.

Besedin also has a more illuminating equation for the resonance frequency of a $\lambda/4$ resonator (the type used for our work):

$$f_r^0 = \frac{c_l}{4l}(2n-1) \tag{4.8}$$

Here, f_r^0 is the resonant frequency of the resonator, c_l is the speed of light in the medium, l is the length of the resonator and n is an integer going from 1 to infinity, representing the harmonic of the resonator. We are usually only concerned with n=1, since the higher frequency harmonics for our resonators are have far larger frequencies than our working regime (15-20GHz for the n=2 harmonic of our resonators)

When designing resonators and feedlines, we use an online calculator to get an approximate idea of the resonance frequency and external Q of the system. The calculator is based on the Besedin paper[21], and made by Ilya Besedin[22]. To use the calculator, you define the geometry of the resonator by adding pieces of geometry, and defining the length of each piece. As an example, i have defined the M19 R4 resonator (also corresponding to the DMNS003 R1 resonator) in figure 4.2.

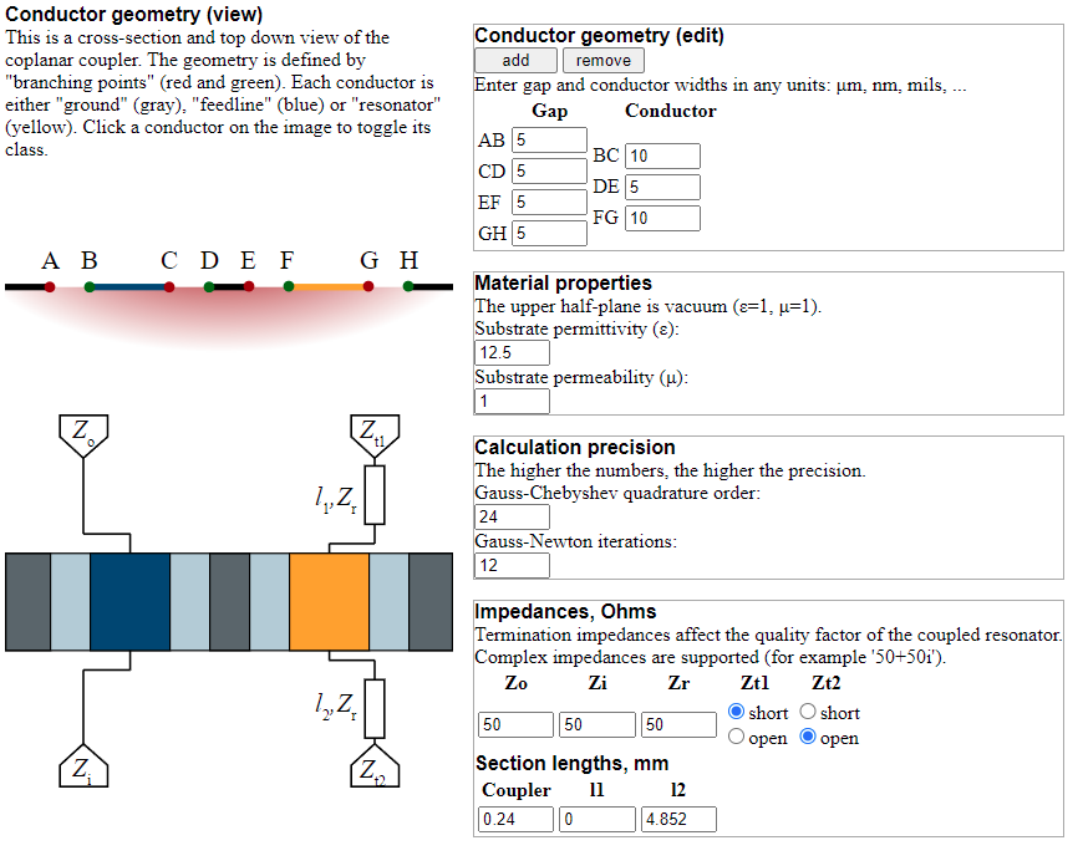

Figure 4.2: Besedin online calculator used to estimate the resonance frequency and other parameters of resonators. This image shows the setup for a simulation of the M19 R4 resonator (or DMNS003 R1 resonator). The blue part in the illustration is the feedline, the yellow part is the resonator. We define the coupling piece length, and l2 defines the length of the resonator. The DE distance is the distance to the feedline. The substrate permitivity has been set to the permitivity of InP.

After setting up the calculation, the online calculator gives a plethora of results. These results for M19 R4 are shown in figure 4.3. The estimated resonance frequency from the calculator was $f_r^{calc} = 5.6840GHz$, and the actual resonance frequency of M19 R4 was $f_r^{meas} = 5.6885GHz$. In this case, it is very close to the actual resonance frequency. However, the resonance frequency of the DMNS003 R1 resonator has the same parameters, but the resonance

frequency was measured to be $f_r^{DMNS003,R1} = 5.8256GHz$, which is still close to the calculated value, but around 200MHz off. This is one of the reasons why we use the Besedin calculator as a rough estimate of the resonators. The external quality factor is also quite different than measured, it is estimated to be 38K, but we measured around 22K both on M19 R4 and DMNS003 R1. This is one of the reasons why it is necessary to make actual chips to estimate the external quality factor.

Per-unit-length effective inductance, nH/m:

	Feedline	Resonator
Feedline	406.224	36.373
Resonator	36.373	406.224

Per-unit-length effective capacitance, pF/m:

These value can be used to estimate the capacitance of interdigital capacitors.

	Feedline	Resonator
Feedline	186.377	-16.688
Resonator	-16.688	186.377

Effective characteristic impedances:
Z0 (feedline): 46.686 Ohms,
Z0 (resonator): 46.686 Ohms,
κ: 0.0895

Full per-unit-length inductance, nH/m:

BC	DE	FG
483.463	226.343	113.613
226.343	663.275	226.343
113.613	226.343	483.463

Full per-unit-length capacitance, pF/m:

BC	DE	FG
186.377	-57.907	-16.688
-57.907	152.753	-57.907
-16.688	-57.907	186.377

Resonances

First-order corrected resonance frequencies in the "resonator" (yellow) conductors and TLs 1 and 2.

n	Frequency, GHz	Linewidth, MHz	Decay time, μs	Quality factor
1	5.68397	0.15	2.154	38464
2	17.05027	1.31	0.242	12971
3	28.41180	3.57	0.089	7968
4	39.76586	6.74	0.047	5903
5	51.11041	10.59	0.030	4828

Figure 4.3: Besedin online calculator result from the M19 R4 (and also DMNS003 R1) resonator. The first thing to note is the charecteristic impedances of the feedline rand resonator, it is calculated to be 46.686 Ω. This likely means that our system is not exactly 50 Ω terminated, and will result in some loss of signal due to reflection. We also see an estimate of the resonance frequency $f_r = 5.68GHz$, the linewidth, decay time and Quality factor.

Most of the work of this thesis has been spent designing, fabricating and measuring "test chips", meant to tailor the measurement environment to our specific qubit system: the dotmon. I have also designed, developed, fabricated and measured crossovers to improve the qubit microwave environment of the qubit, which i thoroughly discuss in section 3.1

4.2 Resonator Tests M19 and DMNS003

4.2.1 Motivation

This section is about results from two "test chips", made with the purpose of designing an ideal resonator for the dotmon qubit project. The pertinent question is, what is an ideal resonator for the dotmon qubit? This project builds upon two previous projects from Qdev: the 2DEG gatemon from Casparis et. al[14] and the nanowire gatemon with an accidental quantum dot from Kringhøj et. al[16]. The dotmon aims to combine these two projects by making a 2DEG dotmon with a controllable and tunable qunatum dot in the Josephson junction. The first iteration of the dotmon (M11 chip) was designed based on the previous projects, and electrostatic simulations. During initial VNA measurements, it was determined that the actual value of the external quality factor was much higher than designed. We measured the resonators to have $Q_e \approx 20k$, they were designed to have $Q_e \approx 2k$, see figure 4.4. They were designed to have a small external quality factor to allow for fast measurement of the qubit. We were unsure of the lifetimes of the qubits, and if the liftime was short, fast measurement would be needed.

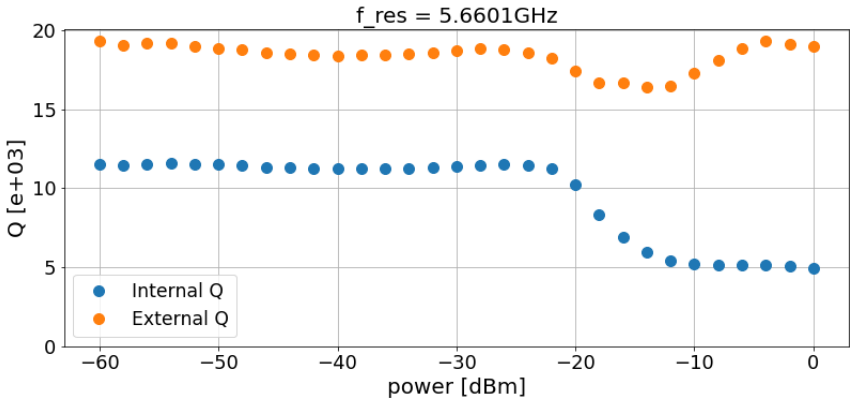

Figure 4.4: Measurements of a resonator on the first generation dotmon chip, M11. It shows the internal and external quality factor as a function of power, extracted from a VNA power scan.

We chose to design a new resonator test with similar resonators as the qubit chip, but with slight changes in design meant to decrease the external Q. Two easily tweakable parameters affect the external Q of the resonators: The distance from the feedline to the resonator and the length of the "coupling piece" of the resonator. The coupling piece is the part of the resonator closest to the feedline.

This intuitively makes sense, the closer the feedline and resonator are, the easier it is for photons to enter the resonator. If they have more space to do it, corresponding to the coupling piece, that also increases the coupling (and decreases the external Q). There are limits on these parameters however. The resonators are serpentine, and placed in a hanger configuration. The length added to the coupling piece must be shortened in the other end of the resonator, if the resonance frequency must be kept constant. Since other resonator are present on the feedline, there needs to be space for the coupling piece extension. Essentially, the lengthening of the coupling piece negates some of the positives of having a serpentine resonator.

The distance to the feedline is also constricted. The resonators used for the M11 dotmon qubit chip had a distance of $15\mu m$ to the feedline. However, this distance is split in three: 5 μm is the strip line used to define the resonator, $5\mu m$ is a thin piece of the groundplane going between the resonator and feedline strip lines, and the last $5\mu m$ is the strip line from the feedline. We can not change the strip line width, and there needs to be a small piece of the

groundplane between the resonator and feedline. We tried removing the piece of groundplane for one resonator, and it dramatically changed the resonance frequency of the resonator, and possible more, we were not able to resolve useful data from the specific resonator. See figure 4.6 for optical images of the resonatorss. That means we effectively can only decrease the distance between the resonator and feedline by $0-4\mu m$

4.3 M19 Chip

4.3.1 Design of M19

For the design of the first resonator test, we wanted a few different variations on the coupling piece length and the distance to the feedline.

The first resonator test chip, M19, was fabricated on the same material stack as the qubit chips: M04-16-20.1 (See figure 2.1.) The fabrication was intended to be quick, with few e-beam steps. We only needed a control layer to define the feedline and resonators, no qubits or crossovers included. The wafer stack can be split into three components: The InP substrate, the 2DEG stack and the epitaxial aluminium. The control layer must have no aluminium or 2DEG beneath it. To get to the InP substrate we usually start by etching the 2DEG and aluminium (the mesa etch) to create the Josephson junction for the qubit, requiring multiple e-beam steps. For this chip, a blanket etch of the epitaxial aluminium and 2DEG was the only step required before deposition of the control layer. For a qubit chip, we also use alignment marks: a set of gold crosses at the edge of the chip that ensure layer alignment across e-beam exposures. They were also not needed here, the center of the chip is instead used for exposure alignment.

The chip was fabricated on a 3.35mm x 4.3mm piece of the wafer. On this chip we were able to fit 4 resonators, coupled to the feedline hanger style, see figure 4.5. The resonators are labelled by ascending frequency, R1 is the lowest frequency resonator, R4 has the highest frequency. R4 is the reference resonator, it has the same design as the highest frequency resonator on the M11 qubit chip. The coupling piece length of R4 is $240\mu m$, and the distance to the feedline $5\mu m$. R3 has an extended coupling piece compared to the reference, extended by $200\mu m$ (to a total of $440\mu m$). R2 also has an extended coupling piece, extended by $400\mu m$ (to a total of $640\mu m$). R1 has both an extended coupling piece by $400\mu m$, but it has also been moved $5\mu m$closer to the feedline. We found out that moving R1 $5\mu m$ closer to the feedline was a mistake, since it removed the ground plane piece between the feedline and resonator. The thought process behind moving R1 as close as possible to the feedline was to try and get the lowest Q_e possible from our designs, with a reasonable coupling piece length. The design variations are summarized in table 4.1.

Parameter	R4	R3	R2	R1
Length	$4852\mu m$	$4927\ \mu m$	$5002\mu m$	$5077\mu m$
Coupling Piece Length	$240\ \mu m$	$440\ \mu m$	$640\ \mu m$	$640\ \mu m$
Feedline Distance	$5\mu m$	$5\ \mu m$	$5\ \mu m$	$0\ \mu m$

Table 4.1: M19 Resonator variations summarized in this table. The length of the resonators increase in steps of $75\mu m$ from R4 to R1. The distance to the feedline is here defined as the distance between the striplines of the resonator and feedline, allowing for a $0\mu m$ distance for R1. This results in no strip of groundplane between the resonator and feedline, as shown in the bottom left panel of fig 4.6

As evident on figure 4.5, it is difficult to fit the resonators on the chip with coupling pieces of $640\mu m$, without interfering with other resonator or devices on chip. Having the full qubit

design in mind is important, a qubit design also needs gate lines and transport lines.:

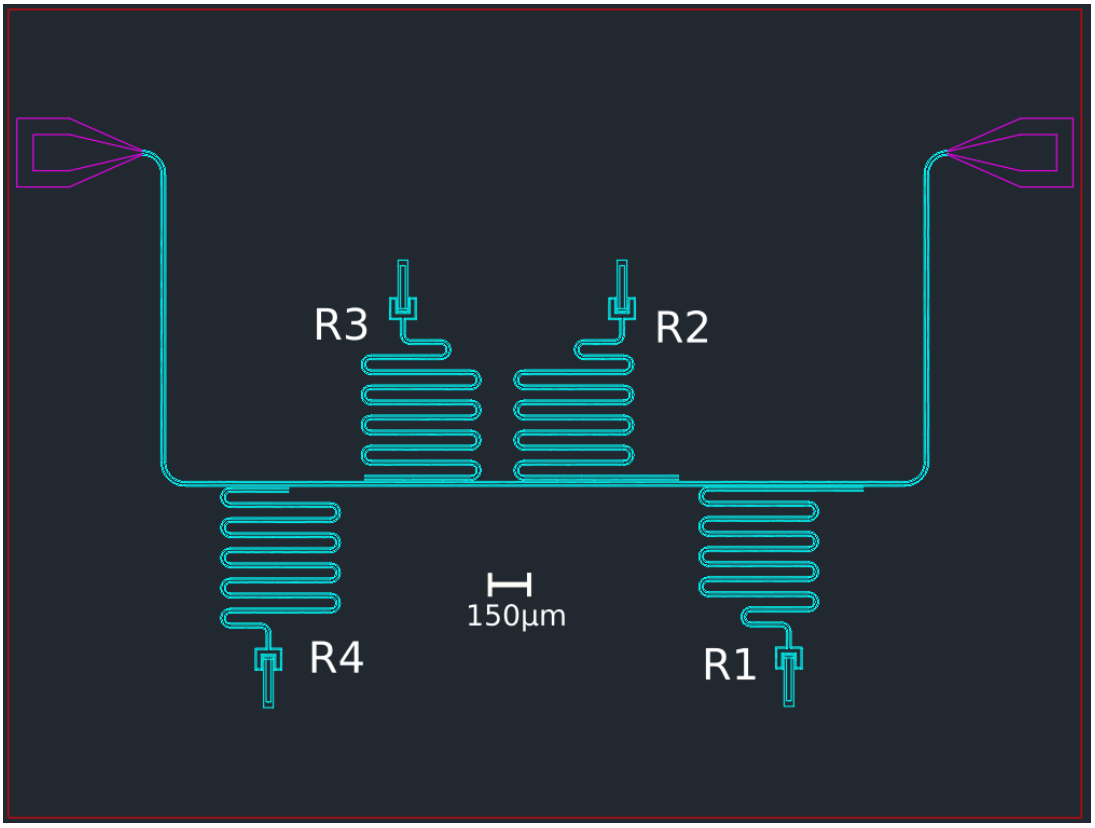

Figure 4.5: M19 resonator chip design, red marks the outline of the chip, blue and purple marks the strip lines of the resonators. 4 resonators are coupled to the feedline, mentioned in descending order of frequency: A reference resonator identical to the one from the M11 qubit chip (R4, bottom left), a resonator with a 200 μm longer coupling piece than the reference (R3, top left), a resonator with a 400 μm longer coupling piece than the reference (R2, top right) and finally a resonator with 400 μm longer coupling piece than the reference, but also moved 5μm closer to the feedline (R1, bottom right).

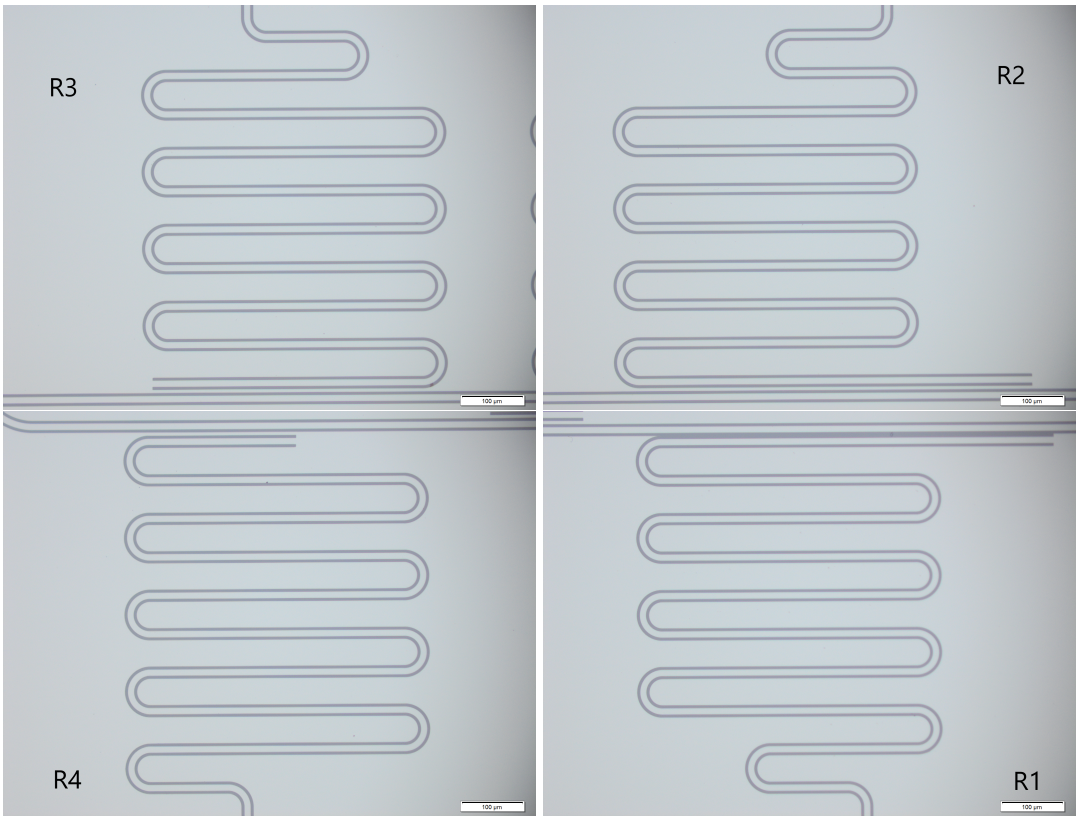

Figure 4.6: Optical images of M19 resonators post-liftoff. The white parts are deposited aluminium, the grey lines is the InP subtrate showing through the feedline and resonator striplines. It is clear to see the coupling piece length difference of the 4 resonators, and that R1 has been moved close to the feedline, removing the small piece of groundplane going between the feedline and resonator. See figure 4.5 for design details

4.3.2 Fabrication of M19

The fabrication steps of the M19 resonator test are few and straight-forward

1. *Clean Chip:* Strip post-cleaving resist with acetone and ultrasonication, inspect chip for defects
2. *Blanket Aluminium and Mesa etch:* Aluminum etch with Transene D (Aluminum etchant type D), 2DEG etch with mix of MiliQ Water, autophsophoric acid, citric acid and hydrogen peroxide, clean chip thoroughly in MiliQ water, ash with oxygen plasma.
3. *Control Layer:* Spin Bilayer EL9 and PMMA A4 resist, E-beam expose control layer, develop with MIBK:IPA 1:3, ash with oxygen plasma
4. *Control Layer:* Evaporate 100nm Al, liftoff unwanted metal

For fabrication detail, see appendix A.2.

The fabrication seems an easy one, with fairly few steps. Reality often disappoints however, as many issues with the recipe were encountered during fabrication. All issues encountered were with the control layer step, first with the e-beam exposure and development, and later with aluminium liftoff. Many details of the process can be found in the appendix, i will summarise them here:

For a successful e-beam exposure and development, a recipe is developed. The e-beam exposure has a multitude of settings that can be tweaked for a specific purpose and resist. The

first step is to choose a suitable resist, and if needed, a combination of resist layers. The next step is to make a dose test, to determine what charge per area results in a stable development of the resist. There are several parameters that influence the dose:

- **Writefield Size:** The size of the area that the beam will expose in one gun position
- **Number of dots:** The number of points inside the writefield that the beam will be deflected onto in one gun position
- **Aperture size:** The size of the aperture that the electron beam is focused through
- **Beam Current** The Current of the electron beam
- **Area Dwell time / Dose time** The dwell time on each dot

Choosing these parameters will result in a specific electron dose in $\mu C/cm^2$. The dose for a specific resist on a specific substrate should be the same, but variations occur from wafer to wafer. The other parameters are changed to fit different purposes, a 60nm wide QPC arm needs a much higher resolution than a several hundred micron large resonator, for example.

After choosing a dose and exposing a desired pattern for the test, the resist needs to be developed. A development should be slow enough to control, meaning that it should be resistant to a small change in development time. The lowest bound for a stable development process is around 10 seconds, preferably it is 20-30s. The dose test is used to establish a development time for the recipe. It is generally important to check the patterns after development, sometimes a pattern might be under or overdeveloped even after following the recipe, see figure 4.7 for reference. If underdeveloped a couple of seconds in the developer can usually fix it, if overdeveloped the exposure must be re-started.
A couple of things are important to consider when doing an e-beam exposure. The exposure

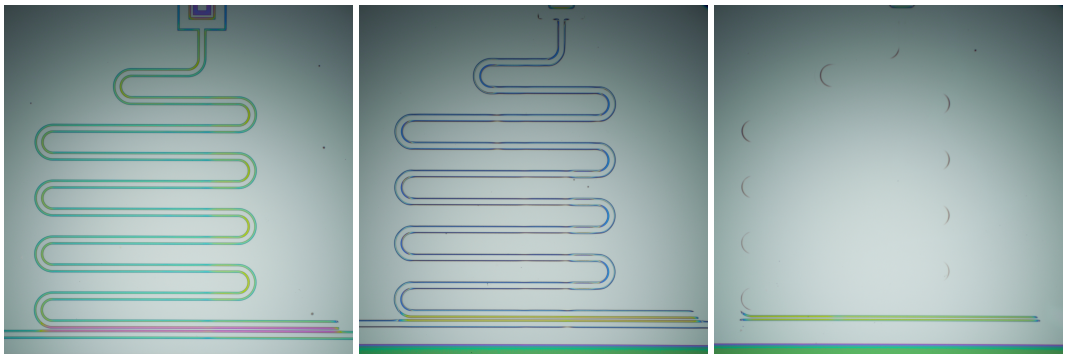

Figure 4.7: Optical images of a dose test, showing a resonator with different amounts of development. The white background is the InP substrate, the coloured parts is a bilayer of PMMA A4 and EL9 resist. The leftmost image show a correct development, with a very slight overdevelopment. The middle image shows a clear overdevelopment, note the thinness of the lines, the breaks, and the missing part in the top. The rightmost image shows an extreme overdevelopment, where most features are completely washed away.

should not take more than 1-2 hours, ideally below one hour. The accuracy and current of the electron beam drifts over time, and long exposures introduce failure modes associated with this drift. It is also possible to use multiple currents and doses in one exposure, a schedule file is uploaded into the e-beam machine that instructs it to change the current between patterns. It is important that the beam-settings are focused and tuned before starting the exposure, and making sure that the patterns overlap in the exposure design. The beam setting need to be updated over time by a technician, to counteract the setting drift. This introduces another failure mode, if each preset is not checked before exposure. A recipe developed might not work if the

beam parameters are slightly changed because of the drift, a problem also encountered during this fabrication

I am mentioning these considerations because it is important to understand the complexity of the fabrication step. A myriad of failure modes are ready to ruin your fabrication.

Since metal will be deposited on the exposed areas of the chip, and we mean to form a groundplane on the chip, most of the chip area will need to be exposed. This is a lengthy procedure, to shorten it we split the exposure into two: A high current exposure and a low current exposure. The high current exposes the ground plane of the chip and the bondpads. The low current exposure exposes the feedline, resonators and qubit island. After splitting the exposure, it still lies in the high end of exposure times, at roughly 3 hours.

During the first attempt at fabricating the control layer, it was discovered that the parameters used for the M11 qubit did not work for this chip. The chips came from the same wafer (the M11 and M19 pieces of M04-16-20.1 respectively), and the reason for this discrepancy is unknown. Much of this thesis was spent optimising the parameters to create a stable development for the control layer. Dose tests were performed, but unfortunately did not translate directly to the actual exposure. I suspect that this is because the long exposure times of the actual exposure were not replicated in the smaller features of the dose test.

After finding suitable parameters for the exposure, liftoff proved the next challenge. The striplines of the feedlines and resonators are small and winding compared to the ground plane, and are hard to properly lift off. Liftoff can be tricky, the chip needs to be constantly wet to avoid the resist drying up. An ideal liftoff only takes one soak in solvent (acetone or dioxolane), either an overnight soak in cold solvent, or 5-10 minutes in hot acetone . After the soak, a squirt bottle or syringe is used to liftoff the material with the pressure. If this does not work, the sample can be ultrasonicated. These methods can be iterated to ensure liftoff, but with each iteration the chance of failure increases.

4.3.3 M19 Q Measurements

The M19 was loaded in a cQED daughterboard and wirebonded. I unfortunatley have no images of this bonding, see section 4.4.3 for an example of bonding and sample packaging.. The first thing to measure when the sample is loaded is the full transmission through the sample. This is done with a Vector Network Analyzer (VNA) over a wide range of frequencies, here 0-9GHz. The full transmission data is shown in figure 4.8.

There are a couple of important things to take notice of in this data: First the low transmission, we generally see a 40dB loss of signal in the range 4-8Ghz. This is the range the LNF cryoamp amplifies in, and by the fridge setup we should see 0dB attenuation in this range. This indicates something terribly wrong with the sample. We think the low transmission was caused by a faulty wirebond. It can be tricky to get the wirebonds to stick to this specific material, and sometimes they seems to be connected but are only partially connected. Another thing to note on this sample is the wild rippling in the signal. This could also be a feature of the suspected broken wirebond, but it could also be box modes. The daugtherboard chosen for this chip had a trench that was a size too big for the chip, resulting in lots of empty space between the chip edges and the trench edges. This could be a cause for low-Q cavities that couple to the signal, creating the rippling resonances we see.

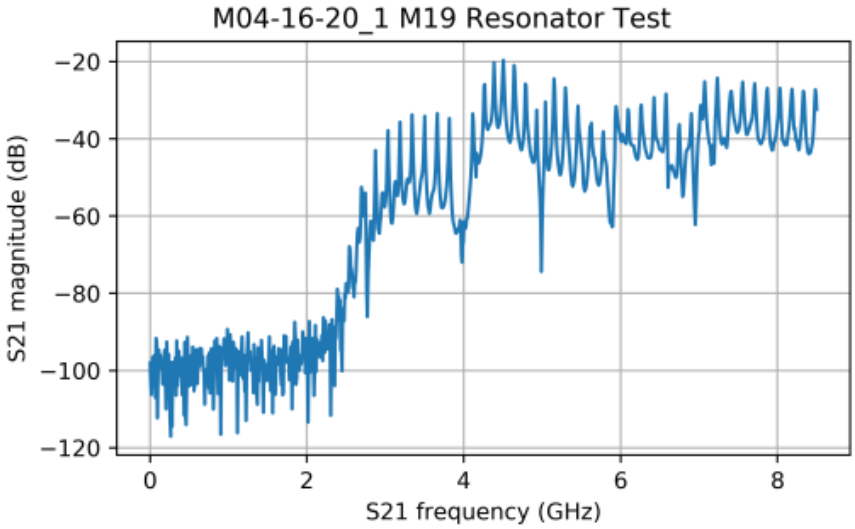

Figure 4.8: Full transmission through the M19 resonator chip, see clear parasitic modes (lots of ripples) and 40Db loss of transmission, indicating a serious issue with the sample. Measurement of previous samples rules out issues with the measurement circuit.

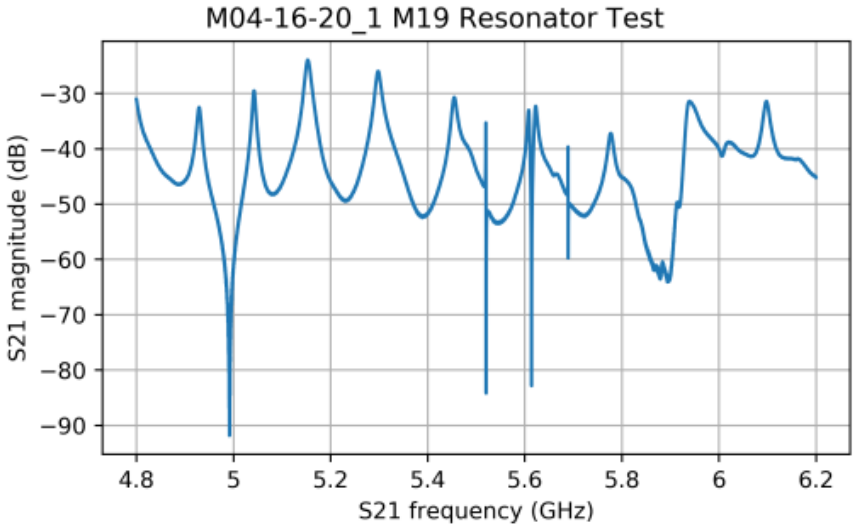

Figure 4.9: Zoom in on resonators on the M19 feedline, large ripples in transmission visible, likely due to some kind of reflection on the sample. Ripples clearly affect resonator dips, R1 (lowest frequency) looks especially strange, it is at a much lower frequency than designed, and the resonator dip seems very wide compared to R2,R3 and R4.

We take another set of data, choosing a narrower range of frequencies where we expect our resonators to show up. This is shown in figure 4.9. We see 4 clear resonator dips, and the rippling discussed previously. The resonators should be evenly spaced in frequency, since the frequency scales linearly with the length of the resonator, and we have a flat 75 μm increase in length for each resonator. We see the 3 highest frequency resonators follow this trend, but the lowest frequency resonator (R1, 5Ghz) is far away from the other resonators, deviating

from the pattern. The resonator dip also looks much broader than the 3 others, we think this is caused by the design flaw mentioned in the fabrication and design section. The removal of the piece of groundplane in between the feedline and resonator had some unforseen effect, somehow broadening the dip, and lowering the frequency of the resonator. The broadening could also be attributed to some non-design related issue, as seen around 5.9Ghz. An attempt

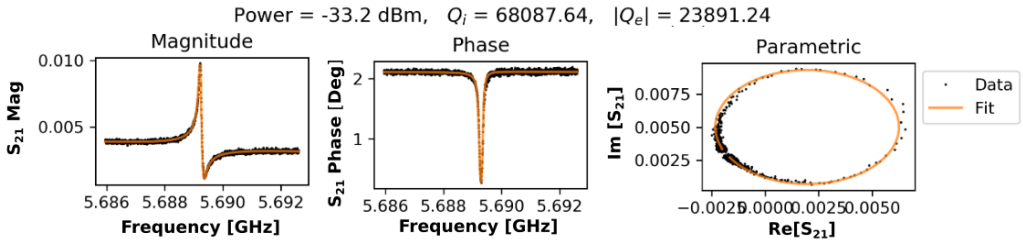

Figure 4.10: Data and fit of R4, shown in two different representations: Mag and Phase, and parametric. Q_e and Q_i are extracted as fit parameters, and are shown in the title of the plot. The $Q_e \approx 24K$ is consistent with the previous measurements of a resonator with the same design, on qubit chip M11, seen in figure 4.4.

was made to fit the resonators, but we only succeeded on R4. We believe that the extra rippling in the signal and the low transmission through the sample complicated the fitting process. The fit result of R4 is shown in figure 4.10, the fit looks satisfactory and resulted in an internal Q of $Q_i = 68.1K$ and $Q_e = 23.9K$. R4 has the same design as the highest frequency resonator on the M11 qubit chip, which also had an external quality factor around 20K. We expect a difference in results since no qubits are present on this chip to affect the Q values. I am using loose numbers here, and comparing in orders of magnitude, because we have many uncertainties in our model and data. The M19 chip was also measured in a different fridge than the M11 qubit chip, the comparison is therefore fairly week. The lack of useful data from M19 was also an issue, it was therefore decided to construct a new test chip.

4.4 DMNS003 Chip

4.4.1 DMNS003 Introduction and Motivation

After the failure of the M19 resonator test, a new resonator test was needed. Concurrently with the measurements of M19, the crossovers had been developed and tested. It was therefore decided to make a chip that could test the effect of crossovers on cQED measurements, and also give us useful info on the resonators external quality factors.

The chip was named DMNS003, and was fabricated on the same material as the M11 and M15 qubits chips. The design is shown in figure 4.11.

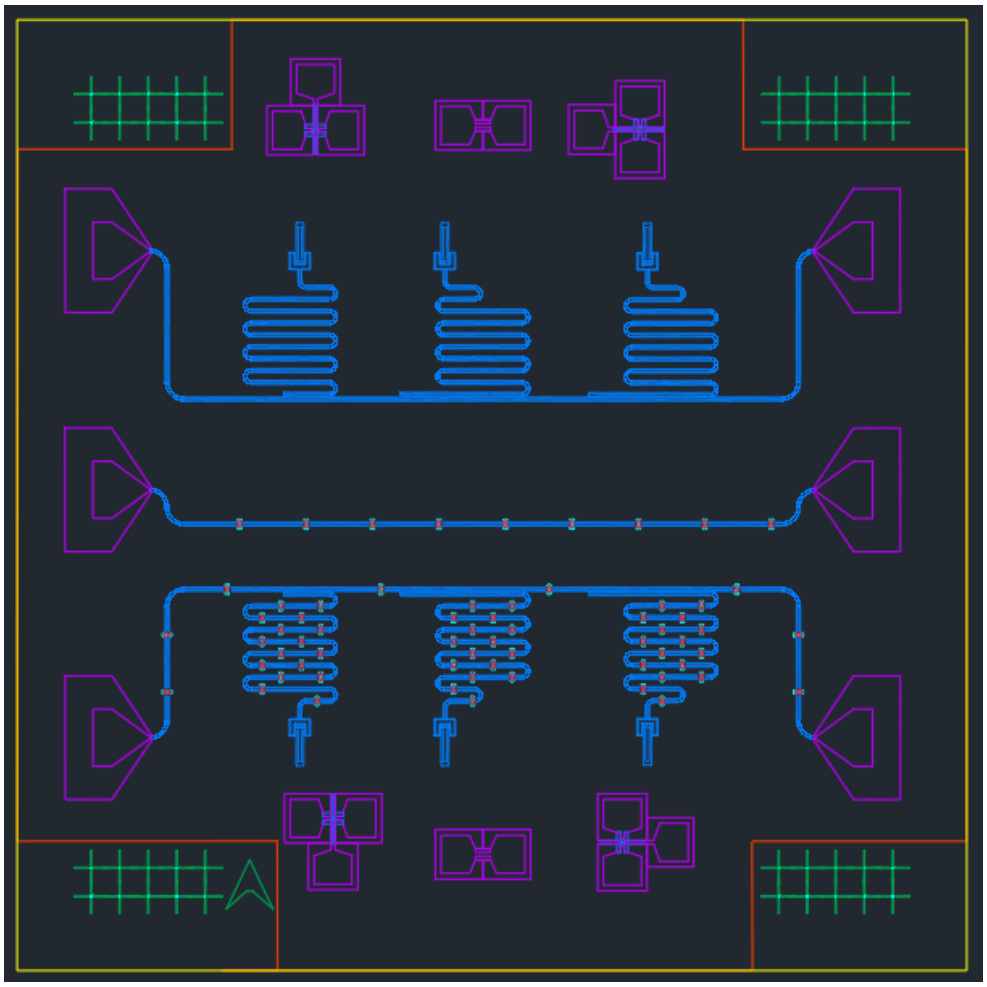

Figure 4.11: Overview of DMNS003 design, Three feedlines are present, and six DC test structures. The gold box shows the outline of the chip, the green crosses are alignment marks. The small structures on the middle and bottom feedline + resonators are crossovers. The blue and purple marks the high and low current exposure parts of the chip, purple is high current, blue is low current.

Three feedlines are present on the chip, one hosting three resonators without crossovers, one hosting a feedline with no resonators, but with crossovers and one feedline with resonators and crossovers. The chip also hosted six DC test structures, that would allow us to test the crossovers in a DC probe station if we encountered issues in the cQED measurements. The idea is to be able to compare measurement of resonators with and without crossovers, and also to see if the crossovers have a defined effect on a bare feedline. The resonator designs are smiliar to the M19 resonator, but slightly different. The design variations are shown in table 4.2. Notice that there are only two variations in coupling piece length, the reference length

from M11 (R1 and R4) and reference plus 400 μm (R2, R3, R5 and R6). The feedline distance variation has also changed, mainly to avoid the issues with the M19 R1 resonator. The lowest distance to the feedline we dared to go was $3\mu m$, because we were worried about development of a thin strip of ground plane between the resonator and feed lines. Images of the resonators with and without crossovers can be seen in figure 4.13.

Parameter	R1	R2	R3	R4	R5	R6
Length	$4852\mu m$	$5002\ \mu m$	$5077\mu m$	$4852\mu m$	$5002\mu m$	$5077\mu m$
Coupling Piece Length	$240\ \mu m$	$640\ \mu m$	$640\ \mu m$	$240\ \mu m$	$640\mu m$	$640\mu m$
Feedline Distance	$5\mu m$	$5\ \mu m$	$3\ \mu m$	$5\ \mu m$	$5\mu m$	$3\mu m$
Crossovers	No	No	No	Yes	Yes	Yes

Table 4.2: DMNS003 Resonator variations. R1, R2 and R3 are present on the top feedline, R4, R5 and R6 are present on the bottom feedline. R1 and R4 are reference resonators, identical to the ones on qubit chip M11

4.4.2 Fabrication of DMNS003

Fabrication of DMNS003 was also plauged with troubles, much like M19. The dose needed adjustment again, and liftoff was still quite difficult. The fabrication steps are very similar to the InP-H3 crossovers sample, since we needed to incorporate the crossovers. They are as follow:

1. *Alignment Marks:* Spin PMMA A4 resist and E-beam expose alignment marks, develop with MIBK:IPA 1:3, ash with oxygen plasma
2. *Aligment Marks:* Evaporate 10nm Ti sticking layer, Evaporate 40nm Au layer, liftoff unwanted metal
3. *Control Layer:* Spin Bilayer EL9 and PMMA A4 resist, E-beam expose control layer, develop with MIBK:IPA 1:3, ash with oxygen plasma
4. *Control Layer:* Evaporate 100nm Al, liftoff unwanted metal
5. *ALD:* Spin PMMA A4 resist and E-beam expose ALD area, develop with MIBK:IPA 1:3, ash with oxygen plasma
6. *ALD:* Use ALD to grow 15nm HfO2, liftoff unwanted HfO2
7. *Crosslinked Resist:* Spin PMMA A4 resist and E-beam expose crosslinked resist (high E-beam dose), strip unwanted resist with acetone
8. *Crossovers:* Spin trilayer EL9 + EL9 + PMMA A4 resist and E-beam expose crossovers, develop with MIBK:IPA 1:3, ash with oxygen plasma
9. *Crossovers:* Kaufmann mill with Ar ions in AJA metal evaporator, removing native Al oxide on control layer for contacting crossovers
10. *Crossovers:* Evaporate 5nm Ti sticking layer, 50rpm stage rotation. Evaporate 50nm Al, 5deg stage tilt, 50rpm rotation. Evaporate 300nm Al, 0 deg tilt, 50 rpm rotation. Evaporate 50nm Al, 10deg tilt, 50rpm rotation.
11. *Crossovers:* liftoff unwanted crossover Al.

It is a long fabrication process, and with many steps. However, it did finish almost perfectly, the finished product is shown as optical images in figure 4.12. There is a slight jarring

in the middle of the image, not to worry, it is only an artefact of the microscope.

Unfortunately R4 did not lift off properly, and had a patch of Al ripped off due to an error in the resist. This is shown in figure 4.14. We did not expect this resonator to function after noticing these flaws, and indeed it does not show up on our transmission measurements, see figure 4.22 and 4.23. It was decided to move forward with the chip, since all other resonators looked intact on visual inspection.

The chip was set to be bonded, but there was a glaring issue. With M19, the chip was too small for the trench, with DMNS003 the chip was slightly too large. This made it impossible to properly glue the chip to the motherboard, and we had to sacrifice part of the chip. An experience process engineer cut the bottom of the sample away, sacrificing the 3 bottom DC transport structures. The sample now nicely fit in the daughterboard trench however. The chip post-cleaving is shown in figure 4.12

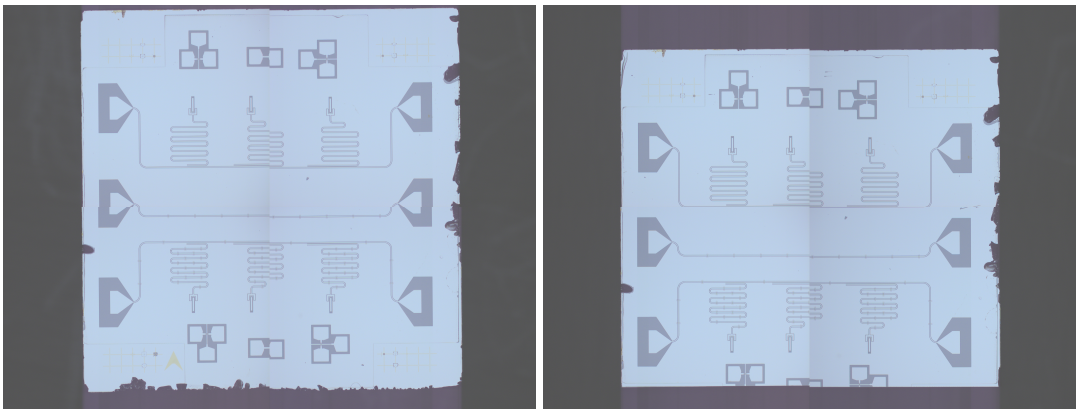

Figure 4.12: optical overview image of DMNS003, the left image shows the chip before cleaving to fit the daughterboard trench, the right image shows post-cleave.

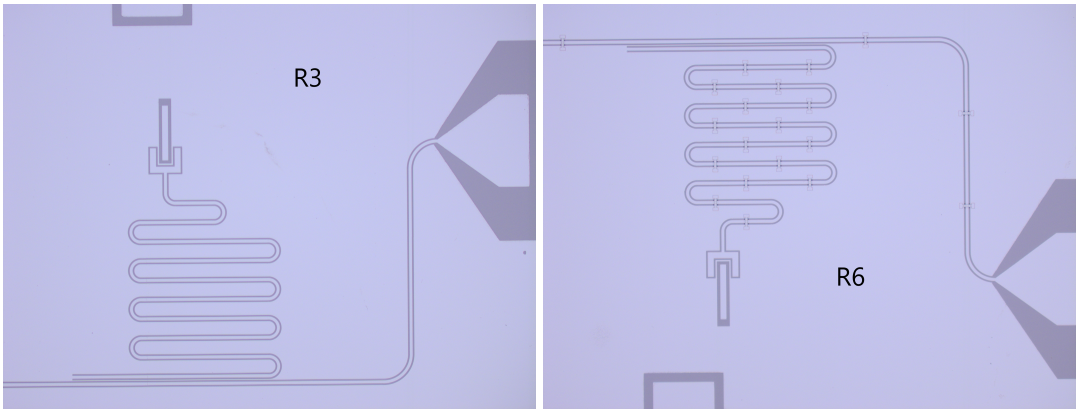

Figure 4.13: Resonators R3 (left) and R6 (right) are shown with a piece of feedline and a bonding pad. R3 and R6 are expected to have the lowest external Q of the resonators on DMNS003, both the R6 resonator and feedline have crossovers.

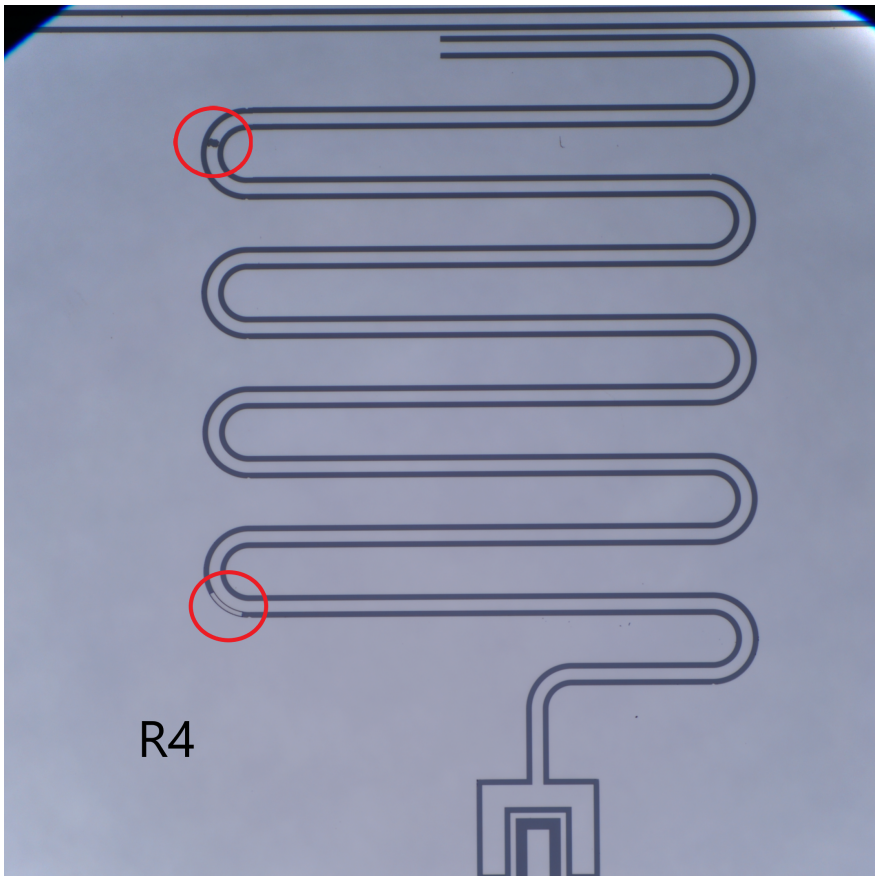

Figure 4.14: Image showing R4 on DMNS003, with issues highlighted in the red circles. The spot of missing aluminium was caused by a defect in the resist or chip surface, causing liftoff of the piece. The spot of aluminium in the stripline is a result of a failed liftoff, most likely because the spot got dried prematurely. This could usually be fixed if spotted before completing liftoff, but it would sometimes be near impossible to liftoff all the material.

4.4.3 DMNS003 Bonding and Sample Packaging

When fabrication of a sample has finished, the chip is mounted in a daughterboard. The daughterboard has a trench that should fit the chip dimensions snugly, where the chip is glued to the board with a small droplet of PMMA resist. When the glue is dry, electrical connection are made from the daughterboard to the chip using wirebonds. Wirebonds are thin aluminium wires that are punched into the daughterboard and chip to form connections. Figure 4.15 shows DMNS003 after being cleaved to fit the trench, and bonded to the daughterboard. After bonding, the sample is mounted in several layers of packaging. The daughterboard is encased in a box closed with an indium seal. Inside the box, the daugherboard is placed on a riser and protected by a lid, see figure 4.16, 4.17, 4.18, 4.19. The sample box is then mounted inside the puck, a hollow cylinder with electrical connectors that interface with the coldfinger on the fridge. Drive rods are also present on the puck, allowing us to screw the puck into the colfinger when the fridge is cold. The puck is shown closed, with the DMNS003 sample inside in figure 4.21.

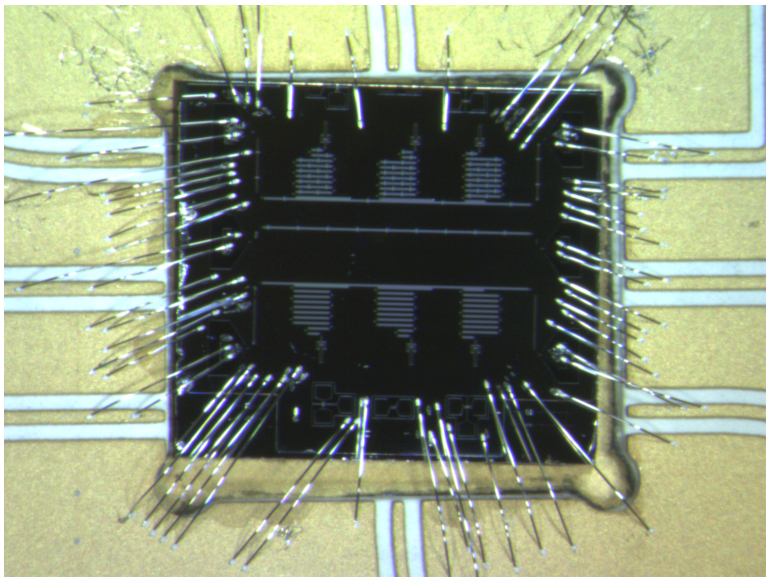

Figure 4.15: Optical image of DMNS003 after bonding

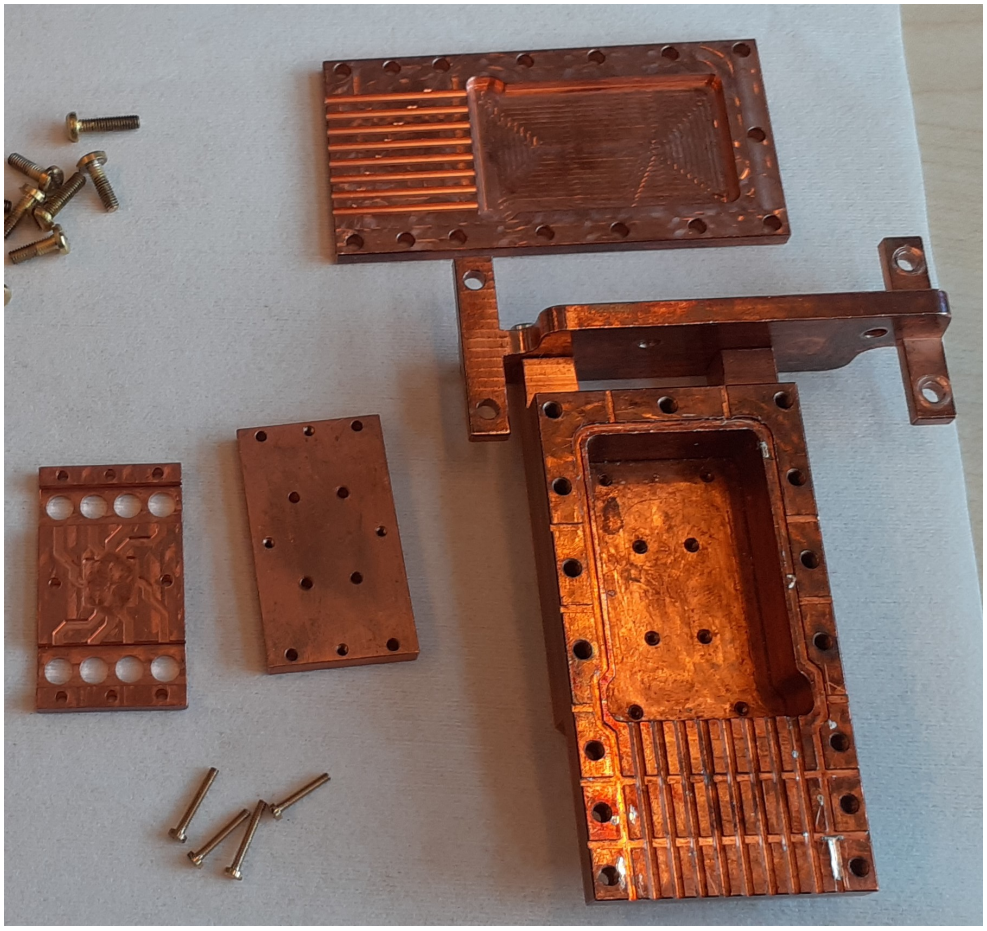

Figure 4.16: Overview of sample packaging from DMNS003. Going from left to right: The first object is the lid for the daughterboard, with patterning to protect the wirebonds and daughterboard wires. Next is the riser, placed beneath the motherboard in the box. Then there is the box, with lines engraved for SMA wires and the Indium seal. At the top is the lid for the box, with screws, at the bottom is the screws that hold the daughterboard, riser and lid in the box.

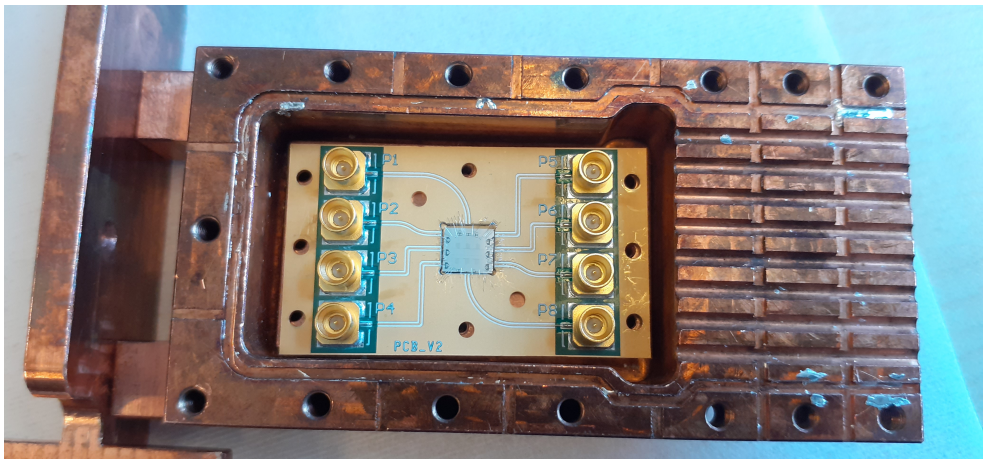

Figure 4.17: DMNS003 in daugherboard, in copper box

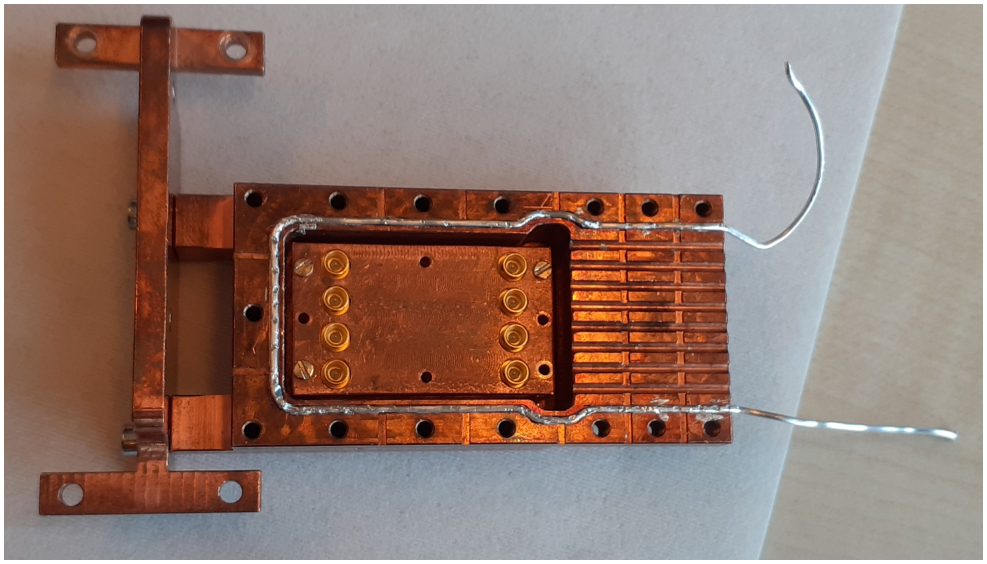

Figure 4.18: DMNS003 in daugherboard, in copper box, with lid and indium seal

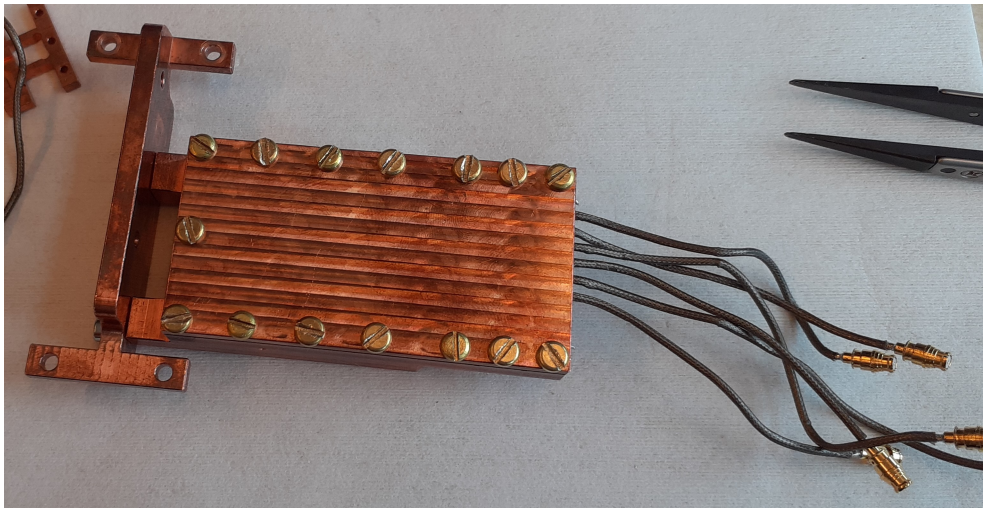

Figure 4.19: DMNS003 in daugherboard, in copper box, closed with SMA wires sticking out. Two wiresd for each feedline, to measure other feedlines the wires need to be switched in the puck.

Figure 4.20: DMNS003 in copper box, mounted in the puck

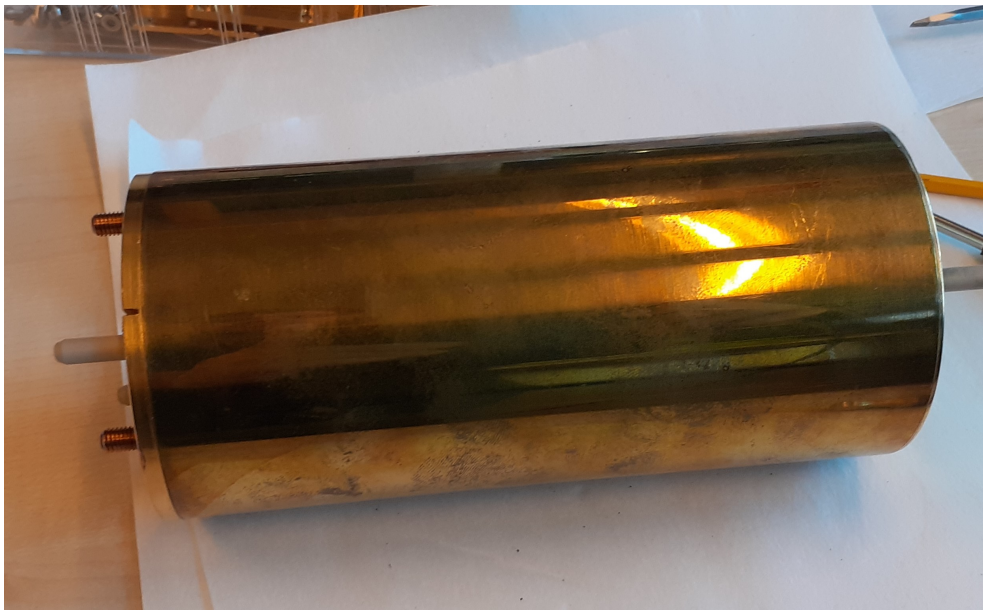

Figure 4.21: The puck with DMNS003 inside

4.4.4 Measurements of DMNS003

DMNS003 was measured in Triton 3 using the VNA measurement configuration described in section 2.3.1, at the fridge base temperature of 50mK-70mK. A slight omission was made in the measurement of the full transmission and zoom-in on resonators, the room temp amplifier was turned off for these measurements. It was turned on when measuring the power dependence, that ultimately results in the Q data. A transmission scan in the full range of our system is shown in figure 4.22, and a zoom in on the resonator frequency range is shown in 4.23. All three feedlines are shown in the same plot in figure 4.22, and the two feedlines with resonators are shown together in figure 4.23. It is worth noting that the total of 40dB loss in the 4-8GHz range is not expected, and is currently still an unresolved issue in this fridge.

As expected, we see that R4 is not showing up on the transmission scan. An interesting observation is that the resonators with crossover are designed to have the same resonance frequencies as the ones without crossovers, but they are consistently lower in frequency. The resonators without crossover have resonance frequencies of $f_{R1} = 5.8256GHz$, $f_{R2} = 5.6366GHz$, $f_{R3} = 5.371GHz$, whilst the resonators with crossovers have resonance frequencies of $f_{R5=4.6250GHz}$, $f_{R6} = 4.5638GHz$, an entire GHz lower than expected. We also see slightly more loss on the crossover feedline. This might not be crossover related, especially since it is only a couple of dB. It could be a bad SMA cable used for the line, a bad wirebond, or something else along those lines. This is quite worrying when considering the usefulness of the crossovers, it might also indicate some issues with the crossover design that only shows itself in radio frequency measurement. No immediately noticeable positive effect of the crossovers is observed, from these measurements. This does not mean that there is no noticeable effect, they might provide an improvement on the qubit measurements, but that requires implementation of the crossovers on a qubit chip.

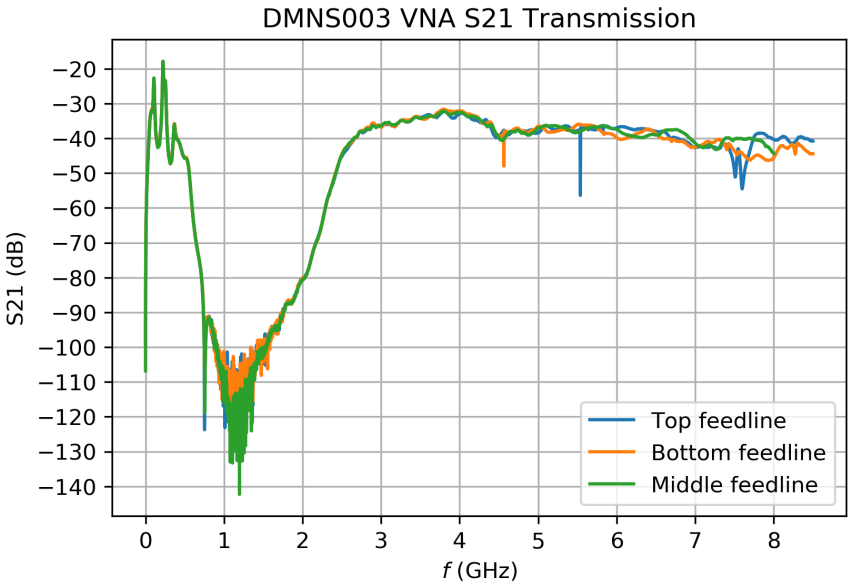

Figure 4.22: Full transmission through the feedlines of DMNS003. The top feedline had resonators without crossovers, the middle feedline had no resonators but had crossovers and the bottom feedline had both resonator and crossovers. The crossovers do not seem to have a huge effect on the rippling of the overall transmission. It is also clear to see that the two visible resonator dips are 1 GHz apart, their resonance freqency should be the same.

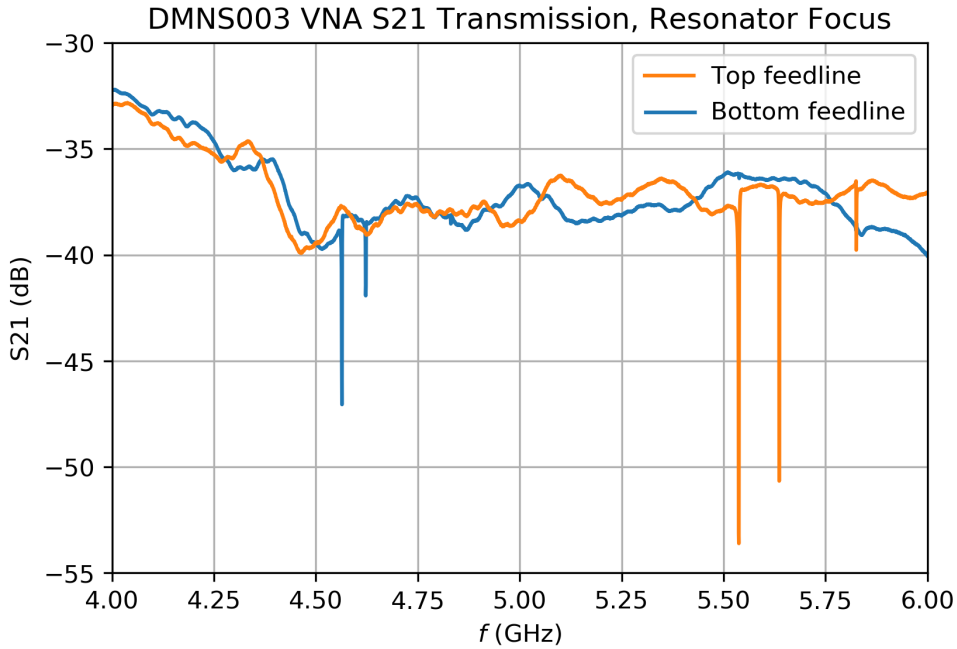

Figure 4.23: Transmission through the bottom and top feedlines of DMNS003, focused in the resonator frequency range. The top feedline has resonators without crossovers, the bottom feedline has resonator with crossovers. We clearly see that the resonators with crossover have a reduced resonance frequency compared to the ones without. From design, they should have the same resonance frequency. This indicates an issues with the crossover design or fabrication.

The resonator power scans of the working resonators, with their fitted Q values as a function of power, are shown in figures 4.24, 4.25, 4.26, 4.27, 4.28. For these power scans, the room temperature amplifier was turned on. A summary of the external quality factors of the resonators can be found in figure 4.29

The first thing to note is that the measured value is not in dB, but in S21 magnitude. This is because we measure the magnitude and phase of the S21 response to fit the resonators. Another very strange effect is the apparent push on the resonators at high power. this looks quite a lot like a resonator being pushed by a qubit, but it most decidedly is not. There are no known 2 level systems on this chip. We did not spend time examining why this frequency push happens a high power. Some of the resonator dips are hard to distinguish, this is partly because of the power scale, and mostly due to this data being taken to fit the Q's, and not for easy visibility of the dip.

It is difficult to make a strong conclusion on the crossovers effect on the resonators. We have few data points to make our conclusion from, but there are still observations to be made. The internal quality factor is generally less stable as a function of power on resonators with crossovers. This indicates that the resonators are somehow coupled to the crossover metal, increasing the parasitic loss of the "bare" resonator. It is also worth noting the higher values of Q_e on the resonators with crossovers. This could indicate that the coupling to the feedline is weaker with crossovers, but it could also be a symptom of other effects. These effect could likely be remedied by design tweaks, such as increasing the size of the ALD HfO2 and crosslinked resist separating the crossover metal from the resonators, or making the ALD thicker.

It was chosen not to include crossovers on the M15 qubit sample. The first reason for this is practical, it requires an extra fabrication step, and introduces more failure modes to the

process. During the control layer step of M15 it was discovered that the recipe developed for these chips was not stable when dealing with very small features, and needed to be revised. In the interest of time, we did not want to risk the fab going wrong by including the crossovers. The second reason not to include the crossovers on the qubit chip is the odd effect on the resonator resonance frequency, and the apparent effect on the Q values of the resonators. We did not prioritise to examine the crossovers effect on the resonators, we instead prioritised a working qubit chip.

It has been proposed to include the crossovers in a new variant of the M15 qubit, this might require a further examination of the effect of crossovers resonators.

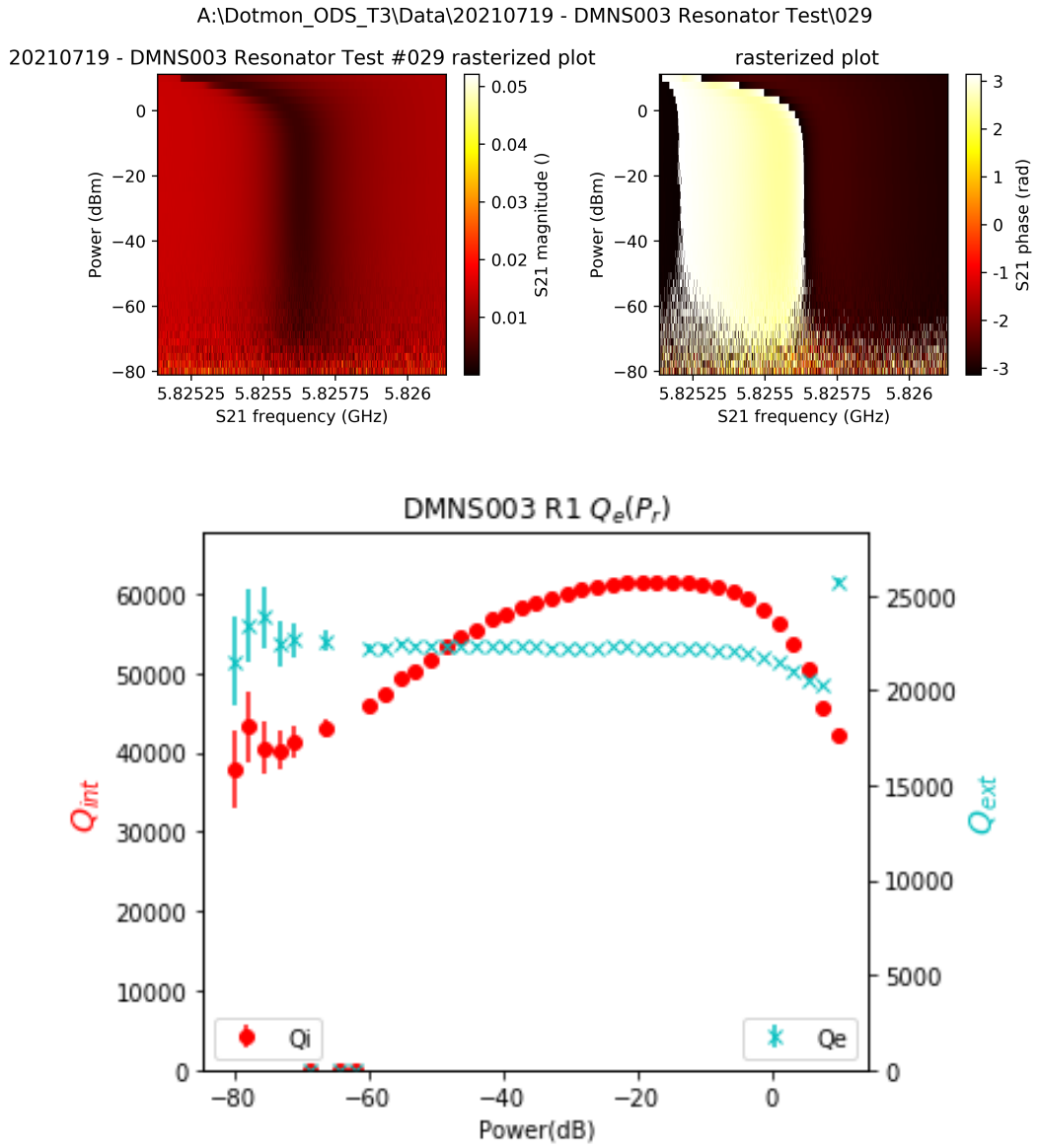

Figure 4.24: Power scan and fitted Q as a function of power for DMNS003 R1, R1 has no crossovers. This resonator has the same design as the M19 R4 resonator, and the M11 qubit resonators. We see an internal quality factor in the range of 40-60k, and an external quality factor of 22k, consistent with the data from the previous chips. The power scan shows the unexpected resonator push at high powers, from 10dBm to -5dbm approximatley. We currently have no explanation for this push, there are no intended non-linearities coupled to this resonator

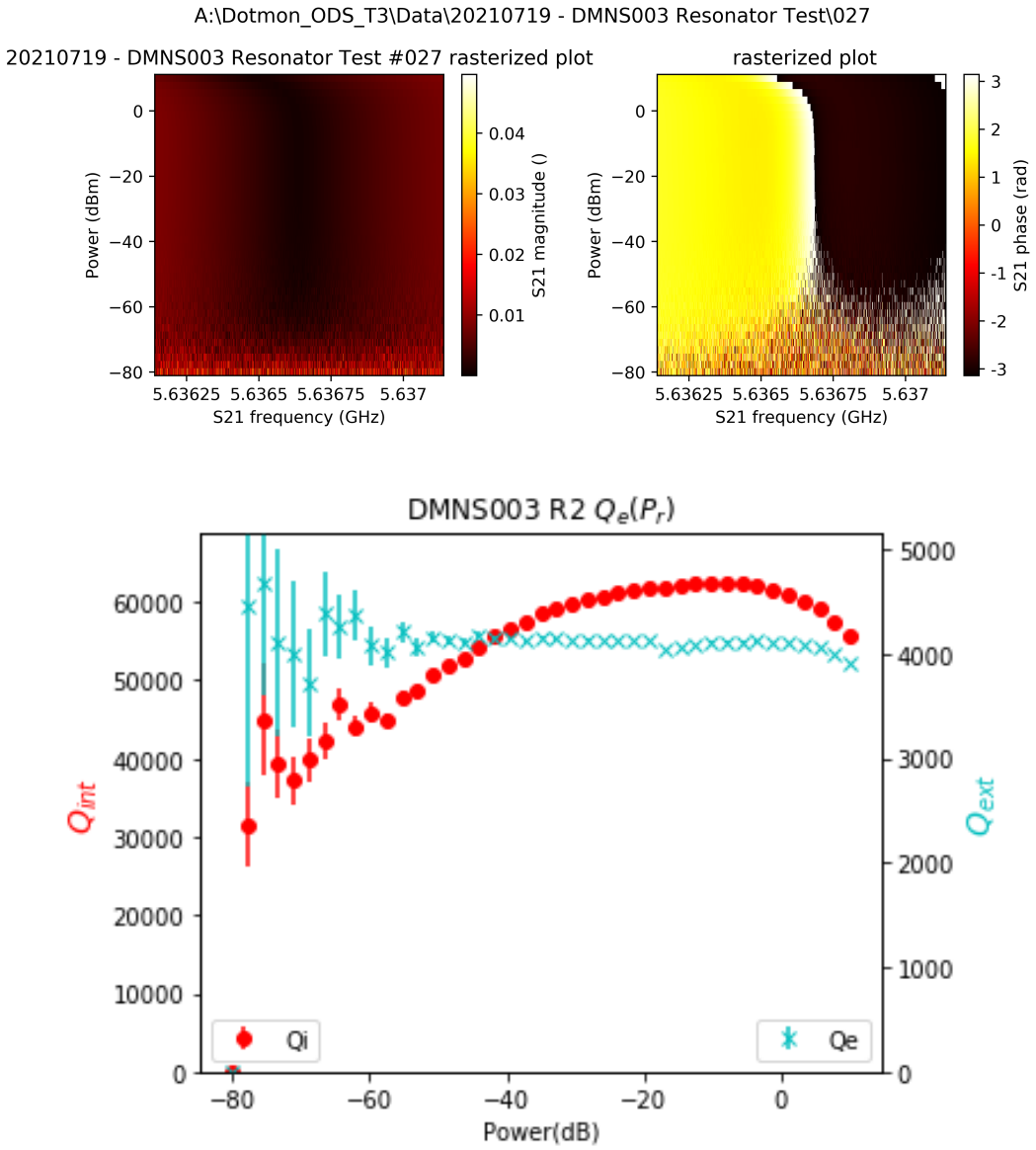

Figure 4.25: Power scan and fitted Q as a function of power for DMNS003 R2, R2 has no crossovers. Q_i is in the range 40-60k, Q_e is approximately 4K. We also see the unexplained high power push on this resonator.

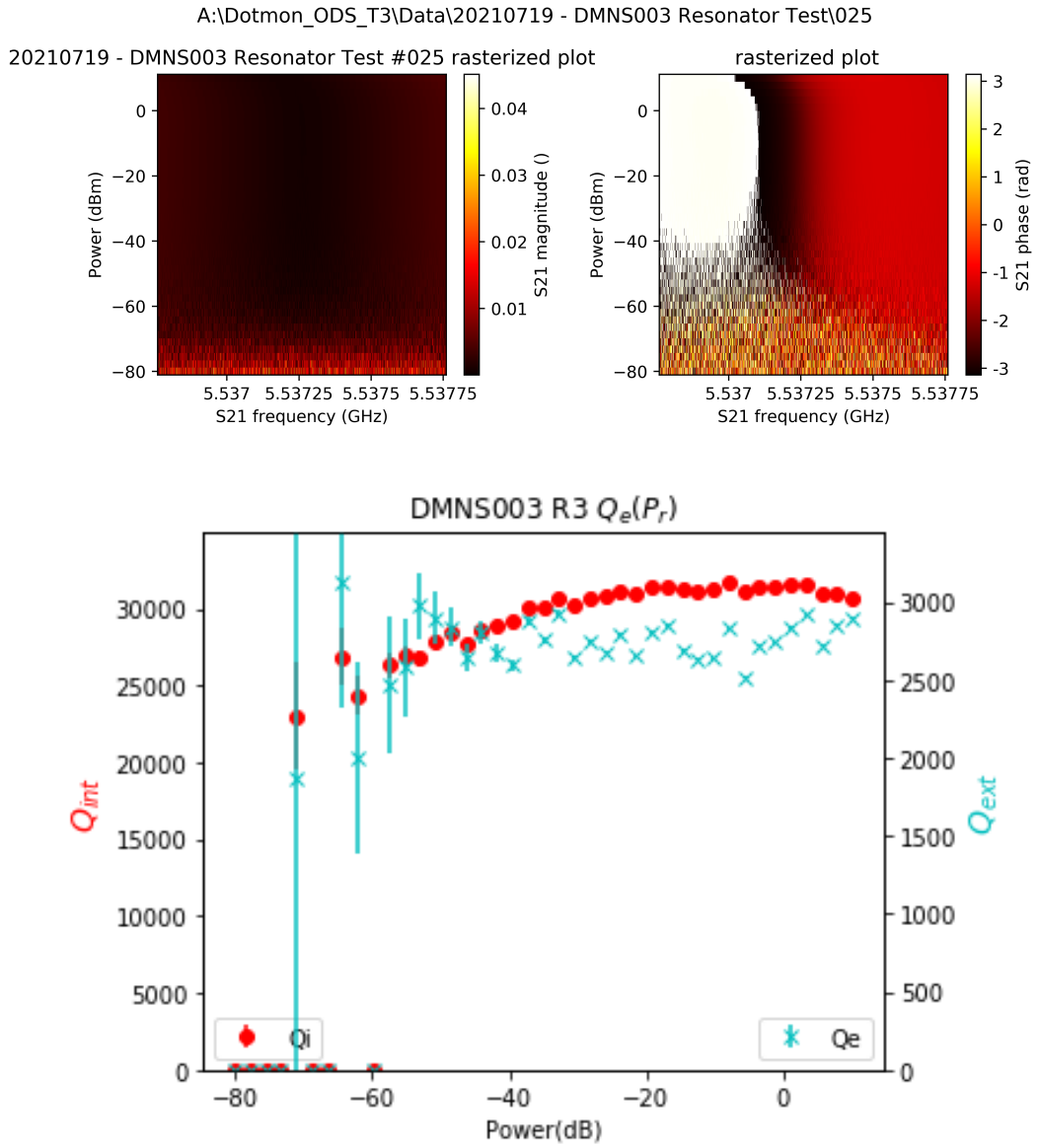

Figure 4.26: Power scan and fitted Q as a function of power for DMNS003 R3, R3 has no crossovers. Q_i is in the the range 25-30K, Q_e is approximately 2.7K. An interesting thing to note is the reduced Q_i compared to R1 and R2, suggesting that the distance to the feedline has an impact on Q_i. Q_e is also less stable as a function of power compared to R1 and R2, however Q_e is in the desired range for our qubit chips.

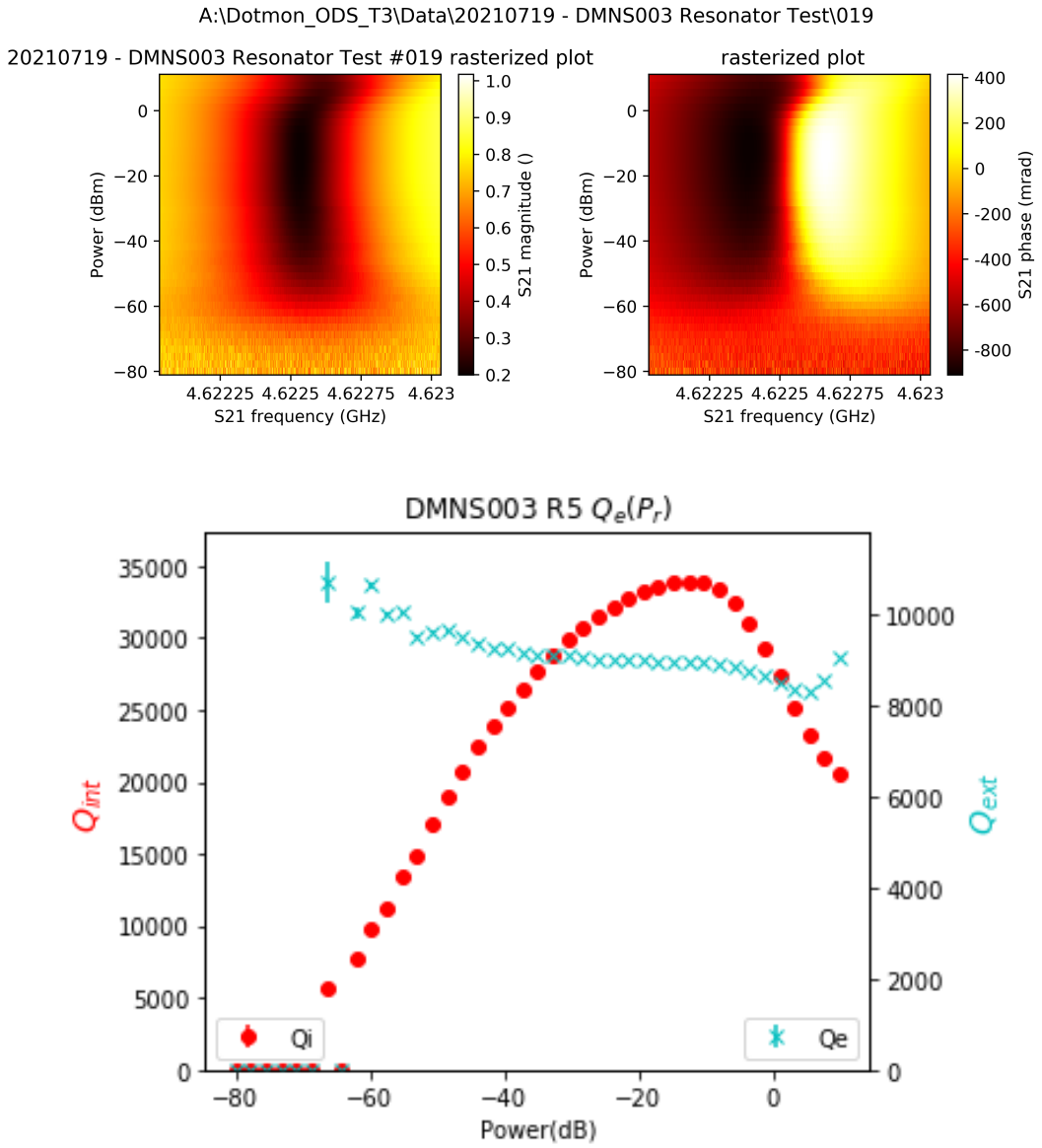

Figure 4.27: Power scan and fitted Q as a function of power for DMNS003 R5, R5 has crossovers.Q_i is in the range 5-35K, Q_e is approximately 8-10K. The power scan also shows the unexplained push at high powers. The range of both Q_i and Q_e is clearly larger than R1, R2 and R3, causing concerns to the stability of the system with crossovers. Q_i is also markedly lower than this resonators non-crossover counterpart, R2. Q_e is markedly higher for this resonator compared to R2-

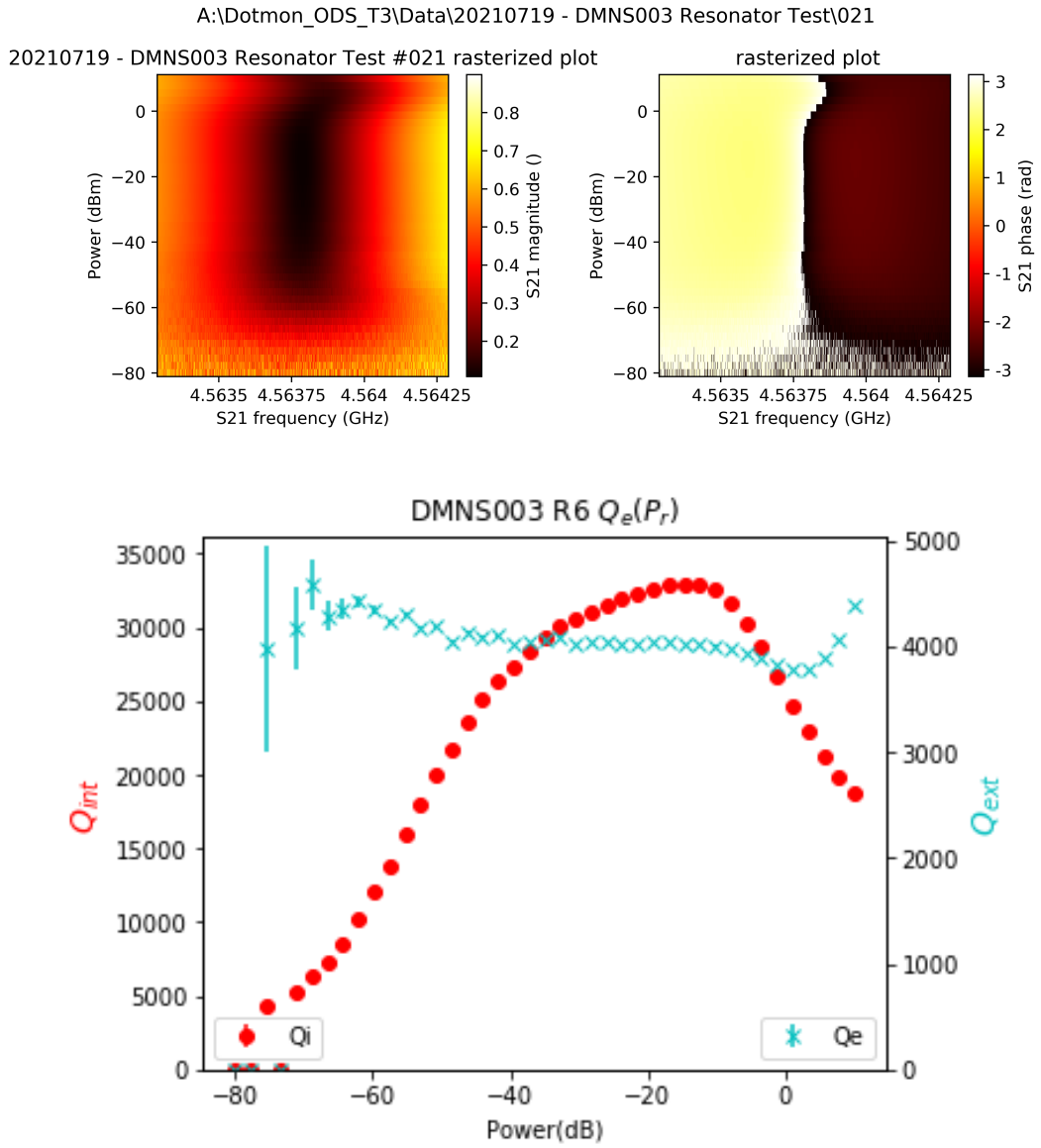

Figure 4.28: Power scan and fitted Q as a function of power for DMNS003 R6, R6 has crossovers. Q_i is in the range 5-32k, Q_e is approximately 4k. We also see the unexplained resonator push at high powers. The range of Q_i as a function of power compared to R3 is concerning, however Q_i for R6 is comparable to R3.

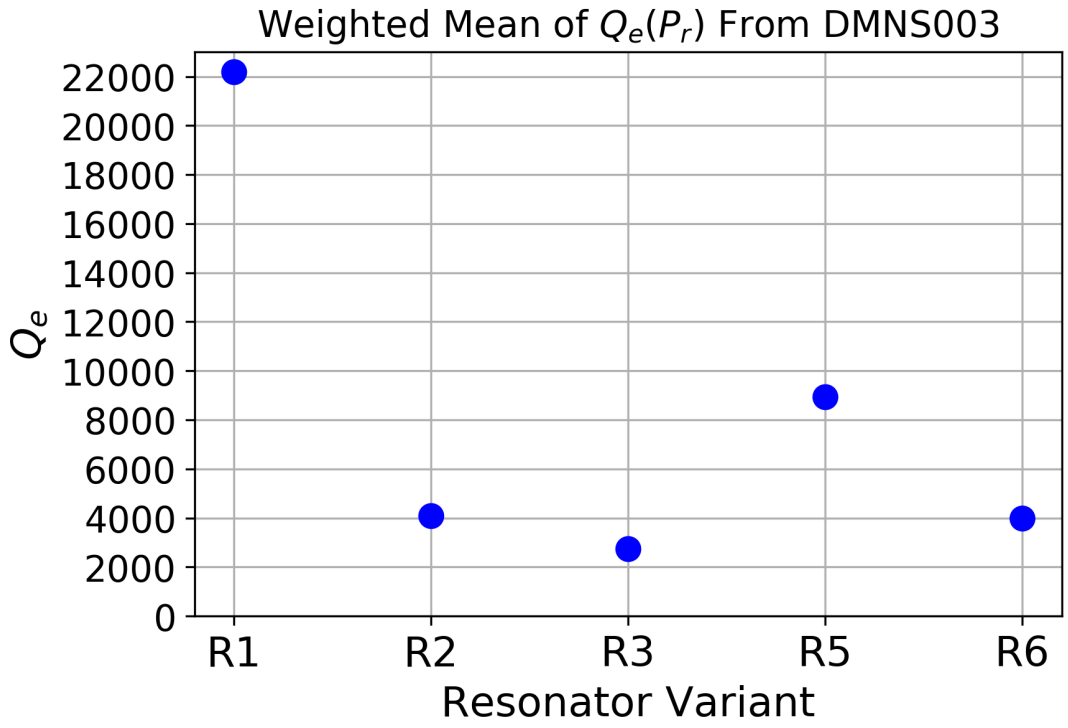

Figure 4.29: Mean of Qe of all resonators on DMNS003

The weighted mean of Q_e as a function of readout power P_r has been calculated for each resonator, and is shown in figure 4.29. The plot has errorbars, but they are too small to be seen on a relevant axis. From this data, it is clear to see the decreasing trend of Q_e as a function of the coupling piece length, and the distance to the feedline. It is also clear that R1 replicates the Q values from both the M19 resonator chip and M11 qubit chip. It is interesting to not that the resonators with crossovers, R5 and R6, have a higher Q_e than the resonators without (R1, R2 and R3). We were originally aiming for a Q_e in the range of $2-4k$, which has been achieved by both R3 and R6. It was therefore decided to use the resonator design from R3 for the coming qubit chip, the M15 chip. Since crossovers would not be included, we expect the M15 resonators to have approximately the same characteristics as R3. The qubit coupling to the resonator does modify the system, and we can therefore not expect an exact replication of R3 properties on the qubit chip

4.4.5 Part-Conclusion on Resonator Experiments

This concludes the resonator experiments in this thesis. During the fabrication of the resonator chips, we discovered that the fabrication procedure previously used for the control layer step was not usable anymore, and had to be revised. The recipe was tweaked for both M19 and DMNS003, and proved to work for each sample. Issues with bonding and the measurement setup resulted in only one useful dataset from the M19 sample, allowing us to fit the M19 R4 resonator that replicated the resonators on the M11 qubit. We saw similar Q values for this resonator, even when not coupled to a qubit. DMNS003 allowed us to study the effect of crossovers on cQED systems like our resonators and feedlines. It also gave us information on how design parameters of the resonator, the distance to the feedline and the length of the coupling piece of the resonator, affect the Q values of the resonators. We could controllably go from $Q_e \approx 22k$ to $Q_e \approx 2.5k$ by extending the coupling piece of the resonator from 240 μm to 640 μm and reducing the distance to the feedline from $5\mu m$ to $3\mu m$. The addition of crossovers to the feedline had no marked effect on the overall transmission through the sample, however it is unclear if it benefits time domain and spectroscopy measurements. The addition of crossovers to the resonator decreased the resonance frequency of the resonator by

approximately 1GHz, and seemingly increased the Q_e of the resonators compared to similar resonators with no crossovers.

CHAPTER 5

Qubit Devices

5.1 Circuit Quantum Electrodynamics

Circuit Quantum Electrodynamics (cQED) is the solid-state electrical version of Cavity Quantum Electrodynamics. Cavity QED describes the science of coupling atoms to photons, quantized modes of light. It is possible to couple coherent photons to the atomic levels of an atom placed in a cavity, exploring fundamental quantum mechanics. Circuit QED is the electrical version of this, using superconducting coplanar waveguides instead of cavities, and qubits instead of atoms[20]. Applying microwave AC signals in superconducting transmission lines, we can capture coherent photons in a superconducting resonator and perform Quantum Non-Demolition (QND) measurement on a qubit coupled to the resonator. The specific nature of the couplings is critical to defining the qubit system, and will be explored in detail in the following section.

5.1.1 Dispersive Readout

We use the method of dispersive readout to readout the qubit state[8]. We entagle the qubit with the resonator, and measure the resonator to infer the state of the qubit. When thinking about these systems, it is helpful to think of all elements as some kind of LC oscillator. The interaction between the qubit and the resonator is described by the Jaynes-Cummings hamiltonian:

$$H_{JC} = \omega_r(a^\dagger a + \frac{1}{2}) + \frac{\omega_q}{2}\sigma_z + g(\sigma_+ a + \sigma_- a^\dagger) \tag{5.1}$$

ω_r is the resonator frequency, ω_q is the qubit frequency, g is the coupling between the resonator and qubit, σ_+, σ_- is the lowering and raising operators of the qubit, a,$a^\dagger$ is the creation and annihilation operators for photons in the resonator. The dispersive hamiltonian is a specific case of this hamiltonian, defined from the relationship between some of the defining variables. The detuning (difference) between the resonator and qubit frequency is an important parameter, defined here as $\Delta = |\omega_q - \omega_r|$ (not to be confused with the superconducting gap, also denoted by an uppercase delta). The dispersive limit is defined when the detuning is much larger than the resonator linewidth (κ) and the coupling between the qubit and resonator g: $\Delta >> g,\kappa$. When we operate in the dispersive regime, there is no direct energy exchange between the qubit and resonator; instead the qubit and resonator push on each others frequencies. This can be used for a Quantum Non Demolition (QND) measurement.

If we take the limit of a few photons in the resonator, and a two-level qubit system, we can approximate a hamiltonian that illuminates this pushing effect. The dispersive hamiltonian is as follows:

$$H_{disp} = (\omega_r + \chi\sigma_z)(a^\dagger a + \frac{1}{2}) + \frac{\omega_q + g^2/\Delta}{2}\sigma_z \tag{5.2}$$

This is very illuminating, we see that the resonator frequency is shifted by a value $\chi = g^2/\Delta$ called the dispersive shift. The shift is dependent on the qubit state σ_z, allowing us to infer the qubit state by measuring the resonator. The qubit frequency is also modified by the Lamb shift, g^2/Δ, caused by vacuum fluctuations in the resonator.

Another important aspect of this system is the critical photon number n_c [8].

$$n = a^\dagger a,\ n_c \equiv \frac{\Delta^2}{4g^2} \tag{5.3}$$

If too many photons are present in the resonator, the dispersive hamiltonian is no longer valid. If we measure near the resonator frequency at this point, we will only see the bare resonator frequency.

The critical photon number corresponds directly to a specific power of the readout signal P_r, we therefore need to readout below this power when performing qubit measurements . The critical photon number and the dispersive shift can both be measured directly in a power scan of the resonator: We sweep the readout signal frequency near the resonator frequency, for a large range of readout powers. At high power (technically a relative term, but usually anything above 40dBm) we measure the bare resonator frequency. If we lower the readout power, we will see tge resonator "washes out" just before hitting the critical photon number. Lowring the power further, the resonator reappears below the critical photon number, now with the dispersive shift to the resonator frequency. Not only can we measure the dispersive shift from this, and calculate either the detuning or qubit coupling, we can also quickly confirm the presence of a qubit. This type of measurement has been done with a Vector Network Analyzer (VNA) for the purpose of this thesis, details of the measurement setup can be found in section 2.3.1. It is an amazing tool that takes care of all the complicated I-Q mixing and demodulation, whilst being fast and easy to use.

5.2 The M15 Qubit Chip

5.2.1 Design and Fabrication

The M15 qubit chip was designed with one main experiment in mind: The quenching of charge dispersion of a Gatemon from resonant tunneling through a quantum dot in the Josephson junction. For this purpose a Dotmon was designed to allow for in-situ switching between transport measurement and cQED measurements. This will also allow us to correlate dot resonances seen in transport with an enhanced qubit frequency in spectroscopy, and ideally also charge dispersion quenching.

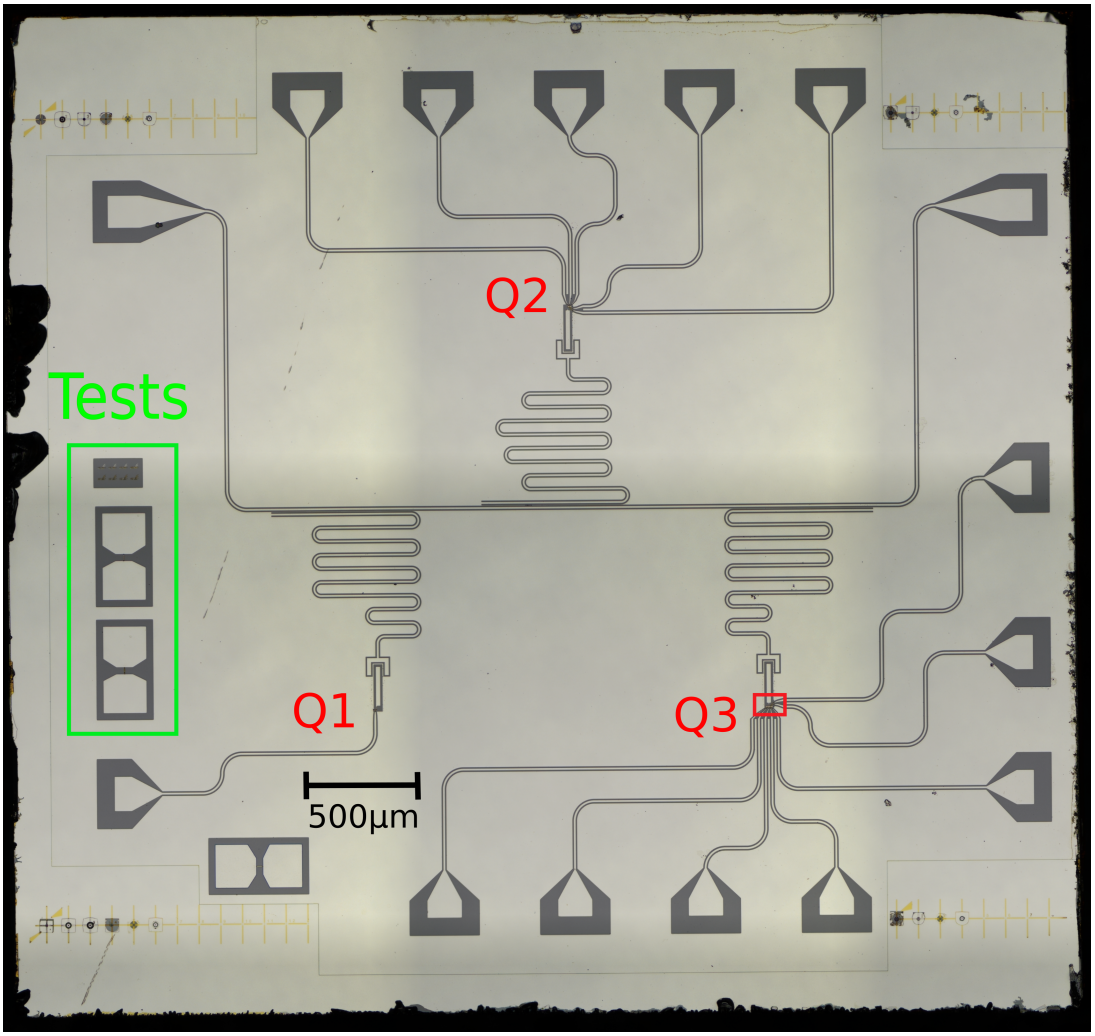

Figure 5.1: Overview of the finished M15 qubit chip, hosting three qubits and test structures. The test structures are marked with a green square, the qubits are labelled with red lettering, and the qubit island of Q3 is shown with a red square. The three qubits are coupled to the same feedline, through resonators with different resonance frequencies. Gate and transport lines extend to bondpads at the edge of the chip, from each quibt. Q1 only has one line for the topgate of the junction, Q2 has lines for the dot-forming gates and Q3 has lines for the dot-forming gates, the FET gate and the transport bias. The chip has dimensions of 4.6mm X 4.9mm.

An overview of the finished M15 chip is shown in Figure 5.1, the three different qubits on the chip are labeled Q1 for the simple gatemon, Q2 for the dotmon without transport leads and Q3 for the dotmon with transport leads. The test structures used for SEM images are also marked. The Q3 system is shown in figure 5.2, showing the feedline, resonator, shunt capacitor

and qubit island of Q3. I have highlighted where attributess of the system are represented physically on the chip: The Josephson energy E_j is associated with the qubit island hosting the Josephson junction, the capacitative energy E_c is associated with the shunt capacitor, and determined by the area of the capacitor. The qubit-resonator coupling g is determined by the geometry of the shunt capacitor and resonator coupling fork. The linewidth of the resonator κ and external quality factor Q_e is associated with the geometry near the feedline and resonator.

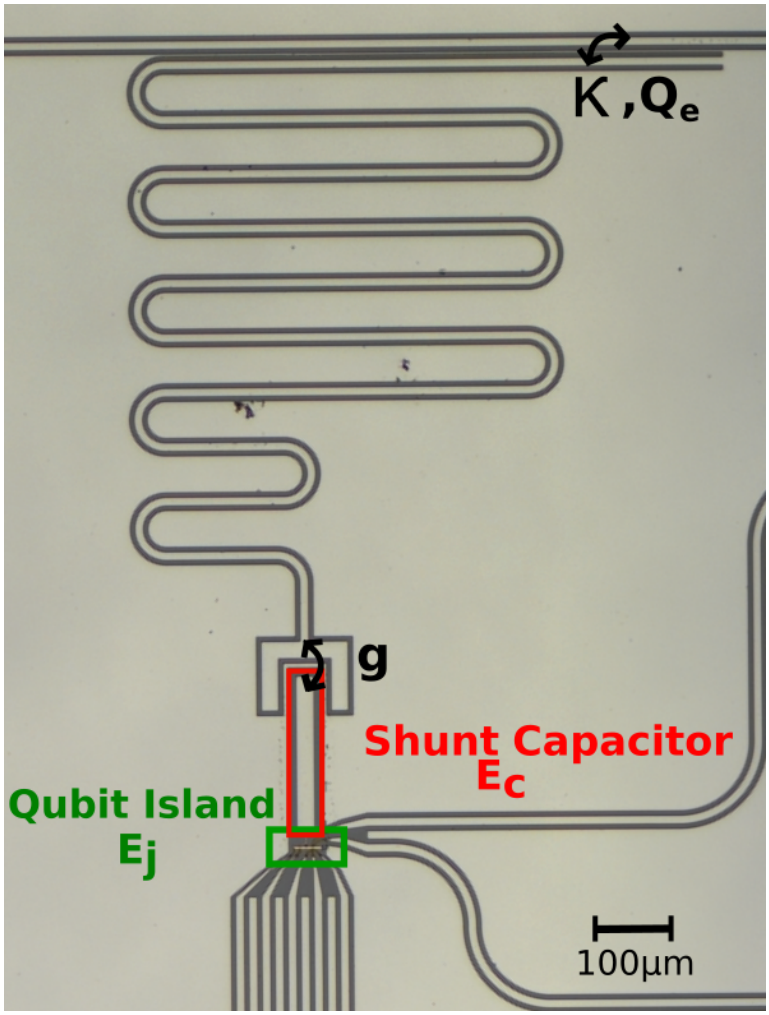

Figure 5.2: Image of Q3 with qubit island, Shunt Capacitor, resonator and feedline visible. I have marked the physical locations associated with attributes of the qubit system, the resonator linewidth κ and external quality factor Q_e, the qubit-resonator coupling g, the capacitative energy E_c and the inductive Josephson energy E_j. E_c was designed to be 500MHz, determined using an electrostatic simulation.

E_c was designed to be $500MHz$, using electrostatic COMSOL simulations for estimation. We expect to be able to tune I_c in the range 10nA-100nA, which should result in an E_j range of 5GHz-50Ghz, resulting in an E_j/E_c ratio of 5-50. Having a high E_j/E_c ratio will put our qubit in the transmon regime, having a low E_j/E_c ratio will allow us to measure the quenching of charge dispersion associated with resonant tunneling through the quantum dot.

Figure 5.3 shows an overview of the 2DEG mesa with a zoom in of the dot-forming Josephson junction. The mesa is $4\mu m$ wide and $35\mu m$ long. The mesa hosts two Josephson junctions: One for forming the dot (the dot junction) and one for switching between cQED and transport measurements (the FET junction, see figure 5.9 for a current bias measurement of the FET junction). The mesa is connected by electrical contact to the shunt capacitor between the two junctions. On the right side of the dot junction, the mesa is connected to the

ground plane, and on the left side of the FET junction, the bias line is connected by electrical contact to the mesa. The FET junction is 150nm long (measured from the left to the right superconductor) and the dot junction is 440nm long at the shortes point and 3.8μm long at the widest point. The dot junction fans out in the bottom along with the plunger and QPC gates. This design was chosen based on previously measured transport devices, it helps to deplete the semiconductor in the bottom half of the junction, ensuring transport occurs through the intended dot region at low gate voltages. Optical and SEM images of the device is shown in figure 5.4

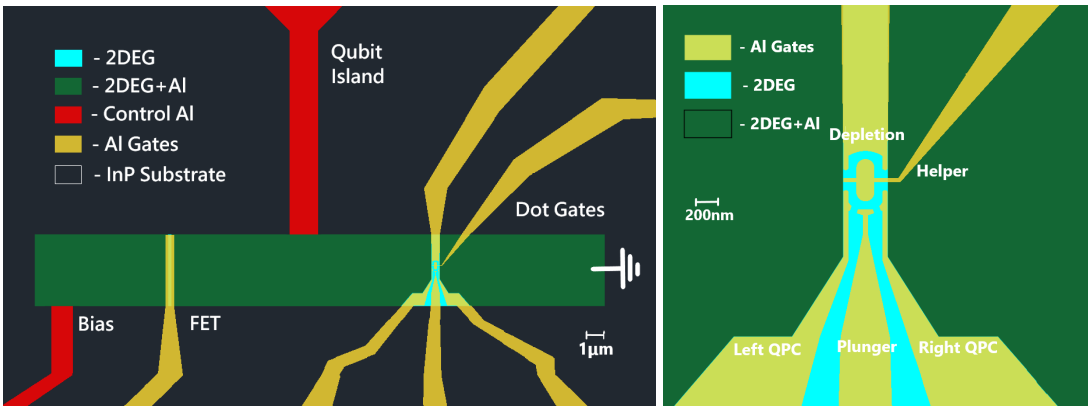

Figure 5.3: Design of the dotmon qubit, the entire qubit island shown to the left, with a zoom-in on the dot junction to the right. The green parts is the 2DEG mesa covered with epitaxial aluminium, the gold is the gates and the blue is the etched Josephson junction (only 2DEG). The FET junction is 150nm long, the dot junction is 440nm long in the dot-forming region. The QPC distance (between the fingers of the QPC) is 200nm

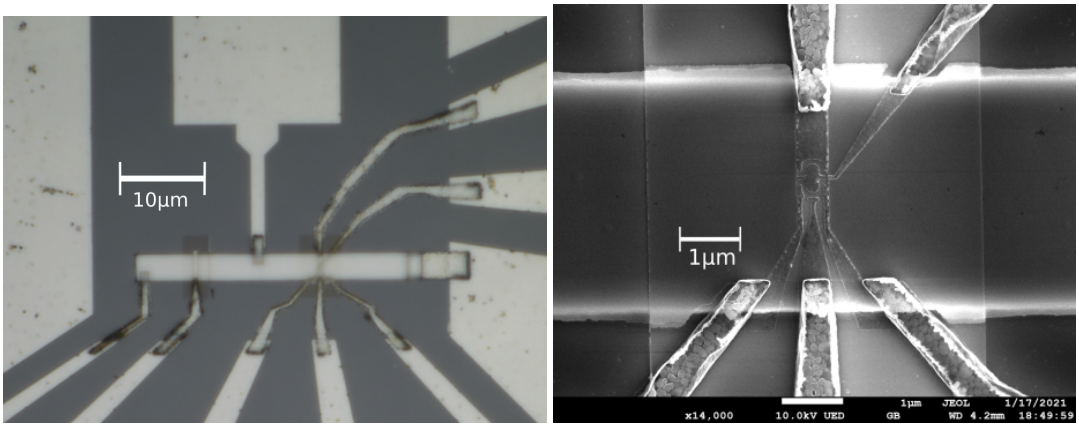

Figure 5.4: Optical image (left) of Q3, showing the qubit island. The 2DEG mesa and qubit shunt capacitor is visible, and the FET and dot junctions are also visible. SEM image (right) of a test device with the same geometry as Q3. The SEM can damage the 2DEG, and it is therefore not advised to take SEM images of the actual qubit mesa before measuring. The dot junction is clearly shown, with all the dot forming gates clearly visible

The device can be operated in two modes, transport and cQED, defined by the FET gate. If the FET junction is open, at 0 or positive gate voltages, it is possible to apply a bias current or voltage through the bias line (see section 2.3.2 for the transport setup). The junction with the lowest resistance defines the properties of a multi-junction mesa, we therefore need to ensure that the resistance of the dot junction is larger than the FET junction when performing transport measurements. This is usually trivial, since we apply negative gate voltages on the dot-gates to shape the potential. If the FET gate is at 0 or positive voltages, the resistance will

be smaller in the FET than the dot junction (based on previously measured transport devices). To switch to cQED measurements, we pinch-off the FET junction with the FET gate. Then the mesa is closed to the left, and RF measurements can be made using the feedline-resonator system coupled to the qubit island through the shunt capacitor. For detail on exactly how the depletion of the FET junction affects cQED measurements, see chapter 6 of Anders Kringhøjs PhD thesis[10], see figure 5.5 to see the effect of the FET on the DC I-V curves of our device . This measurement configuration was also used for his similar nanowire experiment. All cQED measurements presented in this thesis are done with the FET junction thoroughly closed, at a minimum of -1.4V on the FET gate. In this configuration , we measure 0 differential voltage on the lockin, and 0 DC current through the junction. All transport measurements are performed with the FET at 0V (grounded).

All measurements presented in this chapter are performed at the base temperature of the dilution refrigerator, ranging from 50mK-70mK during this project.

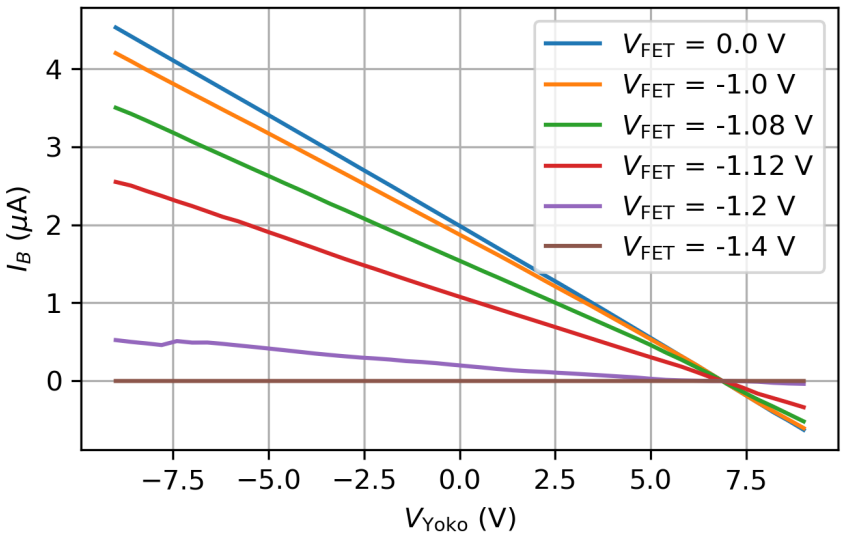

Figure 5.5: I-V curves for different FET voltages, going from entirely open (0V) to closed (-1.4V). V_{yoko} is the applied DC voltage from the yokogawa DC source.

The role of the dot forming gates is as follows: The depletion gates and the right and Left QPC gates form the quantum dot by creating two quantum point contacts in the tunneling regime. The QPC gates then tune the tunneling rates on and off the dot, Γ_1, Γ_2, see figure 1.3. The plunger gate controls the energy of the dot level ε_r once formed, like a textbook quantum dot (i.e. the one described in Ihn[23]). The helper gate is an ad-hoc addition to the system based on previous test devices. The exact effect of the helper gate on the electrostatic potential is unknown, but it helps form the quantum dot (thereby the name). textbook Coulomb diamonds could only be seen when the helper was tuned to -0.6V on our previous transport devices. This gate setup should allow for individual control of the tunneling rates on and off the dot, and the resonant level of the dot. The tunnel barriers need to be balanced for the quenching of charge dispersion[16].

5.2.2 Transport Measurements

The effect of each gate on the measured bias current is shown in figure 5.6. This data helps build an intuition on the "strength" of each gate. The QPC gates are here called "cutters". The sweeps were taken independently, with all other gates grounded. The drop in current is

associated with the local depletion of each gate. Since a current path will always be available for transport when only one gate is used, we can not pinch off the junction with a single gate. The helper gate is shown to have the least effect, intuitively making sense since it is the smallest gate (both in area and in length of covered junction). The depletion gate is next-weakest, which might be surprising, but i have an explanation. The depletion gate covers the entire length of the junction (from S to S), but it does not cover much of the width of the junction (approx 1/3). The "gate strength" shown here is predominantly proportional to how much junction width the gate covers. Both the QPC gates cover the most width and length of the junction, and therefore are the "strongest". The takeaway is that all the gates seem to work as expected.

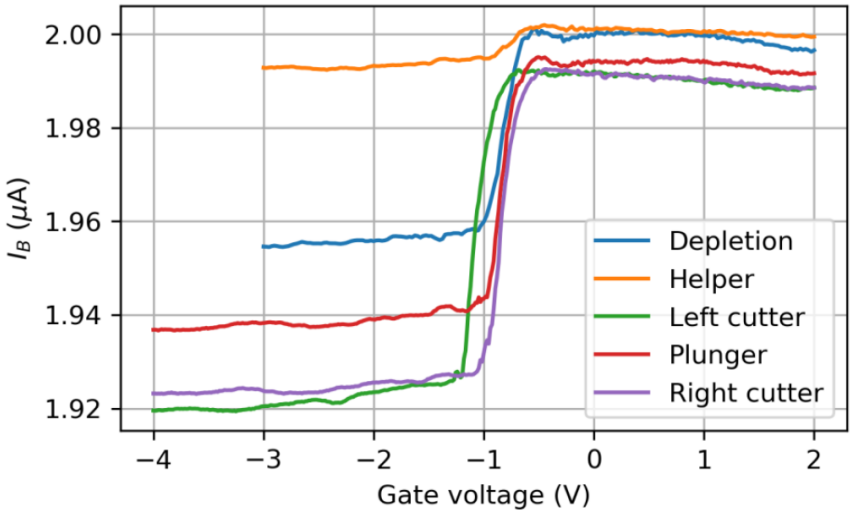

Figure 5.6: Measured bias current as a function of gate voltage on each of the dot-forming gates. Measurements taken with the FET junction open, at $V_{FET} = 0V$

Having established that the FET gate can open and close the FET junction, and that all gates work as expected, we move on to more interesting measurements. Knowing how the critical current of the dot junction is affected by specific gate configurations is critical for more advanced tuning of the system.

We start by making a current bias measurement, measuring the differential resistance as a function of applied current bias, as a function of gate voltage. We start with using all the gates of the dot juntion, except the helper gate. The data is shown in figure 5.7. The applied bias ranges from -50nA to 50nA, the gates are swept from 0V to -4V, since we know the gates do not leak in this range. From $V_g = 0V$ to $V_g = -1.25V$, the switching current (the experimentally measured critical current) is larger than the maximum applied bias, we therefore measure 0 resistance differential in this range of bias and gate. From $V_g = -1.25V$ to $V_g = -1.75V$ we measure a switching current going from 50nA to 10nA, the zero resistance supercurrent is still well defined in this range. From $V_g = -1.75V$ to $V_g = -4V$, we enter a regime we call the "resistive" or "dotty" regime. In this regime, the 0 resistance supercurrent is not well defined, and a small differential resistance is measured from bias close to 0nA. "dot resonances" also seem to open and close as a function of gate, with a large resonance especially notable at $V_g \approx -3.75V$ deep in the resistive regime. We now know that we can controllably go from a junction with a high critical current, to a low critical current, and enter a "resisitve" and "dotty" regime. We wanted a larger bias range, and a better resolution for our next current bias measurement, and we also wanted to test if we could tune the critical current similarly with only QPC pairs. This measurement is shown in figure 5.8

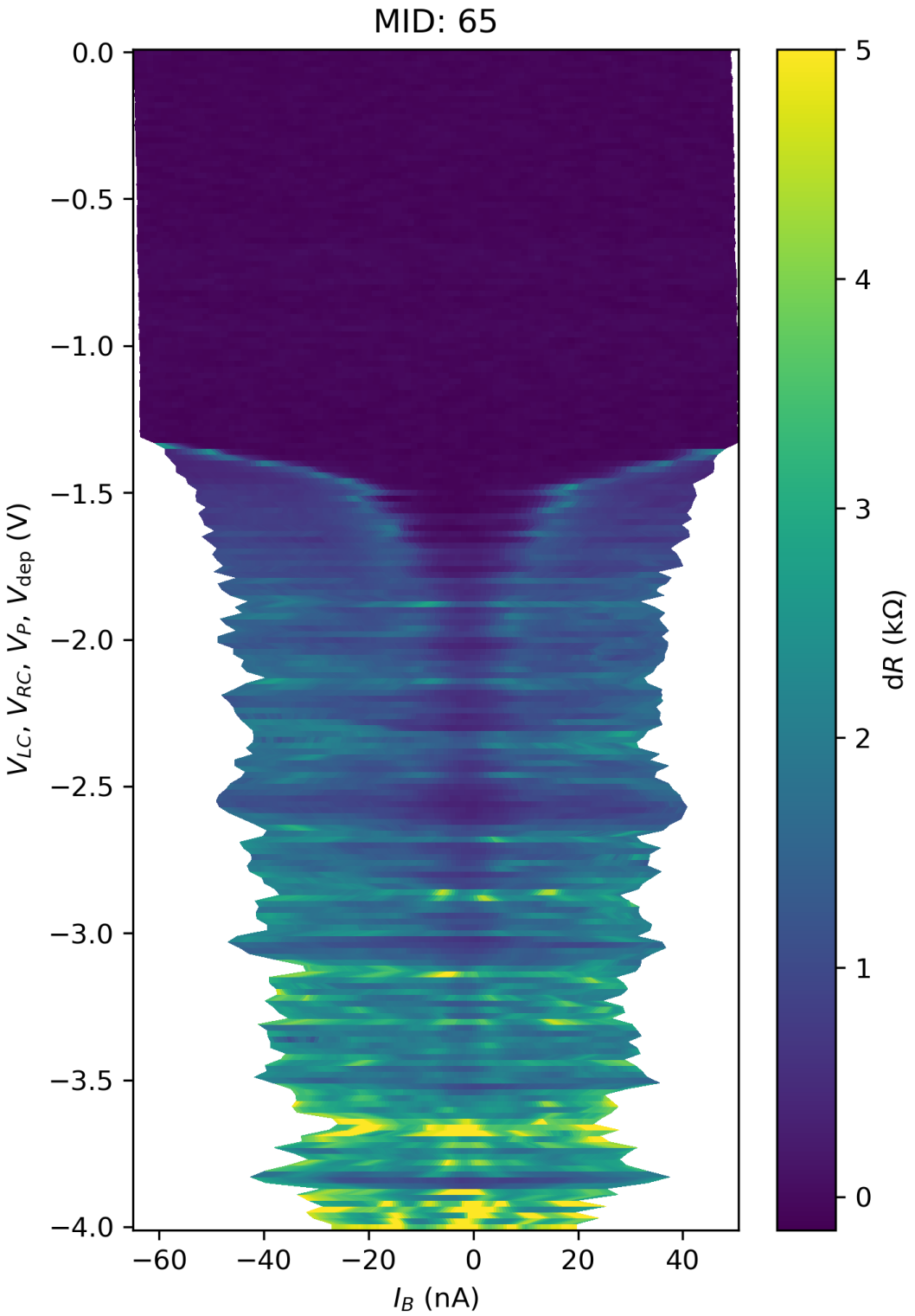

Figure 5.7: Current bias measurement of M15 Q3 showing the differential resistance of the dot-junction as a function of bias current and gate voltage. The gates used are the "Transmission gates", both QPC's, the depletion and the plunger gate. Helper gate is at -0.6V, baseline determined from previous experiment, not necesarrily best value for this experiment. I_c varies from 100nA to 10nA in this gate range, suitable for qubit operations. Measurements taken with the FET junction open, at $V_{FET} = 0V$

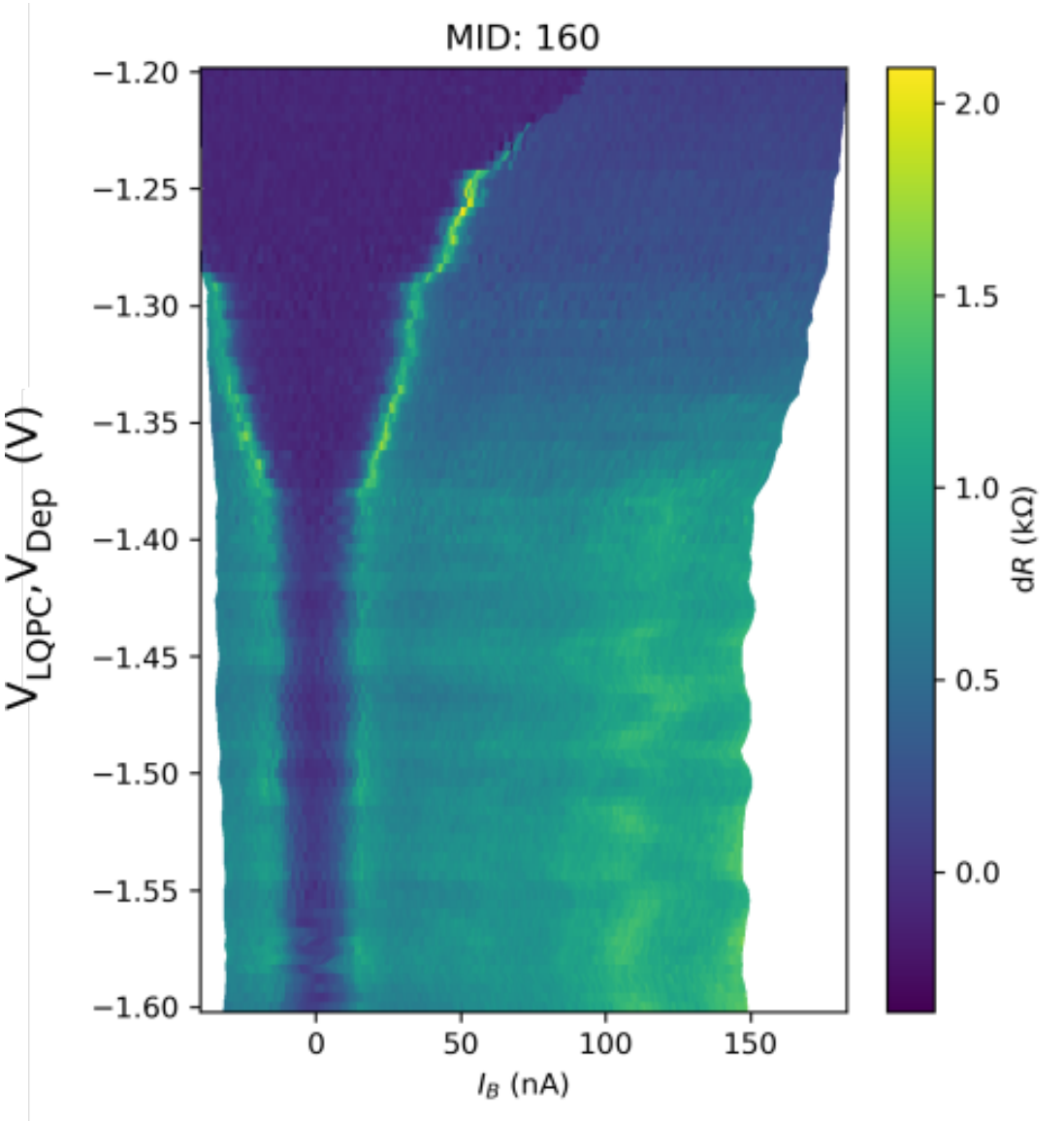

Figure 5.8: Current bias measurement of M15 Q3 showing the differential resistance of the dot-junction as a function of bias current and gate voltage. The gates used are the left QPC and depletion gate. Helper gate is at -0.6V.. I_c varies from 100nA to 10nA in this gate range, suitable for qubit operations. Measurements taken with the FET junction open, at $V_{FET} = 0V$

We should be able to go from an open to pinched-off junction with either set of QPC gates, the Depletion gate + the left QPC gate and the Depletion gate + the right QPC gate. MID 160 shows the left QPC + the depletion gate, near the closing of the well defined critical current, and moving into the "dotty/resonant" regime. This data shows the switching current narrowing from 100nA to 10nA (the actual critical current is usually larger than the switching current, see chapter 6 of Anders Kringhøj's PhD[10]). This marks the regime needed for qubit operation frequencies in the 1-10GHz range. Features associated with multiple Andreev reflection are present as a consistent "rippling" in the resistive regime of the bias scan (after exceeding I_c), and the differential resistance increases from roughly $0.5k\Omega$ to $1.5k\Omega$ at high bias in the restive regime (100nA and above).

The bias axis changes as a function of gate because the junction becomes more resistive: the constant bias voltage applied results in a smaller bias current, see section 2.3.2 for an explanation of the measurement setup. The reduction of the critical current as a function of gate follows expectations from previous measurements of transport chips made in preparation

of the dotmon qubit (see figure 5.9). The critical current not going to 0 at lower gate voltages was not expected. The supercurrent also behaves strangely at low gate voltages, the differential resistance at 0 bias is not quite 0, but very close. The gates also seems to induces dot-like resonances in the critical current, that in this case would be accidental. This could also be caused by the current bias becoming less reliable as the resistance of the dot junction increases, and gets closer to the line resistance.

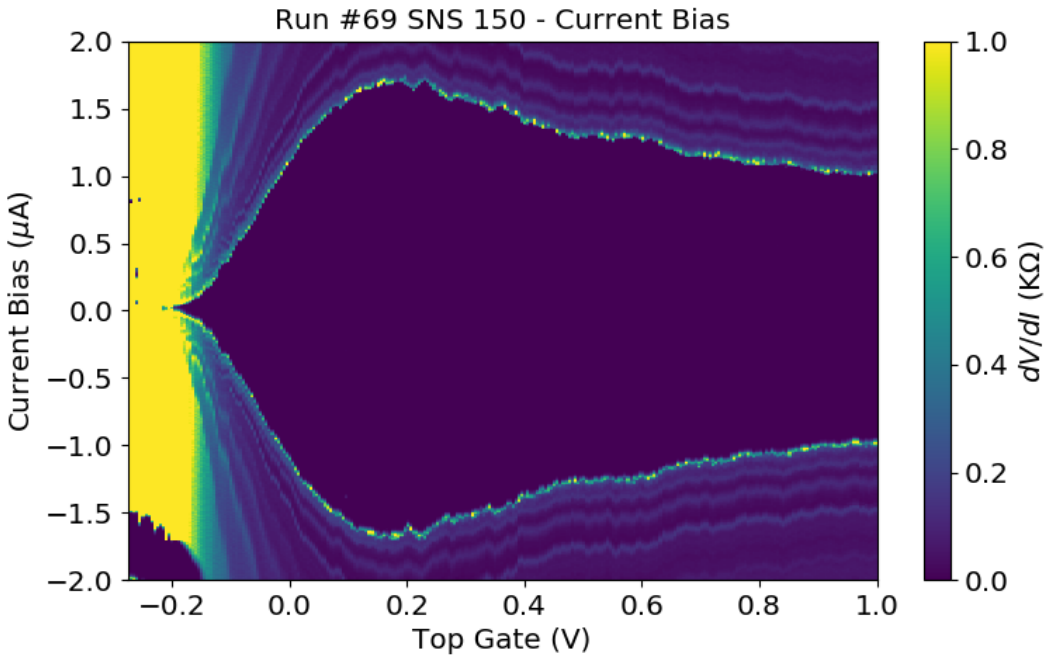

Figure 5.9: Current bias measurement of 150nm long SNS junction from transport chip made in preparation of the dotmon qubit chip. The design of this junction corresponds exactly to the dimension of the FET junction and gate. This measurement was done with a 4-terminal setup, and clearly shows the critical current going to 0 at low gate voltages, unlike our dot-junction. The enhancement of the critical current around 0.2V on the top gate is currently unexplained.

5.2.3 cQED Measurements

Now having established the foundational transport properties of the dot and FET junction , we move on to some cQED measurements. We start by closing the FET junction, allowing for cQED measurements. The junction was shown to be closed at $V_{FET} = -1.4V$. The cQED setup is set to the VNA configuration for initial measurements of the resonators, including power dependence and gate dependence of the resonator signal, see figure 2.2 for details.

The full transmission scan through the feedline is shown in figure 5.10. As seen in figure 5.1, the chip hosts 3 qubit devices on a single feedline. The three resonator dips are visible in the range from 5-6GHz, as expected from design and measurements of DMNS003. For this thesis, I am focusing on the Q3 qubit on the chip, the dotmon with transport leads. Q2 is a dotmon without the transport leads, and Q1 is a regular gatemon, with only an FET style gate on a single Josephson Junction. Q3 has a resonance frequency of 5.682GHz, the resonator dip is shown in figure 5.11. A power scan of the Q3 resonator is shown in figure 5.12, along with the calculated Q values. It is worth noting that we see no dispersive shift in the power scan. This is likely caused by a very large detuning Δ. A very large detuning results in a large critical photon number, but also reduces the dispersive shift χ. We can infer the qubit frequency to be much larger than the resonator by the critical current scan from figure 5.8. The gates are at 0V for this measurement, meaning the critical current is likely several hundred nanoamps or even microamps, bringing the qubit frequency way above the resonator of 5.682GHz. The

fitted Q values are in agreement with DMNS003, showing a $Q_e \approx 4K$ and $Q_i \approx 20K$. The internal quality factor is slightly smaller than expected, possibly due to the qubit coupling to the resonator. Figure 5.14 show a power scan of the Q3 resonator at lower gate voltages, where the dispersive shift is clearly seen.

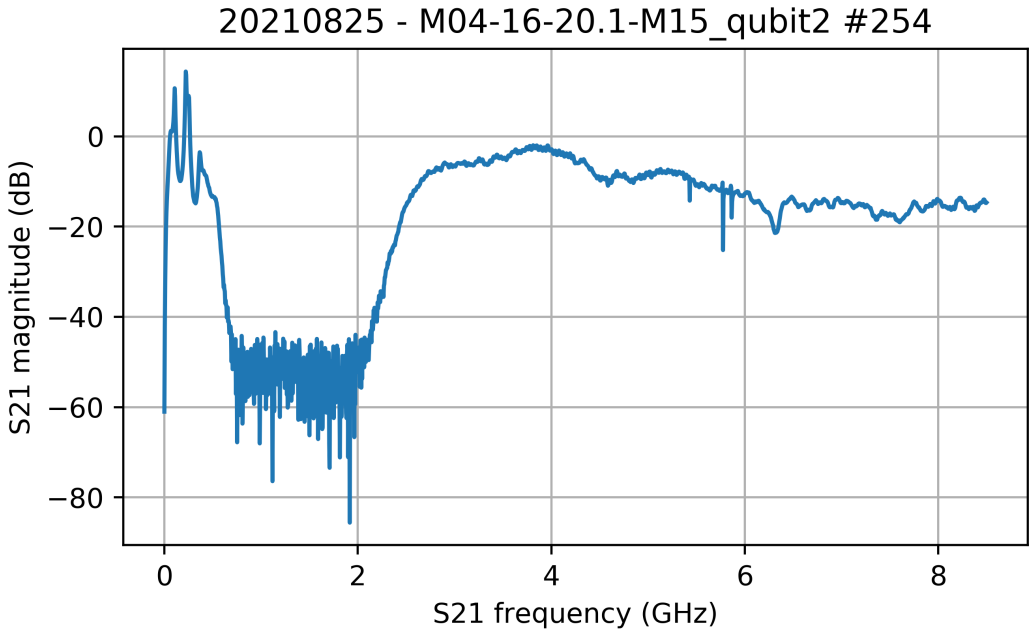

Figure 5.10: Full transmission scan of the M15 qubit chip. The three resonator dips are clearly present in the 5-6GHz frequency range, as expected from design.

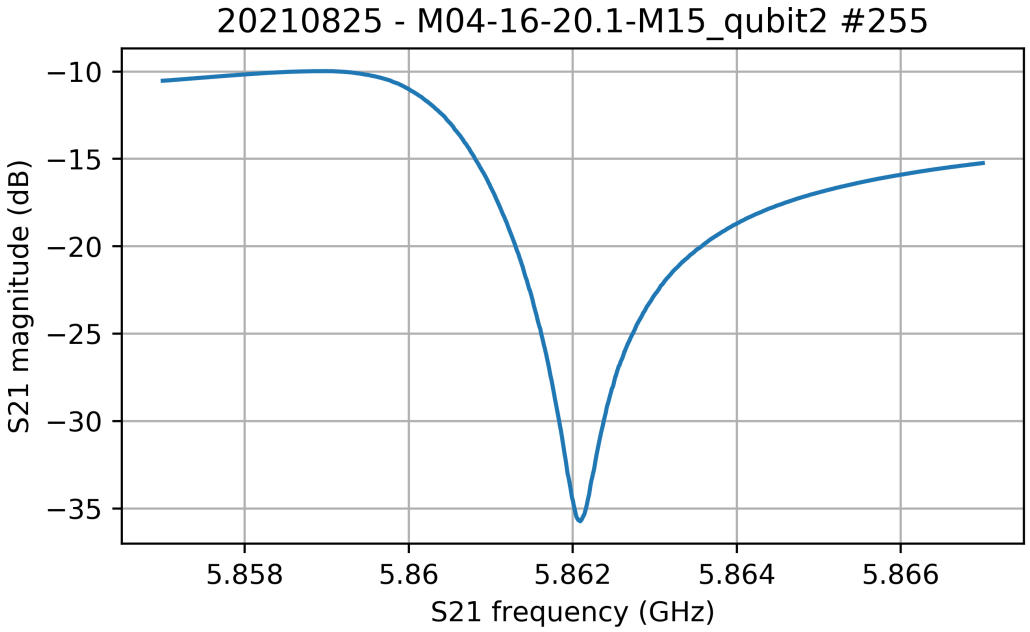

Figure 5.11: Resonator dip of Q3 on the M15 qubit chip. The resoannce frequency of the Q3 resonator is 5.862Ghz, a power scan of the resonator is shown in figure 5.12.

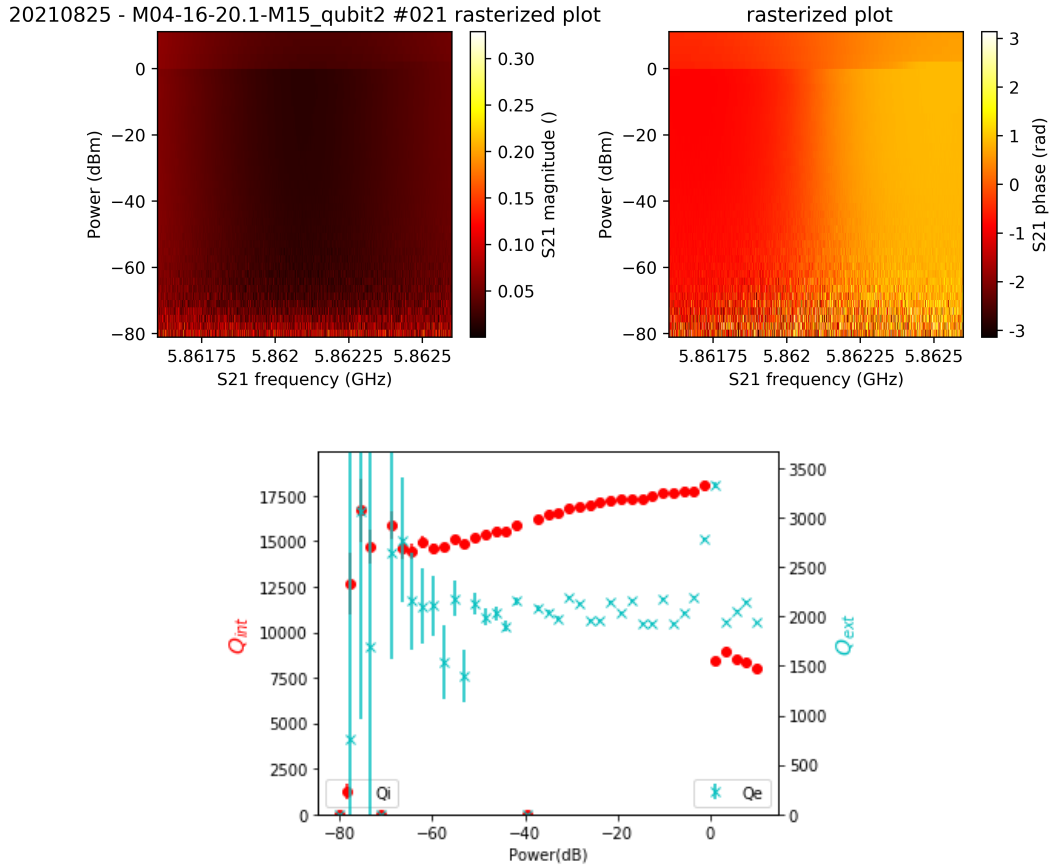

Figure 5.12: Power scan of the Q3 resonator on the M15 qubit chip, with fitted quality factors shown in the bottom plot. Q_e is consistent with measurements of DMNS003, Q_i is reduced compared to the DMNS003 resonators.

We now move on to a cQED measurement not mentioned before in this thesis: The resonator signal as a function of gate voltage. The gates used for this measurement is the gate-grouping named "transmission gates", consisting of all dot gates except the helper gate. This grouping was used since it approximates the gatemon top gate. For this measurement, the helper is set to $V_{help} = -0.6V$, and all other gates are swept from 0V to -4V. The gates effectively control the detuning of the resonator and qubit. They control the critical current, which controls the qubit frequency. When the detuning tends toward 0, the dispersive Hamiltonian is no longer valid, and the resonator signal disappears. This is called the "Avoided crossing", since the resonator signal disappears when the qubit frequency crosses the resonator frequency. The gate voltage brings the qubit from above the resonator to below the resonator, and as shown in figure 5.13, the resonator signal start to warp and disappears from -1.5V to -4V on the transmission gates. Ideally, we would like to see the resonator re-appear at lower gate voltages, as the detuning increases when the qubit goes further below the resonator. This is not seen for this gate configuration, but can be seen in figure 5.14.

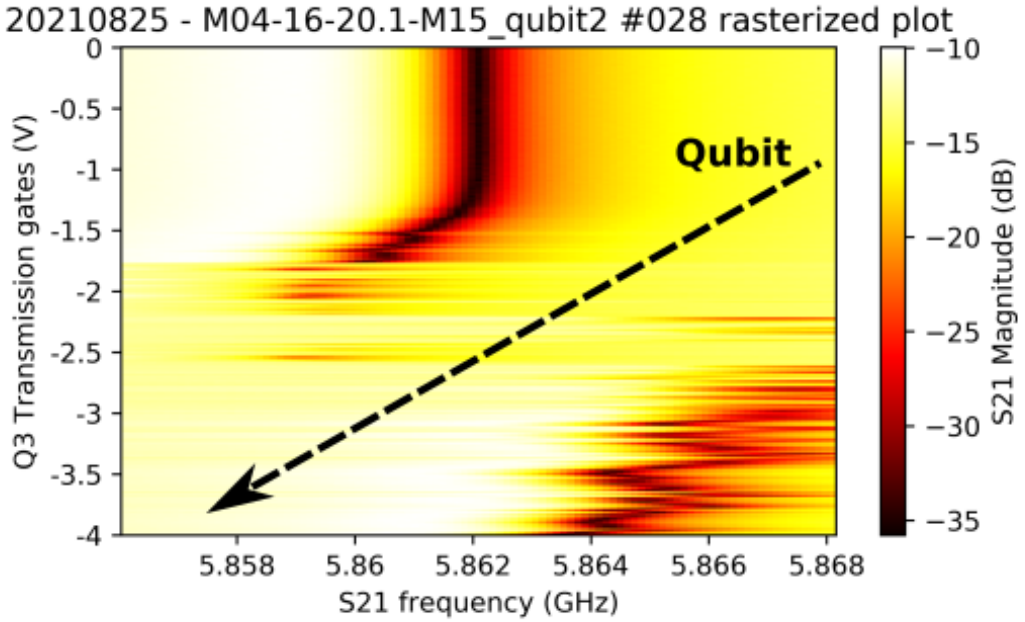

Figure 5.13: The avoided crossing, qubit frequency is lowered with gate, effectively tunes the detuning. When the detuning is tending towards 0, the resonator signal dissappears. Qualitatively looks like the qubit "punches through" the resonator.

These measurements conclude my results from my work on the M15 qubit chip. However, many interesting measurements were performed "after", where i followed on the sidelines. It would be a shame not to mention what this device uniquely achieved, i will therefore dedicate the next chapter to measurements i find crucial to the dotmon project. The following measurement were primarily performed by Oscar Erlandsson, the PhD student in charge of the later parts of the Dotmon project. I will not go into great detail in the interpretation of the data, it is mainly included for the curious reader.

5.2.4 Extra Measurements

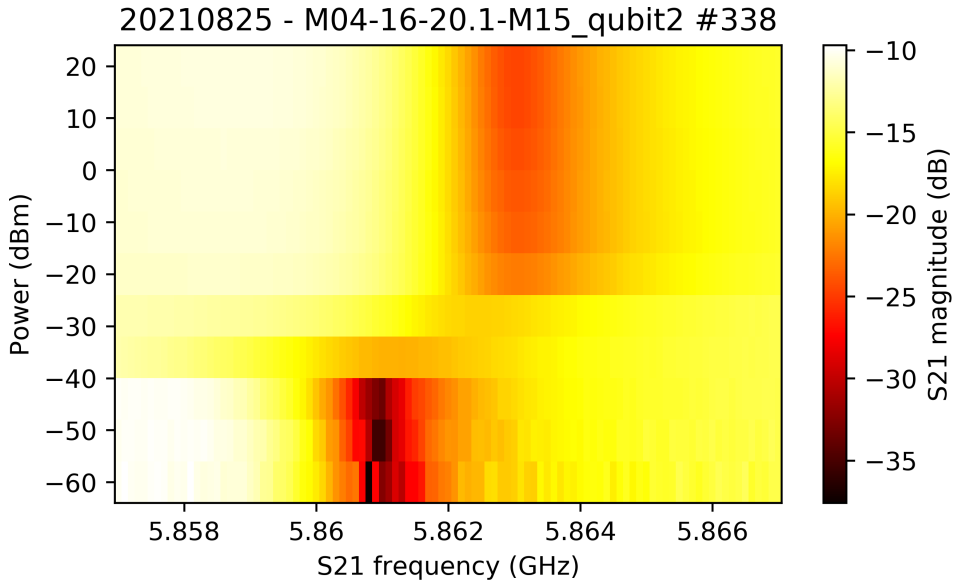

Figure 5.14: Power scan of the Q3 resonator where the dispersive shift is clearly visible. The

I will first show a clear dispersive shift of the Q3 qubit. In Figure 5.12, some feature that could be a dispersive sight occurs at high powers, around 0dBm readout power, but the system is not usable as a qubit in this sttate. This was because the gates were effectively set at 0V, corresponding to a very high qubit frequency. A dispersive shift of the Q3 qubit is shown in figure 5.14, where we see a clear resonator shift of around 2MHz from -40dBm to -25dBm readout power. The helper gate was set to $V_{help} = -1.0V$, the left QPC and Depletion gates were set to $V_{LQPC} = V_{Depletion} = -0.9V$ for this scan.

The next two plots i want to show are related. The first data is non-overlapping spectroscopy of the qubit, using the alazar readout configuration shown in figure 2.2. It shows the qubit frequency moving with the plunger gate, at a "dot resonance", see figure 5.15. The gate configuration is as follows: $V_{help} = -0.8V$, $V_{dep} = -3.0V$, $V_{LQPC} = V_{RQPC} = -1.75V$. This is related to the next data, one of the most important from the dotmon project as of writing this thesis (shown in figure 5.16). It shows a current bias scan taken at the same gate voltage configuration as for the qubit peak in figure 5.15 , whilst sweeping the plunger. It shows multiple "dot resonances" opening and closing as the plunger varies. It is correlated with a spectroscopy measurement showing the qubit peak appearing and disappearing as the plunger varies. The gate plunger voltages for the transport and cQED measurement do not exactly align, we believe it is due to some hysteresis, and the changing of the FET gate between the measurements. These measurements are a direct correlation between cQED qubit spectroscopy and quantum dot transport measurements, that bodes well for the future of the project. More exploration of the gate space, and troubleshooting of the setup is needed to advance the project however.

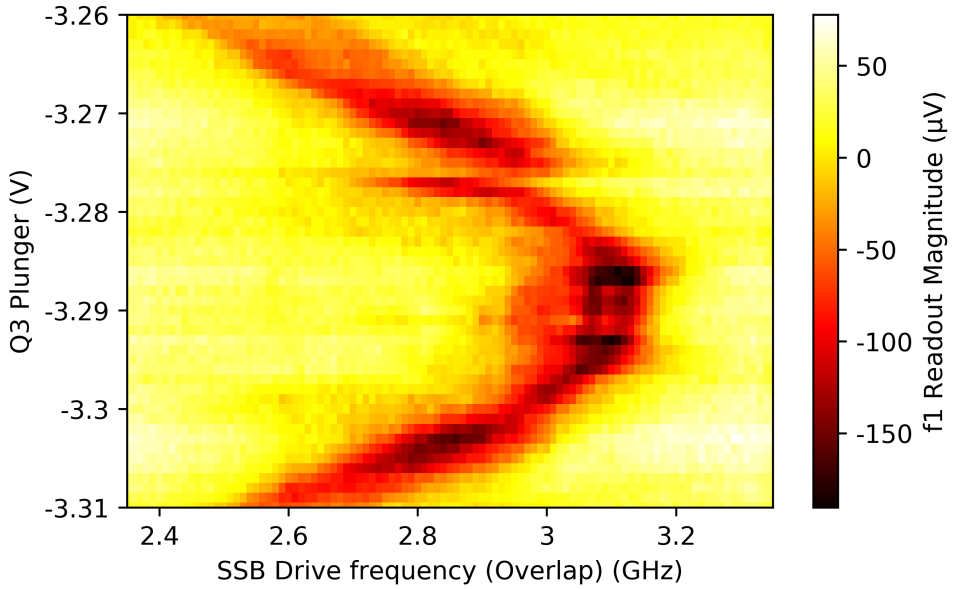

Figure 5.15: TEMP IMAGE - Nice spectroscopy

Time domain Raabi measurements were also performed on the qubit, in the same gate configurations as figure 5.15. They showed a qubit lifetime of $T_1 \approx 150ns$. This was lower than expected, and it is unclear if the suppressed charge dispersion by resonant tunneling through the quantum dot can be explored with qubit lifetimes of this magnitude. The other two qubits on the chip, Q1 and Q2, were also probed in time domain, and showed similar results to Q3.

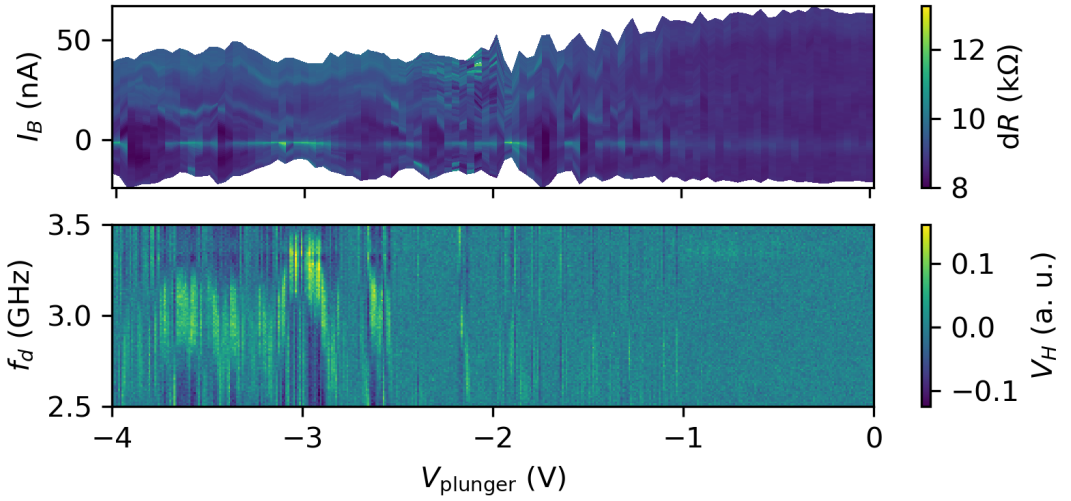

Figure 5.16: Transport and cQED shown side by side

CHAPTER 6

Conclusion

To conclude this thesis, i will summarize the results of the experiments performed:

6.1 Crossover Devices

Crossovers for implementation in qubit chips were designed, fabricated and measured on a specifically designed test chip, on an InP substrate. Optical and SEM images of the finished crossovers can be found in Figure 3.6. Multiple crossover variations were tested, a design with 15nm HfO2, crosslinked resist and 400nm evaporated aluminium as components and a wide profile proved the best candidate in DC resistance measurements, see table 3.1 and 3.2 for measurements of all crossover variations. The crossover were implemented in a cQED resonator test, to examine the impact of crossovers on RF measurements. The crossovers were implemented on two feedlines, one without resonators and one with resonators. No significant improvement from the crossovers was observed on VNA transmission measurements of the bare feedline, full transmission scans of both feedlines are shown in figure 4.22. We can not rule out benefits for time-domain measurements. The crossovers reduced the resonance frequency of resonators on the crossover-feedline by 1GHz, most likely due to more capacitance being added to the resonator system. This effect is shown in figure 4.23. The resonators have not been implemented on a qubit chip yet, but have been proposed for the feedline of the 3rd generation of Dotmon qubits.

6.2 Resonator Devices

Two resonator test chips were designed, measured and fabricated for the purpose of this project. The M19 resonator test was designed to bring down the external quality factor Q_e of the qubit resonators from approx 20k to approx 2k. 4 resonators were included on the chip, with different design variations shown in table 4.1. The only resonator that gave useful data was R4, the resonator with the same design as the first qubit chip. The results of the fit is shown in figure 4.10, Q_e was approx 22K as expected. The next resonator test DMNS003 had a dual purpose: bringing down the external Q (like M19), and examining the effect of crossovers on feedlines and resonators in RF measurements. The first goal was achieved, and is summarized in Figure 4.29. 5 resonator variants were tested, the design of R3 with a 640 μm coupling piece and a $3\mu m$ distance to the feedline resulted in $Q_e = 3K$, and was implemented in the M15 qubit chip.

6.3 Dotmon Qubit

The M15 qubit chip included three quibts with varying designs, the most promising being Q3. Q3 is a dotmon qubit with transport leads, allowing for in-situ swtiching between transport and cQED measurements. I measured the critical current I_c of the dot-junction as a function

of gate, shown in figure 5.8. The critical current could be varied controllably through 10-100nA, the regime neededd for qubit operations in the 4-10Ghz operating range. The quality factors of Q3 were measured using a power scan, and is shown in figure 5.12. The external quality factor was 3K as expected. The avoided crossing was also measured, showing control of the qubit-resonator detuning Δ, shown in figure 5.13.

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Appendices

APPENDIX A

Fabrication Recipes

A.1 DC Crossover Test Recipe

29-03-2021: Fabrication Recipe

Monday, 29 March 2021 14.53

Alignment Marks
Short exposure 1-1.5 hours with loading and conditioning

Strip resist:
1,3-Dioxolane – 5min sonication (80kHz, 100%pwr)
Acetone – 2min
IPA – dip
N2 – blowdry

Spin:
A4 – 4000 rpm 45 s
185C – 2min

Exposure:

Elionix - 500pA, Dose 680 µC/cm2, Field Size 150um, 60000 dots, 0.085 µSec/Dot

Develop:
MIBK:IPA(1:3) - 60s (swirl gently)
IPA – 5s (swirl)
N2 – blowdry
ash - 45s

Evaporate:
Ti – 10nm , 1.5Å/s
Au - 40nm , 1.5 Å/s

Lift off:
1,3-Dioxolane – 30-90min soak
Acetone - squirt (bottle or syringe)
IPA dip 30s
check sample in IPA
IF NOT SUCCESFUL: 60s sonication AND/OR60C hot acetone 5 min
N2 blowdry

Control Layer
Long exposure 2.5-3 hours with loading and conditioning

Spin:
EL9 - 4000RPM 45s
Bake 185C 2 min
A4 - 4000RPM 45s
Bake 185C 2 min

Exposure

Elionix - Dose 700 µC/cm2

1nA for lines - Field size 600um, 60000 dots, 0.6 µSec/Dot
40nA for bondpads - Field size 600um, 20000 dots, 0.14 µSec/Dot

Develop
MIBK 20s
IPA 10s

N2 blowdry
Ash - 60s

Evaporate
100nm Al, 1.5A/s

Lift off
Acetone Overnight
Hot acetone 60C 5 min
Ultrasonication 1 min 37(Hz? The low setting on the machine)
Acetone Squirt
Check sample in IPA
N2 blowdry

ALD
Short exposure ~ 1 hour with loading and conditioning

Spin
A4 45s 4500RPM
Bake 185C 2min

Exposure
Elionix - 500pA , Dose 680µC/cm2, WF 300µm, Dots 60K, Dose time 0.3 µSec/Dot

Develop
MBIK 30s
IPA 10s
Ash - 1min

ALD
15nm HfO2, 90°C, 150cycles, 10Hr pre-bake, 25Hrs process

NOT CORRECT PROCESS - process has been changed to a quick 6 hour process, more info available somewhere

Lift off
Acetone overnight
Hot acetone 60C 10min
Acetone Squirt
(Maybe sonication)
IPA rinse
Check in IPA before completion
N2 blowdry

Crosslink PMMA
Short exposure ~ 1 hour with loading and conditioning

Spin
A4 45s 4500RPPM
Bake 185°C 2 min

Elionix F-125 (125kV) - 100nA, WF 500 um, 200k dots, pitch 2, res 2x2.5nm, dose 60000 uC/cm^2, dose time 0.15 us/dot

Strip resist - Acetone soak 2 min, IPA rinse 30s

Crossovers
Short exposure ~ 1 hour with loading and conditioning

Spin
EL9 45s 4500RPPM
Bake 185°C 2 min

EL9 45s 4500RPPM
Bake 185°C 2 min

EL9 45s 4500RPPM
Bake 185°C 2 min

Exposure
Elionix 100kV - Current 500pA, Dose 680µC/cm2, WF 300µm, Dots 60K, Dose time 0.3µSec/Dot

Development
Develop - MBIK 1min
Develop - IPA rinse 10s
Develop - N2 blowdry

Evaporation
Kaufmann Milling - Ar Ions, 4.5min, 300V, 0.4mTorr, 15sccm Ar, 5min wait, 2min warm up

5nm Ti 5deg tilt, 50rpm rotation
50nm Al, 5deg tilt, 50 rpm rotation
300nm Al, 0 deg tilt, 50rpm rotation
50nm Al, 10deg tilt, 50rpm rotation

Lift off
Overnight Dioxolane Soak
Acetone Squirt (bottle or syringe)
check sample in IPA
IPA rinse
N2 blowdry

A.2 Resonator Test M19 Recipe

22-03-2021: Fabrication Recipe

22. marts 2021 09:39

Note: This recipe is intended to be used on a chip etched to the InP substrate (No 2DEG or Epitaxial Aluminium left).

Control Layer

Spin:
EL9 - 4000RPM 45s
Bake 185C 2 min
A4 - 4000RPM 45s
Bake 185C 2 min

Exposure

Exposure

Elionix F-125 (125kv) -

3na for lines - dose 800, field size 500um, 50000 dots, res 10nm, aperature 120um, 0.3 µSec/Dot, PEC 100% uniform clearing
60nA for pads and chip - dose 800, Field size 500 microns, 50000 dots, res 10nm, Aperature 240 um, 0.01 µSec/Dot

(These parameters were found after extensive testing, they are still not perfect however. This dose causes slight overdevelopment at 10s in MIBK, which is not ideal. More tests might be made to find a better dose combination)

Develop
MIBK 10s (+3s increments, check between)
IPA 10s
N2 blowdry
Ash - 60s

Evaporate
100nm Al, 1.5A/s

Lift off
1,3 Dioxolane Overnight
Acetone Squirt
Check sample in IPA
If not complete:
Ultrasonication 10s low power (Increase time and power if not complete)
Hot Acetone 70C 5min
Iterate until complete
If complete:
N2 blowdry

A.3 Combined Resonator and Crossover test DMNS003 recipe

12-07-2021: Fabrication Recipe

Wednesday, 7 April 2021 11.48

***Notes:** Sofus
***Work:** Sofus

Note: This recipe is intended to be used on a chip with 2DEG and Al at start of fab.

Alignment Marks
Short exposure 1-1.5 hours with loading and conditioning

Strip resist:
Acetone – 5min, 2min sonication (80kHz, 100%pwr)
IPA – 30s
N2 – blowdry
Ash - 4min

Spin:
A4 – 4000 rpm 45 s
185C – 2min

Exposure:

Elionix 100kV - 680 uC/cm2, 500 pA.

Write field 150 um, Dots 60k, Pitch 1, Aperture 40um, Dose Time 0.085 us
Design "DMNS002_AlignmentMarks", Layer(s): "L1D0_Alignment_inner", "L1D0_Alignment_outer"

Develop:
MIBK:IPA(1:3) - 60s gentle agitation
IPA – 5s agitation
N2 – blowdry
ash - 60s

Evaporate:
Ti – 10nm , 1 Å/s
Au - 40nm , 1 Å/s

Lift off:
1,3-Dioxolane – 30-90min soak (or overnight)
(NEW STEP) - Sonicate quickly for 5s, low power 80hz, before putting in overnight cabinet. Allows solvent to "break" barrier and flow easily.

Acetone - squirt (bottle or syringe)
IPA dip 30s
check sample in IPA
IF NOT SUCCESFUL: 10s high power sonication AND/OR 60C hot acetone 5 min
N2 blowdry

Mesa Etch

Spin:
A4 - 4000RPM - 45s
Bake 185C - 2min

Exposure:

Elionix 100kV - 500 uC/cm2, 40 nA, dose time 0.1125us.

Write field 600 um, Dots 20k, Pitch 1, Aperture 250um
Design "CROSSXRESIST_MESA", Layer(s): "L1D0"

Develop:
MIBK:IPA(1:3) - 30s - Gentle agitation
IPA – 5s - Agitation
N2 – blowdry
ash - 60s
Reflow(bake) - 115C 2min

Al Etch:
Transene D – 50C 15s
MQ – 50C 20s
MQ – r.t. 40s
N2 – blowdry

III-V Etch:
H2O : Citric Acid : H3PO4 : H2O2
220 : 55 : 3 : 3
10min, magnetic stirrer, rotate 90deg/2min
2 MQ rinses – 60s total (vigorous agitation)
N2 - blowdry

Note: Use profilometer to check mesa etch depth

Strip resist:
Acetone – 5min, 2min sonication (80kHz, 100%pwr)
IPA – 30s
N2 – blowdry
Ash - 4min

Control Layer

Spin:
EL9 - 4000RPM 45s
Bake 185C 2 min
A4 - 4000RPM 45s
Bake 185C 2 min

Exposure

Elionix F-125 (125kv) -

3 nA for lines, 60nA for rest of chip.

Lines: Write field 500 um, Dots 50k, Res 10nm, Aperture 120um, dose 800 uC/cm2, 0.2667us/dot, PEC 100 uniform clearing
Chip: Write field 500um, Dots 50k, Res 10nm, Aperature 240um, dose 800 uC/cm2, dose time 0.133us/dot
Design "CROSSXRESIST_PostDose_Control", Layer(s): "L3D0_CONTROL", "L3D0_CONTROL_PADS", "L0D0"

Develop (tricky step)
MIBK 12s - Static Development!
IPA 5s
N2 blowdry
Ash - 2min + 2min - Critical Step, Clears Resist Dots!!!

Evaporate
100nm Al, 1.1A/s

Lift off
1,3 Dioxolane - 3hrs, or Overnight
(NEW STEP) - Sonicate quickly for 5s, low power 80hz, before putting in overnight cabinet. Allows solvent to "break" barrier and flow easily.

Acetone Squirt
Check sample in IPA
If not complete:
Ultrasonication 5s-10s high power
Hot Acetone 70C 5min
Iterate until complete
If complete:
N2 blowdry
Ash - 2min

ALD
Short exposure ~ 1 hour with loading and conditioning

Spin
A4 45s 4500RPM
Bake 185C 2min

Exposure
Elionix 100kv - 680 uC/cm2, 500 pA.
Write field 300 um, Dots 60k, Pitch 1, Aperture 40um, Dose time 0.3 usec/dot
Design "CROSSXRESIST_ALD", Layer(s): "X_JUMPER_ALD"

Develop
MBIK 30s
IPA 10s
Ash - 1min

ALD
ALD 1 - 15nm HfO2, 90°C, 150cycles, 10Hr pre-bake, 25Hrs process

Lift off
Acetone overnight
Hot acetone 60C 10min (Quite important, liftoff difficult without)
Acetone Squirt
(Maybe sonication, high power 10s)
IPA rinse
Check in IPA before completion
N2 blowdry
Ash 60s

Crosslink PMMA
Short exposure ~ 1 hour with loading and conditioning

Spin
A4 45s 4500RPPM
Bake 185°C 2 min

Elionix F-125 (125kV) -
60000 uC/cm2, 100 nA.
Write field 300 um, Dots 200k, Pitch 2, Aperture 240um, Dose time 0.15 usec/dot
Design "CROSSXRESIST_Crosslink", Layer(s): "X_JUMPER_Resist"

Strip resist - Acetone soak 2 min, IPA rinse 30s

Crossovers/Contacts
Short exposure ~ 1 hour with loading and conditioning

Spin
EL9 45s 4500RPPM
Bake 185°C 2 min

EL9 45s 4500RPPM
Bake 185°C 2 min

EL9 45s 4500RPPM
Bake 185°C 2 min

Exposure
Elionix 100kV - 680 uC/cm2, 500 pA.

Write field 300 um, Dots 60k, Pitch 1, Aperture 40um, Dose time 0.34 usec/dot
Design "CROSSXRESIST_Contacts", Layer(s): "X_JUMPER"

Development
Develop - MBIK 1min
Develop - IPA rinse 10s
Develop - N2 blowdry
Ash 60s

Evaporation
Kaufmann Milling - Ar Ions, 4.5min, 300V, 0.4mTorr, 15sccm Ar, 5min wait, 2min warm up

5nm Ti 5deg tilt, 50rpm rotation
50nm Al, 5deg tilt, 50 rpm rotation
300nm Al, 0 deg tilt, 50rpm rotation
50nm Al, 10deg tilt, 50rpm rotation

Lift off
Overnight Dioxolane Soak
Acetone Squirt
check sample in IPA
IPA rinse
N2 blowdry