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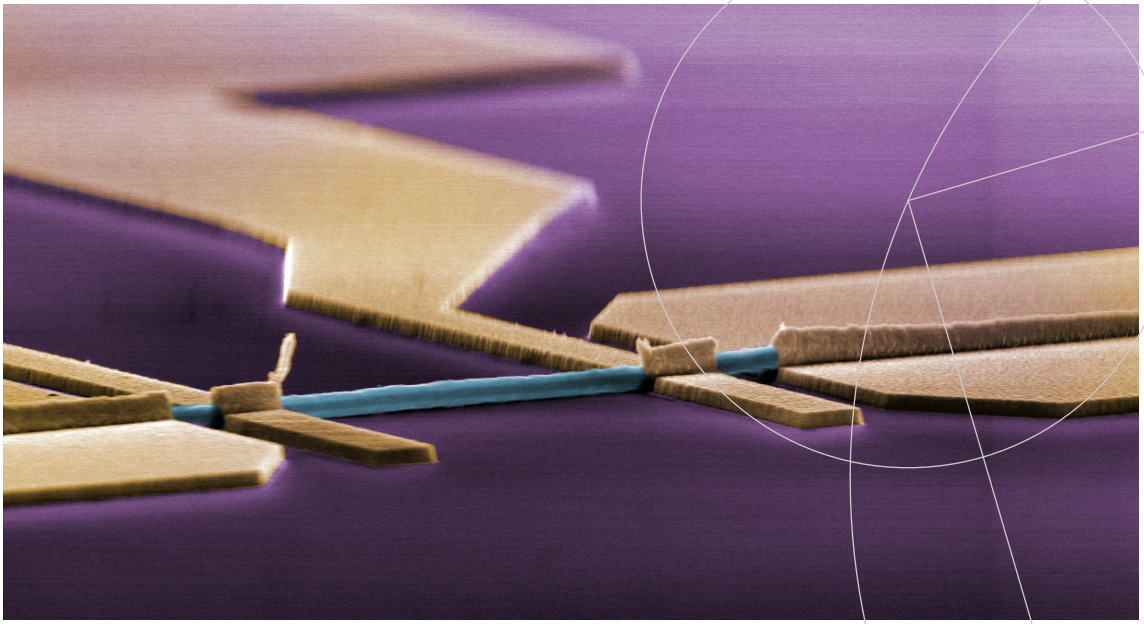
Device Fabrication and Low Temperature Measurements of InAs Nanowires with Superconducting Al Shells

Master's thesis



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Abstract

This master's thesis is about the process of device fabrication based on InAs nanowires with superconducting Al shells. Two types of devices have been measured at low temperatures at which aluminum enters the superconducting phase. In the first case the resistance across the shell was measured in a four-probe measurement in dependence of temperature and externally applied magnetic fields. For certain diameter and thickness of the shell enhanced Little-Parks oscillations were observed, in which the critical temperature T_c oscillates with periodicity of the flux quantum $\Phi_0 = h/2e$. From these data the effective ratio between the cylinder diameter and coherence length could be estimated by a simplified model. In the second case, the conductivity across an exposed segment is measured in dependence of applied bias and back-gate voltage as well as magnetic field. From these data the superconducting gap-size Δ of the aluminum shell could be estimated and was found to be around $2\Delta = 0.6\,\mathrm{meV}$. Furthermore, a detailed description of the device fabrication is presented.

Acknowledgement

I would like to thank Thomas Sand Jespersen for giving me the opportunity to participate in his research project; it has been very inspiring and a pleasure working with you. Secondly I would like to thank Anders Jellinggaard for introducing me to the basics of device fabrication and especially for the great work he has done with the software *align* which saved me a lot of time. Furthermore, I would like to thank Ferdinand Kuemmeth, Willy Chang, Morten Kjærgaard, Andrew Higginbotham and Shivendra Upadhyay for the great help with technical problems and great discussion in general. Thanks to Jesper Nygård and Charles Marcus for letting me being part of QDev and in general thanks to all of the staff and students of QDev for a really great time. Special thanks to Merlin von Soosten for being such a great friend and always open for some discussion, it is great knowing you!

Contents

Introduction

This thesis is about the experimental work performed during the last year on the subject of device fabrication and low temperature measurements on indium arsenide (InAs) nanowires (NWs) with cylindrical superconducting Al shells. The main goal was the optimization of the process of device fabrication for the production of a superconductor-nanowire-normal conductor junction. To achieve the targeted junctions, devices where prepared with contacts to the aluminum shell at each of the ends, subsequently the central region of the shell was etched away to enable the production of normal-metal contacts to the InAs core. On the way towards this goal, two intermediate stages have been measured at low temperature, namely an intact Al shell surrounding the entire nanowire and a shell in which the central part has been removed without the addition of the normal contact. Both cases showed rather unique phenomena; whereas the superconducting state of the intact shell fluctuated with periods of magnetic flux quanta, the supercurrent across the exposed nanowire in the other case could be completely suppressed by a negative gate potential.

The general outline of this thesis is as follows: In the first chapter a brief introduction to superconductivity will be given including some of the phenomena observed for the geometry of cylindrical superconducting shells. It includes brief introductions to the topics of the critical values that destroy superconductivity, i.e. critical magnetic field, temperature and current density. Furthermore, some of the main aspects of Little-Parks oscillations, Josephson effect and Andreev reflection will be presented. The following chapter starts out with an introduction to nanowire growth and characterization and continues with the basic principles of device fabrication by electron beam lithography. At that point some of the considerations and tests for the optimization of device fabrication will be presented, and the chapter

concludes by an introduction to cryofree dilution refrigerators and the setups used for the electrical measurements at room- and low temperatures. The last chapter is divided into three parts each devoted for the results obtained for one of the three samples. At the end the results are summarized in the conclusion and some outlooks for future studies is given.

During this project a publication was prepared including some of the results presented here. At the time of the end of this project, however, it was still in the finalizing phase, but is expected to be submitted in the nearest future. A draft of the manuscript is included in Appendix F. It is further expected that another publication will be prepared based on the additional results presented in the second part of the result discussion. For this, however, a profound analysis and preferably additional measurements are needed and might be subject to future studies.

Motivation

The main motivation of this study was to investigate the quality of the induced superconducting state in a nanowire in close contact with a superconducting material. Usually the contact interface between the two materials is disrupted due to inhomogeneities of the surface, impurities and the naturally occurring native oxide layer. Apart from the oxide, InAs nanowires are generally easily contacted with the occurrence of a weak Schottky barrier. The reason why InAs nanowires are so easily contacted is due to the surface accumulation layer. However, the oxide layer typically limits the conductance, and it is a rather hard task to remove it without damaging the surface of the nanowire too much. This was tried to be overcome by evaporating the Al contacts onto the wires directly after their growth, without breaking vacuum and thus preventing the newly formed nanowires from oxidation. When a superconducting material, such as aluminum, is in good contact with a normal-state material, the order parameter of the superconductor is partially induced into the normal material. However, the hardness of the induced gap depends on several parameters, such as impurities, and inhomogeneities[1], which tend to soften the gap. In studies towards the observation of Majorana Fermions a detailed recipe, i.e. certain criteria that have to be fulfilled, has been presented[2]. The main ingredients to obtain a system, in which Majorana Fermions may exist, i.e. topological superconductor or p-wave superconductor, is given as: the system has

to be one-dimensional with strong spin-orbit interaction, and large g-factor, superconductivity has to be present at the same time as a weak magnetic field is applied. In semiconductor nanowires several of these parameters are fulfilled, except for e.g. the superconductivity. That has to be induced, which is why it is desired to have good contact to the superconductor.

However, a part of the wire (at the position where superconductivity is induced) has to be gate-able i.e. the chemical potential has to be adjustable, which is not possible when the nanowire is completely surrounded, which is why a system with half-shells, grown in the MBE chamber would be desirable. The full-shell wires are thus a good starting point to investigate the general parameters obtained for the grown contacts.

1. Theory

This section will give a brief introduction to superconductivity (SC) and some of the key theories used to analyze the results of the low temperature measurements. A few of the relevant phenomena observed in the field of superconductivity will be introduced.

1.1. Superconductivity

At temperatures below a critical temperature T_c certain materials, such as aluminum, undergo a phase transition from the normal-metal to the superconducting phase. This was first observed by the Dutch physicist H. Kamerlingh Onnes in 1911[3] by measuring the conductivity of mercury while cooling it with liquid helium, for which he received the Nobel Prize in Physics (1913).

For certain metals the resistance drops abruptly to zero when the temperature is decreased below a certain value T_c, which is specific for the material under investigation. When the temperature of the superconductor is lower than the critical temperature its density of states (DOS) splits and creates a gap around the Fermi level, E_F with the gap size of 2Δ (one Δ from the Fermi level up/down to the excited-/ground-state energy, respectively), as seen on Figure 1.1.1. In the center of the gap at the Fermi level, electrons can only exist in pairs, so-called Cooper pairs[4]. Cooper pairs consist of two interacting electrons, so they carry a charge of $2e$, furthermore, the two electrons have to have opposite spin and momentum, thus cooper pairs are bosons. The relatively weak binding energy between the electrons is due to electron-phonon interactions, and the binding energy equals Δ, i.e. to be split they have to leave the bound state and enter either the ground or excited state, as single electrons are not allowed in the gap. So cooper pairs are bound to

the Fermi level as there are no other states available in the gap, however they can move freely through the superconductor without resistance. The concept of Cooper pairs is part of the BCS theory (named by Bardeen, Cooper and Schrieffer), which is rather involved and will not be discussed in further detail. However, from the BCS theory, it is known that the gap-size is dependent on the temperature. An approximation of the gap size compared to the temperature is given as[3]:

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74 \left(1 - \frac{T}{T_c}\right)^{1/2} , \tag{1.1.1}$$

where $\Delta(0)$ and $\Delta(T)$ is the size of the energy gap at zero and finite temperature, respectively. Up to a temperature of around $T \approx 0.2T_c$ the gap is rather constant at its maximum value, and with increasing temperature, the gap begins to close until it vanishes at T_c. Without the gap, the metal behaves as a normal metal with finite resistance.

It has further been observed that superconducting metals (below T_c) expel magnetic flux when placed in a (low) magnetic field (Meissner effect). This perfect diamagnetism, however, is limited to a critical magnetic field B_c. This is because the magnetic flux has a finite penetration depth λ into the material. As the magnetic field increases it becomes harder to expel the flux, and finally when B_c is reached, superconductivity is suppressed and the magnetic flux can penetrate the metal. Additionally to the temperature dependence, it is known from Douglass[5] that the gap in the superconductor is dependent on the applied magnetic field. The London penetration depth λ_L is one of two important length scales in superconductors and it is a property of the material. The other important length is the coherence length ξ_0, which again is an intrinsic property of the superconducting material. It is a measure of the distance over which the electron-electron interaction can be maintained. However, both of these length scales are temperature dependent and when the temperature approaches T_c the penetration depth diverges whereas the coherence length decreases to zero.

An additional way to suppress superconductivity is when the current through the sample is increased and reaches the critical current density J_c. The reason for that is that the current effectively induces a magnetic field (which is circumferential in the case of a wire or cylinder). An estimate for the critical current density through a wire of a typical superconducting material is $10^8\,\mathrm{A/cm^2}$.[3]

For bulk aluminum the other values are given as: $T_c = 1.14\,\mathrm{K}$, $B_0 = 10.5\,\mathrm{mT}$, $\xi_0 = 1.6\,\mu\mathrm{m}$ and $\lambda_L = 16\,\mathrm{nm}$[6]. However, these values might change quite drastically when the sample size is decreased to the mesoscopic regime, e.g. when the boundaries of the geometry are on the same length scale. For example was ξ_0 found to be $\sim 0.1 - 0.2\,\mu\mathrm{m}$ for mesoscopic Al discs and squares[7],[8]. Furthermore, the coherence length will be decreased by inhomogeneities as it adds disorder in the electron-electron interaction, and it plays a much larger role in mesoscopic samples.

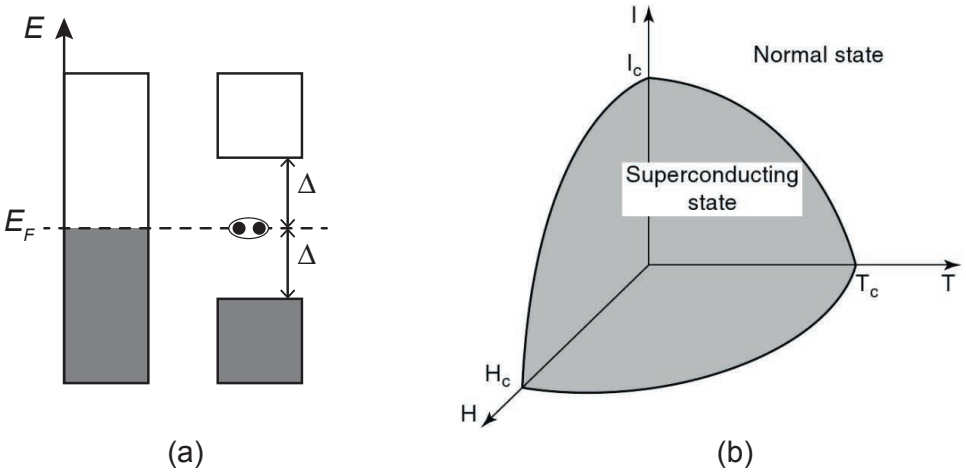


Figure 1.1.1.: (a) simplified schematic for comparison of the density of states in the normal-metal (left) and superconducting (right) phase, E_f denotes the Fermi level. In the superconducting state single electrons are forbidden inside the gap (denoted by the two Δ) and only Cooper pairs are allowed at the Fermi level. (b) schematic diagram of the relation between the critical temperature T_c, critical magnetic field H_c and critical current I_c, above which the superconductor is driven into the normal state. Figure (b) was adapted from[9].

1.1.1. Superconducting Cylinder

The geometry of the sample may play a role in the critical magnetic field as well, as the projection of the surface area of the sample normal to the field direction is proportional to the magnetic flux Φ. So for a superconducting material to stay in the superconducting phase it has to expel the magnetic flux, which is related to the projected area. So for a thin wire it is expected that the expelled magnetic flux is larger in the perpendicular direction compared to the parallel (along the wire) direction.

However, for a superconducting ring or cylinder in a magnetic field perpendicular to the plane of the ring or parallel to the wire, it has been shown that a certain flux might be able to penetrate the central region without the destruction of superconductivity. What, however, is observed is that the measured resistance oscillates periodically when the magnetic flux is increased. This is known as Little-Parks oscillations and is observed as oscillations in the critical temperature. The period of these oscillations is found to be in units of the flux quanta $\Phi_0 = h/2e = 2.07 \times 10^{-15}\,\mathrm{T}\cdot\mathrm{m}^2$,[3] where h is the Planck constant and e is the electron charge. The maximum reduction in T_c as a function of Φ is found to be at odd multiples of $\Phi = \frac{1}{2}\Phi_0$ and the oscillations are found up to a critical field, below which superconductivity is maintained.

This has been known, and experimentally confirmed for over half a century now, and without going into further details it is mainly referred to the work of Liu *et al.*[10] and Sternfeld *et al.*[11] in which a similar sample geometry, compared to this work, has been investigated. The main difference, compared to the rather classical experiments of Little and Park, occurs when the sample geometry, e.g. the diameter and thickness of the cylinder, becomes comparable to the coherence length. In this regime, it has been predicted that superconductivity would be destroyed, even at $T = 0$. The phase boundary between superconducting and normal regime has been given by[10]

$$\left(n - \frac{\Phi}{\Phi_0}\right)^2 = \left(\frac{d/2}{\xi(0)}\right)^2 \left(1 - \frac{T}{T_c}\right) \ , \tag{1.1.2}$$

where n is an integer that minimizes the term on the left side, d is the diameter of the cylinder, $\xi(0)$ is the zero temperature coherence length and T_c is the zero field critical temperature. For this simplified model it has been assumed that $d < \xi(0)$ and the width of the cylinder is $L = 0$.

This is somewhat in contrast to the model used in the work of Sternfeld *et al.*, where the boundary between the superconducting and normal phase has been given as[11]:

$$\ln\left(\frac{T_c(n,\Phi)}{T_c(0,0)}\right) = \psi\left(\frac{1}{2}\right) - \psi\left(\frac{1}{2} + \frac{\alpha(n,\Phi)}{2\pi T_c(n,\Phi)}\right) \ , \tag{1.1.3}$$

where $T_c(n,\Phi)$ is the (reduced) critical temperature at a specific integer n and flux ϕ which solves the equation. ψ is the digamma function, and $T_c(0,0)$ is again the zero field critical temperature. $\alpha(n,\Phi)$ is the pair breaking parameter, which was

given by:

$$\alpha(n,\Phi) = \frac{\xi(0)^2}{\pi R^2} T_c(0,0) \left[4\left(n - \frac{\Phi}{\Phi_0}\right)^2 + \frac{t^2}{R^2}\left(\frac{\Phi^2}{\Phi_0^2} + \frac{n^2}{3}\right)\right] , \tag{1.1.4}$$

where R is the cylinder radius and t is its thickness. This is a more complete model, as it does not neglect the thickness of the cylinder, however, it is still limited to $d \leq \xi(0)$. In the case of $n = 0$, i.e. at flux below $0.5\Phi_0$, and if the thickness $t < R$, the contribution of the ratio t/R is only weakly and the two equations become quite comparable (when seeing apart from the digamma functions), and a fit to the phase diagram below $0.5\Phi_0$ can be used to estimate the ratio $R/\xi(0)$. However, as Equation 1.1.3 is of the form of a recursive function, it has to be solved numerically, whereas Equation 1.1.2 is rather simple to fit. In the case of $n > 0$, $\alpha(n,\Phi)$ depends strongly on t/R, which eventually sets the upper limit for the flux at which the cylinder is still superconducting. At finite $n > 0$, Equation 1.1.3 can be used to estimate the thickness by using the ratio t/R as a fitting parameter as well for the numerical solution.

Experimentally, to obtain this phase diagram the resistance of the cylinder has to be measured in dependence of the magnetic field at different temperatures. The diameter is often known, however the effective diameter might vary due to e.g. disorder in the superconducting material, so the effective diameter can be calculated if the oscillations are obtained, due to the quantization of the flux. To set up the phase diagram, which is a plot of T_c vs. Φ/Φ_0, a threshold resistance R_c, separating the superconducting/normal state, has to be chosen. It is, however, still not clear what the right ratio between the critical R_c and normal R_N resistance should be, and several different values have been used. The intersections between R_c and the measured curves then make up the points in the $\Phi - T$ phase diagram.

This is a very useful technique to estimate the coherence length, which, as mentioned above, might deviate quite drastically from the bulk value when the sample geometry is in the mesoscopic regime.

The zero field critical temperature and perpendicular critical magnetic field is easily measured experimentally by measuring the resistance while increasing the temperature or applying an external magnetic field. The critical current, however, could not be measured. This was mainly because of the relatively high current necessary to suppress the superconductivity. From the estimate above multiplied

with the cross-sectional area of the nanowire and its shell (with $r = 60\,\mathrm{nm}$) resulted in a theoretical $I_c \approx 10\,\mathrm{mA}$, which is rather large. As this measurement has to be conducted below T_c, a cryostat is needed. However, the cryostat has some build-in RC-filters close to the sample. These filters have a resistance of around $2.3\,\mathrm{k\Omega}$ per line, which will warm the system when a large current is sent through it. Even assuming a necessary current of $0.5\,\mathrm{mA}$, this would result in heating power of around $I^2 \cdot R \approx 1\,\mathrm{mW}$. The cooling power of the cryostats is estimated to be $200\,\mu\mathrm{W}$ at $100\,\mathrm{mK}$, which is, up to a heating power equal to the cooling power the temperature can be maintained. However, the heating power exceeds the cooling power immensely and would warm the sample probably above T_c.

1.1.2. Josephson Effect and Andreev Reflection

So far only the intact cylindrical shell has been considered, however, at a later point in device fabrication a segment of the superconducting shell is removed in the central region exposing the InAs core. The resulting structure is called weak link of the type superconductor-semiconductor-semiconductor junction. The characteristic behavior of weak links, which can consist of a variety of junctions such as superconductor-normal-metal-superconductor (S-N-S), S-insulator-S or S-point-contact-S, is very similar, regardless of the material between the superconductors. When the distance between the superconducting materials is close enough, Cooper pairs can tunnel from one side to the other, through the intermediate material. If this is possible, the junction is able to transport a supercurrent even if not in direct contact. The effect of supercurrent tunneling through an intermediate material is called Josephson effect and the maximal supercurrent is given by $I_s = I_c \sin(\Delta\varphi)$, where I_c is the critical current of one of the superconductors and $\Delta\varphi$ is the phase difference of the two superconducting phases. The distance between the two superconductors at which superconductivity is maintained is limited by the distance over which phase coherence is maintained and it depends strongly on the mobility of the intermediate material. So at zero applied bias the Cooper pairs can tunnel through the non-superconducting material, however, when a bias is applied, the energy of the two sides is no longer aligned, and as no states are available inside the gap there will be no current across the junction. This is shown on the sketch on Figure 1.1.2 (a).

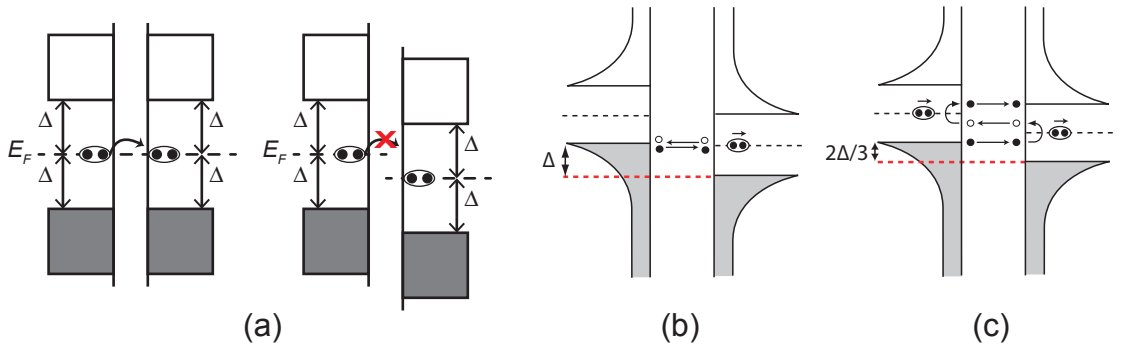


Figure 1.1.2.: (a) schematics of the tunneling of Cooper pairs from one superconductor to another through an insulating barrier, in the case of zero bias (left) a supercurrent can flow, whereas in the case of a finite bias (less than Δ) tunneling is not possible as no states are available in the gap. (b) and (c) show the process of single and multiple Andreev reflections, respectively, as discussed in the text. Figure (b) and (c) were adapted from[12]

However, if the applied bias is further increased, eventually it will match the energy of the gap Δ. In the normal Josephson effect, this would still be an insulating regime until the energy of 2Δ is reached and the junction becomes normal conducting. On the other hand, there is another case, when the bias corresponds to Δ as depicted on Figure 1.1.2 (b). As the ground state of the one superconductor is aligned with the Fermi level of the other, an electron might tunnel through the barrier and into the superconductor. At the interface to the SC it forms a Cooper pair with another electron, however, as energy, charge and momentum have to be conserved, a hole is send back (reflected) from the interface with an energy equal to, but with opposite sign, of the electron, i.e. symmetrically around the Fermi level. This process is called Andreev reflection (AR). Furthermore, at a different bias, which matches e.g. $2\Delta/3$ these AR can occur at both interfaces, as depicted on Figure 1.1.2 (c). As an electron tunnels from the left to the right SC it is reflected as a hole symmetrically around the Fermi level on the right. This hole then tunnels to the left SC where it is reflected as an electron with an energy symmetrically around the left Fermi level. This electron has gained enough energy to enter the exited. This is known as multiple Andreev reflections.

The diagrams shown on the pictures are for the case of an S-N-S junction, i.e. there is a continuity of states available in the normal-metal. In the case where the intermediate material is a semiconductor, the available states are gate-dependent.

So for Andreev reflections to occur, not only the bias, but also the gate has to be adjusted, to be aligned for the respective process. In general it can be concluded that the supercurrent travels through the semiconductor when it depends on an applied gate.

The appearance of Andreev reflection is not limited to the case where two superconductors are in close vicinity. When only one superconductor-normal metal (or any other conducting material in the normal state) interface is present, electrons from the normal metal are still able to enter the superconductor by the process of reflecting a hole. In the other direction, Cooper pairs are able to tunnel into the normal metal as well and maintain their phase coherence for a certain distance until it is lost due to scattering. This carries some order parameter into the normal metal, which in the vicinity of a superconductor acquires some superconducting properties. This is known as proximity effect or proximity-induced superconductivity. The strength of the induced superconductivity depends on several parameters, such as the induced coherence length in the normal material, which in turn depends on the electron mobility in e.g. a semiconductor. Furthermore the induced SC-gap might be broadened, i.e. less profound, due to inhomogeneties such as interface disorder, (magnetic) impurities and temperature[1].

This is why the MBE grown superconducting contacts are of such interest, as the interface between the superconducting Al shell and the semiconducting InAs core is expected to be very clean and ordered. In this work, however, none of these effects have been studied in further details as the main focus was on the optimization of device fabrication.

2. Materials and Methods

This chapter is divided into several sections. In the beginning the focus will be on nanowires; how they are produced and characterized. The following part provides an introduction to device fabrication and towards the end the principles of dilution refrigerators and the measurement setups will be presented.

2.1. Nanowires

This section will focus on the production, characterization and some of the main properties of InAs nanowires (NW). Nanowires are rod-shaped crystals with diameters ranging from tens to hundreds of nanometers and lengths of several microns. Semiconducting nanowires can be made purely of group IV elements, such as Si or Ge, or a large variety of compositions of materials, such as III-V combinations (InAs, GaAs, InP, InGaAs, just to name a few), group II-VI combinations (ZnO, ZnSe/CdSe) and potentially more exotic combinations such as group I-VII combinations or even more complex combinations across the groups.

During the last decades, several techniques for producing NWs have been developed, in both top-down and bottom-up approaches. In top-down design, the NWs are typically fabricated directly from a bulk substrate by removing the surrounding material in a controlled way e.g. by dry or wet etching. The remaining NW structures are then typically found either standing upright on, or lying on top of, the substrate. The most prominent bottom-up approaches for NW synthesis include metalorganic chemical vapour deposition (MOCVD), chemical beam epitaxy (CBE) and molecular beam epitaxy (MBE). The nanowires are grown directly on the substrate in the bottom-up approach. In all three techniques the materials are led to the substrate in their respective way, where they aggregate, either self- or

catalyst-assisted, to form the crystalline structure making up the NW.

The InAs nanowires used in this study were grown by MBE; its working principle will be explained further in the next section. For the purpose of obtaining ohmic contacts to the nanowires, an oxide-free interface between the InAs NW and the metal contacts is needed. Several techniques have been developed for this task, such as etching the oxide chemically followed by passivation to prevent the wire from re-oxidizing or by physically removing the oxide by *in situ* ion milling directly prior to metal evaporation. However, both approaches have the potential of attacking the nanowire as well, resulting in a damaged surface and hence a non-uniform NW/contact interface. The strategy in this study was to use epitaxial aluminum contacts directly grown on the InAs NWs in the MBE system. As the aluminum was deposited directly after NW growth in the same reaction chamber, the nanowires have not been exposed to ambient atmosphere and hence no native oxide has been formed. The characterization of the nanowires and the interface to the aluminum shell will be discussed in Section 2.1.2.

2.1.1. Molecular Beam Epitaxy

MBE is a technique for the production of ultra-clean crystalline structures. It is often the method of choice when low incorporation of impurities, only few crystal defects and high control of composition is needed. These properties are optimized in MBE, as the main chamber is kept at ultra-high vacuum and the deposition rate of the elements is rather low. Furthermore, ultra-pure materials are used as sources in the effusion cells. The name-giving principle of MBE is the process in which beams of elements (atoms or molecules) collect at a surface to form epitaxial[1] crystals. The beams are targeted at the typically rotating growth substrate where the elements aggregate and form a crystal, layer by layer.

InAs nanowires are typically grown on an InAs(111)B substrate prepared with catalyzing gold particles. The gold particles can be applied in controlled arrays using electron beam lithography. The growth model for Au-assisted NW growth is usually the Vapor-Liquid-Solid (VLS) model. For InAs NWs, the model predicts

[1] Epitaxy can be translated from the Greek words *epi*, meaning *above* and *taxis*, meaning *ordered*, which combined could be translated/interpreted as *to arrange upon*, referring to the alignment of the deposited materials to the underlying crystal structure.

that the indium and arsenic vapors collect at the liquid Au droplet and diffuse to the bottom of the droplet, where they nucleate and form the crystal. The newly formed nanowire crystal lifts the gold droplet as it grows higher. Figure 2.1.1 summarizes these steps, where in (a) the gold is evaporated onto the substrate, forming the droplets, (b) In and As particles collect on the Au droplet until it saturates and (c) the NW crystal is formed underneath the Au droplet. The size of the gold droplet is the main control-parameter for the diameter of the NWs.

To form the aluminum shell on the nanowires, the substrate is cooled to about $-15\,^{\circ}\mathrm{C}$ directly after NW growth and aluminum is deposited. The diffusion length of Al is very low at this temperature, so it is possible to form a uniform shell of around $10 - 100\,\mathrm{nm}$. As the aluminum source is positioned at an finite angle to the normal direction of the substrate, the substrate can be rotated to obtain a uniform coverage from all directions (full shell) or kept still to obtain coverage from only one side (half shell). An example for each case is presented on the transmission electron micrographs on Figure 2.1.2. However, only the full-shell InAs NWs have been used for device fabrication in this study.

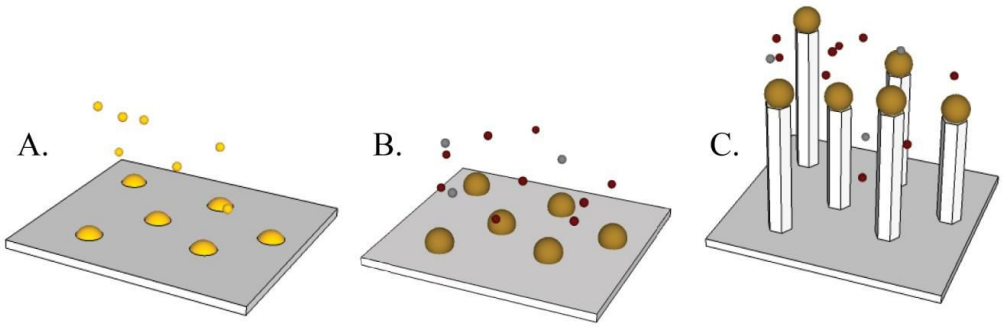


Figure 2.1.1.: Simplified model of Au-assisted nanowire growth. (A) Gold (yellow dots) is deposited on the growth substrate and the substrate is heated to melt the gold so that the catalyzing Au-particles are formed. (B) The substrate is set to growth temperature and evaporation of In and As (red and gray dots, respectively) is initialized. The materials collect at the Au-particle and nucleation is initialized at the bottom of the particle when it is supersaturated. (C) The NW crystals lift the catalyst particle and continue to grow in the vertical direction. Figure adapted from[13].

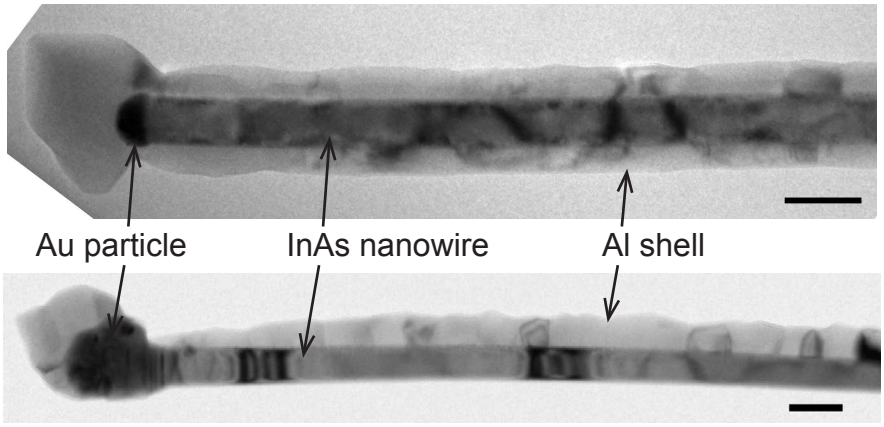


Figure 2.1.2.: Transmission electron micrographs of two core/shell InAs/Al nanowires. The top/bottom-image shows a nanowire with a full-/half-shell respectively. The Au-catalyst particle, InAs and Al regions are indicated; the scale bars correspond to 100 nm. The nanowire on the top-image is from the same growth-batch as those used for device fabrication (*NBI718*). The lower image is adapted from[14].

2.1.2. Nanowire Characterization

This section will focus on some of the characterization of the crystal structure of InAs nanowires and an intermediate layer between the InAs core and the Al shell. Usually, InAs nanowires are grown on [111]B terminated InAs wafers, which predetermines the growth direction of the NW. The bulk InAs has a cubic zink blende (ZB) crystal structure, which is mostly observed for the nanowires as well. However, a second possible crystal structure that the nanowires might adapt is the hexagonal wurtzite (WZ) structure. The main difference between the two crystal structures is the stacking sequence of the crystal planes in the growth direction (the [111] direction for ZB is equivalent to the [0001] direction in WZ). This is indicated on Figure 2.1.3 where it is seen that for the ZB structure, the stacking sequence is ABC ABC whereas for WZ it is AB AB. It is known that the crystal structure is dependent on the growth conditions, however no complete theory has yet been able to give detailed predictions. Furthermore, the crystal structure can change during growth, i.e. along the wire, resulting in stacking faults or twin-planes, in which the structure has shifted for several layers or for a single crystal layer, respectively. It is also known that the crystal structure depends on the Au particle, and hence the diameter, with thin wires consisting of pure WZ with only few crystal defects and for

wires with large diameters the structure is mainly ZB[13]. Either way, it is wanted to obtain as pure (both in the sense of impurities and crystal structure) nanowires as possible, as all crystal defects result in disorder and changes in the energy bands of the semiconducting material. The crystal structure of nanowires is usually analyzed by transmission electron microscopy (TEM) and selected area electron diffraction (SAD). Whereas electron diffraction gives a reciprocal-space representation of the crystal lattice averaged over the selected area, the direct image mode gives a direct representation of the structure. So while the crystal structure can be determined by electron diffraction, the direct mode can be used to localize crystal defects.

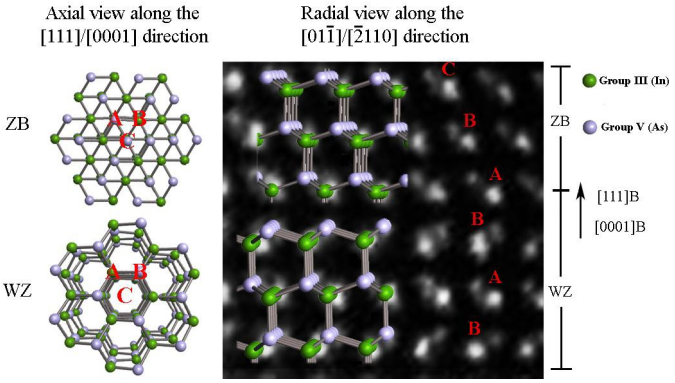


Figure 2.1.3.: Atomic models of the two crystal structures ZB and WZ. The left side is a view along the nanowire growth axis [111]/[0001] and shows the positions of the stacking sequence. On the right side the model viewed along [11$\bar{1}$]/[$\bar{2}$110] direction is shown on top of a scanning tunneling micrograph. Figure adapted from[15]

The nanowires used in this study were produced and analyzed by Morten Hannibal Madsen. The nanowires for the core/shell geometry were prepared by evaporating aluminum on the newly grown NWs directly in the growth chamber. It turned out that the temperature in the growth-chamber and the substrate has much influence on the homogeneity of the aluminum shell. This might be explained by the diffusion length of the Al-particles on the growth surface. To minimize the free energy, i.e. the effective surface area, the aluminum particles collect in grains (typically around 20-30 nm, which is unwanted as it introduces inhomogeneities in a thin deposition layer. However, it turned out that at lower temperatures the coverage was more uniform and continuous.

TEM analysis of the core/shell NWs showed that this method produces oxide-free interfaces between the InAs core and the Al shell. For some batches, however,

it was found that a different kind of interface appears between the core and shell and it seemed to be growth related, such as the time between NW growth to be terminated and the start of Al deposition. In an earlier project[14] this interface was analyzed by high-resolution TEM and energy-dispersive X-ray spectroscopy (EDX). Both techniques gave indications for that the intermediate layer might consist of AlAs. The EDX measurements were performed in scanning TEM mode, which enabled it to perform line-scans across the interface. The position at which the signals for In and As decreased towards the Al coating was slightly shifted, and the signal for As was found to be around 2 nm further towards the Al region. This distance corresponded quite well with the measurements from the HR-TEM image, in which the thickness of the layer was measured. Furthermore, the ratio between the interplanar spacings for the InAs nanowire and the intermediate region was estimated and found to be in correspondence with the ratio in lattice spacing between InAs and AlAs. However, further profound study of these interfaces is still needed to fully understand the composition. An explanation for the occurrence of this interface is that a background of As still was present in the growth chamber when the Al deposition was initialized, which might be prevented by increasing the time between core/shell growth.

The electrical properties of this interface has not yet been analyzed, and it will be neglected in this study. For one of the NW growth batches used in this study (*NBI585*) the appearance of the interface was found on some of the wires, however, for these wires only measurements on the intact shell were conducted, which is why it has been neglected. The crystal structure of these nanowires was estimated to be pure WZ with a few stacking faults near the tip. The diameter of the nanowire-core was estimated to be around $40 - 60$ nm with a shell thickness of around 13 nm, and the length was around $6\,\mu$m. The other batch used was *NBI718* for which no intermediate interface was observed. The crystal structure was expected to be ZB and the core-diameter was estimated to be ~ 80 nm. The shell thickness was ~ 30 nm and the length of the wires was around $8\,\mu$m.

2.2. Fabrication

The devices produced for this study were fabricated in three separate rounds of lithography using two different electronic beam lithography (EBL) systems. The

overall procedure was the same for all three rounds, varying only in some of the intermediate steps. A detailed recipe, including each of the intermediate steps in the standard procedure, can be found in Appendix A. The overall purpose and the materials used for each round are as follows:

Round 1: In the first round, the foundation for about 60 chips was produced in a single batch[2] on a piece of heavily doped n-type silicon (Si) wafer capped with a 500 nm silicon oxide (SiO_2) layer. For this initial round, the electron beam lithography (EBL) system used to expose the double layer electron beam resist was the Raith eLiNE system located at HCØ. The pattern for the foundation will be discussed in Section 2.2.2.

Round 2: In the second round, the contacts to the aluminum encapsulation around the InAs nanowires are formed. The NW's were deposited on batches of typically 4 chips. The contacts were defined into a double layer resist using the Elionix electron beam lithography system (ELS-7000).

Round 3: In the last round, the normal contacts in the center region were produced. For this, the chips prepared in round 2, were covered by a single layer of resist. After defining the areas for the normal contacts by EBL, the shell was removed by chemical wet etch at the corresponding region.

The general workflow for the steps involved in round 2 and 3 is summarized on Figure 2.2.4. In (a) the nanowire was deposited onto the substrate and both were covered by a double layer of resist (PMMA/copolymer) and the areas of the contacts to be formed are exposed to electron beams. In (b) the exposed regions are removed by development, and the substrate is covered by a metal layer (c). After lift-off (d) the resist has been removed together with excess metal on top of the masking resist, leaving only the metal that makes up the contacts. To form the normal contact in the center part, the chip is covered by a single layer of resist and exposed with electron beams (e). The Al shell around the wire is then etched, which leaves an undercut between the wire and the resist (f) and the chip is cov-

[2]Supervised by Anders Jellinggaard. Anders, as well as other colleagues and students, received several of these chips for their studies. In total, around 17 chips where used in this study.

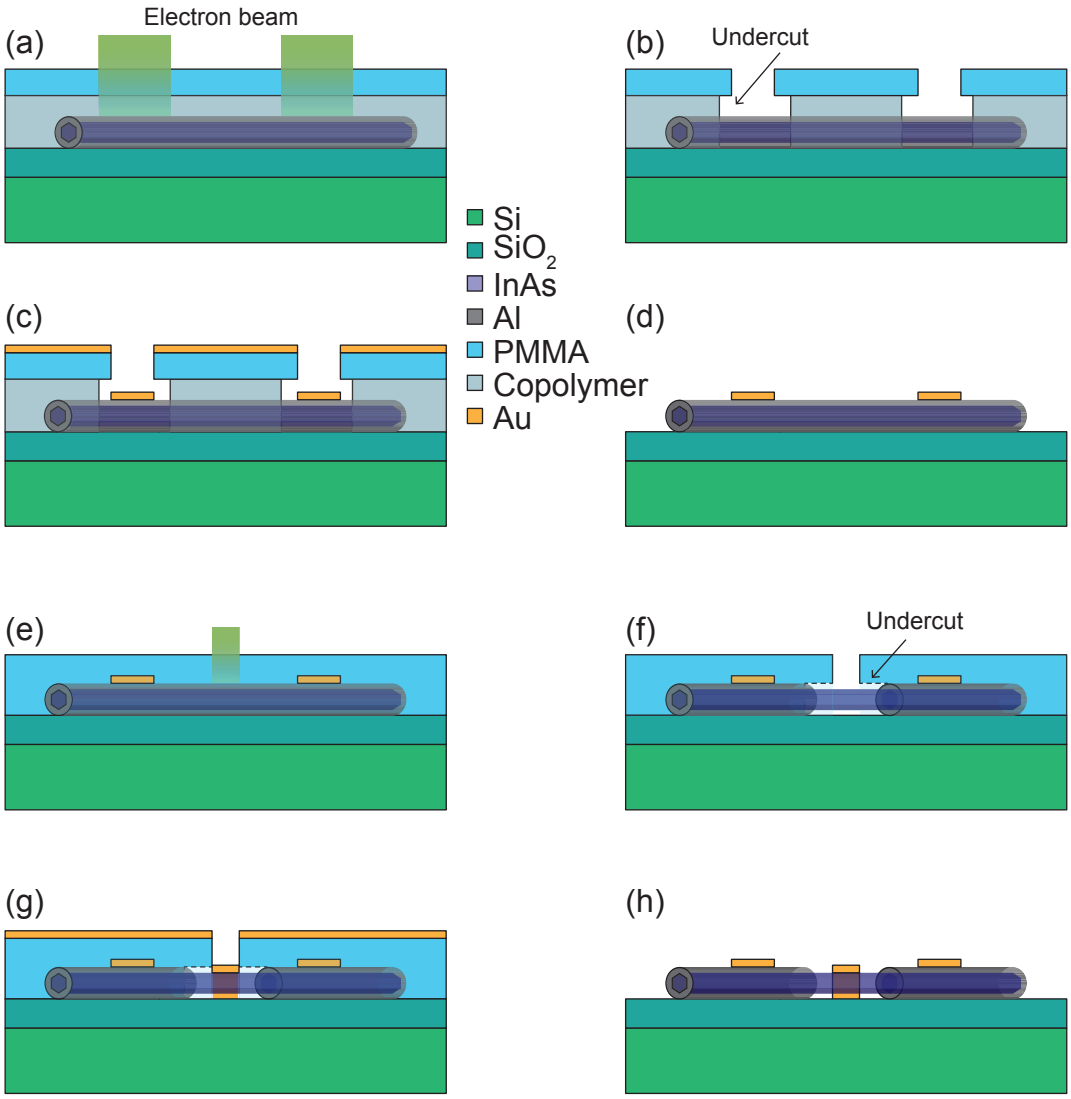


Figure 2.2.4.: Schematic overview of the steps involved in electron beam lithography. The substrate has been covered by a double/single layer of resist in (a) and (e), respectively, which is then exposed to electron beams. The exposed regions are developed (b,f). In (f) the Al shell is etched. The chip is then covered with metal in the evaporation chamber (c) and (g) and the excess metal and the resist is removed, lift-off (d,h).

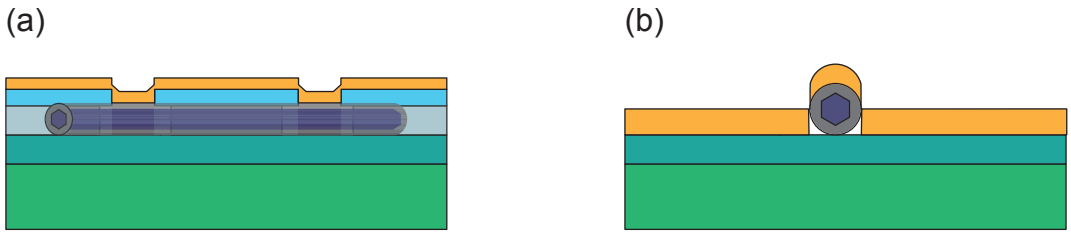


Figure 2.2.5.: Schematics of the result when the resist is too thin compared to the thickness of the metal layer (a). The metal is connected between the masked and unmasked regions and might prevent lift-off. (b) The reason why the metal layer has to be of a certain thickness to contact (and hold onto) the nanowire.

ered by a metal layer as before (g). After liftoff (h), the chip is ready for electrical measurements at the probe station. To measure the chip at ultra-low temperatures, it has to be bonded to a chip carrier suitable for the socket used at the respective cryostat. An example of a chip (*D19*) bonded to a chip carrier is shown on Figure D1 together with two SEM images showing the the bonded chip at higher magnification as well as a magnification of the device *Dev3*, which has been measured in one of the cryostats. In general, it is crucial to choose the thickness of the resist to fit the problem at hand. The first batch of chips that was produced had too thin a resist layer, which resulted in lift-off problems. Out of the 4 chips, with 10 devices on each, only one device was successful. The first chip had lift-off problems in which the metal in some of the areas between the contacts could not be removed, so the devices where shorted (Figure C1). The second chip had stitching-faults, so all nanowires were missed; the developed chip was covered by a 10 nm Al layer to visualize how the resist covers the NW (Figure C2 and Figure C3). On the third chip, all nanowires except one were ripped off. The remaining NW was measured in one of the cryostats, and a tilted SEM image is presented on Figure C5. At the position of a different device, the nanowire was found lying almost across two of the contacts and it is seen where the wire was covered by the metal (Figure C4). From these images it was clear that the resist was too thin, compared to the NW diameter and the thickness of the metal contacts. Too thick of a metal layer results in lift-off problems (Figure 2.2.5(a)), a too thin metal layer does not cover the NW sufficiently to hold it in place and to achieve good contact (Figure 2.2.5(b)). So in this case, the two effects were balanced so that most of the wires were removed. The

last chip of this batch had no NWs left after lift-off. The following batches were produced with a thicker resist layer which resulted in a much better yield, where (almost) every device was successful and functional.

2.2.1. Electron Beam Lithography

This section covers the working principles in and the processes involved for electron beam lithography (EBL). EBL is typically used when high-resolution lithography of fine (submicron or nanoscale) features is needed and it was the only lithographic technique used in this study.

In electron beam lithography, patterns are defined by focused high-energy electron beams into a layer of resist which has been applied onto a substrate. The resist is typically made up of a single- or multi-layer of polymers, such as indicated on Figure 2.2.4 (a), where the upper layer consist of *polymethyl methacrylate* (PMMA) and the lower layer of a copolymer. NANO™ PMMA provided by MicroChem Corp. [3] (MCC) was used in this study and it consists of PMMA polymers (950,000 MW), in anisole solution.[16] When the solution is applied on a surface and the solvent evaporates, the residue forms a stable polymeric layer. The long polymer chains are partially destroyed or shortened in regions radiated by electron beams; this is called exposure (Figure 2.2.4 (a) and (e)). These weakened regions are then easily removed by a methyl isobutyl ketone (MIBK) solution with isopropanol (IPA); this is called development (Figure 2.2.4 (b) and (f)). The non-radiated regions remain during development and act as the masking layer to the underlying substrate. This is known as a positive resist, in contrast to negative resists where the radiated regions remain as masking layer and the non-radiated regions are removed during development. The copolymer consists of several kinds of shorter (lower MW) methyl methacrylate (MMA) polymer chains which are weaker against the MIBK developer. Exposure and development of a double-layer resist, as in this example, results in an undercut as indicated on Figure 2.2.4 (b). Typically, the substrate with the masking resist on top is then covered by a layer of metal (Figure 2.2.4 (c) and (g)) followed by lift-off in solvents like MCC's Remover PG or acetone (Figure 2.2.4 (d) and (h)). The undercut allows the solvent to access the resist more easily and improves lift-off quality.

[3] MicroChem Corp., Newton, MA.

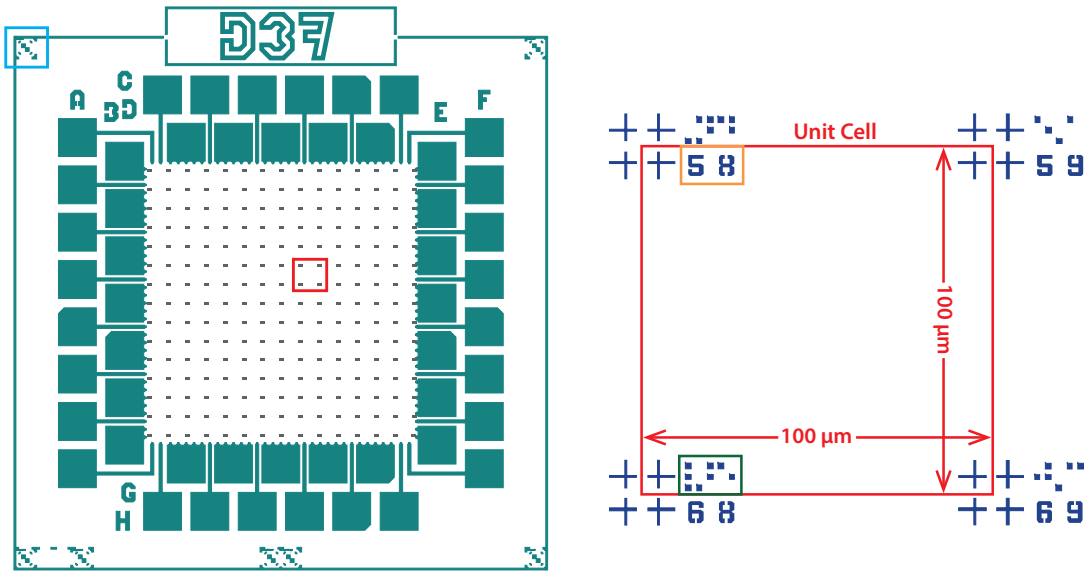
2.2.2. Alignment marks

This section presents the layout used in the first fabrication round to produce the chips, which are the base for all further device fabrication. As mentioned, the substrate was a heavily n-type doped silicon (Si) wafer capped with a 500 nm silicon oxide (SiO_2) layer. A doped wafer was chosen as it can be used as a global back-gate and the oxide layer prevents current to flow between the back-gate and the devices.

The template for the chips consisted mainly of alignment marks (blue square), bonding pads (green filled squares) and a coordinate grid as seen on Figure 2.2.6a. All three of these essential structures were produced within a single fabrication round as none of the structures were overlapping. Furthermore, the layout included alignment marks and names for each of the fields in the coordinate grid, names for each row of bonding pads, 8 rows named by $A, .., H$, (52 bonding pads in total) and a field in the top middle for naming each chip individually. The dimensions of the chip are 2.8 mm $\times$ 2.8 mm.
The grid in the central region consists of 14×14 unit cells (uniform squares with side lengths of 100 μm), each named by coordinates in the xy-format where $x, y = 0, .., 9, a, .., d$, e.g. $xy = 58$ as seen in the top left corner on Figure 2.2.6b (orange rectangle). In the button left corner (green rectangle) the corresponding binary barcode is shown, which consists of three rows with each five bits. The barcodes simply count binary up to 196, giving each unit cell an individual number.

After the chips have been produced by standard electron beam lithographic methods as described above, the NWs were deposited and investigated under an optical microscope (OM). Images were captured for interesting unit cells which have to fulfil the criteria of containing at least one isolated and fairly straight NW. The captured images were then processed by a Python script[4], which automatically crops the images to the size of the unit cell and produces a macro file for loading the images to their right position in a DesignCAD layout file. The next step was the so-called routing, which is the process of "drawing" the contacts between the bonding pads and the leads at the nanowires. The design of the leads will be discussed next.

[4]Written by Anders Jellinggaard, very useful!



(a) Layout **(b)** Unit Cell

Figure 2.2.6.: Overview of the chip layout (a) and a single unit cell (b). The chip layout consists of 52 bonding pads (green filled squares) surrounding the 14×14 unit cells (red square) and a set of alignment marks in each corner (blue square). Furthermore, each chip has an individual name (D37 in this case). The side length of a unit cell is $100\,\mu$m and is defined by a cross in each corner (here in blue) as well as its coordinate with respect to the other unit cells (written in numbers in the upper left corner (orange rectangle) and as binary code in the lower left corner (green rectangle)).

2.2.3. Contact design

This section describes the layout of the leads contacting the nanowires and the aluminum shells. The leads have been designed to be as flexible as possible, leaving options open for different kinds of measurements at different stages of the fabrication process as described later. In total, five contacts are formed to generate four contacts to the superconducting shell (referred to as superconducting contacts) and one normal contact. The contacts consist of a Ti/Au (typically about 5/125 nm) layer on top of the Al coating for the superconducting contacts, whereas the coating has been removed for the normal contacts. The standard template for the contacts is shown on the right side of Figure 2.2.7, where the four orange/brown colored contacts indicate the superconducting contacts and the cyan colored the normal contact.

The width of the contacts was chosen to be rather large, to ensure that the gap between the contacts is as parallel as possible over a larger area, so that small misalignments would not affect the quality of the contacts. The width of the innermost superconducting contacts and the spacing between two superconducting contacts on one side were both set to 500 nm. The initial design of the normal contact had a width of 500 nm as well and the distance to the innermost superconducting contacts was typically of 1.3 μm. In a second design the normal contact in the middle was divided into two separate contacts with a width and spacing of 300 nm as seen on the left side of Figure 2.2.7. The superconducting and normal contacts had to be produced in two separate lithographic steps, as the aluminum shell had to be etched chemically to reach the InAs NW. To ensure that ohmic contact to the shell was achieved, the devices were measured in the probe station when the four leads to the shell were formed before continuing with the fabrication. To investigate the transition from the normal-metal to the superconducting state of the shell, some of the devices with the shell still intact were measured at ultra-low temperatures and the results are presented in the corresponding chapter below.

2.2.4. Ion Milling

This section presents the main aspects of ion milling which is one type of dry etching, and it is concluded by the results from a test series which was used to estimate a suitable milling time for device fabrication. In situ ion milling prior to

Figure 2.2.7.: Template of the two different kinds of contact layouts on top of optical micrographs of the nanowires (the colors have been inverted for clarity). The contacts are outlined in orange/brown and cyan to indicate the superconducting and normal contacts, respectively. On the left side two normal contacts are drawn as described in the text; the right side contains only one and it was this template used the most.

metal evaporation is a very useful tool to produce ohmic contact to metals and semiconductor materials, as they are usually covered by a stable native oxide. This native oxide is formed immediately as the material comes in contact with the oxygen in the atmospheric air. It has often been a great task to remove the insulating oxide by wet etching and passivation to achieve good and reproducible ohmic contact. In situ ion milling is a good solution around this problem as it is a fast and easy way to remove a oxide layer directly in the ultra-high vacuum chamber of a evaporation system, without the breaking vacuum before metal evaporation.

The two AJA[5] evaporation systems, situated at the Center for Quantum Devices, NBI, are of the ATC ORION type and are equipped with two different ion milling systems. Both systems have some custom extensions (such as rotating sample stage, sample heater, just to name a few) and their base pressure is around $8 - 10 \times 10^{-8}$ Torr. The working principles behind the two ion sources are quite different; while the ions are produced by a Kaufman DC source in one of the system, the other system produces RF plasma. Although other gases where available, only argon was used as ion source. Figure 2.2.8 shows a sketch of the Kaufman DC discharge ion beam source configuration. The argon gas is led into the discharge chamber where it is ionized by the potential difference between the cathode filament and the anode. The ionized argon atoms are then accelerated through a grid and form the ion beam which is directed to the target substrate. To prevent the substrate from charging by

[5]AJA International, Inc., N. Scituate, MA

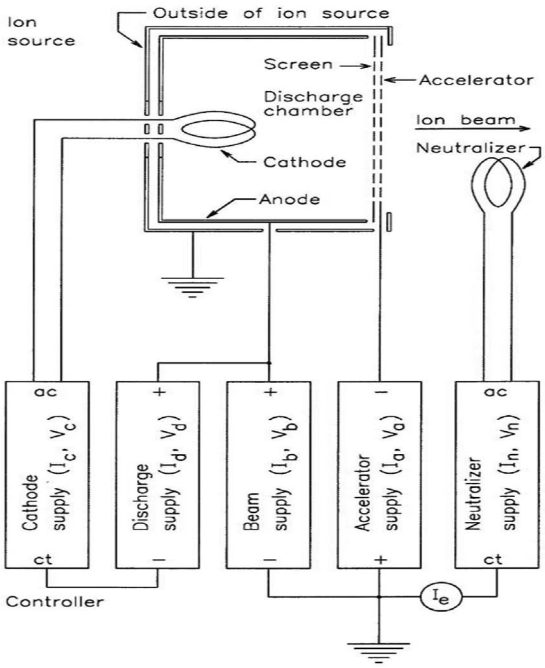


Figure 2.2.8.: Schematic drawing of KRI's Kaufman DC discharge ion beam source. Adapted from KRI's brochure[17].

the positive argon ions, a second filament is placed outside the discharge chamber, producing electrons which are sent along with the ion beam. When the argon ions have sufficient energy on collision with the substrate, atoms or small molecules are kicked out from the substrate surface. At the same time, some rearrangement of the surface particles is likely resulting in a smoother surface. On the other hand, there is a chance that some argon atoms are implanted into the substrate which in general is unwanted.

Table 2.1.: Standard set point values of the Kaufman Source Controller (at 300 V).

	Cathode	Discharge	Beam	Accelerator	Neutralizer	Emission
Voltage	$\approx 7\,\mathrm{V}^*$	40 V	300 V	120 V	$\approx 8.8\,\mathrm{V}^*$	
Current	7.0 A	0.5 A	23 mA	50 mA	11 A	46 mA

*These values are measured only.

To estimate the milling rates for PMMA, SiO_2 and Al/Al_2O_3, a test series was carried out on a set of samples, which were prepared on the same kind of substrate as used for the actual chips. The test substrate was spin-coated with 6% copolymer

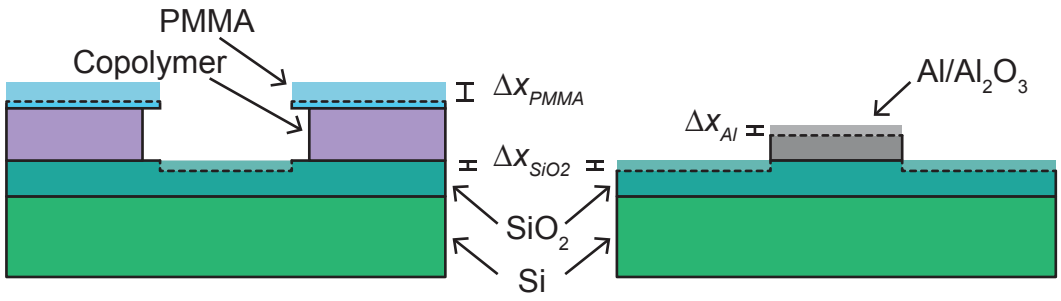


Figure 2.2.9.: Sketches of the two types of test samples for ion milling, indicating the differences thicknesses of the PMMA, aluminum and SiO_2 before and after ion milling.

and 4% PMMA and several squares were defined by EBL following the standard procedure. After development, the substrate was cleaved and one half was covered with a 50 nm layer of aluminum, followed by lift-off in acetone. The thicknesses of the PMMA and aluminum layers were measured with an atomic force microscope (AFM) before and after milling. To measure the lowering of the substrate (Δx_{SiO2}), the PMMA was removed and the substrate was measured again with the AFM. Figure 2.2.9 shows sketches of the test samples before and after milling and the different heights are indicated. The net change in height of PMMA (Δx_{PMMA}) and Al/Al_2O_3 (Δx_{Al}) could then calculated by subtracting the change in the substrate from the sum of the combined changes as it is the quantity measured with the AFM. Two different milling times were tested using the Kaufman ion source with identical parameters, as summarized on Table 2.1; the usual parameter which might be changed is the beam voltage, however it was always set to 300 V for this project. The results of the measured rates are presented in Table 2.2. The rates were expected to be somewhat linear with time, but this could not be concluded as only two tests were performed. However, the goal was to achieve an estimate of the rates to predict suitable milling times to remove the aluminum oxide for good contacts, without removing too much material. Only one test was performed with the RF plasma and it seemed as if nothing of the Al was etched, so that technique was not considered further.

2.2.5. Wet Etching

In this section the considerations and results for chemical wet etching of aluminum are presented. As discussed in Section 2.2.1, the aluminum shell has to be partially

Table 2.2.: Height difference Δx after Ion Milling for the indicated times.

Milling time	SiO_2	PMMA	Al/Al_2O_3
1 min	~ 3 nm	~ 23 nm	~ 3 nm
3 min	~ 8 nm	~ 55 nm	~ 8 nm

removed to be able to obtain a normal contact on the nanowire. The wire is covered by the shell all the way around the circumference, so to remove it from all sides it has to be attacked from every direction equally. As ion milling is anisotropic, i.e. reacts only from one direction, it would never be possible to remove the shell entirely between the wire and the substrate (Figure 2.2.10 (a)).

As no other etching technique was available or suitable, such as electrolytic/electrochemical etching[18],[19] or dry etching, the strategy was to wet etch the shell in solution. The advantage of the wet etch is that it is very likely to "over etch", creating an undercut as indicated on Figure 2.2.10 (b). This undercut allows for direct metal evaporation after the etch without the need of further lithography (Figure 2.2.4 (f-h)). Whitesides et al.[20] have been able to produce reproducible etch trenches down to 50 nm in thin films of chromium and aluminum. One of their conclusions was that a minimum amount of undercut is unavoidable when the film has to be etched all the way down to the underlying substrate. In the context of this study, however, the shell is rather thin compared to the desired undercut so the etching rate and time had to be adjusted to produce the desired length of the "bare" wire after the etch. Normally, aluminum is isotropically wet etched which means that the etching rate is the same regardless of the crystal orientation. This typically results in round edges in the direction of the under-cut (Figure 2.2.10), which would result in a smeared transition from the shell to the wire, which has been observed in some of the tests and it seems to be dependent on the etching temperature. However, as aluminum etching is highly exothermic, a local increase in temperature is expected at the reaction sites covered by the PMMA. The etching rate of aluminum etchants is very temperature sensitive, so a local increase in temperature will result in a higher etching rate in the undercut region. For this reason the theoretical etching rates were not directly applicable and a thorough test series was needed to estimate the effective rates.

Previous etching tests with buffered hydrofluoric acid (BHF) performed by Thomas

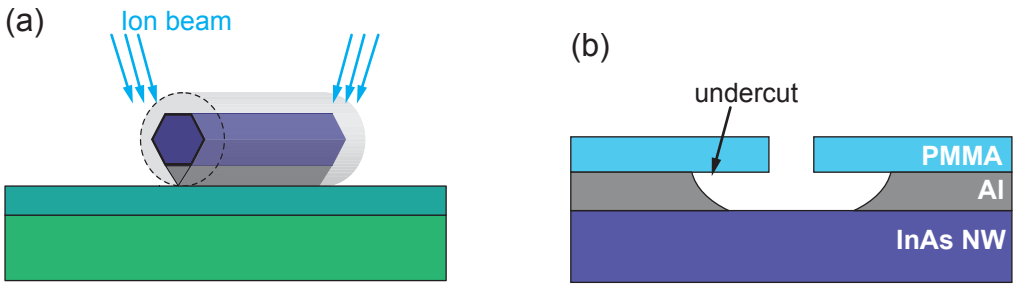


Figure 2.2.10.: (a) Sketch of a core/shell InAs/Al nanowire on the substrate. It illustrates the expected residue of the shell when it was to be removed by anisotropic etching, such as ion milling, as the ion beam cannot be applied parallel to the substrate. (b) Sketch of the effect of isotropic wet etching. The undercut is indicated and it is this region where the temperature, and hence the etching rate, is locally increased.

Table 2.3.: Transene Aluminum Etchant etching rates at different temperatures given by the manufacturer[21].

	Type A	Type D
Temperature	Rate [Å/s]	
25 °C	30	40
40 °C	80	125
50 °C	100	200
65 °C	240	–
75 °C	550	–

S. Jespersen on the same type of core/shell InAs/Al nanowires, showed that there is very little control over the amount of undercut. Even with diluted and cooled BHF the results were far from reproducible. However, the sharp edge formed at the transition from the shell to the "bare" wire was quite reproducible. For comparison, one chip (*D12*), with two devices on it, was etched using BHF at room temperature. Dipping the sample into the BHF for $1-2\,\mathrm{s}$, followed by neutralization in two baths of DI water and IPA, for 30 s each, resulted in undercuts ranging from $0.75\,\mu\mathrm{m}$ to $1.1\,\mu\mathrm{m}$. The desired undercut is around 200 nm, so a much slower reaction, e.g. by a weaker etchant, was needed. Transene[6] offers three types of aluminum etchants; Type A is designed for general purpose Al etching, Type D for GaAs and GaP devices and Type F is designed for etching AlSi materials. Type A etchant contains nitric acid (HNO_3) to oxidize the aluminum and phosphoric acid (H_3PO_4) to dissolve the formed aluminum oxide. However, the nitric acid attacks InAs as well, which is undesirable. Type D is nitric acid free; instead, Sodium-M-Nitrobenzene Sulfonate is used to oxidize the aluminum, making it compatible with GaAs, GaP and presumably InAs as well, which is why it was used for the test series. The theoretical etching rates at different temperatures given by the manufacturer are presented in Table 2.3. For the test series, 4 chips were prepared with the same type of nanowires as described above, however only the part of the pattern for the normal contact was exposed. The chips were cleaved into smaller pieces after development so that more tests could be implemented. Prior etching, most of the chips were ashed with oxygen plasma to remove residues of the resist in the developed regions. Etches at different temperatures and for different times were tested and in general the room-temperature chip was dipped into the warmed/cooled etchant for the respective time, followed by rinsing in a bath of DI water at room temperature. Only in one case the method suggested in the paper by Whitesides et al. was tried, but it was unsuccessful. (Their approach was to apply a droplet of the warmed etchant to the chip at RT).

After etching, the PMMA was removed with acetone and the wires were investigated in a scanning electron microscope (SEM). An example of such a SEM image is presented in Figure 2.2.11 clearly showing the etched region and the transition from the InAs wire to the shell. The insets show higher magnifications of the two

[6] Transene company Inc., Denvers MA

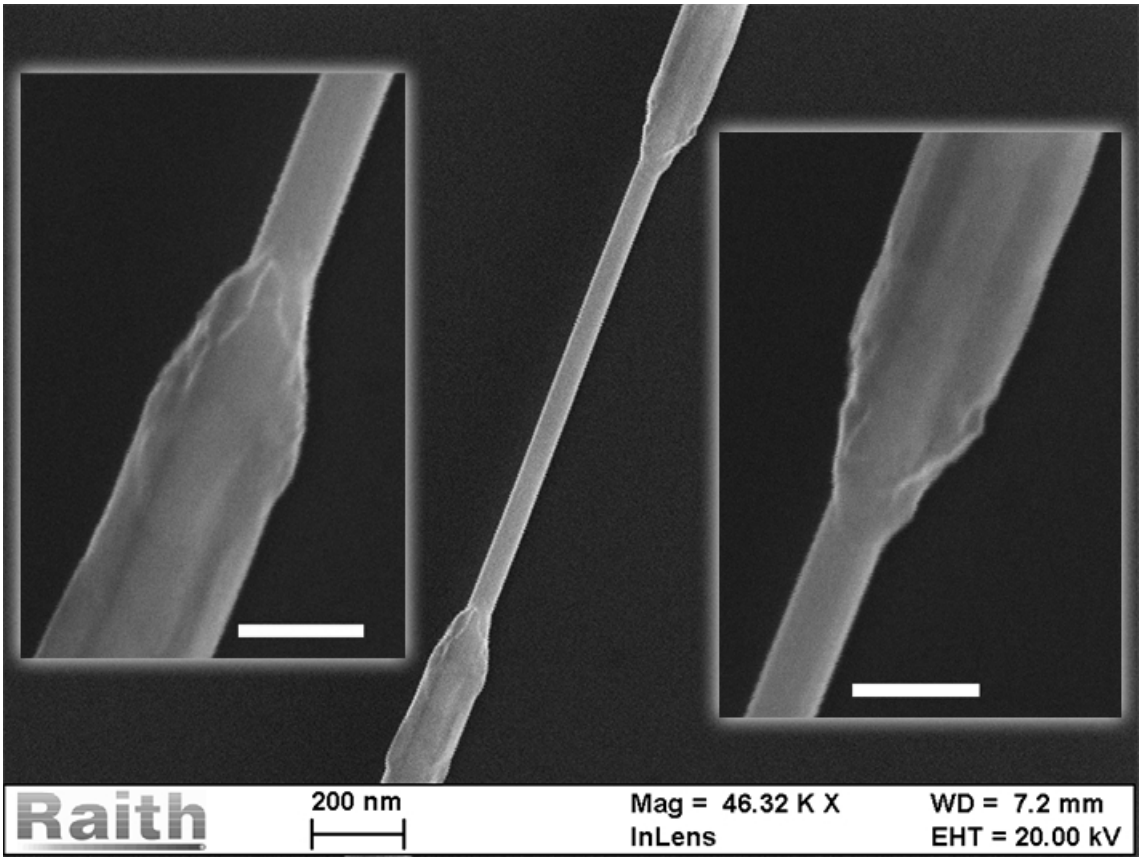


Figure 2.2.11.: Scanning electron micrographs of a nanowire where its shell has been etched away in the central part. The two insets show higher magnifications of the two transitions, and the scale bars correspond to 100 nm).

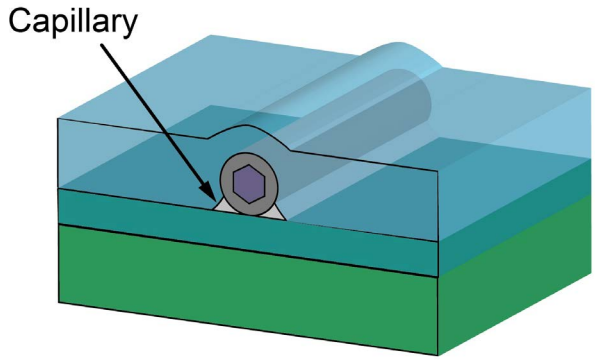


Figure 2.2.12.: Sketch of an InAs nanowire with Al shell on the substrate covered by a layer of resist. The capillaries indicated along the NW are expected to gain access of the etchant to the sidewalls of the shell.

transitions. The length of the etched segment was measured to be around 1 μm (Test 11 in the table below) and the diameter of the wire, with and without shell is around 125 nm and 52 nm respectively. The V-shaped structure of the transition was observed for most of the etched wires and might be explained by the assumption that the resist does not cover the wires "tightly" all the way to the substrate, but rather leaves small capillaries open along the wire (see Figure 2.2.12), allowing the etchant to access the sidewalls of the wires more easily. One way around this issue could be to post-bake the chip after development, letting the PMMA reflow around the wire. However, this would make it unsuitable for direct metallization after the etching as the softening of the PMMA-edges could prevent lift-off.

The results from the test series are summarized on Table B.1 in the appendix, where the undercut rate was estimated from the average length of the etched segments, Δx_{ave} by: rate $= (\Delta x_{ave} - 500\,\text{nm})/2t$, where the 500 nm is the width of the opening of the resist and t is the etching time in seconds. The best results were obtained by dipping the chip (from RT) into the etchant (at 55 °C) for 10 s, which resulted in an over-etch of around $200 - 250$ nm.

2.3. Measurements

This section is about the setups and measuring instruments used for the electrical measurements on the devices. Firstly, all measuring instruments will be introduced and typical applications will be presented. Secondly, a short introduction to dilu-

tion refrigerator will be given and lastly, at the end of this section, the setups for the electrical measurements, at the probe station as well as the cryostats, will be explained.

Lock-In Amplifier Stanford Research Systems[7] Lock-In amplifiers Model SR830 DSP were used for low noise measurements on the samples in the cryostats. One of its major advantages is the ability to extract a signal from a noisy background by relating it to a carrier wave of known frequency. In its main operation mode, a lock-in amplifier generates the carrier wave (AC signal), which can be added to a DC bias for the measurement. The measurement results are then extracted, while suppressing most of the surrounding noise.

Voltage source Keithley 2400 SourceMeter[8] was the voltage source used at the probe station. It is a low noise and high precision voltage and current source with the capability to be used as multimeter. It has a General Purpose Interface Bus (GPIB) interface for communication with a data acquisition and control computer. As it was configured to measure the outgoing current with respect to ground (GND), it was not suitable to measure the current through the devices in combination with a voltage divider (through which the majority current runs directly towards GND).

Current preamplifier The Ithaco Current Preamplifier Model 1211[9] was the main instrument to measure the currents. The basic principle is that it measures an input current and converts it to an output voltage, with conversion sensitivity ranging from $1 \times 10^{-3}\,\mathrm{A/V}$ to $1E-11\,\mathrm{A/V}$. The output voltage can then be measured with a digital multimeter connected to the acquisition computer, where the corresponding current can be calculated using the sensitivity set at the preamplifier. These preamplifiers are henceforth referred to as Ithacos.

Digital Multimeter Agilent 34401A Digital Multimeter[10] (DMM) was mainly used to measure the signal voltage from the Ithacos or to measure the output signal from

[7] Stanford Research Systems, Inc., Sunnyvale, CA.
[8] Keithley Instruments, Inc., Cleveland, OH, USA.
[9] DL Instruments, LLC, Ithaca, NY, USA.
[10] Agilent Technologies, Inc., Santa Clara, CA, USA.

some of the Lock-in amplifiers. It has a GPIB interface for readout at the acquisition computer.

Preamplifier The LI-75A Low Noise Preamplifier[11] was used at one setup (Triton 1) to increase the measurement sensitivity at the lock-in amplifier. It has two main application modes, one where only a single input is directly amplified and another where the differential voltage, between two input-signals, is amplified.

2.3.1. Probe Station

The first electrical measurements, on each chip that passed the lithographic procedures successfully, were performed at a probe station. A probe station is a relatively simple setup that allows electrical measurements directly on the bonding pads of a chip without the need to wire-bond the chip to a chip carrier. The advantage of a probe station lies in the flexibility of the probes, thin metal needles attached to cantilevers, which are freely movable over the extent of the chip, so that the quality of several devices can be analyzed in short time. This way, faulty devices can be detected before the chip is bonded. The chips produced for this study, usually contained 10 devices, usually with 5 contacts on each device. However, the number of pins on the chip carriers was either 14 or 24, so the devices of highest quality had to be found by probing before bonding. The probe station used (for most of the chips) was a LakeShore Model TTPX Cryogenic Probe Station[12], which is equipped with 6 probes, and the bottom plate could be used to contact the back gate. The sample can be placed in vacuum and it is possible to cool the chamber to 4 K by liquid helium. However, as the transition temperature for aluminum to become superconducting is around 1.2 K, this last feature was not used. The main goal at the probe station was to check for ohmic contacts on the intact shell and at a later point to see the back gate dependency of the nanowires after the shell has been etched away in the center part.

The setup for these measurements is sketched on Figure 2.3.13. A DC bias was supplied by a Keithley voltage source which was connected to the input of a voltage divider (VD) (10,000:1), the VD output was connected to one of the probes con-

[11] NF Corporation, Yokohama, Japan.
[12] Lake Shore Cryotronics, Inc., Westerville, OH.

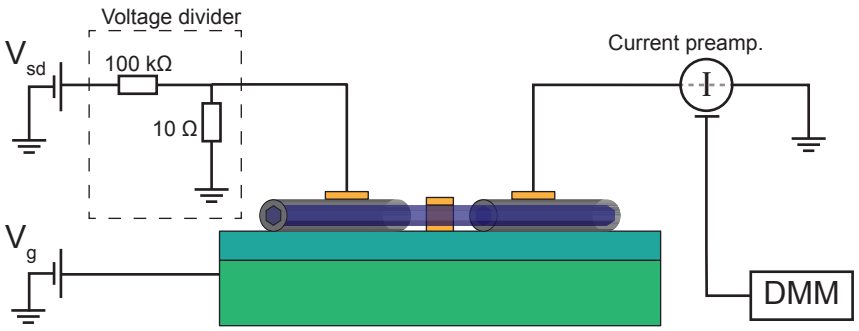


Figure 2.3.13.: Schematic diagram of the setup at the probe station. The voltages V_{sd} and V_g are provided by two Keithleys. The current is measured, as a function of the source-drain bias, through a current preamplifier which is connected to a DMM. The Keithleys and the DMM are controlled by the acquisition computer via a GPIB connection.

necting one of the contacts on the shell. The current flowing through the shell was then measured with another probe that was connected to a current amplifier. The signal from the current amplifier was then measured with a DMM. The resistance through the setup and device could then be calculated from the slope on the I-V curve[13]. For back gate dependence measurements, a second Keithley was connected to the bottom plate of the probe station, which was in contact with the substrate.

2.3.2. Cryofree Dilution Refrigerator

For the low temperature measurements three different cryofree dilution refrigerators were used: Triton 1 and 3 produced by Oxford Instruments plc[14] and a cryostat by Leiden Cryogenics B.V.[15] (which will be referred to as Leiden). Dilution refrigerators are often used when ultra-low temperatures (well below 1 K) are required as they are capable of reaching temperatures as low as 10 mK. The general working principle of a so-called wet dilution refrigerator will be explained based on the sketch seen in Figure 2.3.14. The setup consists of several stages where a flow of ^{3}He isotopes is steadily cooled until it reaches the lowest temperature in a mixture with liquid ^{4}He isotopes. At the beginning of the ^{3}He cycle, the gas is pumped into the condenser where it is pre-cooled by a pumped ^{4}He bath (at around 1 K) so that

[13] The in-line resistance has to be measured as well, e.g. by placing the probes on the same bonding pad, as it adds to the resistance.
[14] Oxford Instruments plc, Abingdon, Oxfordshire, United Kingdom.
[15] Leiden Cryogenics B.V., Leiden, The Netherlands.

it liquefies. To maintain the pressure in the condenser and to control the flow of the liquid ^{3}He it passes through a constriction (also called impedance) which can either be fixed or adjustable. The ^{3}He is then further cooled by a heat-exchanger connected to the still (or as seen on the sketch, it is led through the still tank). The ^{3}He then passes through the inner tube of a counterflow heat exchanger where the mixture from the mixing-chamber flows in the outer tube. It is led into the mixing chamber where it mixes with ^{4}He. When the temperature in the mixing chamber drops below 0.87 K, the two isotopes undergo a transition into two separate phases; a upper phase of (almost) pure liquid ^{3}He (rich phase) and a denser lower phase consisting of a mixture of ^{4}He with about 6-10% ^{3}He. The mixture of the lower phase flows through the heat exchanger into the still where it is heated to about 0.7 K to distill the ^{3}He from the mixture. At this temperature the vapor pressure of ^{4}He is much lower than that of ^{3}He, so the evaporating gas is almost pure ^{3}He and only a steady minor background of ^{4}He present in the rest of the cycle. The gas is then pumped out and reenters the system at the condenser. The cooling power to reach ultra-low temperatures in the mixing chamber occurs at the interface between the two phases: as the ^{3}He concentration in the lower phase is reduced by pumping it out in the still, the equilibrium is maintained by quasi-evaporating ^{3}He from the upper phase into the lower, which is a endothermic process. This constant flow of ^{3}He in a closed loop through the system allows for very stable low temperatures. All of the low temperature regions throughout the system are surrounded by several high-vacuum chambers and heat shields to shield it from the surrounding room temperature. Furthermore, the systems are often immersed in liquid ^{4}He or liquid nitrogen to shield it even more.

All three cryostats, used in this study, are of the so-called dry dilution refrigerator type, which, in contrast to the wet type, do not consume any liquid cryogens such as nitrogen or helium during operation. The working principles are almost identical and the main difference in the setup is that in the pre-cooling stage, the pumped ^{4}He bath is replaced by a pulse tube cooler capable of reaching about 4 K. As this temperature is not sufficient to liquefy ^{3}He at the usual pressure, a compressor is needed to increase the pressure at the condenser. The higher pressure increases the temperature at which ^{3}He enters the liquid state. Furthermore, the pulse tube cooler is used to replace the surrounding ^{4}He bath, so that no cryogen is consumed. However, the systems might deviate slightly in the general setup as the dry type is

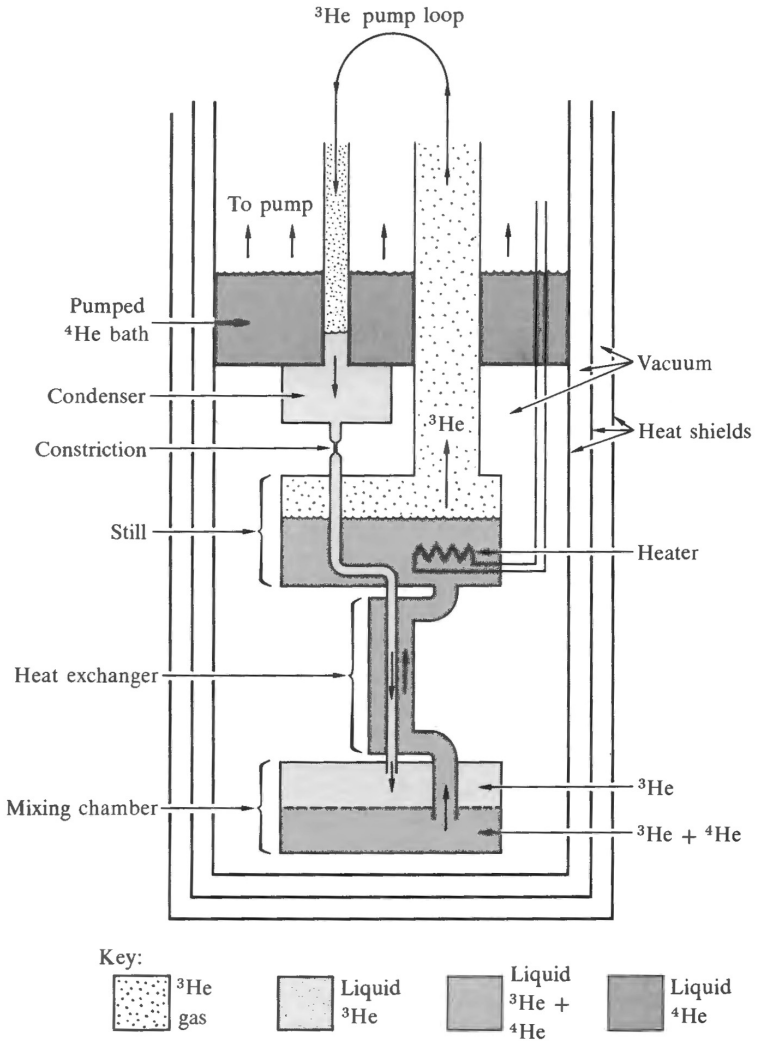


Figure 2.3.14.: Schematic overview of a dilution refrigerator showing the flow of ^{3}He through the system. Details are found in the main text. Figure adapted from[22].

the newer invention. So there might, for example, be more constrictions and heat exchangers along the way to the mixing chamber to increase the cooling efficiency.

The two Triton cryostats have a theoretical base temperature of 10 mK and are both equipped with a 3-axis vector magnet. The maximum fields in the X-Y-Z-directions are 1-1-4 Tesla and 1-1-6 Tesla for Triton 1 and Triton 3, respectively, where the Y- and Z-directions are parallel with the substrate plane. The third system, the Leiden cryostat, is equipped with a 12 Tesla magnet and has a theoretical base temperature of < 25 mK. Its magnetic field is fixed to the vertical axis at the sample-position and parallel to the substrate plane; however, it has a home-made sample holder with a piezo-motor driven rotation stage which makes the socket rotatable in the substrate-plane. This convenient feature makes it possible to align a nanowire on the substrate to be either parallel, perpendicular or at any arbitrary angle to the magnetic field.

2.3.3. Low Temperature Measurements

The ultra-low temperature measurements were performed at three different cryostats, as mentioned above: Triton 1, Triton 3 and Leiden.

In total, six devices were measured at low temperatures, three of which were on the same chip. The devices measured in Triton 1 and Triton 3 consisted of nanowires with an intact Al-shell of thickness ~ 13 nm (*D19*; 3 devices) and ~ 30 nm (*D38* and *D46*; 1 device each), respectively. For these devices, the electrical resistance of the center part of the shell was measured in a four-terminal configuration.

At Triton 1, the setup consisted of: a lock-in amplifier supplying the 10 mV AC signal through a 1 MΩ resistor and a set of filters to one of the outer leads of the device. The other outer lead was grounded, as the current is expected to be known (within a few %). The voltage drop between two inner leads was amplified with a preamplifier and the differential voltage was measured with the lock-in.

At Triton 3, the setup was slightly more complex: again, a lock-in amplifier supplied the AC signal through a 100 MΩ resistor and a different set of filters to one of the outer leads. The current through the device was measured at the opposite outer lead with the lock-in. The reference output of the first lock-in was connected to a second lock-in, which in turn was connected to the two inner leads to measure the differential voltage across the device.

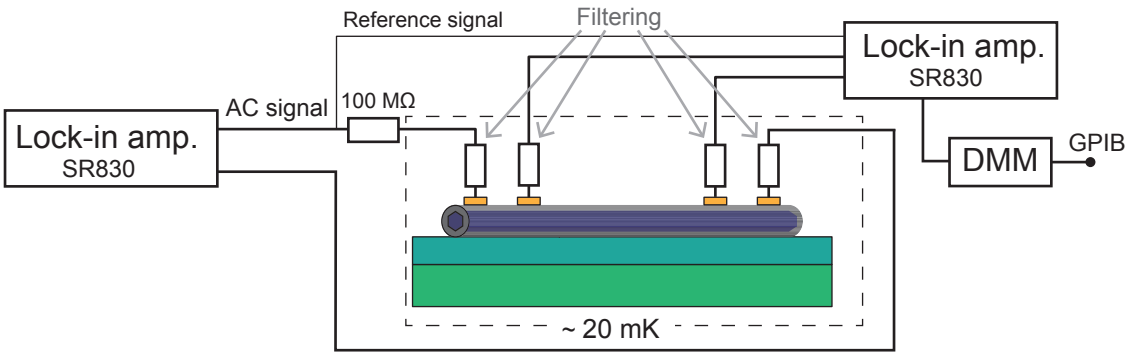


Figure 2.3.15.: Schematic diagram of the setup at Triton 3.

Figure 2.3.15 shows an overview of the setup used at Triton 3. The setup for Triton 1 was as mentioned slightly different, as the differential voltage was pre-amplified and measured with the lock-in directly. A second lock-in amplifier was used to measure a second device at the same time. Despite the differences, the main principle is the same; a current is applied between the two outer leads and the voltage drop between the two inner leads is measured. The large resistor is included for safety reasons to limit the current across the device, whose resistance is much lower, and as the resistor was much larger than the line- and contact resistance, all of these were neglected as they only contributed with a few percent.[16]

The device measured in Leiden consisted of a nanowire with an Al shell, which has been partially removed in the center region by BHF-etching, and it was produced by Thomas following a similar procedure as presented above, however, the oxide on the shell had to be overcome by burn-through. The device had only two contacts to the nanowire, one on each side of the gap in the shell. As the NW is exposed in the center region, the device has a back gate dependency which adds a parameter to be investigated.

The overview on Figure 2.3.16 shows the main instruments used for the measurements at the Leiden cryostat: a lock-in amplifier is used to supply the AC signal, regulated through a voltage divider to $\sim 10\,\mu$V. The AC signal is offset by a DC bias, which is connected to a second input of the voltage divider as indicated in the figure. The DC bias is supplied by the acquisition computer through a NI-DAQ digital-to-analog converter (DAC). The combined signal at the output of the voltage

[16] The resistance of the filters in the cryostat was 2.3 kΩ per line, so a maximum contribution of $\sim 0.5\,\%$ was expected.

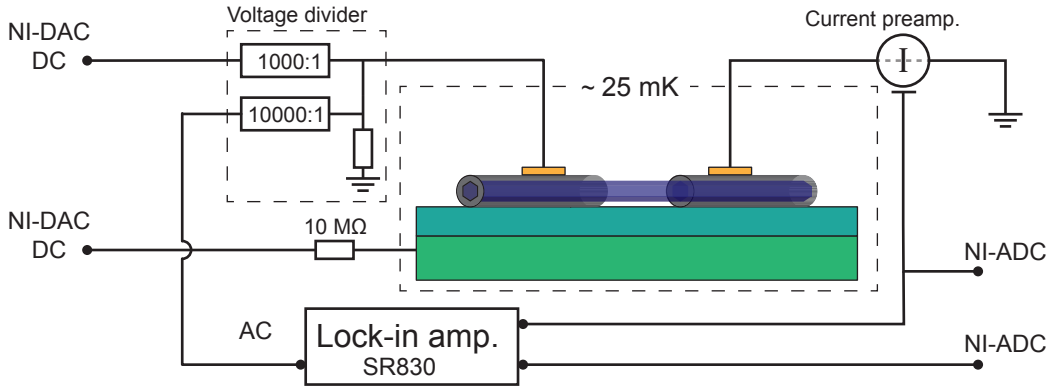


Figure 2.3.16.: Schematic diagram of the setup at Triton 3.

divider is then connected to one of the connectors at the break-out box which leads it down to one of the contacts of the device. The other lead is connected to an Ithaco current preamplifier and the signal is measured both with the lock-in amplifier and the acquisition computer through the NI-DAQ analog-to-digital converter (ADC). The back gate voltage is supplied from a second channel at the DAC and has a 10 MΩ resistor in series, which is inserted for safety, so that any possible leakage current through the back-gate is limited. As this device only allows for two-terminal measurements, the line- and contact-resistances contribute to the results just as the filters would. This is why it was chosen to disable the filters which are installed in the cryostat, as they include large resistors, and the line resistance was neglected.

3. Results and Discussion

This chapter is divided into four parts. The first part is about the room temperature measurements performed in the probe station. The tree following parts consider the results obtain at the three different cryostats.

3.1. Probe Station Measurements

As mentioned in Section 2.3.1, all chips that passed the fabrication process successfully, were initially measured in the probe station to check the quality of the contacts. The measurements at the probe station where all performed at room-temperature and under vacuum.

3.1.1. Intact Shell

To measure the contact-resistance, together with the resistance of the shell, 2-probe measurements were performed between each of the contacts. The setup was as mentioned above; a voltage source was connected to a voltage divider (VD) which in turn was connected, via one of the probes, to one of the bonding pads. A second probe was placed on a second bonding pad of the same device and connected to a current preamplifier. The voltage divider consisted of a large ($R_1 = 100\,\mathrm{k}\Omega$) and a small ($R_2 = 10\,\Omega$) resistor. It usually regulates the voltage across R_L by the division factor (in this case 10000:1, so applying 10 V to the VD results in 1 mV). In general, when using a voltage divider, it is expected that the load resistance R_L of the measured device is much larger than the smallest resistor of the divider $R_L >> R_2$. The resistors were chosen to fit for most of the measurements across a large range of resistances, as the contact resistance to the aluminum shell was

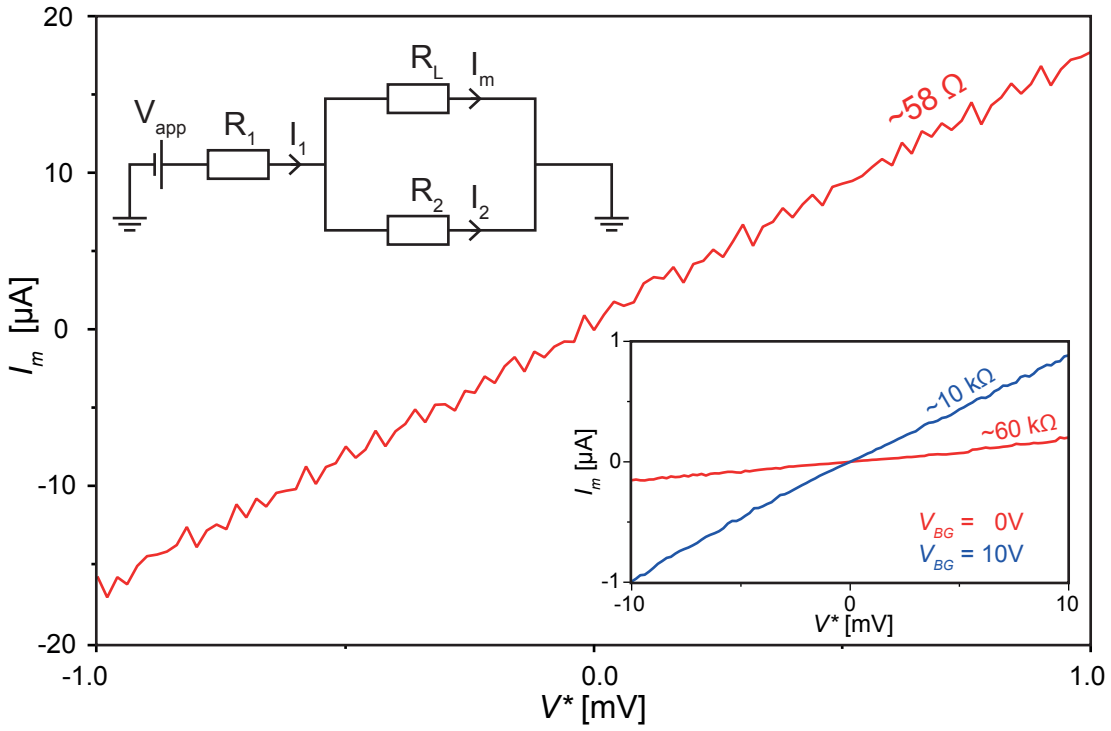


Figure 3.1.1.: Typical $I-V$ curve obtained from the measurements on the Al shells. The upper left inset shows a simplified model a voltage divider, where the sample resistance is R_L. Lower right inset shows two typical $I-V$ curves at different gate voltages for samples where the shell has partially been removed.

expected to be around some hundreds Ohms for good contacts and some kOhms for not so good contacts. However, it turned out not always to be the case as the total resistance often was around 100 Ω for the intact shell. The resistance of the aluminum shell itself was expected to be rather low when the coverage is uniform. A rough estimate of the resistance can be calculated by $R = \rho\, l/A$, where ρ is the resistivity of aluminum, l the length of the shell segment and A is the cross-sectional area. Assuming the shell to be a perfectly uniform hollow cylinder, with inner and outer radius of $r_{in} = 40\,\text{nm}$ and $r_{out} = 70\,\text{nm}$, a segment length of $3\,\mu\text{m}$ and the resistivity of aluminum of $2.74 \times 10^{-6}\,\Omega\text{cm}(at 295\,\text{K}^1)$, the resulting resistance becomes $R \approx 8\,\Omega$. So no large contribution is expected from the shell itself, as long as it is uniform. The line resistance from the coaxial cable connecting

[1]Value taken from C. Kittel, *Introduction to Solid State Physics*[6], chapter 6, Table 3.

the instruments, resistors and the probes is expected to be low as well.

So the main resistance is attributed to the contact resistance between the Al shell and the Au leads, as the aluminum usually is covered by an insulating native oxide. Not so long ago, it was a rather hard task to remove this oxide layer to obtain ohmic contact, as it either had to be removed chemically by etching (e.g. with BHF or $(NH_4)_2S_x$) or, as for the device measured in the Leiden cryostat, it had to be overcome by electrical burn-through. As the latter involves applying a large potential difference between a pair of contacts on the NW, the risk of destroying the device is rather high. This is why a better and more reproducible technique was desired. Fortunately, this problem could be overcome by a new evaporation system, equipped with an ion source for ion milling, which allows for removing the oxide layer immediately prior to evaporation of the metal for the contacts without breaking the vacuum, as discussed in Section 2.2.4. The typical contact resistance was of the order of some tens to a few hundreds ohms. An example of a representative IV-curve is presented on the main graph on Figure 3.1.1. The resistance is easily extracted from these measurements as it corresponds to the inverse of the slope. However, when the resistance of the device is rather low and close to the value of the smaller resistor in the voltage divider, the slope is no longer a function of the resistance of the device alone, as the resistor of the divider contributes to the result. This can be shown by a simple model of the circuitry as shown on the upper inset of Figure 3.1.1. The divider consists of the two resistors R_1 and R_2 and the device is indicated by R_L. V_{app} is the applied potential and the current through the device I_m is measured. From Ohm's law, the current through the resistor R_1 is given by $I_1 = \frac{V_{app}}{R_1+R_p}$, where $\frac{1}{R_p} = \frac{1}{R_2} + \frac{1}{R_L}$, however, as R_1 is chosen to be much larger than each of the two other resistors, the current through it can be approximated by $I_1 = \frac{V_{app}}{R_1}$. From Kirchhoff's current law, the relation between the current and resistance in the parallel region is given as $I_2R_2 = I_mR_L$. Furthermore, the current relation in the parallel and serial part is given as $I_2 = I_2 + I_m = \frac{I_mR_L}{R_2} + I_m$. Isolating I_m and inserting the definition for I_1 gives $I_m = \frac{I_1}{1+\frac{R_L}{R_2}} \Rightarrow \frac{V_{app}}{R_1}\frac{1}{1+\frac{R_L}{R_2}}$. Rearranging this result and substituting $V^* = \frac{V_{app}R_2}{R_1}$, which corresponds to the divided voltage in the case when $R_L >> R_2$, gives $I_m = \frac{V_{app}R_2}{R_1}\frac{1}{R_2+R_L} = \frac{V^*}{R_2+R_L}$. Isolating the two remaining resistances $(R_2 + R_L) = \frac{V^*}{I_m}$ gives the formula to calculate the sum of the two resistances from the inverse slope of the measured current I_m vs. the

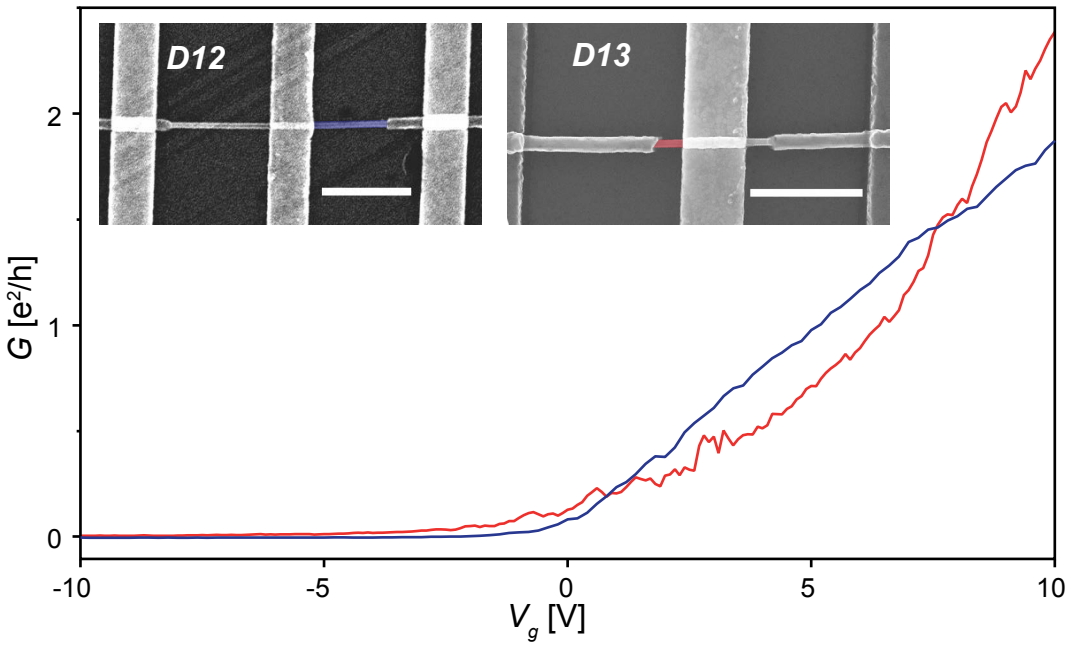


Figure 3.1.2.: Conductance measured as a function of the back-gate for two different segment length as indicated by the colored regions. The scale bars correspond to 1 μm.

theoretically divided voltage V^*. So the resistances, calculated from linear fits of the I-V curve, had to be subtracted by 10 Ω to give the actual resistance. This way, the resistance between the probe-needles and the bonding pads, as well as the line-resistance, could be measured to be around $1 - 2\Omega$, by placing both probes on the same bonding pad.

For the intact shells, the contact resistances were typically of the order of some tens to hundreds Ohms, which indicates for good ohmic contact.

3.1.2. Normal Contact

For devices with a normal contact in the center part, a second set of measurements were performed. Firstly, the usual 2-probe measurement was performed across the wire as described above; however, the resistance was much higher now as the current had to flow through the InAs nanowire instead of the metal-shell. Secondly, the back-gate dependency of the conductance was measured at a finite source-drain bias, as the semiconducting NW can be depleted or opened depending on the sign and strength of the gate-potential. To begin with, the resistance was measured

twice as described above, with 0 V and 10 V on the back-gate (as seen on the lower inset of Figure 3.1.1), mainly to check that the Al shell has been removed completely in the center part and to check if the shell has electrical contact with the NW. As InAs NWs behave like n-type semiconductor, i.e. the charge is carried by electrons, the resistance is expected to decrease with increasing positive gate potential, and it was observed that the resistance dropped down to a seventh of the resistance at 0 V when a gate-voltage of 10 V was applied.[2] In this range of resistances, the small resistor in the voltage divider can be neglected and the measured resistance is assumed to originate from the device only.

In the second type of measurements, the source-voltage was set to 10 mV and the back-gate was swept, typically between ±10 V as seen on Figure 3.1.2. On the figure two traces are seen, one of a device where the shell was etched by BHF (*D12*), resulting in a gap of $\sim 800 - 1100$ nm, and one for a device etched with Al etchant resulting in a gap of ~ 220 nm. Both traces show the characteristic behavior for n-type semiconductor as expected, with a clear pinch-off at negative gate voltages, the so-called closed regime. However, the gate was not swept high enough to measure the saturation region in which the conductance flattens out and becomes constant, i.e. all states are available, also known as open regime.

3.2. Measurements in Triton 3

The first low temperature measurements were performed at the Triton 3 cryostat. Two chips were loaded into the cryostat via the load lock. Each chip carried one bonded device each (chip *D38* and *D46*). However, it turned out that only one of the two devices was useful (the one on chip *D38*) as it was the only with four working leads on the shell. The device consisted of a NW from the batch *NBI718* with a diameter of ~ 80 nm and with a shell-thickness of ~ 30 nm. The shell was contacted by four Ti/Au (10/100 nm) bilayer leads with ion milling prior to metal evaporation. The setup was presented in Section 2.3.3, and the base temperature was ≈ 20 mK. The resistance of the shell was measured by measuring the voltage-drop between the two inner leads. At base temperature and zero magnetic field the

[2] This was the largest change in resistance observed (from $\sim 210\,\text{k}\Omega$ to $\sim 30\,\text{k}\Omega$). For other devices the drop was not that drastic, however, changes down to $\frac{1}{4} - \frac{1}{3}$ of the value at 0 V was typical.

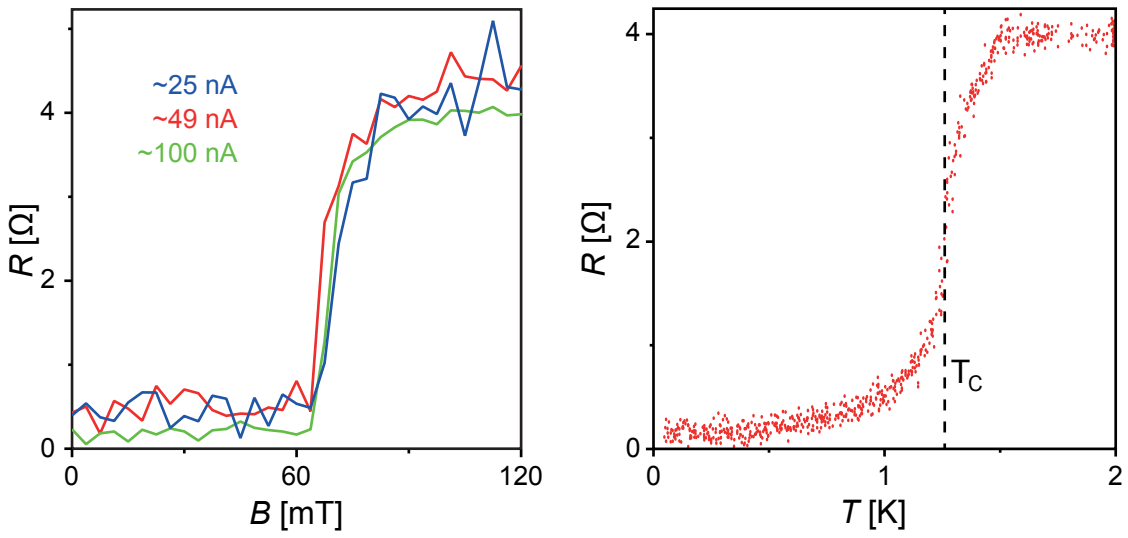


Figure 3.2.3.: Left: measurements of the critical magnetic field in the perpendicular direction to the wire, at three different currents through the device. Right: measurement of the critical temperature T_c for the same device.

shell was superconducting with a resistance of around 0.2 Ω.

To measure the critical field B_c, the voltage drop was continuously measured while turning up the magnetic field (approximately) parallel to the wire. This measurement was repeated at three different currents through the device, to investigate a possible change in the value of B_c as discussed in the theory, which however, was not observed in the chosen range. The resulting traces are shown on Figure 3.2.3 and the critical field has been estimated to be around 72 mT, 68 mT and 69 mT for the lowest, middle and highest current respectively (measured half way to the normal resistance). All three traces are quite similar and no real change in B_c was observed when the current is doubled or quadrupled, which in principle was expected as the critical current was estimated to be much larger (in the range of mA). The main change to be observed, however, might be the noise-reduction at the increased currents. This is because the current is regulated by a large resistor in series, so by increasing the signal amplitude (V_{AC}) the current is increased and the larger signal voltage effectively results in a larger signal-to-noise ratio at the inner leads. All later measurements were performed at the higher current ($I \sim 100$ nA). The resulting normal-state resistance was around 4 Ω.

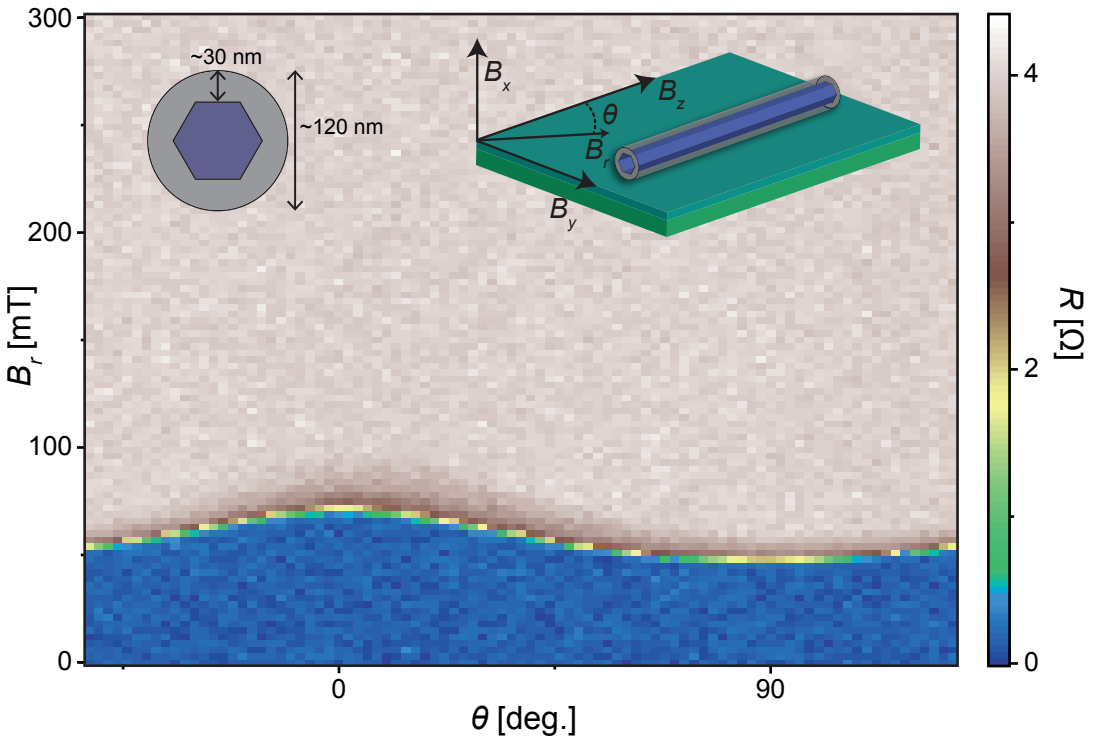


Figure 3.2.4.: Angular dependence of the critical field B_c. It is clearly seen that B_c is higher with the field in the parallel direction to the wire. The inset to the right shows how the applied field B_r relates to the wire axis, where θ defines the angle from B_z (parallel to the wire) in the plane of the substrate. The inset left shows a sketch of the cross section of the wire indicating the estimated diameter and thickness of the shell.

The second type of measurement that was performed had the goal to investigate the change in B_c with respect to the angle θ in plane with the substrate and around the wire (see inset of Figure 3.2.4). Figure 3.2.4 shows that the critical field depends rather strongly on the angle with respect to the wire, which was expected, as discussed in the theory, because the effective area facing the magnetic field varies. The rate at which B_c changes is higher near the parallel direction ($\theta = 0\,^\circ$) compared to around the perpendicular direction ($\theta = 90\,^\circ$), which is a result of the change in the projected area as well, as it changes much faster near the parallel than the perpendicular direction. The reappearance of a superconducting state at higher fields was, however not observed. The magnetic field corresponding to one flux quantum passing through the cylinder, i.e. $\Phi/\Phi_0 = 1$ was calculated to be around 182 mT for a diameter of 120 nm. Above ≈ 75 mT, however, no further change is observed, even for fields up to 300 mT. This reason for the absence of a reappearance of su-

perconductivity might be due to the ratio $d/\xi_0 > 1$, i.e. that the diameter of the shell exceeds the coherence length. On the other hand, it could be because of the thickness of the shell, which plays a larger role when $n > 0$. Lastly, it the absence could be related to poor alignment of the wire. Of course, the in-plane dependency was measured, however, the wire might be bended slightly. It has later been seen on both top view Figure C6 and tilted Figure C5 SEM images that the wire bends slightly at the lower/right-most contact, respectively.

Lastly, the critical temperature T_c was measured by monitoring the voltage-drop whilst continuously increasing the temperature and it was found to be at $T_c \sim 1.3\,\mathrm{K}$ as seen on Figure 3.2.3 (taken halfway to the normal state resistance), which is close to the value for bulk aluminum ($1.14\,\mathrm{K}$)[6].

3.3. Measurements in Triton 1

At the Triton 1 cryostat one chip (*D19*) with several working devices was measured. As one device (*Dev3*) had the nanowire almost aligned with the strongest magnetic field direction, it was the one that was analyzed the most. For comparison, two other devices (*Dev2* and *Dev4*) where measured as well, however not as thoroughly.

The devices on this chip consisted of InAs nanowires from the batch *NBI858* with diameters of around 40 - 60 nm and a surrounding Al shell of $\sim 13\,\mathrm{nm}$ in thickness. The length of the wires was usually around $6\,\mu\mathrm{m}$. As these wires are about $2\,\mu\mathrm{m}$ shorter than those on the chip measured in Triton 3, the distance between the contacts in the center region had to be decreased (from $3\,\mu\mathrm{m}$ to $2\,\mu\mathrm{m}$ between the innermost leads, the distance between the two contacts on each side was still $\sim 0.5\,\mu\mathrm{m}$). Only a few longer wires could be found on the substrate for which the original design was sufficient and *Dev4* is one of those devices. All leads are made of Ti/Au (5/90 nm) bilayers.

The first measurement for each device was to investigate at which magnetic field the Al shell is driven into the normal state, i.e. B_c in the perpendicular direction to the wire (B_x). This was done by measuring the voltage drop, and hence the resistance, across the shell while applying a magnetic field in the direction normal to the substrate. For all three devices B_{cx} was found to be above 100 mT. At fields below the critical field, the shells are superconducting with $R = 0\,\Omega$, whereas at fields above B_{cx} the resistances are constant at some tens of Ohms. The normal-

resistances for each device are slightly different, however, the values of *Dev2* and *Dev3* are $\sim 2/3$ of the value of *Dev4*, which might be related to the distances between the probing leads (which have the same ratio). The normal-resistance stayed constant up to the maximal field of 1 T, however, the results are only shown up to 200 mT on Figure 3.3.5 to clarify the transition region. It is seen that the transitions are not totally sharp as there appear some bumps at different positions for each device. They are identical regardless of the direction in which the magnetic field is swept and it is not exactly known what the cause for their appearance is. It might be explained by some inhomogeneities in the shell or some other intrinsic properties of the device that might cause parts of it to transit into the normal state before others, and thus only contributes with a partial increase in resistance.

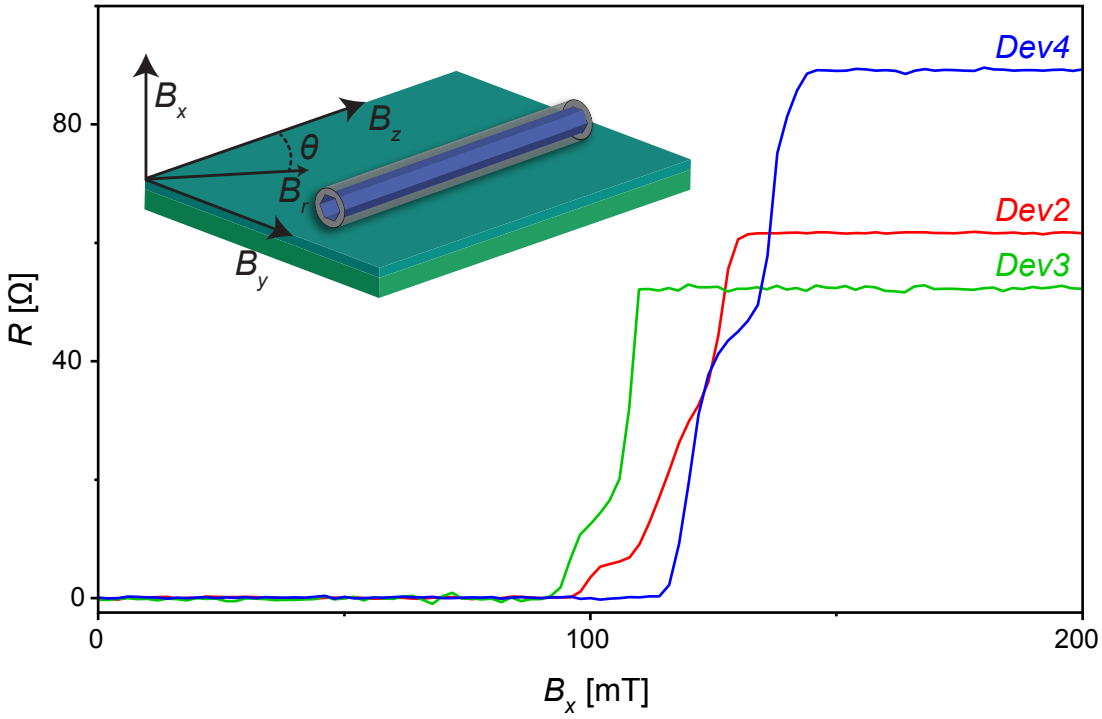


Figure 3.3.5.: Critical magnetic field measurements in the normal direction of the substrate for three different devices on the same chip. The inset shows how the axis are related to the nanowire.

The next measurement on all three devices was to find the orientations of the wires by measuring the angular dependency of B_c, just as for the device in Triton 3. The magnetic field B_r was swept from 0 to 400 mT at different angles in the substrate plane (i.e. in the Z-Y-plane of the magnet). The results are presented

on Figure 3.3.6. The decrease in critical field at the perpendicular direction was observed just as for the device in Triton 3. In the parallel direction, however, a tremendous difference is observed. As in the theory, the cylindrical shells of these wires enter a destructive regime in which the superconductivity is reduced (except for *Dev2*, which seems to stay completely superconducting). As the field is increased further, however, the shells become completely superconducting again with zero resistance and all three devices where still superconducting at 400 mT. Furthermore, it is seen that the resistance in the destructive regime is rather different compared to the normal resistance, whereas *Dev2* stays completely superconducting, *Dev4* becomes almost normal conducting. *Dev3* is somewhere in-between with the resistance at around 20% of R_N.

The next question was up to which magnetic field this superconducting regime can be observed. So the parallel magnetic field was further increased and the result for *Dev4* is shown on Figure 3.3.7. The figure shows three traces; first the field was swept from 0 to 2.3 T, then it was swept from 2.3 T to -2.3 T and finally back to 0. The destructive regime oscillates periodically as expected from the theory for flux quantization. So the destructive regime appears at odd multiples of $0.5\Phi_0$, whereas the superconductive state is reentered at even multiples of $0.5\Phi_0$. No hysteresis was observed, which would be related to a persistent current in the cylinder which would counteract the external magnetic field when it changes sign, i.e. it goes through zero. This would be observed in a displacement in the first peaks with respect to the sweeping direction.

Due to the relation $\Phi = n\Phi_0$ and $\Phi = B\pi r^2$, i.e. the magnetic field times the cross sectional area of the nanowire including the shell, it is possible to calculate the effective diameter of the cylinder. This was performed by plotting the number of flux quanta vs. the absolute magnetic field at which they appear, and making a linear fit through the points (as shown in the inset of Figure 3.3.7). It is to be noted that only positions with clear peaks (or minima) were chosen, i.e. the three peaks closest to zero and the two minima at the highest fields (as indicated by the black arrows on Figure 3.3.7). The slope of the fit could then be used to calculate the diameter. For *Dev4* the effective diameter was calculated to be $d \approx 90.5 \pm 0.5$ nm. This seems reasonable and corresponds roughly to the diameter expected from the growth. From SEM measurements of the wire (Figure D1 lower right inset), the diameter was found to be around 115 nm, which is about 20% more than calculated. The

reason for this is not exactly known, but it could be reasonable that the diameter is larger than expected from the growth, and the SEM measurements might deviate from the real values as well as it has not been calibrated before the measurements. It might equally well be that the effective radius (of the superconductor) is somewhat smaller than the external diameter, as the aluminum shell is surrounded by its natural oxide layer and the surface roughness might decrease it as well. The top axis of Figure 3.3.7 is shown in flux quanta, calculated with the diameter found from the linear fit and seems to coincide with the peaks and minima rather well.

For *Dev2* the same measurement was performed up to the maximal field in the direction of the wire (1.13 T), and it showed a similar behavior as seen for *Dev3*, however, the maximal critical field parallel to the wire could not be found as it exceeded the range of the magnets. The effective diameter was calculated, the same way as above, to be around 91 ± 0.6 nm. The SEM measurements resulted in an external diameter of around 110 nm. Both values are rather comparable to those found for *Dev3*. For *Dev4* the parallel magnetic field has not been measured further than seen on the angular dependence measurement, however, the effective diameter was still calculated from the peak found on this graph and resulted in a diameter of 75 nm, which is somewhat lower than the other two. The SEM measurements resulted in an external diameter of around 97 nm, which is lower than for the other two as well.

Another measurement that was performed on *Dev3* was to investigate the angular dependence of the oscillations in a small range of angles around the parallel direction. The result is shown on Figure 3.3.8 where a line cut along $\theta = 0°$ would correspond to the positive half of Figure 3.3.7. To save time, the measurement was divided into smaller regions so that the resolution with respect to the angle could be increased in the central part and decreased in the outer regions; furthermore, the maximal field was limited as well, which results in the step-like appearance. It has to be noted that the width of the ellipsoidal superconducting regions with respect to the field is not as different as it appears. For example is the width (indicated by the two dashed lines in Figure 3.3.8), i.e. the difference in field from edge to edge projected onto the B_y axis, for the first ellipsoid around 170 mT, whereas it is around 140 mT for the fourth ellipsoid (calculated by $B_r \cdot \sin(\Delta\theta)$, where $\Delta\theta$ is the angle between the two sides). The main result to be drawn from this measurement, however, is the small range of angles for which the last ellipsoid, and hence the

last oscillation is observed. The field has to be aligned within 1°, which was easily performed with the vector magnets at hand.

The last, and probably the most interesting, measurement that was performed on *Dev3* was to repeat the magnetic field-sweep at different temperatures. This was possible because of the integrated heater near the sample in the cryostat. However, it turned out to be a rather time-consuming measurement, as the ramp-rate of the magnetic field had to be reduced. Generally it is known that when a magnetic field changes, an eddy is induced in surrounding conducting materials, which in a cryostat results in heating power. However, it was observed that, while gently trying to heat the sample, the eddy current heated the *still*, which causes more ^{3}He to evaporate and hence *cooled* the sample. So the ramping-rate had to be decreased to maintain a stable temperature.

The measurements where performed at several temperatures (nonlinear spaced) from 50 mK to just below 1.7 K and the results are presented on Figure 3.3.9 and Figure 3.3.10. The two figures show the same data only plotted in different ways. As expected from the theory, the resistance in the destructive regime increases with temperature as does the minimum resistance in the superconducting regions. As suggested by the theory, the data for the phase diagrams where extracted for different threshold values (R_c/R_N) and an example is shown for $R_c/R_N = 0.9$ and $R_c/R_N = 0.1$ on Figure 3.3.11. The red lines on the graph correspond to the fit of Equation 1.1.2 in the form of $T = T_c - \frac{T_c(n-\frac{\Phi}{\Phi_0})^2}{\left(\frac{d/2}{\xi(0)}\right)^2}$ with $n = 0$, i.e. $\Phi < 0.5\Phi_0$, the fitting parameter $\left(\frac{d/2}{\xi(0)}\right)^2$ and $T_c = 1.5\,\mathrm{K}$ and 1.26 K for the threshold 0.9 and 0.1 respectively. From the fits, the ratios $d/\xi(0)$ have been found to be 1.23 and 1.07, respectively. This means that the coherence length would be slightly shorter than the diameter. However, the applied model is rather simplified and a numerical solution of Equation 1.1.3 might give a more accurate result as the higher order oscillations, i.e. $n > 0$ could be considered as well (an approach on how this problem could be solved numerically is presented in Appendix E).

The results from this study are similar to those presented by both by Liu *et al.*[10][23] and Sternfeld *et al.*[11], however, it should be pointed out that the cylinders in each case are slightly different. Sternfeld *et al.* used InAs nanowires with aluminum coating as well, but the Al shell was sputtered onto the wire in a later fabrication step, so that the insulating oxide layer around the NW could be formed.

In the case of Liu *et al.* the superconducting shell enclosed an insulating material as well, here however, the cylinder is in direct contact with the nanowire and the proximity effect might have some influence.

One of the mayor differences in the results might however be, that the number of oscillations is higher in this study, up to 6 oscillations were observed here compared to up to 2 in the others study.

Further analysis and similar measurements on other devices is still needed to draw any qualitative conclusion on the coherence length the effective thickness of the MBE grown Al shell.

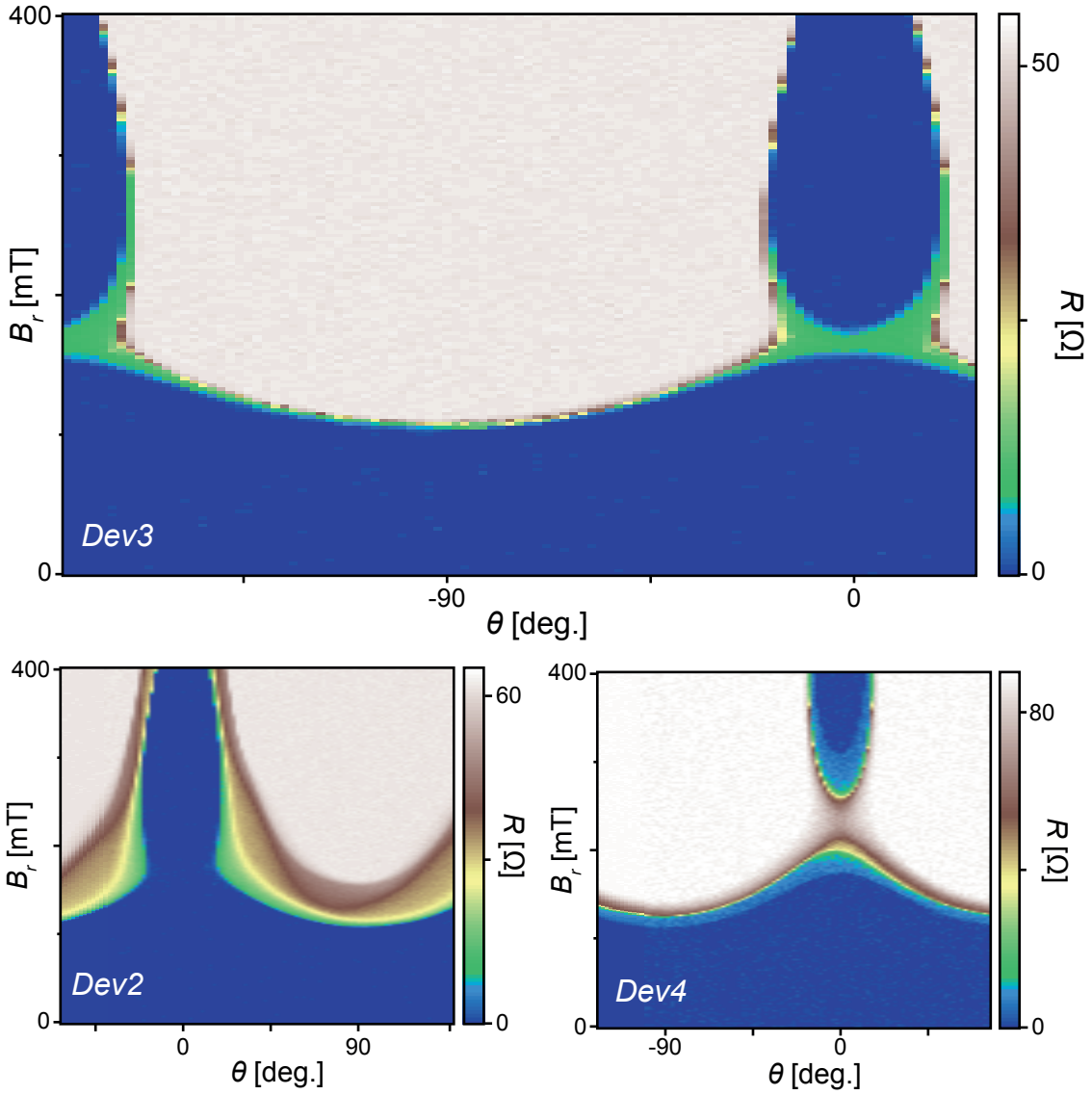


Figure 3.3.6.: Result from the measurement of the in plane angular dependence of the critical field B_c for three different devices. Refer to main discussion for further details.

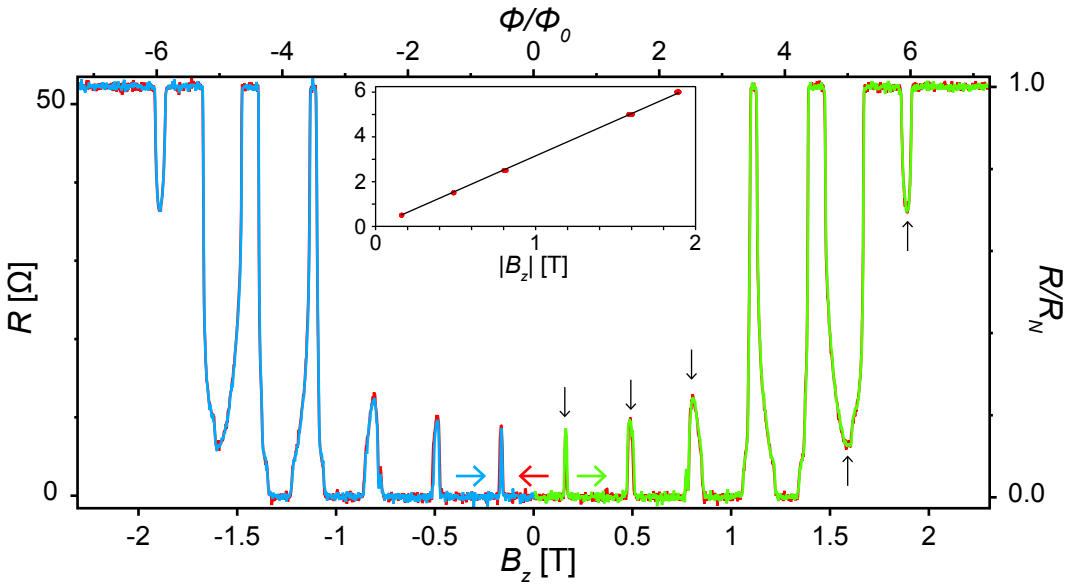


Figure 3.3.7.: Resistance measurements as function of parallel magnetic field. The colorized arrows indicate the sweeping direction of the respective curve. Top axis has been calculated from the linear fit shown in the inset. The points where chosen at the positions indicated by the back arrows.

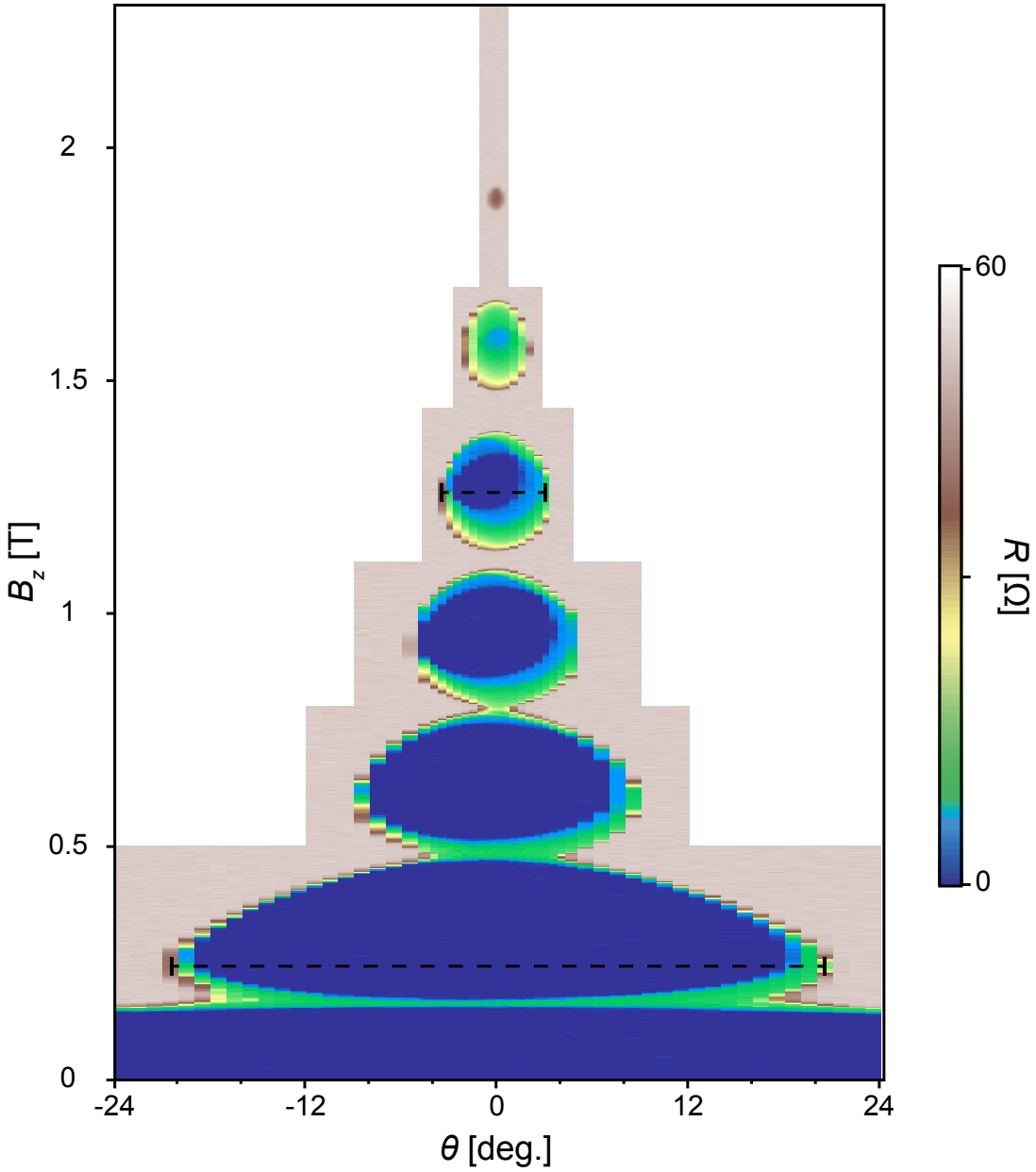


Figure 3.3.8.: Angular dependence of the destructive oscillations around the parallel axis of the wire. The dashed lines correspond to the positions of calculations in the text.

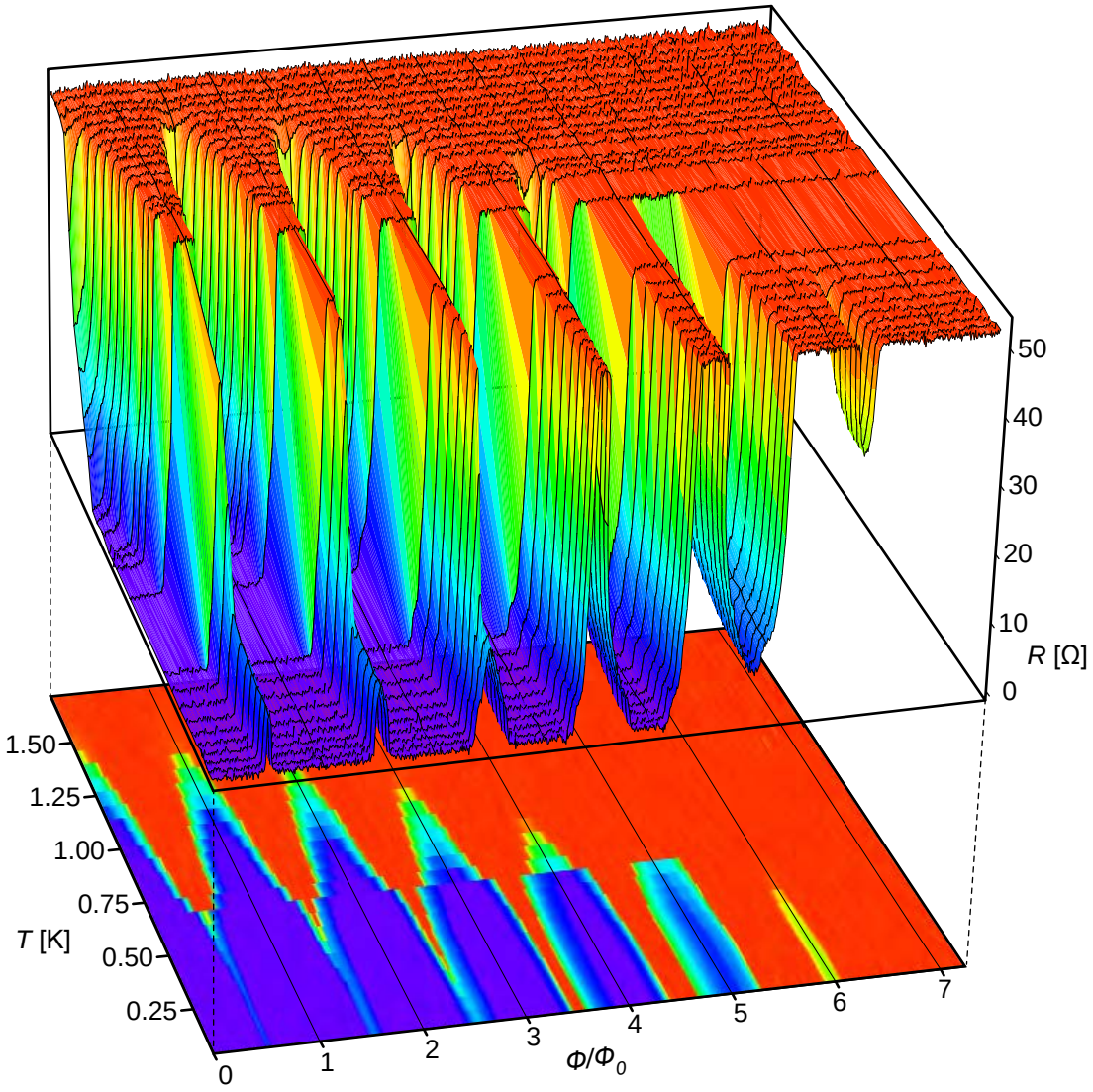


Figure 3.3.9.: Temperature and flux dependence of the destructive/constructive regions. The color scale on the planar projection is the same as on the 3D representation.

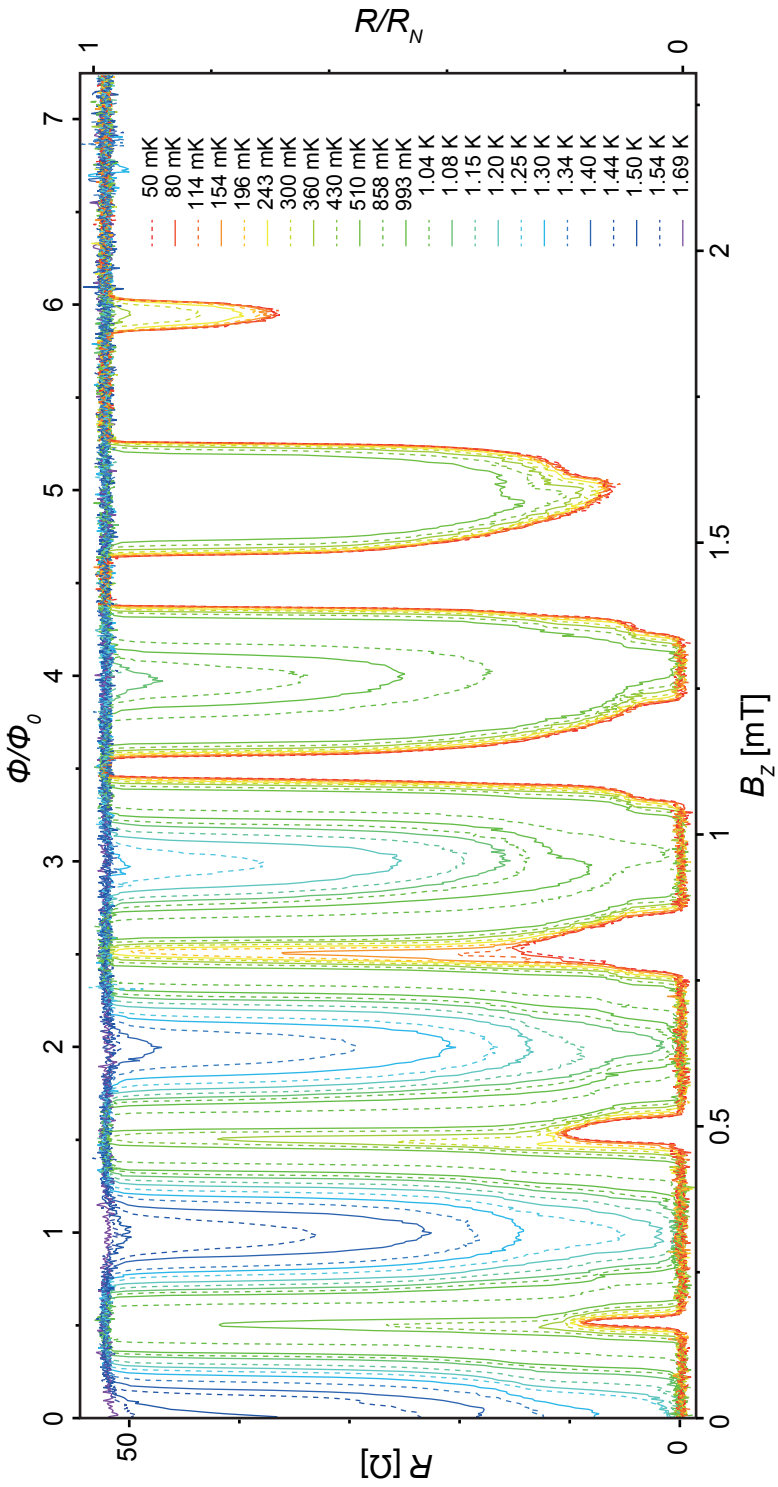


Figure 3.3.10.: Same data as shown on the previous plot. The corresponding temperatures are indicated in the legend.

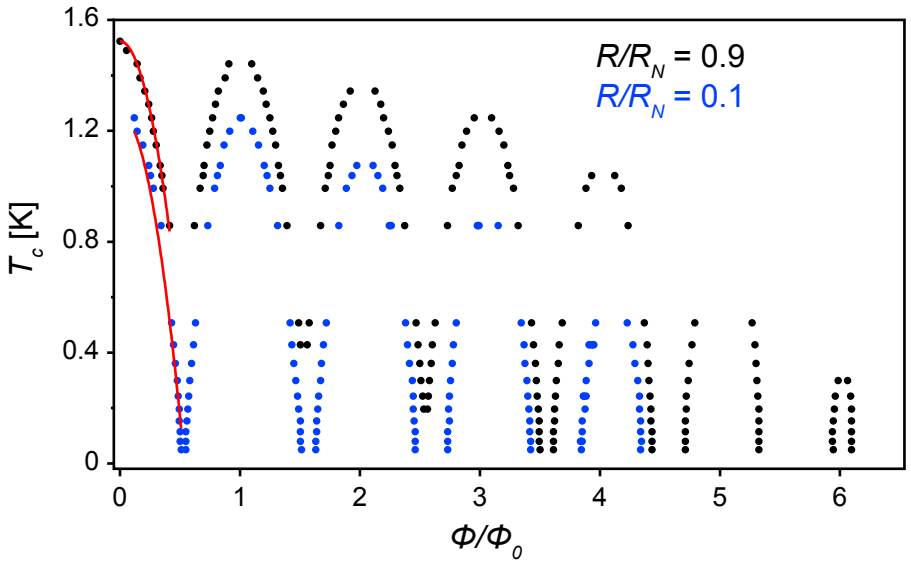


Figure 3.3.11.: $\Phi - T_c$ phase diagram for two different threshold values. The areas below the dots correspond to the superconducting phase, whereas the area above is the normal region. Red lines are fits with the formula presented in the text, between 0 and 0.5 Φ/Φ_0.

3.4. Measurements in Leiden

This section is about the measurements performed in the Leiden cryostat. The device consisted of a nanowire with aluminum shell which has been etched away in the center region, exposing a 600 nm segment of the InAs nanowire. As described above, each side of the shell was contacted by one lead and the differential conductance was measured by a lock-in amplifier. It is the same device referred to as Dev#2 in the article found in Appendix F. This section will briefly discuss two of the measurements performed.

In the first measurement, the conductance was measured as a function of the bias voltage (V_{SD}) and the back-gate voltage (V_g). The result is shown on Figure 3.4.12. At back-gate voltages below -2.3 V the nanowire is completely depleted and no current can tunnel from the one superconductor to the other. However, as V_g is increased, available states in the nanowire are moved in the vicinity of the energy levels in the superconductor, so that current can run at certain bias voltages. With increasing V_g the conductivity increases further until a maximum value is reached which is distributed evenly around zero bias. At these peaks, the bias voltage matches the gap size of the superconductor. From these data, the gap was found to

be $2\Delta = 0.6\,\text{meV}$, which is of the right order of magnitude. Furthermore, coulomb diamond structures are observed around zero bias, which is due to discrete states in nanowire and is an indication for quantum dot behavior of the nanowire.

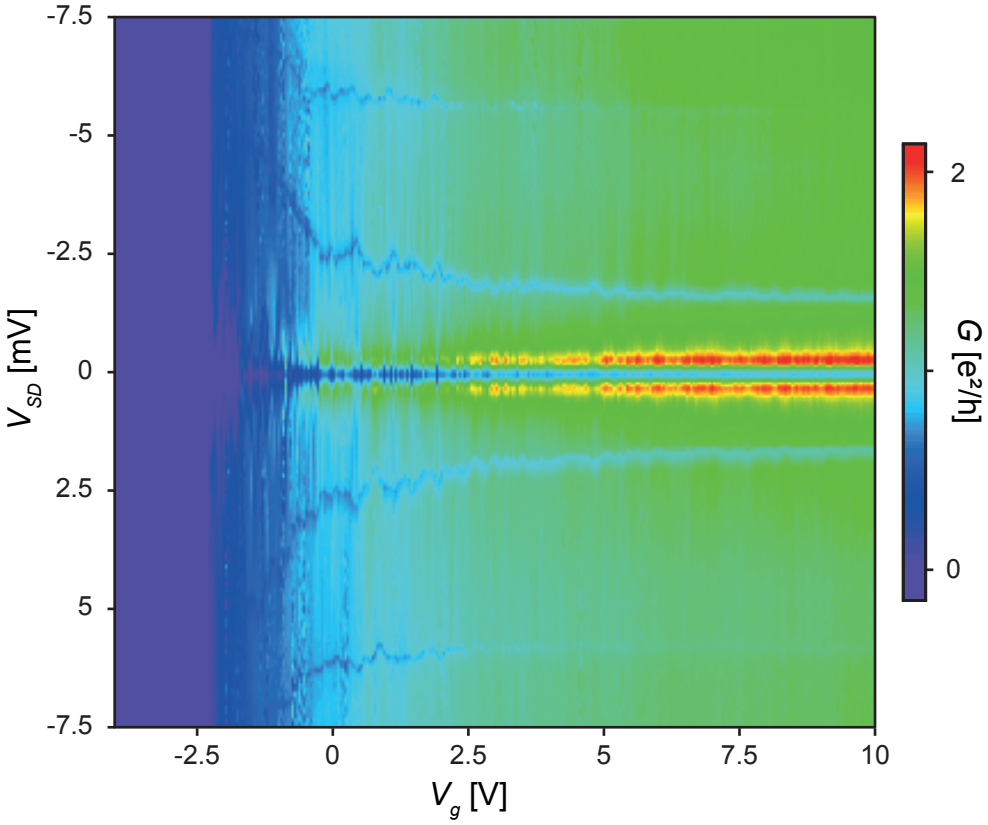


Figure 3.4.12.: Back-gate vs. source-drain bias dependency of the conductance at zero magnetic field.

In the second measurement the conductance was measured as a function of bias voltage and parallel magnetic field. For these measurements the back-gate voltage was set to $V_g = 10\,\text{V}$ to ensure that the nanowire was in an open state. The result is shown on Figure 3.4.13 and a rather complex mesh of features are seen. These features are still not totally understood and will not be discussed further at this point. What, however, can be observed is that for a certain magnetic field, the peaks in the conductance around zero bias disappear, i.e. the superconducting gap closes. At an even higher magnetic field the peaks reappear, though not so profound as at low magnetic field. When the field is further increased, the gap closes again and disappears. The reappearance of superconductivity, as discussed in the previous

section, might be related to the first flux quantum entering pinning through the central region of the cylindrical shell. Assuming that superconductivity partially reappears when the flux trough the cylinder is equal to one flux quantum, the diameter can be calculated to be around 80 nm (with the magnetic field approximately at the midpoint of the reappearance≈ 410 mT). This is around the same size as the calculated results in the section above, and equally, it is lower than the diameter (of the shell) found from SEM measurements ≈ 130 nm. In this device, however, the shell has been removed in the central region, and the InAs core diameter is considerably smaller than the shell. It is however not known how these sizes compare to calculated diameter. Line cuts of Figure 3.4.13 at zero magnetic field, as well as 250 and 410 mT (as indicated by the dashed lines) are shown in Figure 3.4.14, where it is clearly visible that the peaks have disappeared at the intermediate field, and the weak reappearance at the higher field is visible as well.

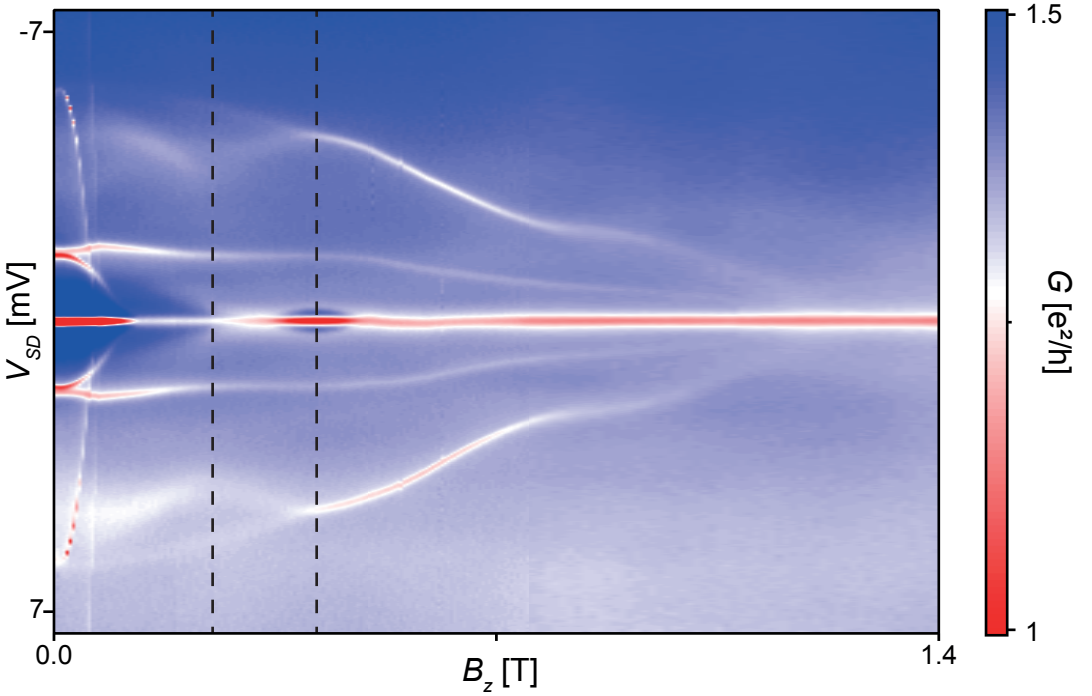


Figure 3.4.13.: Magnetic field vs. source-drain bias dependence on the conductance. It is seen that the peaks symmetrically around zero bias disappear with increasing magnetic field and reappear for a short range at a higher magnetic field. The dashed liens correspond to the line-cuts presented in the next figure.

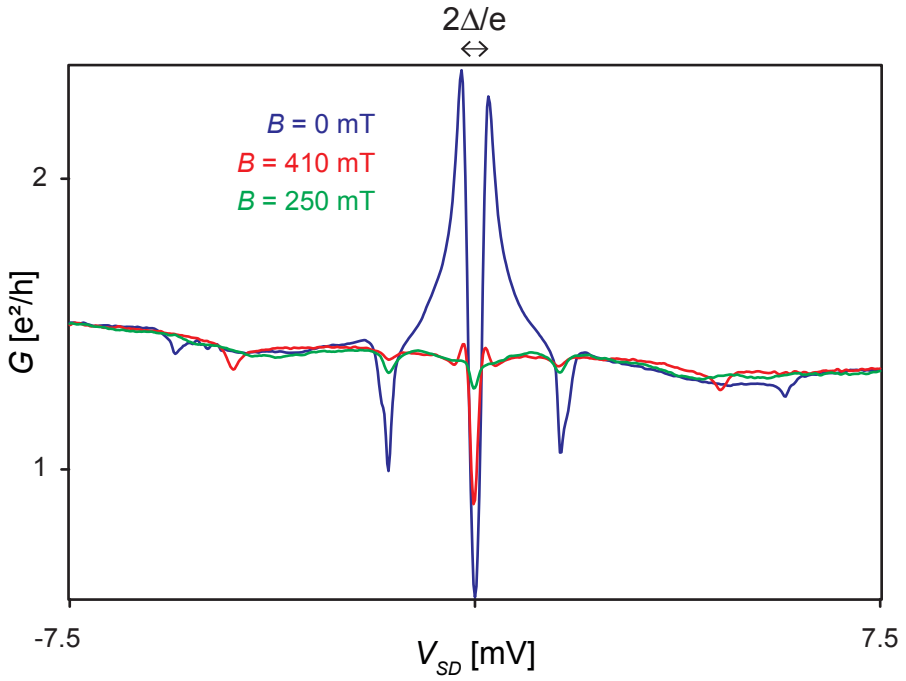


Figure 3.4.14.: Line-cuts from the figure above at zero and two finite magnetic fields as indicated. The potential difference between the two peaks correspond to the superconducting gap size..

4. Conclusion

Finally this thesis can be summarized and some of the main achievements will be pointed out. First of all the process of device fabrication, based on InAs nanowires with superconducting aluminum shells, has been optimized and a detailed recipe for this process has been developed. This allowed for the reproducible production of multiple connected cylindrical superconducting shells, i.e. devices with the intact Al shell, superconductor-nanowire-superconductor junctions and finally superconductor-nanowire-normal metal junctions. Latter have been measured at room temperature and showed the characteristic n-type semiconductor dependence of an applied gate-potential. The other two geometries have been studied at ultra-low temperature and some of the characteristic phenomena where observed.

For cylindrical superconducting shells with sufficiently small diameter and shell thickness oscillations in the critical temperature with respect to an externally applied parallel magnetic field has been observed. Repetition of these measurements, at different temperatures from well below to well above the (zero field) critical temperature, allowed for the construction of a phase diagram between the superconducting and normal-metal phase. The boundary between the two phases could be used to fit a simplified model which revealed an estimate for the ratio between the cylinder diameter and the coherence length in the superconductor. The estimated coherence length was somewhat smaller than observed in the literature; however, the system at hand was more complex, as the superconducting shell is in good contact with the InAs core, as opposed to an insulating core in the literature. The effect of the proximity induced superconductivity or a resulting weakening of the superconductor remains unknown, and will be subject to future studies.

The S-NW-S junction showed similar characteristics as observed for S-quantum dot-S devices in that it showed coulomb diamond shaped regions when the conduc-

tance was measured as a function of bias and gate voltage. The absence conductance when the nanowire is in the closed regime, and the general gate dependence on the supercurrent across the junction implies that the nanowire has a proximity induced superconducting behavior, as opposed to the case when the superconducting leads are in close vicinity so that the Cooper pairs directly can tunnel through the barrier, which generally is independent of an applied gate. Furthermore, when a parallel magnetic field was applied, it was observed that the superconducting peaks disappeared and at a higher field reappeared. This result is similar to that observed for the intact cylinder, however in this case the phase-coherence has to be maintained over the length of the exposed nanowire, which with 600 nm is rather large.

So in summary, it was possible to fabricate nanowire based devices which showed a variety of phenomena typically observed in the field of superconductivity and mesoscopic transport.

4.1. Outlook

Although the results have been discussed and compared to simplified models, the analysis is by no means profound and complete. Further analysis of the data is still needed to qualitatively determine quantities such as the coherence length in the MBE grown aluminum shell. Additionally experiments on similar as well as modified systems could increase the understanding of the observed effects. For example would a normal-conducting tunnel probe on the InAs nanowire close to the Al shell reveal information of the proximity induced superconducting gap and coherence length. This could be supplemented by placing a tunneling probe in-between two regions covered by the shell as the center region would be stabilized from both superconductors.

As mentioned in the section about nanowire characterization, in some cases a transition region between the nanowire and the shell has been observed. If it holds true that this region consists of AlAs the electrical properties should be investigated more thoroughly as this compound might be a p-type semiconductor[24]. Furthermore is the lattice constant of AlAs around 7% smaller than that of InAs, which could induce some strain and thus change the band-gap. It might be worthwhile considering introducing different materials to prevent the formation of such a layer. For example is it known that certain gold alloys become superconducting such as

AuIn, AuGa or $AlAu_4$[25], which are all materials present in the MBE growth chamber. But it would still need extensive study of the effect of an intermediate layer.

When it can be confirmed that the induced superconducting gap from the MBE grown aluminum shell is a so-called hard gap, a further step towards the observation of Majorana end-states would be taken. As the aluminum shell can be grown as a half shell as well, the proximity-coupled region of the nanowire could be gate-able and together with the strong spin-orbit interaction, the high g-factor and electron mobility in InAs, which are the remaining necessary ingredients[2], the half-shell nanowires could be suitable candidates for the observation of Majorana Fermions.

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Appendix

A. Detailed Recipe

This appendix contains a detailed recipe for the device fabrication used in this study. The listed materials and parameters are those for which the highest yield was obtained.

Fabrication of the chip layout In this first list below, a detailed description of the procedure for producing the substrate/chip is given.

- A piece of a Si wafer is cleaved to the desired size. The cleaving edges are marked by a diamond tipped scriber and have to be aligned with the crystal planes of the substrate to obtain clean cleavings.
- The cleaved wafer is then successively cleaned with miliQ water, acetone, methanol and isopropanol (IPA) and dried with nitrogen gas.
- To evaporate any possible leftovers of water and solvent, the wafer is baked on a hotplate for 4 min at 185 °C.
- To remove any organic residues, for example from the solvents, the wafer is plasma ashed with oxygen for one minute.
- The wafer becomes hydrophobic from the plasma ashing, which is neutralized by baking it for two minutes at 185 °C.
- The first layer of the resist consists of 9% copolymer, which is spin coated onto the wafer at 4000 rpm for 45 s.
- The second layer consists of 4% PMMA, which is spin coated onto the wafer at 4000 rpm for 45 s as well.

- After each spin-coating, the wafer is baked for 4 min at 185 °C to evaporate the solvents from the resist.

- The wafer is then loaded into the electron beam lithography[1] system for exposure. The exposure parameters where: aperture 120 μm, acceleration voltage 20 kV, beam current 5 nA, step size 100 nm and dose 300 μC/cm^2.

- After exposure, the resist is developed by submerging the wafer for 60 s in 1:3 MIBK:IPA followed by two baths in IPA to terminate the reaction.

- After development, the wafer is ashed for 17 s to remove possible leftovers of the resist in the developed regions.

- The wafer is loaded for metallization in a electron-beam evaporation system (e.g. E-gun chamber) where it is subsequently covered by 15 nm titanium and 150 nm gold.

- Lift-off is performed overnight in acetone at room temperature (RT).

Fabrication of the contacts to the aluminum shell The next step in device fabrication is to deposit the nanowires and defining the contacts to the Al-shell. The procedure was similar to that listed above, deviating mainly by the systems used. A condensed step by step recipe is listed below; the procedure listed above will be referred to as the initial/standard procedure.

- Four chips are separated (cleaved) from the main wafer produced previously and cleaned as initially in the standard procedure, including plasma ashing and baking.

- A piece of a wafer on which the nanowires where grown on, is submerged in IPA and sonicated for 15 s. Two droplets ($\approx 3\,\mu$l) are applied on the chips and air-dried.

- The results are investigated by optical microscopy (OM) and if the wire-concentration is too low, a further droplet is applied.

[1] Raith eLiNE

- When a good wire-concentration is reached, the chips are covered by a double layer of resist following the standard procedure except for that 6% copolymer was used instead of 9%.

- Images of suitable unit cells (defined in Section 2.2.2) are acquired for each chip with the OM.

- The contacts are designed as described in Section 2.2.3 and the design is written into the resist using the Elionix EBL system. The parameters typically used were: acceleration voltage 100 kV, beam current 0.2 nA, write field size 75 μm, dot map 20000, dose 1640 μC/cm^2 and dose time 1.15 μs/dot.

- The four chips were then separated and developed one at a time.

- For development the chip is submerged for 2 min in 1:3 MBIK:IPA and two baths of IPA for 5 s and 30 s respectively. All three solvents were cooled to 0 °C in a water/ice bath.

- Before proceeding with metallization, the chips were inspected for any stitching or alignment faults that might have occurred during exposure.

- Faultless chips were then loaded into the AJA evaporation system for metallization. Ion milling (see Section 2.2.4) was performed with argon gas for 3 min at 300 V to remove the native oxide layer covering the Al shell prior to metal evaporation. Usually, a $5 - 10$ nm sticking-layer of titanium and a 150 nm were applied onto the chips.

- Lift-off was performed, as in the standard procedure, overnight in acetone at RT. The results were investigated by OM after lift-off.

Fabrication of the normal contacts The goal of the last lithographic round is to produce normal contacts to the InAs nanowires. The procedure is very similar to that for producing contacts to the Al shell, differing mainly in the resist used and an additional step for aluminum etching to remove the shell.

- The chip is cleaned and covered with resist the usual way. However, only with a single layer of 6% PMMA as no undercut is desired for the etching.

- The contacts are defined by the Elionix EBL system with the standard parameters and developed the usual way on ice.
- After development, the chip is oxygen plasma ashed for 15 s to remove residues of the resist in the developed regions.
- The wires are then stripped by etching the aluminum shells away (see Section 2.2.5). Aluminum etching is performed with Transene Aluminum Etchant Type D for ≈ 10 s at 55 °C followed by neutralization in deionized water for > 30 s.
- The chip is then ion milled for 60 s at 300 V and 5 nm Ti and 125 nm Au is deposited using the AJA system.
- Lift-off is performed the usual way and the results are investigated by OM and scanning electron microscopy (SEM).

B. Results From Etchtest

The Table below contains the results from the aluminum etch test.

Table B.1.: The tests 7-9 were excluded as the wires were removed while removing the PMMA.

Test Nr.	Temperature	Time	Comment/Result
without ashing			
1	0 °C	2×30 s	Dipped two times, nothing etched
2	40 °C	6 s	Droplet on chip, nothing etched
with ashing and from here always dipped			
3	40 °C	6 s	nothing etched
4	40 °C	60 s	very soft transition, much etched $> 1\,\mu$m
5	40 °C	30 s	indistinguishable, almost nothing etched
6	60 °C	30 s	very much etched $> 7\,\mu$m ($rate \sim 110$ nm/s)
10	60 °C	10 s	good transition, much etched $\sim 1.8\,\mu$m ($rate \sim 65$ nm/s)
11	55 °C	10 s	good transition, $\sim 1\,\mu$m etched ($rate \sim 25$ nm/s)

C. Batch 1

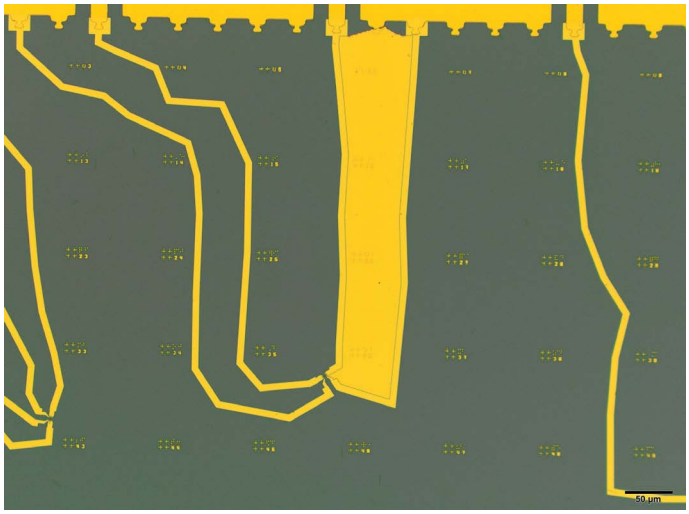

Figure C1.: Optical microscopy image of chip D46 showing the effect of lift-off problems. Scale bar corresponds to 50 μm

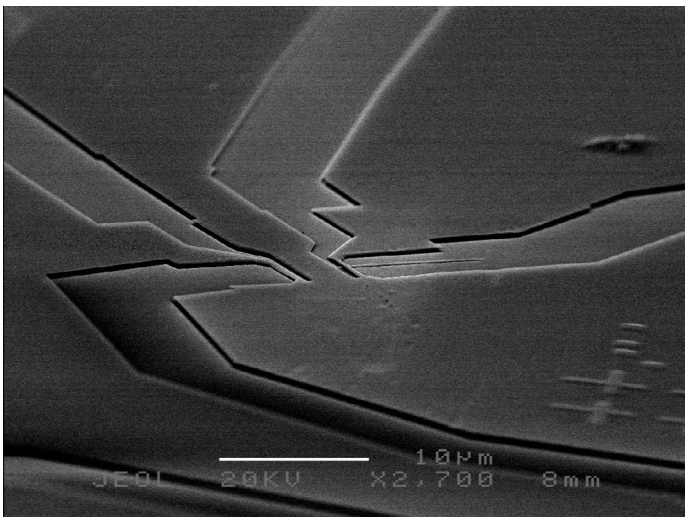

Figure C2.: SEM image of the exposed and developed resist (covered by 10 nm Au). The nanowire is clearly seen in the right contact.

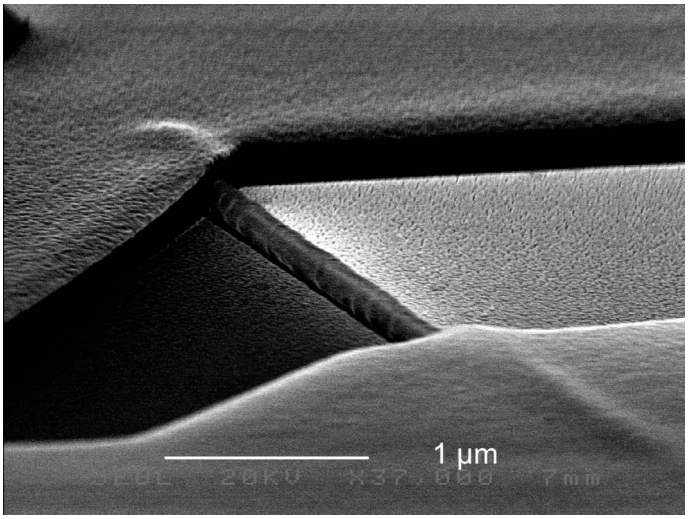

Figure C3.: SEM image of a NW covered by a double layer of resist (covered by 10 nm Au).

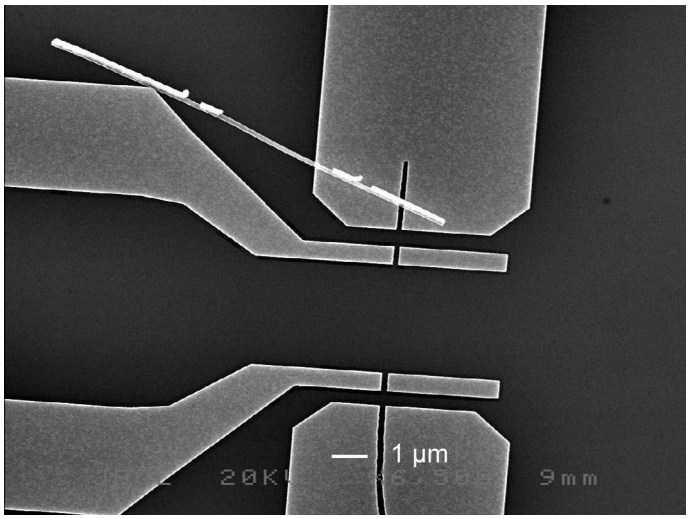

Figure C4.: Top view SEM image showing a nanowire that has been ripped off the contacts. The metal evaporated onto the wire is still seen.

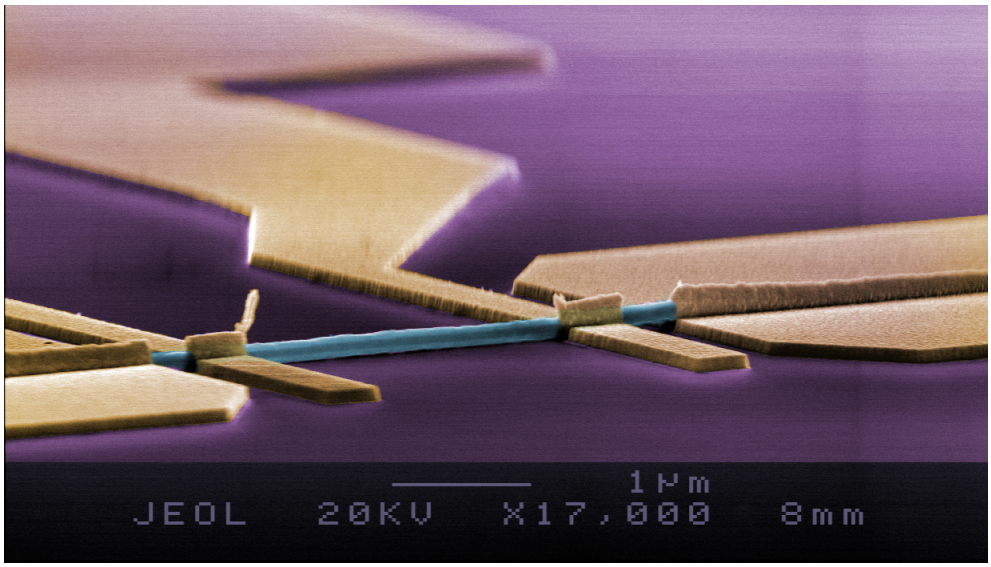

Figure C5.: Tilted SEM image of the divice measured in Triton 3. Chip D38. Colorized for clarity: purple corresponds to the substrate, yellow to the Au contacts and blue for the InAs/Al core/shell nanowire.

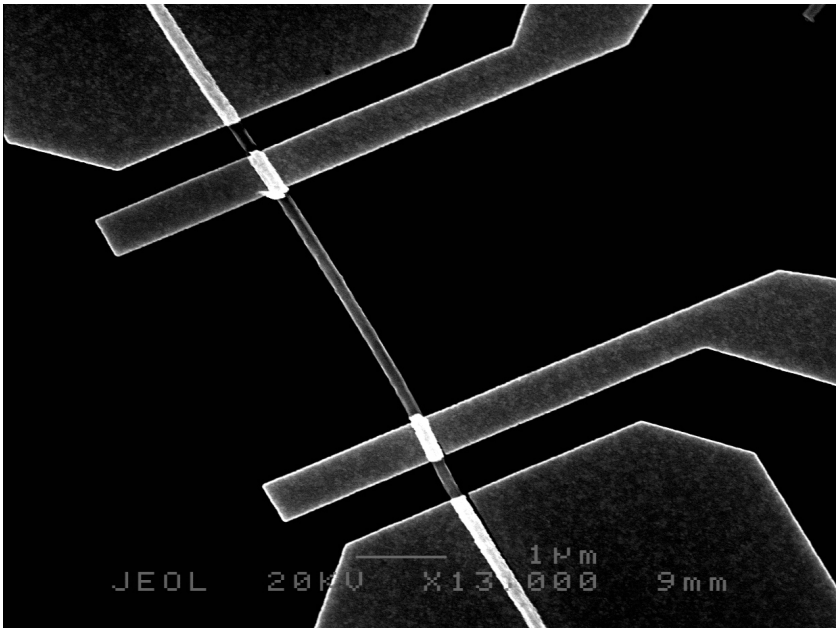

Figure C6.: Chip D38. Top view SEM image of the same device as on the image above.

D. Chip D19

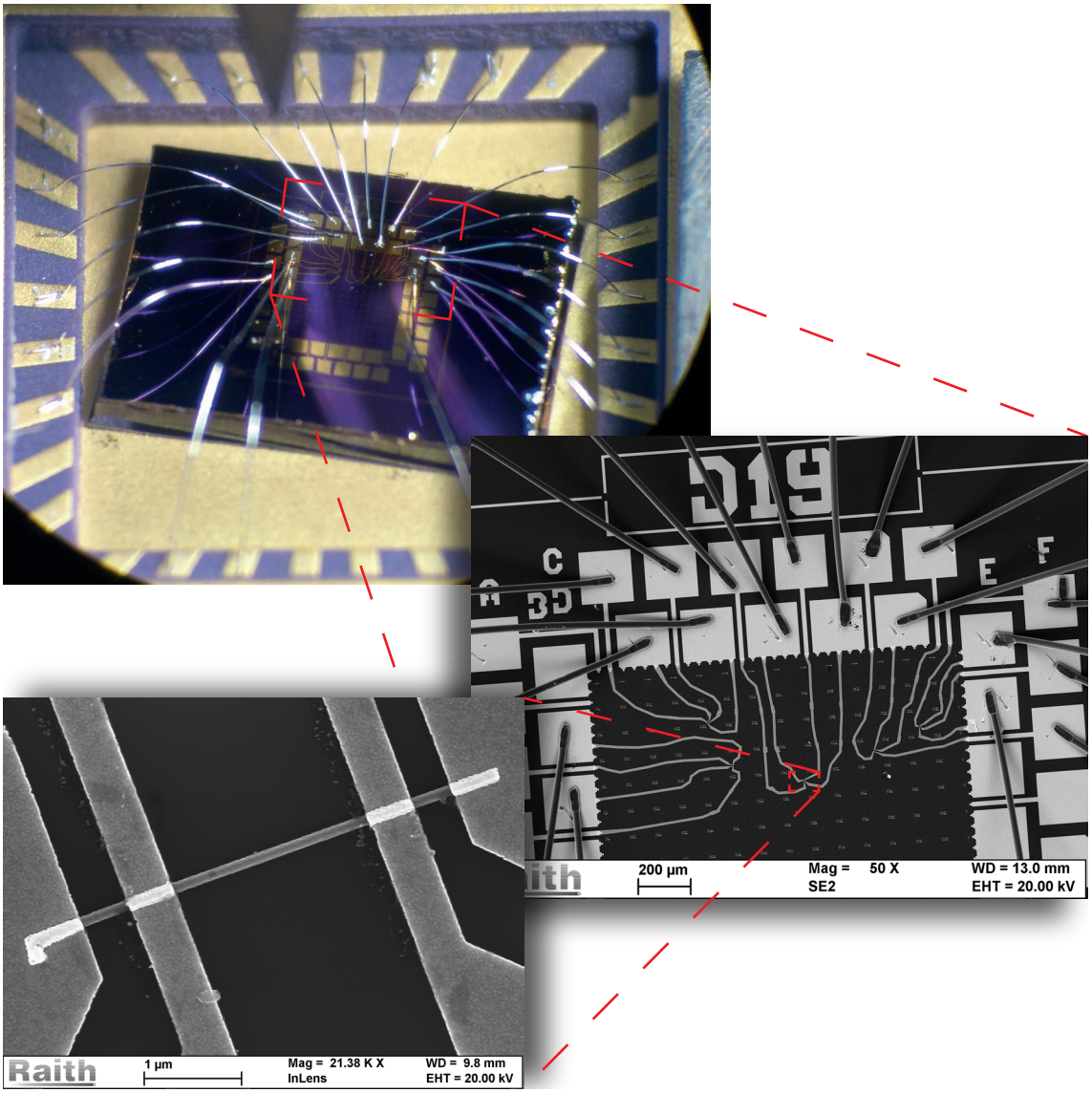

Figure D1.: Photograph and two SEM images of the bonded chip D19 and *Dev3* measured in triton 1.

E. Numerical Fit

In the main text it was mentioned that Equation 1.1.3 is a recursive function, i.e. a function that calls on itself, which has to be solved numerically. An approach on how to solve this problem will be presented in this appendix. The formula was given as

$$\ln\left(\frac{T_c(n,\Phi)}{T_c(0,0)}\right) = \psi\left(\frac{1}{2}\right) - \psi\left(\frac{1}{2} + \frac{\alpha(n,\Phi)}{2\pi T_c(n,\Phi)}\right) \ , \tag{E.0.1}$$

and

$$\alpha(n,\Phi) = \frac{\xi(0)^2}{\pi R^2} T_c(0,0)\left[4\left(n - \frac{\Phi}{\Phi_0}\right)^2 + \frac{t^2}{R^2}\left(\frac{\Phi^2}{\Phi_0^2} + \frac{n^2}{3}\right)\right] \ . \tag{E.0.2}$$

For a chosen threshold (R_c/R_N), a set of data-points are found, which make up the phase diagram. Each data point has a critical temperature $T_c(n,\Phi)$ with an associated flux Φ and an integer n that minimizes $\left(n - \frac{\Phi}{\Phi_0}\right)$. So for a given Φ (and hence n), estimates for the fitting parameters $\frac{\xi^2}{R^2}$ and $\frac{t^2}{R^2}$ have to be made to calculate the corresponding $\alpha(n,\Phi)$. The value for $\alpha(n,\Phi)$ is then inserted into the first equation, for which then a value for $T_c(n,\Phi)$ has to be found which solves the equation. The found $T_c(n,\Phi)$ is then compared to the measured value, if their difference is to large another set of fitting parameters have to be chosen, for which a new value of $T_c(n,\Phi)$ can be found. This has to be repeated until the parameters are found which bring $T_c(n,\Phi)$ closest to the measured value. Then, the next data-point is chosen, and the process starts over again, however, this time the best value found for the prior data-point might be chosen as starting value, as they should be rather close.

As this is a slow process to be done by hand, it would be preferred to write up a short computer program that does the math. This might be preferred anyway due to the digamma function which is easily solved by a computer.

F. Manuscript in Preparation

Epitaxial Aluminum contacts to InAs nanowires

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We report a procedure for Molecular Beam Epitaxy growth of Aluminum contacts to InAs nanowires. The methods results in an oxide-free epitaxial interface and highly transparent Ohmic electrical contact. The fabrication of .

Semiconducting Indium Arsenide (InAs) nanowires (NWs) have been implemented as the active elements in nanoscale electrical devices for a wide range of studies: Their high electron mobilities and low effective mass provide a good basis for superior field effect transistors[1], their surface transport channels and high surface-to-volume ratio make them obvious candidates for use in chemical sensors[2], and their strong spin-orbit coupling[3, 4], large g-factors[5] and relative ease of contacting to superconducting (SC) contacts has led to a number of breakthroughs in quantum transport[6–8].

Common for any such application of nanowires is the need for reproducible ohmic contacts and this often becomes a pivotal step in the fabrication scheme. In this respect the surface accumulation layer of InAs prevents the formation of a strong Shottky barrier at the metal/NW interface and makes contacting easier than for most semiconductors. Nevertheless, to achieve contact, the oxide which covers the wire surface needs to be removed prior to metal deposition and various techniques have been developed to tackle this problem. In the earliest work the oxide was removed by a brief etch in hydrofluoric acid (HF) immediately prior to metal deposition. This process is difficult to reproduce and often entire device batches turn out highly resistive probably due to oxide regrowth. To circumvent this problem Suyatin et. al., developed a procedure based on $(NH_4)_2S_x$ to dissolve the oxide and passivate the surface thus protecting it against further oxidation[9]. This procedure has been very successful and is now widely adapted, and lately also Argon ion milling has been used with success[10].

These approaches successfully removes the oxide, but also potentially etches or damages the InAs nanowire crystal surface. Such microscopic interface degradation has so-far remained irrelevant as the techniques produce highly transparent ohmic contacts. Lately, however, due to a potential use in topological quantum information[11], there has been an intense interest in inducing superconductivity in strong spin-orbit coupling nanowires by virtue of the proximity effect and in order to achieve an induced superconducting gap with a low amount of subgap states (a *hard* gap), Ref. [12] showed that a key parameter is the quality and uniformity of the SC/NW interface. Given the softness of the proximity gaps reported so far[13, 14], alternative contacting schemes needs to be investigated. Here we report new approach to making electrical devices from InAs nanowires with an oxide-free nanowire/metal epitaxial interfaces leading to reproducible low-resistance electrical contacts. The method is based on a single molecular beam epitaxy (MBE) growth of an InAs nanowire core and a metallic Aluminum (Al) nanowire shell. Because of the ultra-high vacuum of the MBE reactor the Al/InAs interface remains oxide-free and leads to good electrical contact between the metal shell and the NW core. We demonstrate the subsequent fabrication of devices in a field effect transistor geometry by contacting the metallic Al shell and locally exposing the InAs channel, and characterize their electrical performance. We discuss the potential of this method for creating superconducting contacts to nanowires and present electrical transport measurements below the critical temperature of the Al shell. We further demonstrate MBE-grown InAs nanowires coated by a partial shell thereby leaving half the nanowire susceptible for gating while preserving the properties of the superconducting contact interface.

The InAs nanowires were grown in the (111)B crystal direction by the Vapor-Liquid-Solid method in a solid source MBE system [15, 16]. Without breaking the reactor vacuum, the substrate is subsequently cooled below $-15°$C and the growth is ended with an Al layer of $50-100$ nm. At such low temperatures the diffusion length of Al is only a few nanometers and the Al crystals are formed uniformly along the side facets of the InAs nanowire. Two types of InAs/Al core/shell structures were investigated; one where the substrate was rotated during the Al growth resulting in a complete shell, and one where the substrate rotation was disabled, resulting in wires with a half Al shell. In the following we first discuss the full-shell structures. Figure 1(a) shows a transmission electron microscope (TEM) image of the resulting wires clearly revealing the InAs core and the surrounding Aluminum shell. The crystal grains of the Al shell have an extension of $\sim 50-70$ nm and are visible through the modulation of the TEM diffraction contrast resulting from different crystal-grain orientations. Due to

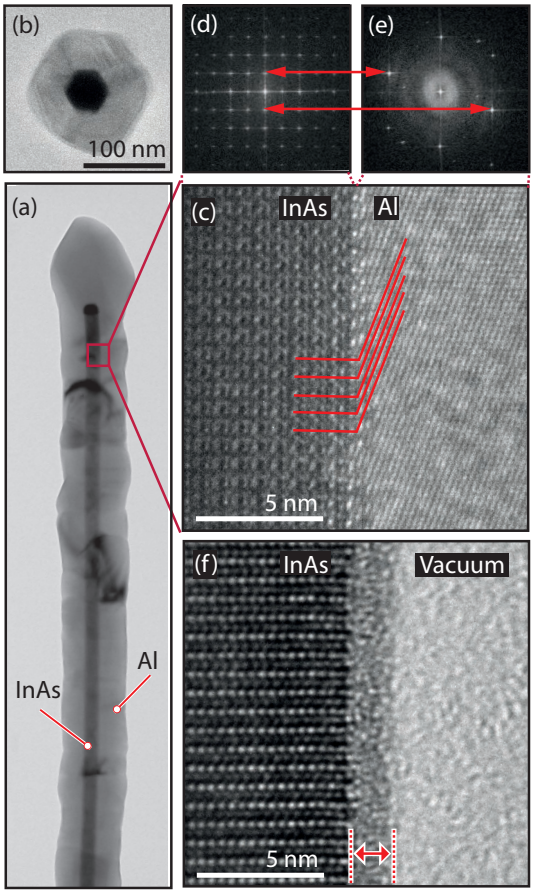

FIG. 1: (a) Transmission electron micrograph of an InAs nanowire encapsulated in MBE grown Al. (b) Top view TEM micrograph of a microtomed $\sim 100\,\text{nm}$ thick NW slice. The hexagonal cross-section of the wire is clearly seen and the Al shell conforms to this shape. (c) High-resolution TEM of the interface between the InAs NW and the Al. (d,e) The FFTs of the InAs and Al part of panel (c), respectively. (f) As (c) for an non-coated NW, showing the amorphous oxide on the surface (arrow).

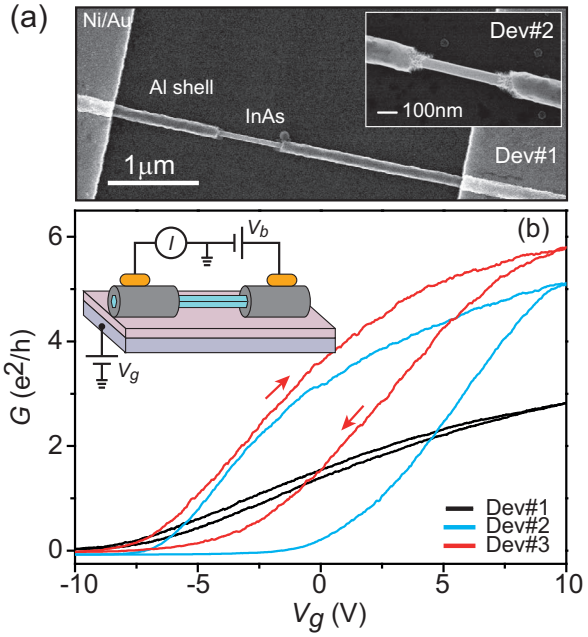

FIG. 2: (a) Scanning electron micrograph of Dev#1. The Al shell has been etched along a 600 nm segment to expose the InAs core. After the etch the device is capped in 30 nm Hafnium oxide and the doped substrate acts as a back gate electrode for modulation the carrier density in the InAs (inset to panel (b)). The inset shows the exposed channel of another device (Dev #2). (b) Room temperature conductance as a function of V_g for three different devices. Arrows indicate the direction of the sweep. Dev#1 is measured in vacuum; Dev#2 and #3 in air.

the short diffusion length of the Al at low temperatures the Al shell conforms to the hexagonal cross section of the InAs core as evident from Fig. 1(b) showing a TEM micrograph of a thin cross section slice cut parallel to the growth substrate using an ultra microtome[17]. Figure 1(c) shows a high-resolution TEM image of the InAs/Al interface from a different wire. The nanowire was oriented to have the [011]-direction along the viewing direction and the In and As atomic columns are clearly visible despite the Al shell. Importantly, the interface between the InAs core and the shell appears atomically abrupt with no intermediate oxide layer to degrade the electrical contact. This should be contrasted to the $2-3\,\text{nm}$ oxide typically forming when an InAs nanowire is exposed to air as shown in Fig. 1(f). Interestingly, in Fig. 1(c) also crystal planes of the Aluminum are visible (red lines). As inferred from the corresponding fast Fourier transform (FFT) in panel (e) the Al is oriented with the [011]-direction along the viewing direction and (1-11) along the NW axis. The visible (1-11)-planes form an angle of 70.5° to the (11-1) InAs/Al interface where the atomic separations 0.682 nm are very close to the InAs lattice spacing of 0.6995 nm. This epitaxial correspondence is indicated by the red lines in Fig. 1(c) and is responsible for the alignment of the (???)-peaks in the InAs FFT to the (-11-1)-peaks of the Al FFT indicated by red arrows between Fig. 1(d,e). Due to the weak TEM contrast of Al it is not possible to resolve the Al crystal planes for every position along the nanowire. However, whenever the crystal planes could be resolved the above relationship to the InAs was observed, and nowhere was an amorphous layer observed in the interface, i.e., the atomically sharp interface continues uniformly along the wire as desired for inducing a hard proximity gap in the wire when the shell is in the superconducting state.

To test the performance of the electrical contact formed by the grown shell, electrical devices were fabricated: The wires were liberated from the substrate by a brief sonication in methanol and a small amount of the resulting suspension was deposited on a Si substrate capped with 500 nm SiO_2. Wires were located with respect to predefined alignment marks using optical dark field microscopy and the ends of the wires contacted using elec-

tron beam lithography and evaporation of Ni or Ti. To break through the native oxide present the Al surface a brief Argon ion milling is performed inside the metal evaporation chamber. This procedure reproducibly creates contact to the Al shell. To gain access to the InAs core, a second lithography step is performed to open narrow windows in a resist between the contacts and the shell is removed by a brief 2-3 sec. etch in 12% buffered HF[18]. Finally, to enhance the performance of the backgate and to reduce switching noise, the device is coated in 20-30 nm of Al_2O_3 using atomic layer deposition. Figure 22(a) shows scanning electron micrograph of typical devices prior to the final oxide deposition, with a $\sim 0.5\,\mu$m wide segment of the InAs core exposed, and the inset to Fig. 2(b) shows the device schematic. We note, that in order to employ the Al shell to aid electrical contacts, the second lithography step is in principle obsolete as the first metal layer can act as the etch mask for exposing the InAs core; here, however, the two-step approach was used to separate the lithography-defined contacts from the region of exposed NW to ensure that close to this region the SC properties of the shell are intact.

Figure 2(b) shows the measured conductance as a function of the voltage V_g applied to conducting back plane of the substrate for three different devices. As expected for undoped InAs NWs the devices act as n-type semiconductors with an increased conductance for increased V_g. The devices are pinched-off at $V_g = -10\,$V and the peak conductance for $V_g = 10\,$V is 2.8, 5.1, and $5.8\,e^2/h$ for Dev#1, Dev#2, and #3, respectively. These values are comparable to the best results we have achieved for devices of comparable lengths and diameters using standard procedures for removing the InAs oxide. Also the temperature dependence of the G vs. V_g measurements shown in Fig. 2(b) indicates the presence of a barrier-free metal-semiconductor interface: At $V_g \gtrsim 0\,$V the conductance increases upon cooling of the device (due to the reduction of phonon scattering) rather than decreasing as is often observed for imperfect contacts due to the reduction of thermally excited transport.

Figure 3(a) shows the four-terminal resistance as a function of temperature of an Al-coated NW before the shell is etched. A clear superconducting transition is observed at $T_c \sim 1.3\,$K close to the value of bulk Al. Figure 3(b) shows the dependence of the resistance on magnetic field as a function of angle of the field with respect to the wire axis. The critical field B_c peaks at 75 mT for the parallel direction and has a minimum value of 50 mT in the perpendicular orientation. These values are comparable to what is obtained in conventional devices with a similar Al thickness[7]. Figure 3(c) shows a plot of dI/dV_{sd} vs. V_{sd} and $B_\perp$ for Dev#2 with the InAs core exposed along a $\sim 600\,$nm segment. As a consequence of the superconducting contacts, a clear conductance increase is observed at low fields for $|V_{sd}| < 2\Delta/e$ disappearing when $B_\perp > B_c \sim 60\,$mT. The absence of a zero-bias supercurrent is attributed to inadequate filtering of the electrical wiring in the cryostat. The results of

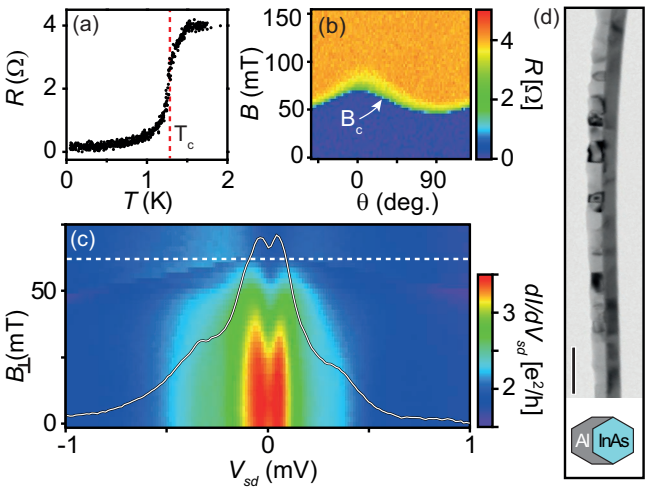

FIG. 3: (a,b) Temperature and magnetic field dependence of the four-terminal resistance of a wire with an intact Al shell (in (b), $T = 20\,$mK). (c) Measurement of dI/dV_{sd} vs. V_{sd} and $B_\perp$ at $T = 50\,$mK for Dev#2 with a $\sim 600\,$nm wide segment of exposed InAs (cf. Fig. 2). A clear conductance increase is observed for $|V_{sd}| \lesssim \pm 2\Delta/e = \pm 0.4\,$meV. White line: $B = 0\,$T trace ($dI/dV_{sd} = 1.8(3.3)e^2/h$ for $V_{sd} = -1(0)\,$mV). (d) TEM micrograph of a half-coated InAs nanowire and schematic top view (inset).

Fig. 3 demonstrates that as a superconducting contact, the MBE grown shell performs as well as conventional planar contacts in the standard SC/NW/SC geometry. In addition, however, due to the perfect uniformity and control of the grown SC/NW interface we expect a harder induced gap[12], better suited for studying Majorana-related physics. To study the characteristics of density of states in the nanowire, hybrid normal-metal/NW/S devices must be realized in the tunneling regime and such devices will be the focus of future experiments.

Finally we note, that for the purpose of creating Majorana end-states in proximity-coupled strong SOI NWs, a tuning of the chemical potential is required and therefore part of the wire must be susceptible to electrostatic gating. For this, a fully covering shell is unsuited. Instead, by disabling the growth-substrate rotation while depositing the Al, a half-covering contact with the same perfect nanowire-superconductor interface can be achieved as illustrated in Fig. 3(d).

In conclusion we have demonstrated a new scheme for producing highly transparent

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