University of Copenhagen

M.Sc. Physics

Master's Thesis
August 2023

Lazar Lakic KU- ID: mjx381

Connecting the dots: Laying the foundation for coupling Ge/SiGe quantum dots via PtSiGe superconductors

Advisors: Anasua Chatterjee and Ferdinand Kuemmeth

Abstract

In this thesis, we work towards realizing an extended range link between two semiconductor quantum dot (QD) spin qubits, mediated by a superconductor, as proposed by M.Leijnse and K.Flensberg in 2013 [1].

This is achieved by fabricating and characterizing quantum dots in strained planar Germanium/SiliconGermanium (Ge/SiGe) heterostructures, alongside a novel approach to fabricating nanoscale Platino-Germano-Silicide (PtSiGe) superconducting structures [2]. We demonstrate single hole occupation of quantum dot and double quantum dots, making use of charge sensing techniques such as dynamic sensor compensation, and RF-reflectometry. Furthermore, we characterize nanoscale junctions between superconducting (S) and normal conducting (N) materials. Specifically, SNS- and NSN-junction measurements of PtSiGe superconducting nanostructures. In addition to this, we characterize a S-QD-S junction, constituting the first reported measurements of a proximitized hybrid quantum dot in the group-IV planar Ge/SiGe platform. By demonstrating these individual components, we provide scope for extended range interactions for quantum dot based spin qubits mediated by a superconductor.

0.1 Aknowledgements

I would like to express my deepest gratitude to **Anasua Chatterjee** and **Ferdinand Kuemmeth** for making this project possible, for welcoming me into your group, and for believing in me. I feel truly blessed to have you as my advisors.
I'm extremely grateful to **William I.L. Lawrie** for being my experimental mentor and guide into the adventures of Germanium, but most importantly for being my friend - I love you brø. I would like to extend my sincere thanks to **Jørn Otto Bindslev Hansen** for agreeing to be the censor for my thesis defense. I would like to give a Special thanks to **Giordano Scappucci** for blessing my project with his wonderful material.
Massive thanks should also go to **David van Driel**, **Fabrizio Berritta**, **Benjamin Joecker**, **Kasper Grove**, **Jens Paaske** and **Karsten Flensberg** for providing theoretical and/or technical support during the project and hopefully also after.
I am also very grateful for my fellow group members in the Copenhagen Spin Qubit team, **Oliver Liebe**, **Charalampos Lampadaris**, **Tsung L. Chung**, **Bertram Brovang**, **Torbjørn Rasmussen**, **Fabio Ansaloni**, **Emily Hajigeorgiou**, **Ida Vaaben Ladefoged**, **Anton Zubchenko** and **Marcin Kepa**, one could not get a better team.
QDev is an amazing place and would not be the same without the wonderful people that work here, thank you **Lena R. Jacobsen**, **Rasmus B. Christensen**, **Johanna Jallberg**, **Ingrid Vernimmen**, **Lars Lemming**, **Smitha Nair**, **Jesper Kock**, **Martin Bjergfelt**, and **Maria João Batista** for making this place run.
I also want to thank my collegues at QDev for always being awesome, helpful and making QDev a wonderful place to be - **Robert G. Larsen**, **Rasmus Dalsgaard**, **Thomas Kanne**, **Joachim Sestoft**, **Tobias Særkjær**, **Michaela Eichinger**, **Zhen Hai Sun**, **David Bofill**, **Malthe M. Nielsen**, **Serwan Asaad**, **Gunjan Nagda**, **Luca Banszerus**, **Sangeeth Kallatt** and **Jakål Hastrup**. I am sorry if I forgot anyone. I would furthermore like to thank my dear friend **Morten Kjaergaard** for dad coffees, shooting the shit and for always having my back. I would also like to thank **LTS society** for supporting young scientists since 2017.
Thanks mom, dad, and little bro, volim vas puno! Finally I want to thank my wife **Lea**, and my two children **Costa** and **Veneda** for your unwavering love and support, I can not express how much I love you three.

I would like to dedicate this thesis to our sensei **Thor Rasmussen**. You were a role model for my son and I, and we will never forgot the time we had with you. May your gentle soul rest in peace.

Contents

1 Introduction and motivation

1.1 The Semiconductor spin qubit platform

From the 1980s through to the early 2000s, theorists from the fields of physics, mathematics and computer science laid the theoretical foundation for a universal quantum computer. Proposing various algorithms which could utilize quantum superposition and entanglement to perform certain tasks more efficiently than would be possible on classical computers. [3, 4, 5, 6, 7, 8, 9, 10]. Since then, many approaches have been taken towards achieving this goal. Qubits [11], being the basic computational units for quantum computers, have since the late nineties been realized in many different platforms. Some of the more established and mature systems to this date include superconducting qubits [12], ion traps [13], neutral atoms [14] and photonic platforms [15]. All with their characteristic advantages and drawbacks, and while all of these systems are promising in their own way, we will in this thesis study and try to advance the semiconductor gate defined spin qubit platform [16]. Specifically in the material platform Germanium/SiliconGermanium (Ge/SiGe).
In the recent years semiconductor qubit systems have rapidly gained ground as a popular contender in the quantum computation race, showing long coherence times [17] and high single gate fidelities [18, 19]. While there still is a long way to go in terms of multi qubit gates and scalability (the latter also being an issue in most other platforms), the semiconductor spin qubit platform however shows promise in regards of scaling due to the small footprint of devices and the compatibility with established semiconductor industry in terms of fabrication and manufacturing.

A proposed approach to scaling spin qubits is to pattern a quantum processor unit with three main components - namely sparse qubit arrays, on-chip classical electronics and long range coupling links between the qubit arrays.
The sparse qubit arrays would then consist of a finite number of qubits being controlled by neighbouring classical circuits in the form of cryogenic multiplexers, analog to digital converters, possibly also filters and RF-switches, and furthermore the long range links that will couple the qubit arrays [20].

These long range coupling links range a plethora of approaches from superconducting resonators [21], gate-based charge/spin shuttling [22] and last but not least the hybrid super-semi route of coupling spins via superconductors [1, 23].

1.2 Strained planar Germanium

Before introducing the overarching experiment this thesis lays the footwork for. We will introduce the material platform we have chosen to work in. Namely Germanium, and specifically strained planar Germanium (Ge/SiGe). Material of this type has in the last couple of years shown to have high mobilities, on the order of $10^6\,\mathrm{cm}^2/\mathrm{Vs}$, and low percolation densities (on the order $5 \cdot 10^{10}\ \mathrm{cm}^{-2}$) [24], which is a metric that indicates disorder in the few charge carrier regime - in which our spin qubit devices inherently are operating. The large spin orbit interaction in Ge/SiGe allows for electrically operated qubits rotations. This means that qubit rotations can be implemented just using global magnetic fields and fast operated gate electrodes. Contrary to Si/SiGe that needs local micromagnets to create an artificial spin orbit interaction, or in doped silicon platforms which need electron dipole spin resonance antennas. Germanium hole qubits have also been shown to have T1 coherence times on the order of tens of milliseconds [25], and T2 times of micro seconds. and single gate fidelties of more than 99.99% [19]. In addition to all of this, Germanium is a group-IV material just as Silicon, and has a naturally low abundance of nuclear spin isotopes. Nuclear spin isotopes are a source of decoherence as they interact with the qubit spin energy levels through the hyperfine interaction [26]. Germanium can however also be entirely isotopically purified, that is removing all spinfull isotopes. In addition to all of the aforementioned, it has been shown that germanium is able to form ternary superconductors with silicon and various metals e.g. Platinum and Iridium [27]. Implementing superconductors with Silicon, is usually not possible as the majority of metals will form Schottky barriers upon contact.

The Ge/SiGe heterostructure material we work with is realized by chemical vapor deposition techniques. Starting with a pure silicon wafer, then Germanium is grown while gradually adding in Silicon for roughly a micron, until reaching a concentration of $Si_{0.2}Ge_{0.8}$ (SiGe) which is grown in that ratio for an additional 160 nm. Then a 16 nm layer of pure Germanium is grown, which then is topped by a 22 nm layer of $Si_{0.2}Ge_{0.8}$ and a 1 nm Si passivisation cap [28] as seen in Fig.1.c). This sort of hetero structure now allows for the accumulation of a two dimensional hole gas (2DHG) in the interface between the top layer of the pure Germanium and the $Si_{0.2}Ge_{0.8}$. We can then proceed with fabricating ohmic contacts and gate electrodes in multi-layer devices. Making it possible to electrically confine, and isolate spinfull charge carriers to use as qubits.

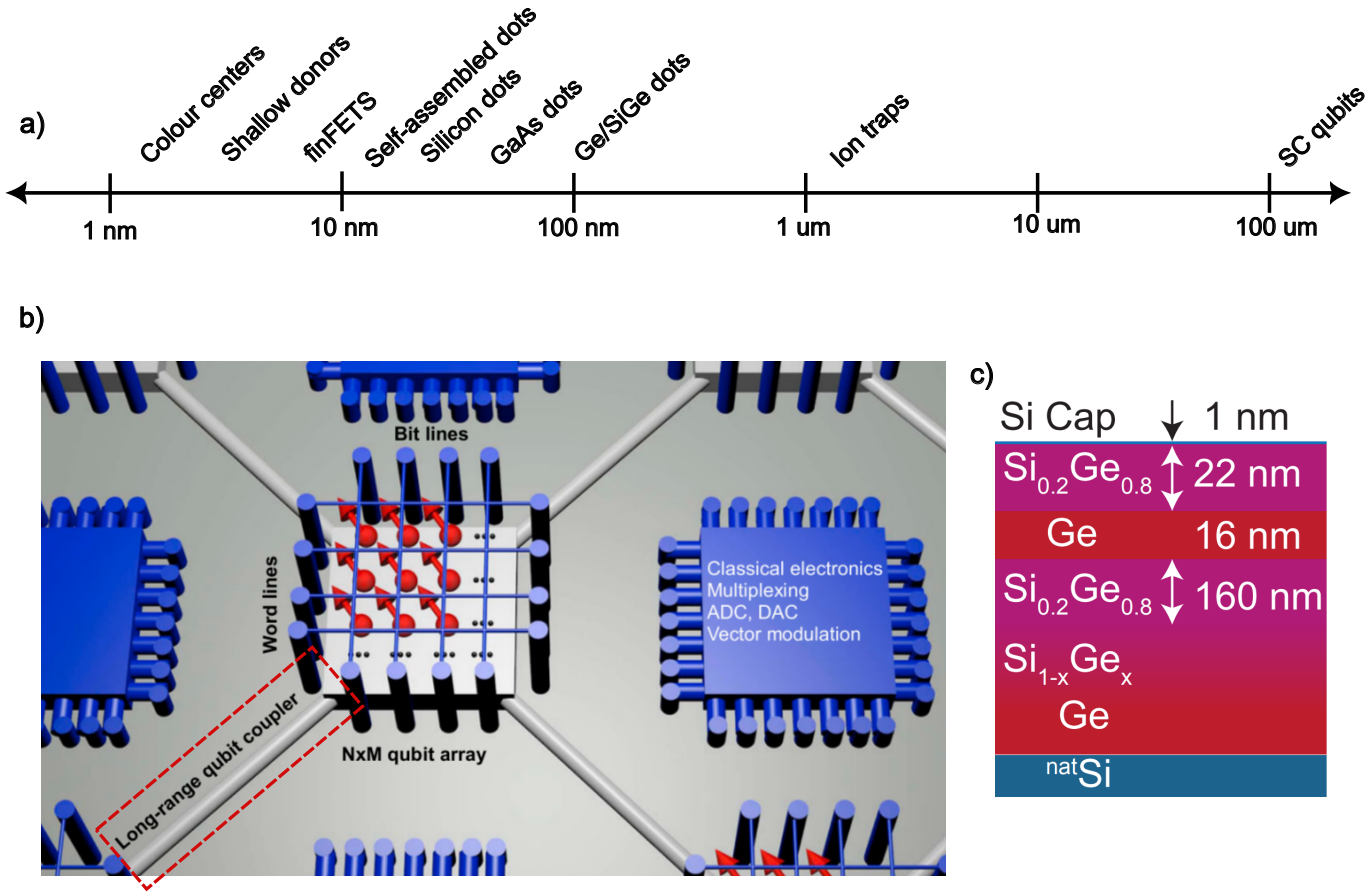

Figure 1: a) Qubit platforms alongside their respective fabrication footprint. Figure adapted and modified from [29]. **(b)** Scaling of spin qubits, Sparse qubit arrays connected with long range coupling links (highlighted in the red dashed line), all neighboured by on-chip classical circuitry. Figure adapted from [20]. **c)** Planar germanium Ge/SiGe heterostructure material stack adapted from [30].

1.3 Coupling spin qubits with superconductors pt.1

The motivation of the work done in this thesis is the long range coupling links seen in Fig.1.b) and specifically the hybrid super-semi route due to its small footprint compared to superconducting resonators and charge shuttlers. The idea of a long-range coupler is to provide a certain distance between the spin qubits, and while all the approaches can do this, the superconducting resonator approach unfortunately brings on-chip microwave feedlines that are millimeter sized and inputs microwaves that potentially add to the thermal load [31, 32]. while the super-semi approach does not. Furthermore the charge-shuttling devices use at least six gates and 4 signal generators to shuttle a charge carrier from one site to another [22] (without entering a discussion of spin state coherence), while the super-semi approach we are about to introduce possibly only uses three gates, which there of - only two are needed to be operated fast.

Delving into the full physics of how to exactly couple two spins via a superconductor will be beyond the scope of this thesis. We will nevertheless try to present the basic mechanisms in order to understand what experimental prerequisites that are needed to perform such experiments. Since the work done in this thesis is mainly about establishing these prerequisites. But before doing so we will introduce the basic theory needed to understand the measurements done in this thesis, as well as understanding the concept of coupling two spins via a superconductor.

2 Theory

2.1 Holes as charge carriers

2.1.1 Bulk Germanium

A remarkable property is that almost every metal brought in contact with Germanium exhibits Fermi pinning to the edge of the valence band [28]. This means that the electrons in the germanium valence bands have enough energy to get excited to the conduction band leaving the holes in our first valence band as our main charge carrier. The valence bands of bulk Germanium would be 6-fold degenerate in the Γ point of the crystal where the momentum $\hbar\mathbf{k} = 0$, $\mathbf{k}$ being the wave vector. The degeneracy being the combination of the spin and orbital quantum numbers l and m, l being 1 due to the valence band being a p-type orbital [33] and thus having $m_l = \{-1, 0, 1\}$ *and* $m_s = \{-1/2, 1/2\}$. Which would yield the combination of states $|m_l, m_s\rangle = \{|-1, -1/2\rangle, |-1, 1/2\rangle, |0, -1/2\rangle, |0, 1/2\rangle, |-1, -1/2\rangle, |1, 1/2\rangle\}$ However due to spin orbit coupling $\delta_{SO}\mathbf{L}\cdot\ \mathbf{S}$ the split off band (SO) is split from the Heavy hole (HH) and light hole (LH) band creating a $\Delta_0 = 0.3\,\text{eV}$ [30] energy gap from the two valence bands to the split off band. This happens since $\mathbf{L}\cdot\mathbf{S}$ does not commute with with L nor S,

$$[\mathbf{L}\cdot\ \mathbf{S}, \mathbf{S}] = i\hbar(\mathbf{S}\times\mathbf{L}),\ \textit{and}\ [\mathbf{L}\cdot\mathbf{S}, \mathbf{L}] = i\hbar(\mathbf{L}\times\mathbf{S}), \tag{2.1}$$

and since we no longer can use the quantum numbers m_l and m_s. We have to invoke the addition of the orbital and spin degree of freedom since $\mathbf{J}$ commutes with $\mathbf{L}\cdot\mathbf{S}$. By dotting $\mathbf{J}$ with $\mathbf{J}$ we get

$$\mathbf{J}^2 = \mathbf{L}^2 + \mathbf{S}^2 + 2\mathbf{L}\cdot\mathbf{S}. \tag{2.2}$$

which can be rearranged to look exactly like our spin orbit operator

$$\mathbf{L}\cdot\mathbf{S} = \frac{1}{2}(\mathbf{J}^2 - \mathbf{L}^2 - \mathbf{S}^2) \tag{2.3}$$

thus the eigenstates at the crystal momentum $\hbar\vec{k}_{x,y,z} = 0$ belong to the total angular momentum $\mathbf{J} = \mathbf{L} + \mathbf{S}$. with a new quantum number j which takes on the values $|l - s| \leq\ j \leq l + s$, we get j=3/2 and 1/2, which generates a m_j ranging from -j to j in integer steps. This means that we now have a p-type orbital of j=3/2 yielding
$\left|j, m_j\right\rangle_{val} = \{|3/2, -3/2\rangle, |3/2, -1/2\rangle, |3/2, 1/2\rangle, |3/2, 3/2\rangle\}$ states and a second p-type orbital of j=1/2 with states $\left|j, m_j\right\rangle_{SO} = \{|1/2, 1/2\rangle, |1/2, -1/2\rangle\}$.
Letting the spin orbit operator $\delta_{SO}\mathbf{L}\cdot\mathbf{S} = \frac{\hbar^2\delta_{SO}}{2}(j(j+1) - l(l+1) - s(s+1))$, with s=1/2, and

l=1 act on these states we get

$$\delta_{SO}\mathbf{L}\cdot\mathbf{S}\left|3/2,\pm3/2\right\rangle = \delta_{SO}/2 \; and \; \delta_{SO}\mathbf{L}\cdot\mathbf{S}\left|3/2,\pm1/2\right\rangle = \delta_{SO}/2, \tag{2.4}$$

and for

$$\delta_{SO}\mathbf{L}\cdot\mathbf{S}\left|1/2,\pm1/2\right\rangle = -\delta_{SO} \tag{2.5}$$

thus seeing that the four fold valence band is split from the other band with energy $\Delta_{SO} = 3\delta_0/2$.

2.1.2 Adding confinement

The dispersion of the valence bands is modelled by the Luttinger-Kohn hamiltonian which is based on $k \cdot p$ theory. and looks like the following expression, which is the simplified Luttinger-Kohn hamiltonian [33] in the spherical approximation which means that when calculating the band structure one can invoke some symmetry arguments due to Germanium being grown on the high symmetry axis [100].

$$H_{LK} = \frac{\hbar^2}{2m_{eff}}\left[\left(\gamma_1 + \frac{5}{2}\gamma_s\right)k^2 - 2\gamma_s(\vec{k}\cdot J)^2\right]. \tag{2.6}$$

We have $\hbar$ as the reduced Plancks constant, k the wavevector (here in all directions), and m_{eff} as the effective mass. γ_s and γ_1, are 'free' parameters called the Luttinger parameters and **J** is the total angular momentum $\mathbf{J} = \mathbf{L} + \mathbf{S}$. An important thing to note is that the direction of motion is correlated with the quantization axis. This means that our total angular momentum points the same way as our carriers move Fig.2.a). So when letting this monster operate on our 4 valence band states, we let the direction of motion be in the direction y direction for simplicity, first, for what we call the heavy hole states

$$H_{LK,\hat{y}}\left|3/2,\pm3/2\right\rangle_y = \frac{\hbar^2 k_y^2}{2m_{HH}}\left|3/2,\pm3/2\right\rangle_y, \tag{2.7}$$

where m_{HH} is the heavy hole mass

$$m_{HH} = \frac{m_{eff}}{\gamma_1 - 2\gamma_s}. \tag{2.8}$$

Then for the light hole states

$$H_{LK,\hat{y}}\left|3/2,\pm1/2\right\rangle_y = \frac{\hbar^2 k_y^2}{2m_{LH}}\left|3/2,\pm1/2\right\rangle_y, \tag{2.9}$$

where m_{LH} is the light hole mass

$$m_{LH} = \frac{m_{eff}}{\gamma_1 + 2\gamma_s} \tag{2.10}$$

this is where the names light and heavy hole states originate from[1].
However as mentioned our material is a hetero-structure and thus confined in the z-direction. The confinement of course comes from the fact that our holes predominantly live in the interface plane between the top layer of $Si_{0.2}Ge_{0.8}$ and the pure germanium layer. We can thus write the Hamiltonian as the following in which k_z is much bigger than k_x and k_y. What this in practice means is that the quantization axis becomes embedded along the confined axis and not anymore the direction of motion. If we first look at the energy along the direction of transport, in this case picking the y-direction we have that

$$H_{LK,\hat{y}} \left|3/2, \pm 3/2\right\rangle_z = \frac{\hbar^2 k_y^2}{2m_{HH}} \left|3/2, \pm 3/2\right\rangle_z, \tag{2.11}$$

where m_{HH} now counter intuitively has become the lighter mass,

$$m_{HH} = \frac{m_{eff}}{\gamma_1 + 2\gamma_s}. \tag{2.12}$$

Then light hole state

$$H_{LK,\hat{y}} \left|3/2, \pm 1/2\right\rangle_z = \frac{\hbar^2 k_y^2}{2m_{LH}} \left|3/2, \pm 1/2\right\rangle_z, \tag{2.13}$$

where m_{LH} has become the heavier mass

$$m_{LH} = \frac{m_{eff}}{\gamma_1 - 2\gamma_s}. \tag{2.14}$$

This has the outcome that the mass of our heavy hole in the transport direction becomes lighter! Making it such that the orbital levels in laterally confined direction become bigger, which in practice means that we can relax the size of our gates in nanofabrication. Contrary to Silicon which has a high effective mass in the transport band, and needs very small gates structures to confine the wavefunction Fig.1.a). Since the momentum in the confined direction is much stronger (we let k_x and k_y be very small)

$$H = \frac{\hbar^2}{2m_{eff}} \left[\left(\gamma_1 + \frac{5}{2}\gamma_s - 2\gamma_s \vec{J}_z)^2 \right) k_z^2 \right], \; k_z >> k_x, k_y, \tag{2.15}$$

[1]Since the effective mass of the $|3/2, \pm 3/2\rangle$ state is heavier in the top band, and vice versa for the bottom band.

if we are to apply that to our states along the quantization axis we get

$$H_{LK,\hat{z}} \left|3/2, \pm 3/2\right\rangle_z = \frac{\hbar^2 k_y^2}{2m_{HH}} \left|3/2, \pm 3/2\right\rangle_z, \tag{2.16}$$

and

$$H_{LK,\hat{z}} \left|3/2, \pm 1/2\right\rangle_z = \frac{\hbar^2 k_y^2}{2m_{LH}} \left|3/2, \pm 1/2\right\rangle_z, \tag{2.17}$$

taking the difference we actually get an energy splitting at $k_y = k_x = 0$, thus lifting our degeneracy with energy

$$\Delta E_{HH,LH} = \hbar^2 k_z^2 \left(\frac{1}{m_{HH}} - \frac{1}{m_{LH}} \right), \tag{2.18}$$

as seen in Fig.2.b) Leaving our heavy hole state two fold degenerate and closer in energy to 0, thus more energetically favorable i.e. our main carrier in this system and also the potential computational basis if one is to make qubits.

However when we split the heavy hole and light hole bands they also anticross, leading to heavy hole and light hole mixing for k_y and k_x different than 0 Fig.2.d), and in reality produce a complicated wave function that is a mix of the orbital and spin degree of freedom. And while we say our computational basis is J=$\pm 3/2$, we still need to mix the light hole and heavy hole in order to flip the spin. Since there is no way for a boson to flip a spin $3/2$ particle in for example spin dipole resonance experiments. If we now add strain to this system, which is a bit out of the scope for this thesis, one would split the light hole states down further by adding a Bir-Pikus strain hamiltonian term which results in some energy Δ_{strain} [34]. This strain comes from the mismatch between $Si_{0.2}Ge_{0.8}$ and the pure Ge, along the Si cap on top. Finally, in order to lift the spin degeneracy in our heavy hole band we would have to see how the spin orbit acts on the heavy hole spin states, this is done with a Rashba type spin orbit hamiltonian [35]. We will not go into depth with the hamiltionan except for mentioning that effect of this hamiltonian, is spin energy states that are highly dependant on the orientation of the magnetic field (usually lead to a high g-factor in the out of plane direction) and of the confinement potential. The latter gives us the advantage of electrical g-factor modulation, however also the disadvantage of the hole spin states being susceptible to charge noise.

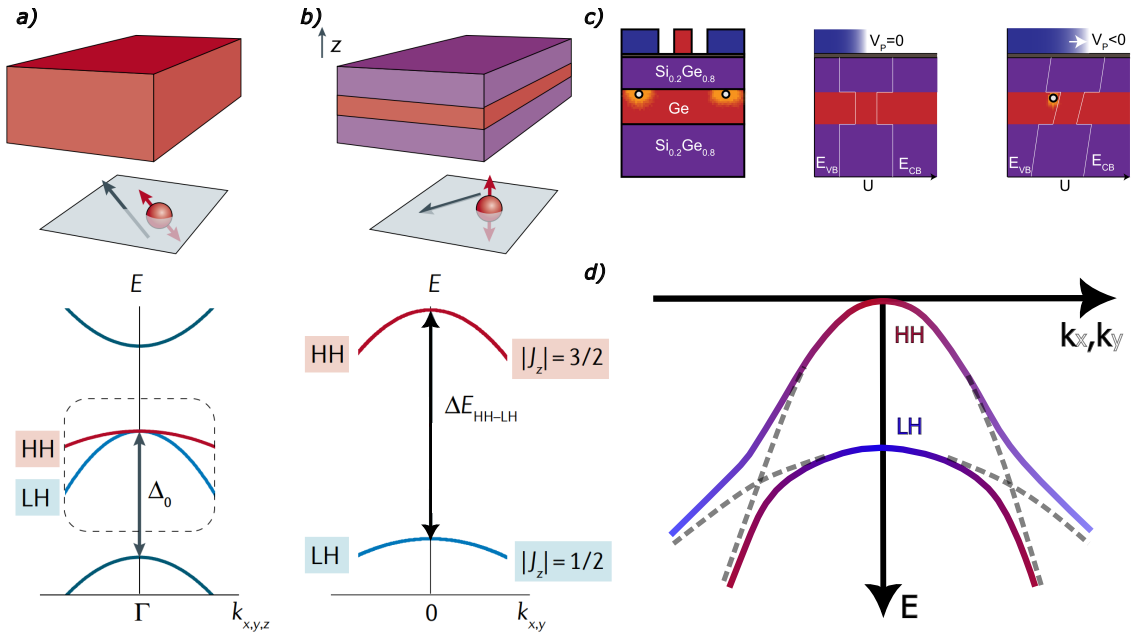

Figure 2: a) Bulk germanium properties showing the quantization axis along the direction of motion alongside the degeneracy of the heavy hole and light hole bands at $\mathbf{k}_{x,y,z} = 0$. Figure adapted from [30]. **b)** Confined germanium properties, quantization axis locked to the z axis, heavy hole and light hole bands are split due to this confinement. Figure adapted from [30]. **c)** Cartoon image of heterostructure bands when applying a negative gate voltage, the bands bend allowing accumulation of holes. Figure adapted from [28] **d)** Zoom in of the bands after both confinement and strain, showing the mixing of heavy hole and light hole bands.

2.2 Hole quantum dots in Ge/SiGe

As we learned before the main carrier in our hetero-structure is the heavy hole located in the valence band. If we were to have no ohmic reservoirs our two dimensional hole plane would be unpopulated, in order to populate our empty plane and make it a two dimensional hole gas (2DHG) we are to accumulate charge carriers from our ohmic reservoirs and into the semiconductor. This is done by applying a negative gate voltage as in Fig.2.d), bending the valence and conduction bands allowing for the semiconductor to have free states in the valence band. A semiconductor gate based quantum dot is a spatially confined nano-structure structure defined and controlled by electrostatic gate electrodes which we call barrier, confinement, and plunger gates. The barrier gates serve as tuneable tunnel barriers from quantum dot to the adjacent source and drain electrodes and other quantum dots. The cutoff/confinement gates in our case serve as a way to confine the holes and their wavefunction to a small region and prevent the charge from crawling up along the gate fan-out. The plunger gate controls the quantum dots chemical potential, and thus the allowed energy states of the quantum dot.

2.2.1 A single quantum dot

We will now briefly introduce the theoretical formalism for a single quantum dot coupled to a source drain reservoir. Where the source and drain resevoit have a chemical potential μ_S, and μ_D which can be controlled with a bias voltage. We start by introducing the electrostatic energy for a quantum dot which usually is called the Coulomb energy , this is given by the self capacitance of the dot and the number of holes residing in it

$$E_{static} = \frac{e^2N^2}{2C} = \frac{e^2N^2}{16\epsilon_0\epsilon_r r}, \tag{2.19}$$

which is directly proportional to the square of the number of holes in the dot and inversely proportional to the dot radius r. If we then want to know how much energy it takes for adding a hole to the quantum dot, knowing that there already is N holes on the dot, we will have to take the electrostatic difference for N+1 and N holes, this is called the charging energy.

$$E_c = E_{static}(N+1) - E_{static}(n) = \frac{e^2N}{8\epsilon_0\epsilon_r r}. \tag{2.20}$$

The energy it costs to add a hole, irrespective of the number of holes on the dot, is

$$\Delta E_C = E_c(N+1) - E_c(N) = \frac{e^2}{8\epsilon_0\epsilon_r r} \tag{2.21}$$

which is confusingly usually referred to as the charging energy aswell [26]. We will from now on only use ΔE_C as the charging energy. This energy furthermore sets a boundary on the temperature needed to charge a dot, since ΔE_C has to be much smaller than k_bT

We have so far only considered the classical energy scales. In order to have the full picture we need to include the energies associated to the confinement energy of the quantum states that reside on the dot. This confinement leads to an energy ΔE which is the quantum mechanical level spacing. In materials with a parabolic dispersion such as Si, GaAs and Ge/SiGe we can consider the confinement as harmonic oscillator potential [26]. From that we can infer the ground state of

$$E_0 = \frac{\hbar\omega_0}{2} = \frac{\hbar^2}{4m^*r^2}, \tag{2.22}$$

where m* is the effective mass, about $0.05m_0$ for a heavy hole in strained planar Ge/SiGe. Furthermore we have r which is the spacial extent $r = \sqrt{\hbar/(4m^*\omega_0)}$, meaning that for a quantum dot of size 150 nm we get an energy scale of roughly $E_0 = 40\,\mu eV$ which is much smaller than the charging energy - usually around 1-2 meV.

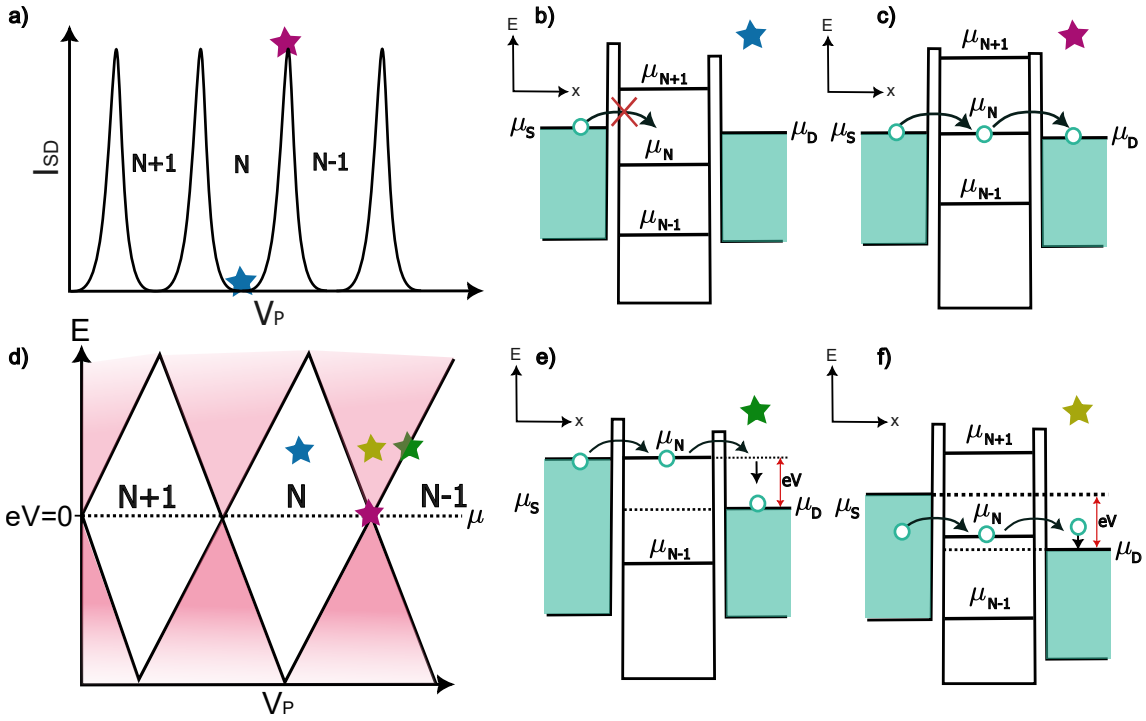

Figure 3: a) Coulomb oscillations with stars representing Couloumb blockade (blue), and elastic transport (Magenta) **b)** Energy level picture of coulomb blockade. **c)** Energy level picture of resonance peak at when all chemical potentials levels are aligned. **d)** Coulomb diamonds source drain bias as a function of plunger gate. Coulomb blockade all the white in the diamonds correspond to coulomb blockade, The pink corresponds to conductance. **e)** Energy level diagram of resonance at finite chemical potential. **f)** Energy level diagram of resonance at $\mu_S > \mu_N(V_P) > \mu_D$. All figures adapted and modified to suit hole carriers from [26]

A particular quantum ground state energy E_N in a quantum dot is dependent on the plunger gate voltage $E_N(V_P)$

$$E_N(P) = E_N(V_P) - |e|N\alpha\Delta V_P \tag{2.23}$$

where $V_P(N)$ is an initial plunger gate voltage corresponding to a dot level and α is the lever arm (A metric for how well the plunger can control the chemical potential of the quantum dot). and ΔV_P is the plunger voltage difference from one Coulomb oscillation peak to the next. Taking the difference in gate voltage dependent state energy, gives us the chemical potential of a quantum dot as a function of plunger gate,

$$\mu_N(V_P) = E_{N+1}(V_P) - E_N(V_P). \tag{2.24}$$

This is thus an expression for the chemical potential of our quantum dot levels, we can alter it by applying a voltage to the plunger gate, and thus engineer situations where current flows

i.e. when μ_S, μ_D, and μ_N are aligned ensuing coulomb resonances Fig.3.c) and when misaligned current is blockaded Fig.3.b). Quantum dots are often characterized by measuring coulomb diamonds in bias spectroscopy, by moving the chemical potential (that is sweeping the bias voltage) vs the plunger gate, we obtain a measurement like in Fig.3.d), where the white regions are coulomb blockaded and have zero conductance, and the pink regions are coulomb resonances. Parking at a finite bias voltage and sweeping the plunger gate, one would retrieve Fig.3.a) with a peak broadening corresponding to the length of the magenta region at the chosen bias voltage. From coulomb diamond measurements we can extract the charging energy, as well as the lever arm , by using

$$\Delta V_P = \frac{E_c}{\alpha} = \frac{V_{SD}}{\alpha}, \tag{2.25}$$

where the V_{SD} is the voltage from the top of a diamond to zero bias.

2.2.2 Double quantum dots

Placing two quantum dots next to each allows for capactive and tunneling coupling between them. To address this situation we have to include a chemical potential for both of the dots, μ_L for the left dot and μ_R for the right dot, which then again depends on the number of holes on each of the dots N_L, N_R residing on them. The energy needed for adding a single hole on one of the two quantum dots becomes dependent on the other dot [36]. Starting with the the left dot

$$\Delta E_{CL} = \mu_L(N_L + 1, N_R) - \mu_R(N_L 1, N_R), \tag{2.26}$$

and for the right dot

$$\Delta E_{CR} = \mu_R(N_L, N_R + 1) - \mu_L(N_L 1, N_R). \tag{2.27}$$

And furthermore a mutual charging energy E_{MC} which denotes the charging energy for one dot when the number of holes changes on the other dot

$$E_{MC1} = \mu_L(N_L + 1, N_R) - \mu_L(N_L, N_R), \tag{2.28}$$

which is the same the other way around for the other quantum dot

$$E_{MC2} = \mu_R(N_L, N_R + 1) - \mu_R(N_L, N_R) \tag{2.29}$$

To understand how the chemical potentials are dependent on capacitive coupling we can use the capacitance model where the total electrostatic energy of the system is given by the

mutual capacitive couplings. But before diving into this we will model our system much akin to that of our device. Since our device is technically three dots, Left dot, right dot and sensor dot, and of them only the sensor dot has a source and a drain. We will thus look at system of two dots in a charge sensing configuration Fig.4.a). Charge sensing is a way of detecting abrupt changes of charge using a sensor dot coupled to a source and drain. The charge sensor dot will be capacitively coupled to the double dot system and be prepared such that it has a finite number of charge carriers, and its chemical potential tuned to a Coulomb resonance. Thus when charge occupation changes occur in the neighbouring double dot system due to off-loading or un-loading of charge carriers the chemical potential of the sensor dot changes, and thus a change in current occurs. The following description of the charge stability diagram neglects the capacitive coupling of the sensor dot for simplicity, and assumes a double dot in series with a source and drain, it will however give rise to the same charge stability diagram as one will see in the charge sensing. The total energy of this system of two dots in series is thus given by

$$U(N_L, N_R) = \frac{N_L^2 E_{CL}}{2} + \frac{N_R^2 E_{CR}}{2} + U_{CC}(V_{LP}, V_{RP}), \tag{2.30}$$

Where U_{CC} is a cross capacitive term, which in reality can include cross coupling terms for all components of the circuit coupled to each other. Sweeping the two dot plungers vs each other reveals a coulomb stability diagram that is a map of couloumb resonances in 2 dimensions. When no mutual capacitive coupling is present between the dots the stability diagram would just look like the one in Fig.4.b) where the lines indicate a coulomb resonance and the space in between coulomb blockade for a specific charge occupation. If we where to turn on the capacitance to a finite level, the dots will couple capacitively to each other and the reservoirs. In our more real situation the left dot would have more horizontal charging lines as it would couple less to the sensor dot since it is further away. And the Transition (0,1), (0,2) and so forth, would be very faint or entirely missing since the right dot has no hole to give the left dot. We furthermore assume that the charge carriers can tunnel between the dot because of final tunnel coupling which can be modelled by a resistor in parallel with a capacitance.

At zero bias, transport only occurs when both islands are simultaneously on resonance with each other and the leads i.e. when the chemical potentials are equal. This situation occurs at so called 'triple' points, two of which are highlighted in the purple circle. The tunneling coupling between the two quantum dots can furthermore be controlled by the tunneling barrier between indicated as t_M, t_S and t_D. The higher the tunneling elements are the larger the anti-crossing will be at the triple points.

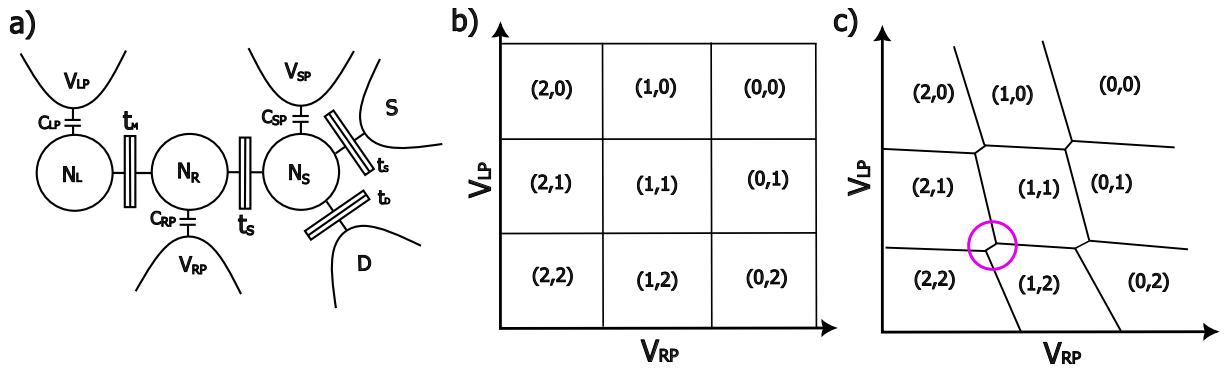

Figure 4: a) Model of our double dot and sensor dot as it is it would look for our real device. **b)** Charge stability diagram for no mutual coupling between the two quantum dots as a function of V_{RP} and V_{RP} in chargesensing. **c)** Charge stability diagram for a finite capacitive coupling as a function of V_{RP} and V_{RP} in charge sensing.

2.3 A brief primer on superconductivity

Before delving into the device measurements we will introduce a brief primer on superconductivity. Superconductivity is a phenomenon that arises when a material crosses a phase transition upon reaching a certain temperature criteria called the critical temperature (T_c). This phenomena was explained by the celebrated Bardeen–Cooper–Schrieffer theory of microscopic superconductivity (BCS). BCS theory states that below the critical temperature of certain materials, a weak fermion-phonon coupling makes it energetically favorable for the fermionic particles with same but opposite momentum (**k**,-**k**) and opposite spin ($\uparrow,\downarrow$) to bunch up in bosonic pairs (Cooper pairs) forming a collective bosonic condensate. A material that has undergone this phase transition exhibits remarkable properties such as zero resistance and perfect diamagnetism. This condensate can be described with a collective wave function corresponding to

$$\Psi = \sqrt{n_s} e^{i\phi}, \tag{2.31}$$

where n_s is the density of Cooper pairs and ϕ is the superconducting phase. The condensate can thus be describes by only two parameters. So ideally all the Cooper pairs have the exact same wavefunction, and are thus coherently connected with the exactly same phase. Reality is however slightly different, as this collective phase coherence can break down over a certain distance. The length scale on which a cooper pair stays phase coherent is called the superconducting coherence length ξ_0. This length is important for our experiment as the superconducting coupler

we will introduce very soon has to have a length smaller than ξ_0. ξ_0 corresponds to

$$\xi_0 = \frac{\hbar v_f}{\pi \Delta}, \tag{2.32}$$

where v_f is the fermi velocity, Δ is an energy which we will explain below. The Cooper pair condensate is energetically separated from single quasiparticle excitation by a superconducting energy gap of size 2Δ. quasiparticles being the broken cooper pairs differing from 'ordinary' metal quasiparticles by having an associated property of being electron like or hole like [37]. This means that in order to break up a Cooper pair, a minimum energy of 2Δ is required. Where as Δ at $T \to 0$ in the BCS model is described as[2].

$$\Delta(T = 0) = 1.764 k_b T_c, \tag{2.33}$$

where k_b is the Boltzmann constant. The superconducting phase can furthermore break down at a critical magnetic field H_C. Given by

$$H_c(T) \approx Hc(T = 0)\left[1 - \left(\frac{T}{T_c}\right)^2\right]. \tag{2.34}$$

Furthermore superconductors can be separated into two classes type-1 and type-2. Type-1 superconductors expel all magnetic flux lines until superconductivity breaks down at a field value H_c and type-2 have a continuous transition starting from a finite field value H_{c1}, where only a few magnetic flux quanta, $\Phi_0 = \frac{h}{2e}$ penetrate the superconductor, leading to kink in the phase transition. Until the amount of penetrating fluxes become to many and fully break down the superconductivity at a finite field H_{c2}. However type-1 superconductors can also have magnetic flux penetration if their thickness, in the direction of applied field is sufficiently small, shorter than the penetration length lambda given by

$$\lambda_L = \frac{mc^2}{4\pi n_s e^2}, \tag{2.35}$$

where m is the effective mass of the fermionic particles in the superconductor. We will from now on be treating PtSiGe as a classic BCS s-wave superconductor for all transport intents and purposes. As whether our PtSiGe superconductor is a type-1 or type-2 superconductor in reality we do not yet know.

[2]This is a very simplified model, to solve it exactly one would have to use numerical methods and several corrections to the formula.

2.3.1 Andreev reflections

As we in this thesis are working with a heterostructure semiconductor which is interfaced with a superconductor, it is worth looking at what happens when a superconductor interface meets a normal interface. When an electron (hole) from the normal region with an energy close to the fermi energy of the superconductor hits the interface, it can either normal reflect back into the normal region, or it can Andreev reflect as seen in to the left in Fig.5. An Andreev reflection occurs as the incoming electron (hole) gets reflected as a hole (electron) with equal but opposite momentum and spin. This effectively transfers two electrons into the superconductor, in form of a Cooper pair. Likewise a hole (electron) can be Andreev reflected as an electron (hole), thus effectively transferring two electrons (holes) from the superconductor into the normal region. This electron hole pair in the normal region remains phase correlated and the phase is kept within some characteristic length ξ_N of the interface. where ξ_N is called the normal coherence length and indicates how far into the normal region coherent processes can occur, or how far into the normal region the superconducting order parameter leaks in as seen in Fig.5 to the right. The normal coherence length is approximately given by [26]

$$\xi_N \approx l_e e^{k_f l_e/2} \tag{2.36}$$

Where l_e is the mean free path of the charge carriers , and k_F is the fermi wave vector - both in the normal region. Important for this thesis is knowing that the Andreev reflections can lead to sub superconducting gap states, and that Andreev reflections are coherent processes. As one of the experiments proposed can use andreev processes for mediating the coupling of the superconductor, and if we are to do so, we need ξ_N to be bigger than any super-normal junction length.

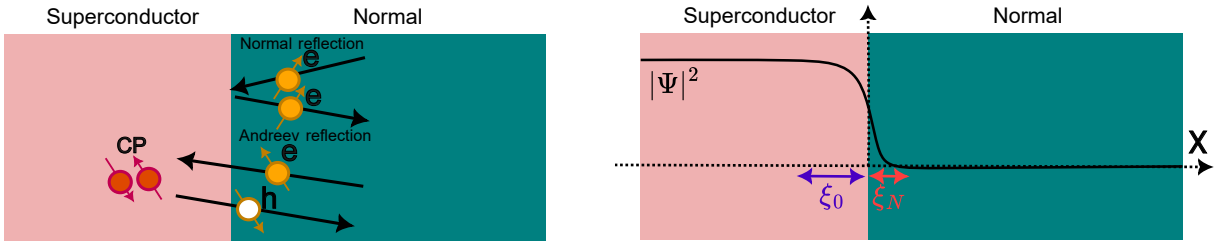

Figure 5: Left figure portrays a normal reflection and an Andreev reflection process, an electron (hole) gets injected and a hole (electron) get sent out creating a Cooper pair in the super region. The right figure is a cartoon depiction of the expectation value of the superconducting wavefunction decohering in the superconductor and in the normal region over a length ξ_N+ξ_0.

2.3.2 SNS junctions

Superconductors are sometimes presented as energy vs the density of states (DOS) plots, in a so called semiconductor picture, where the Fermi level is denoted μ indicating the energy of the superconducting condensate. Around Fermi level there is a zero single particle density of states region spanning an energy from $-\Delta$ to $+\Delta$, referred to as the superconducting gap. The energy of this gap is 2Δ. Beyond this gap we have single particle states, which are not allowed in the gap. All tunneling processes in this picture occur horizontally at a constant energy. One can now place normal metal reservoirs in adjacency as well as superconductors in adjacency to each other. By applying a bias voltage corresponding to some energy eV, we can displace the chemical potential of a superconductor and use this picture to explain the processes that would occur. This picture is particularly useful for experimentalists as it can be retrieved experimentally by measuring the differential conductance, which is directly proportional to the DOS [38]. Thus giving us a tool to translate the phenomena we see in our measurements directly.

In Fig.6 we see two superconductors facing each other with a normal region in between. For eV=0 i.e. the chemical potentials being aligned, we allow for a supercurrent to flow across the system as seen to the left in Fig.6. If we are to align the two quasiparticle peaks then a quasiparticle current is allowed to run which is the situation on the right in Fig.6.

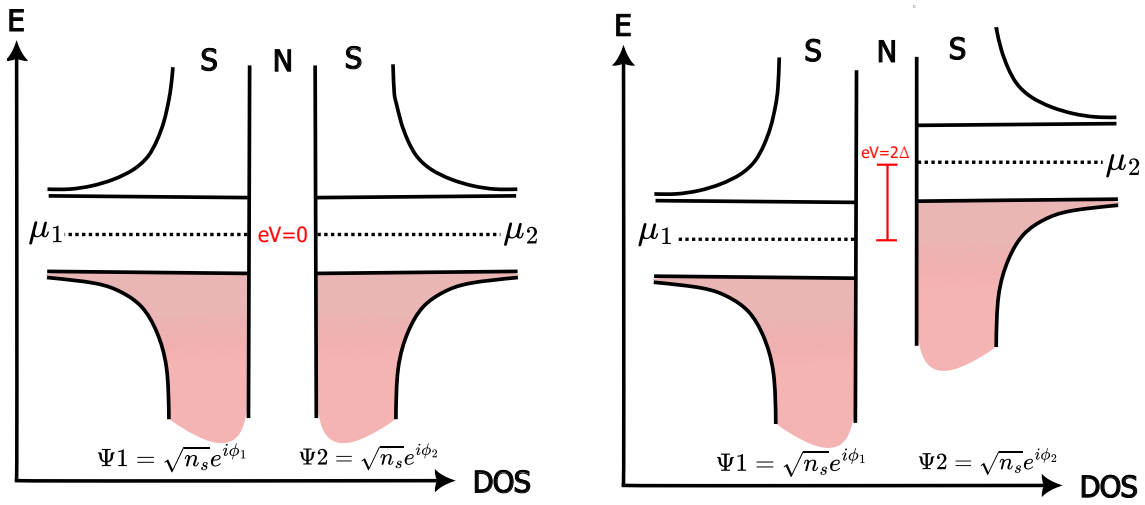

Figure 6: Energy vs density of states for 2 superconductors separated by a normal region. In the left plot the two superconductors align, only allowing Cooper pair transport at zero energy. In the right plot the right superconductors quasiparticle continuum is aligned with the empty quasiparticle continuum of the left superconductor. Allowing a single electron (hole) current to run. This is represented in SNS bias spectroscopy measurements as a superconducting gap that has $\pm 2\Delta$ quasiparticle peaks.

2.3.3 Multiple Andreev reflections

Proceeding with a system of two superconductors facing each other with a semiconductor in between. In a system like this one can measure conductance peaks within the 2Δ superconducting gap, which initially is not allowed. This phenomena can however happen when a quasi-particle from one of the superconductors traverses coherently through the semiconductor normal region as an electron (hole), and the electron (hole) then Andreev-reflects around a subgap state of the opposing superconductor sending out a hole (electron). This reflection process can in the matter of fact happen multiple times, each time transferring a charge of 2e, while accumulating energy until the electron (hole) gains enough energy to escape into the quasiparticle continuum of either of the superconductors. This phenomena is known as multiple Andreev reflections (MARs) [39]. These reflections have a higher probability of happening when the energy of the quasiparticle peak sending out the particle and the quasiparticle peak receiving the particle are commensurate eV with the energy gained at each reflection. Simply meaning that when you match the bias eV with fractions of the gap - a resonance occurs. MAR reflections are thus seen as conductance peaks inside 2Δ gap and the 'order' of the MAR depends on how many times it bounces from superconductor to superconductor. Given by,

$$N_{MARs} = \frac{2\Delta}{eV}. \tag{2.37}$$

where N_{MARs} is the order number and eV is the voltage bias across the junction. Thus the closer the two superconductors are in chemical potential the more reflections a particle will undergo. The probability of a MAR transmission scales as,

$$P_{MAR} = \tau^{N_{MAR}}. \tag{2.38}$$

Where τ is the transparency of the junction and can be from 0 to 1. Thus if the junction is not fully transparent i.e. below 1, higher order MARs will have lower conductance peaks even though more charges travels through the junction [40, 39, 41].

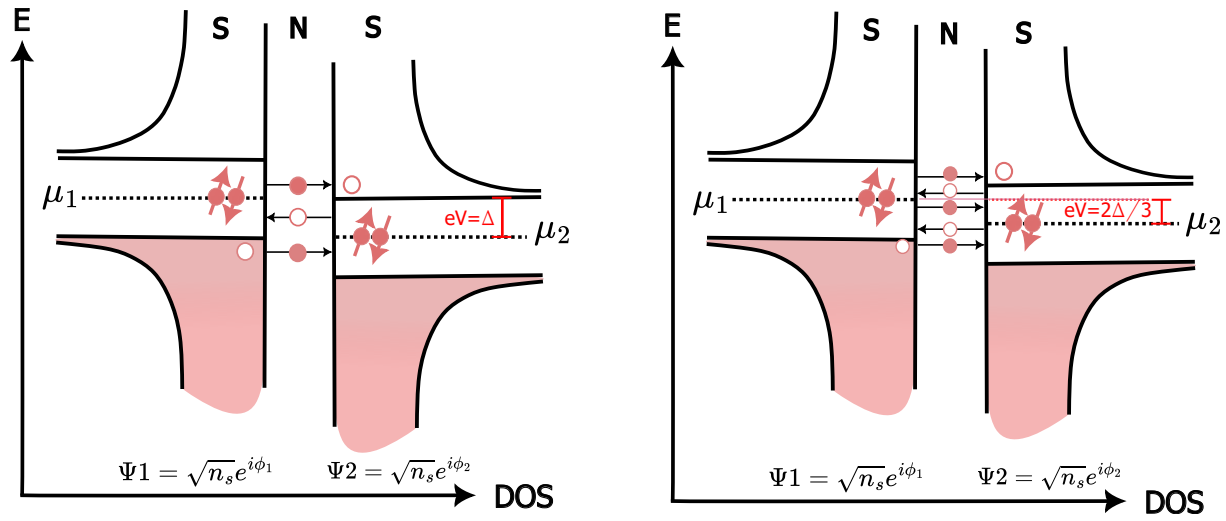

Figure 7: Semiconductor picture of two superconductors facing each other with a normal region in between. Left figure depicts a $N_{MARs} = 2$ order process at $eV = \Delta$, where in an electron from the left superconductor gets reflected as a hole on the second superconductor before entering the quasiparticle continuum in the left superconductor again. Right figure depicts a $N_{MARs} = 3$ order process at $eV = 2\Delta/3$, where in an the reflection process happens three times before getting enough energy to enter the quasiparticle continuum.

2.4 Coupling spin qubits with superconductors pt.2

With the theory presented above we can now safely introduce the "simplest" form of coupling two quantum dots via a superconductor [1] The proposal can however be extended to coupling multiple quantum dots as well as two singlet-triplet qubits over distance, which is enabled by the same principles we now will introduce. Nonetheless, We will now consider two quantum dots, and two charge carriers with each their own spin. We will address this system as two qubits. The two qubits have spin states
$\{|\uparrow\uparrow\rangle, |\downarrow\downarrow\rangle, \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle + |\uparrow\downarrow\rangle)\}$ which are the triplet states T_+, T_-, T_0, and $\{\frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\uparrow\downarrow\rangle)\}$ called the singlet S. Appying a magnetic field in e.g. the z direction splits the energies due to Zeeman splitting and due to small g-factor variations in the dots we get an energy difference ΔB_z [42, 16] between $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ as seen in in the energy diagram in Fig.8.a). The two states T_0 and S are shifted in energy due to the kinetic exchange interaction which is usually denoted by J Fig.8.a). The interaction comes from Virtual hopping between the two quantum dots Fig.8.c), which lowers the energy of the lowest spin singlet by J relative to the spin-triplet energy Fig.8.a). This energy shift is given by J$\sim t^2/U$ [43], where t is the tunneling amplitude as seen in Fig.8.d), and U the onsite coulomb repulsion energy as seen in Fig.8.a) and d).

Being able to tune J with how tunnel coupled the dots are now allows us to implement an operation where we can swap the spin positions on the quantums dots. Initially, J is switched OFF and the spins can for example be prepared in the $|\uparrow\downarrow\rangle$ state, by altering the detuning $\epsilon = \mu_R - \mu_L$ where, μ_R and μ_L are the chemical potentials of the right and left dot respectively - we can move the charge configuration to the to the black star in the energy diagram. When J is switched ON, the spins begin to rotate around J between $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ as seen in Fig.8.b), and if J is switched back OFF after half a rotation the spin states are swapped. We can thus implement specific two spin operations with timed barrier gate pulses.

In a double dot device, J can be tuned by the gate electrodes that alter the potential landscape and effectively control J by modulating the overlap between the qubit wavefunctions, that is by tuning the tunneling coupling. The constraint here is that J is only big when the interacting particles are in almost direct proximity to each other, and drops of fast as they are moved away from each other. We thus have to find some mechanism that works as though it was J but over a longer scale to realize our long range coupling links.

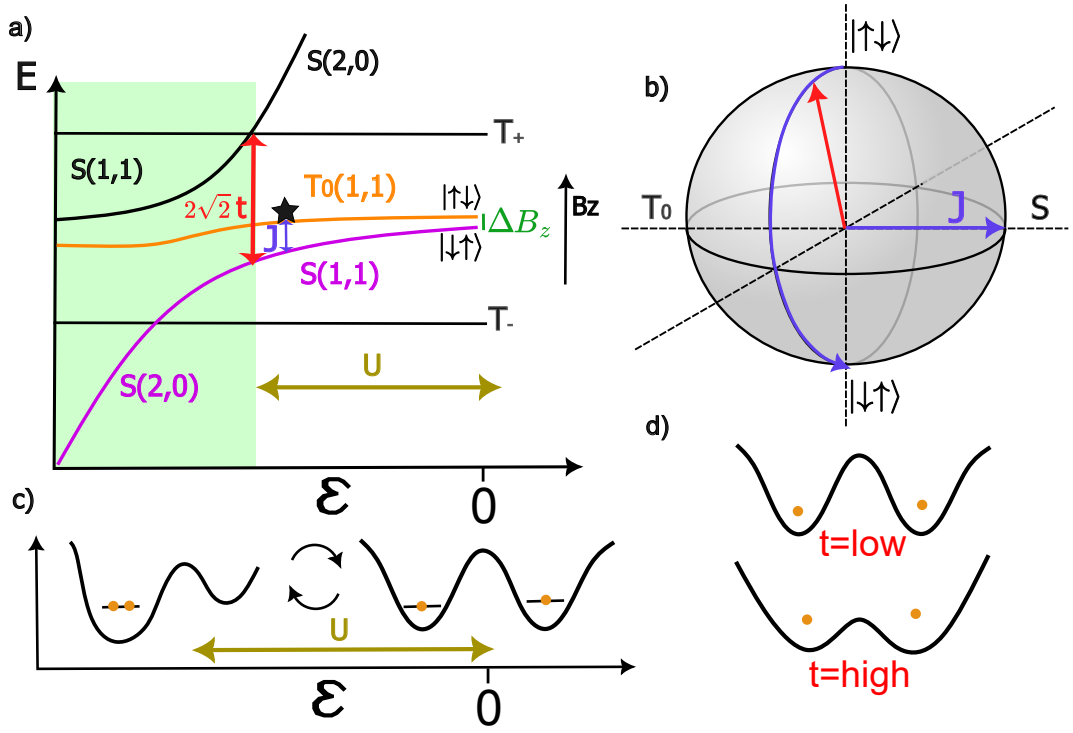

Figure 8: a) Energy diagram of two quantum dots next to each other with a finite tunnel coupling having energy on the y-axis and $\epsilon = \mu_R - \mu_L$ called the energy detuning on the x axis. $S(2,0)$ and $S(1,1)$ are the singlet states where (N_L, N_R) is the charge occupation. T_0 is the triplet state. ΔB_z is the field gradient level splitting in green. J is the exchange inter action energy splitting in blue. U is the value of detuning required to overcome Coulomb repulsion in a single quantum dot. Adapted from [44, 16] **b)** Cartoon of a Bloch sphere depicting the Bloch vector(red arrow) rotating from $|\uparrow\downarrow\rangle$ to $|\downarrow\uparrow\rangle$ due to J being ON. **c)** Depiction of the charge occupations when tunneling back and forth, where U is the classical Coloumb repulsion energy. **d)** Cartoon depicting the effect of tunnel coupling t at $\epsilon = 0$.

It is here, where we turn our attention to the proposal of using superconductors to couple spins as sketched in Fig. 9.a) and b). Two quantum dots QD1 and QD2 are connected to both sides of an elongated superconductor via tunable tunneling junctions with tunneling rates t_1 and t_2 Fig. 9.a) and b). The tunneling junctions are in experiment realized by gate electrodes. The chemical potential in the superconductor (μ_{SC}) can be controlled by side gates or top gates which in Fig. 9.a) and b) are called $V_{\mu SC}$. In such a device, the exchange interaction is replaced by a general energy shift δE between the singlet and triplet states of the quantum dot spins. There are two specific mechanisms that allow for such an energy shift, namely the crossed Andreev reflection (CAR) sketched in Fig. 9.a) and elastic co-tunneling (ECT) shown on the in Fig. 9.b).

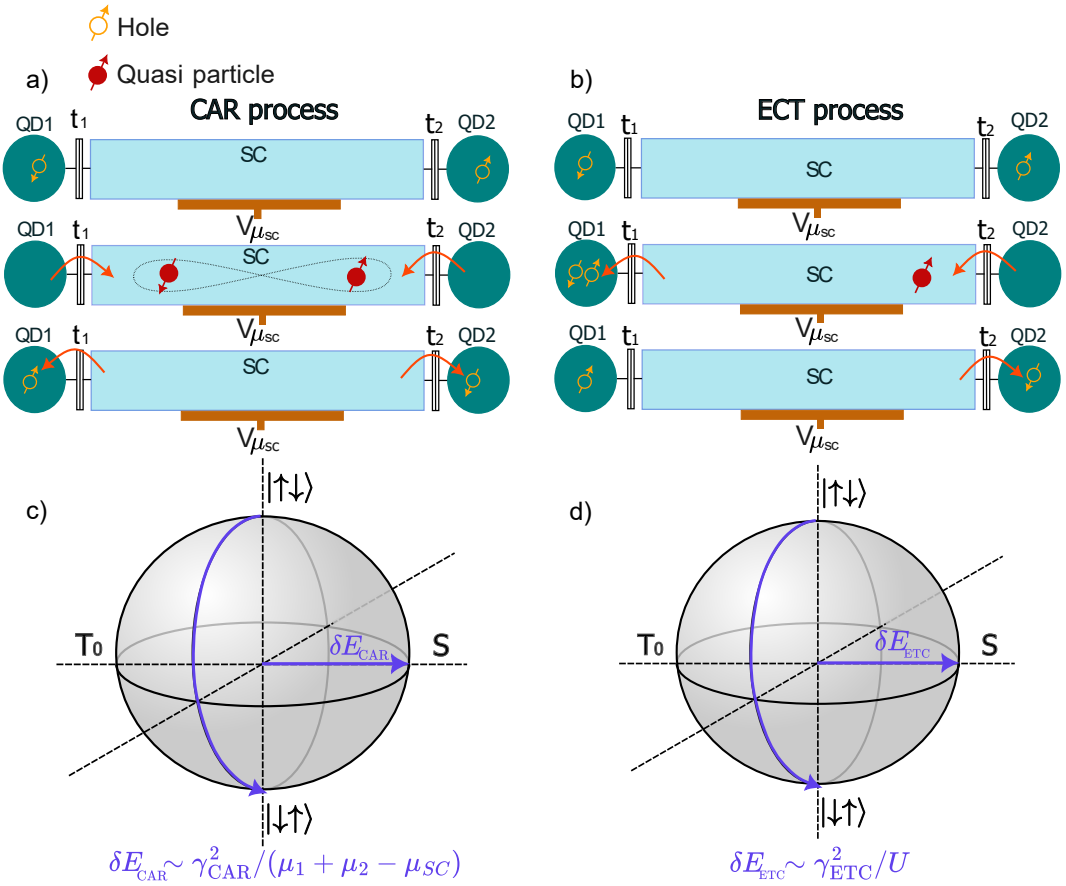

Figure 9: a) CAR process - Two holes with opposite spins enter and form a cooper pair, and exit to their respective dots again. **b)** ECT process, a single dot enters the SC and into the next dot via the super conductor, and tunnels all the way back again. **c)** Cartoon of a Bloch sphere depicting the bloch vector (red arrow) rotating from $|\uparrow\downarrow\rangle$ to $|\downarrow\uparrow\rangle$ due to δE_{CAR}, **d)** Cartoon of a Bloch sphere depicting the Bloch vector (red arrow) rotating from $|\uparrow\downarrow\rangle$ to $|\downarrow\uparrow\rangle$ due to δE_{ETC}

In both cases, each dot initially contains one spin. In the ECT process, the spin on QD2 tunnels to QD2 via the superconductor by underway occupying states in the superconductor over the superconducting gap Δ (or Andreev bound states if present). The rate of this happening, is given by the ECT amplitude γ_{ECT} which depends on t_1, t_2, and that Δ is small compared to the quantum dot energies μ_1 and μ_2. Just as in a standard tunnel process discussed above the energy of the singlet spin configuration will then be shifted by $\delta E_{ECT} \sim \gamma^2_{ETC}/U$ instead of the J, as the spin on the right tunnels back and forth.

In the CAR process, the two quantum dot spins can only jump into the superconductor via t_1 and t_2 and form a cooper pair if they from a spin singlet. The rate of this happening, i.e. the CAR amplitude γ_{CAR}, again depends on the tunnel rates $\gamma \sim t_1 t_2$ and decays as $e^{(-l/\xi_0)}$ [1] in a superconducting coupler which is confined in 1D with lenght l, where ξ_0 is the superconducting

coherence length. As long as $l < \xi_0$ the CAR process can couple spins over over the distance In the superconductor the energy of the cooper pair directly depends on the chemical potential μ_{SC}. So as the cooper pair is split again in the reverse CAR process, the singlet energy is in total shifted by $\delta E_{CAR} \sim \gamma^2_{\text{CAR}}/(\mu_R + \mu_L - U)$ [1], where μ_R and μ_L again are the quantum dot onsite energies i.e. chemical potentials.

In summary, if we can the tune t_1, t_2, and μ_{SC} to switch δE_a ON and OFF and engineer controlled swap gates [11] over a distance l smaller than the coherence length of our superconductor. Thus for realizing this kind of experiment we need to be able to fabricate and control nano scale superconductors in compatibility with Ge/SiGe as well as being able to create and control single hole occupied quantum dots. This entails being able to control the energy levels of the quantum dots, the chemical potential of the super conductor, and the tunneling coupling between the quantum dots and the superconductor. We also need a way to read out the spin states, this can be done with spin to charge conversion, which is a scheme that utilizes a helper dot initialized in a certain spin state to block or allow tunneling depending on its neighbours spin state, helper dot seen in Fig.10 as STC .

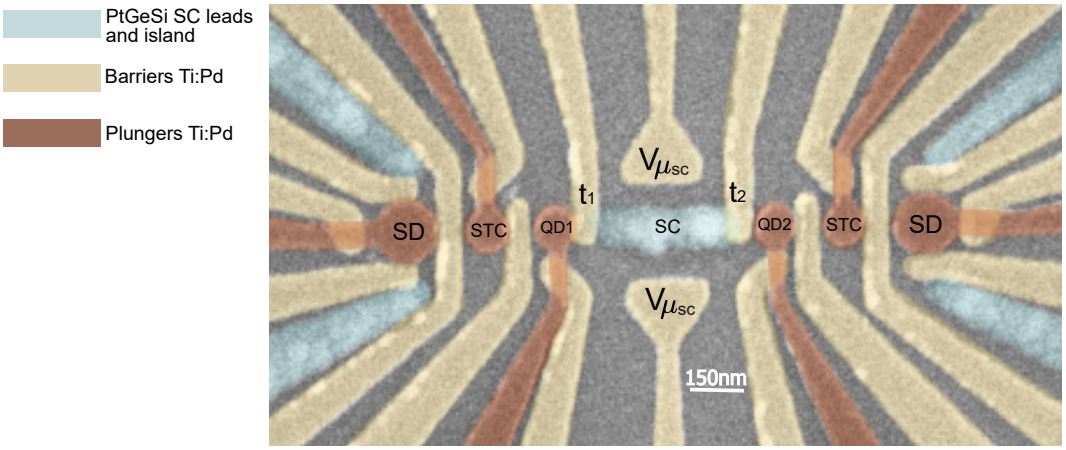

Figure 10: a) SEM micrograph of the actual device we wish to realize this experiment in. The Light blue being PtSiGe superconductor. Yellow denotes barrier gates and the red denotes plunger gates.

The false colour SEM in Fig.10 is the first generation of devices fabricated for realizing this experiment. The blue being PtSiGe superconductor, with the island in the middle being the mediating superconductor. The yellow denotes barrier gates for controlling the barrier potentials and couplings T_1, and t_2. The red gates being plunger gates for controlling the quantum dot onsite chemical potentials. The dots denoted STC are for read out with spin to charge conversion, while dots denoted SD are sensor dots, intended for charge sensing of the charge occupation of

the STC dots.

3 Fabrication and experimental setup

In the following chapter we will outline and describe the fabrication process, from CAD design to final device, the experimental setup as well as the equipment used to measure the device. We will furthermore present the pitfalls of fabricating with shallow Ge/SiGe and PtSiGe superconductors and especially how we solved these issues.

3.1 Design and process

The first step of every fabrication process is to make the design, this is done using AutoCAD2023 software.
This is a computer assisted design program (CAD) which allows us to draw and design our devices to scale and export them to the various files that the software of various fabrication tools can process. Design choices of size and geometry are made on background of literature, theory and previous experiments all incooporated in a feedback loop. In Fig.11.a) we see the CAD drawing of the first generation of devices that was fabricated at the cleanroom facilities of the Niels bohr institute. Besides it in Fig.11.b) is seen a false colour SEM micrograph of the finished device with all the finished layers present.
The heterostructure material arrives in either wafers or pre-cut bigger chips usually called 'coupons', which needs to be diced into smaller sample holder friendly pieces. The whole fabrication process entails several minor steps outlined in the Appendix.A. The crucial steps in the multilayer process of these devices are listed as the following in the order of which they are done

- Platinum alignment markers 5 nm Ti and 40 nm Pt
- Platinum Ohmics and super conductors - Hydroflouric acid dip - 15 nm Pt - Annealing (Light blue)
- SiliconOxide bonding protectors - SiO_2 100 nm. (optional)
- 1st Atomic layer deposition of Alumina 5-8 nm (Green)
- Palladium barrier gates - 5 nm Ti and 20 nm Pd (Yellow)
- 2nd Atomic layer deposition - Alumina 5-8nm (Brown)
- Palladium plunger gates - 5 nm Ti and 25 nm Pd (Orange)
- Bonding protectors - Alumina Etch followed by Ti/Au/Ti/Al Bonding protectors

Markers, ohmics, gates and plungers are done using electron beam lithography followed by a metalization step using electron beam evaporation. The Aluminuium oxide (Alumina) dielectric is deposited using atomic layer deposition. Both types of bonding protectors are done using either EBL or optical lithography followed by e-beam metalization.

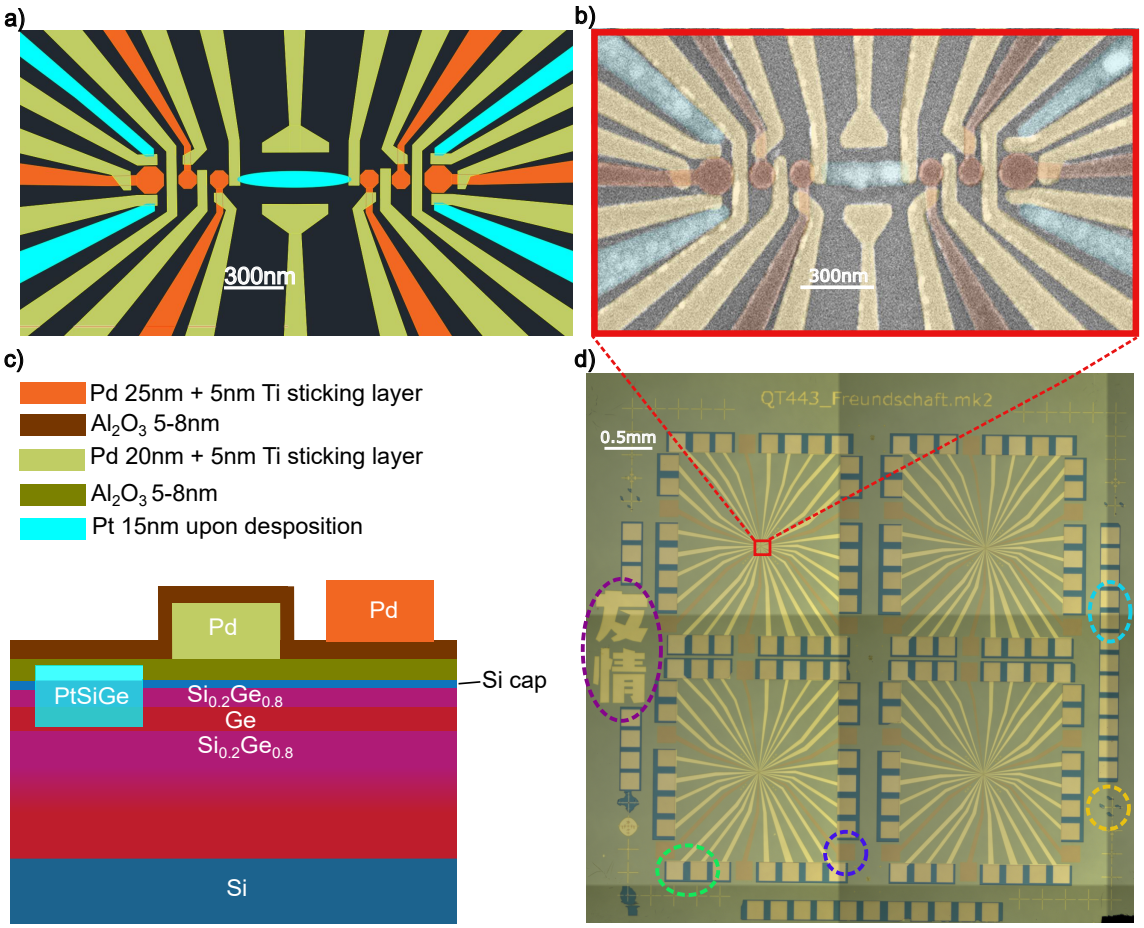

Figure 11: a) AutoCAD illustration picturing a device, the colours illustrative different layers in the EBL process. **b)** False colour SEM micrograph of a finished device using the AutoCAD design in a). **c)** Layer stack of the device in b), notice it does not include the final Ti/Al/Ti/Al bonding protectors as they were added later. **d)** Optical microscope image of a finished chip with 4 full devices. The SEM micrograph resides in the center of the red square. The japanese symbol in the purple circle is an optical indicator, being big enough to see without a microscope. Such that one can align the chip correctly in the various tools. In the green circle we have the bonding pads from a barrier layer, and a plunger gate layer, the blue underneath is the SiO_2 bonding protector. Within the blue circle there is an ohmic bonding pad. In the teal circle wirebonding practice pads are seen, placed in order to calibrate the wirebonder before bonding on the real device. In the orange circle a global alignment marker is seen.

3.1.1 E-beam Lithography

The main workhorse in the fabrication of these devices is the electron beam lithography tool (Elionix 125kV). The EBL tool lets us ”draw” our intricate design on the nanometer scale by collimating an electron beam with magnetic coils into a very small point. This beam is then used to weaken a polymer into the pattern extracted from the design we made using our CAD tool. The polymer is referred to as a resist. Different resists have different properties, some are resilient against etchants and some create different exposure profiles. The weakened polymer is washed away using the appropriate chemicals, this step is called development. The exposed design is revealed as a gap or a missing resist, and then used as a stencil, depositing our metals on top (metalization). Finally removing the remaining resist leaving our designed pattern in our chosen metal, this final step is called lift-off. The entire process is seen in Fig.12.a), b), c), and d). Many preparations go into EBL testing in order to get the designed patterns, such as which current to use, what beam size, which resist, what resist thickness and most importantly what dose. The dose is the amount of energy that is deposited pr.unit area usually given in micro coloumb pr. cm^2 - if too low the resist will not be removed, if too high the resis may over expose and cause enlarged or blurred features.

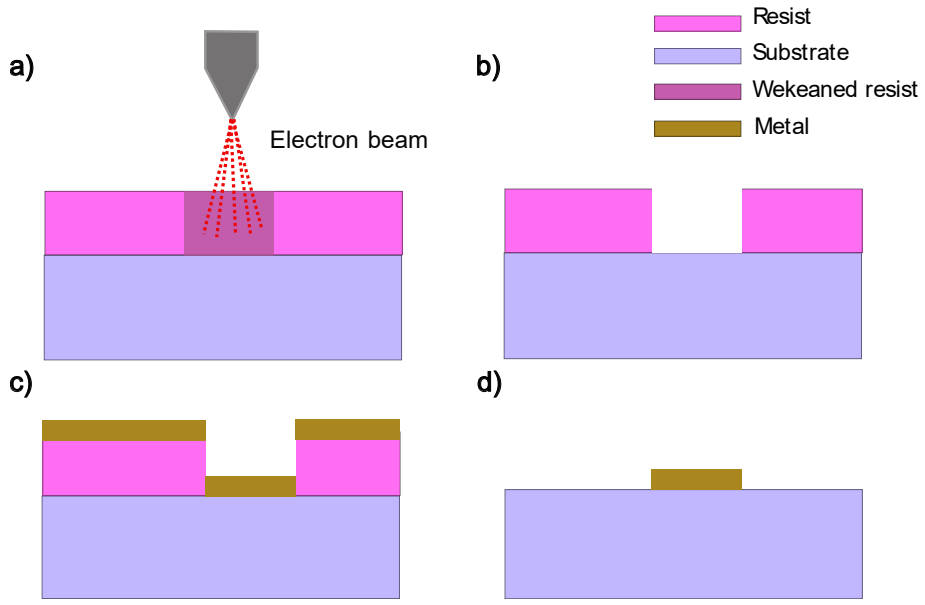

Figure 12: Electron beam lithography **a)** First step the resist is weakened in the pattern of of your design. **b)** In the Second step the weakened resist is removed by a chemical developer matching the resist used. **c)** A deposition material is chosen and deposited, filling the developed gap. **d)** Finally the remaining resist is removed with product specified specified chemicals - usually Acetone, Dioxolane or NMP

3.1.2 Electron beam evaporation

A total of 6 lithography steps are needed to realize the multilayer devices presented in this thesis. After each lithography step a metal or SiO_2 layer is deposited as seen in Fig.12.c) using an electron beam evaporator of the brand AJA. The concept of this type of process is using an electron beam with some set power to heat and thus evaporate various materials situated inside a crucible onto the sample in a very high vacuum environment - cartoon drawing of this can be seen in Fig.13.a). The AJA withholds a range of materials with different evaporation point. The materials evaporated in this thesis count, Palladium for the barrier gates and plunger gates. Aluminium, Gold and Titanium for top portion of the wirebond protecters. SiO_2 for the bottom part of the bonding protectors was evaporated with a very low evaporation current of $\sim 12.5\,mA$, and a maximally broadened electron beam. Platinum for the ohmics and superconducting structures, platinum was a particularly hard process as it needs a very high evaporation current of $\sim 130\,mA$. The high current generates a lot of radiation heat, which can heat the sample and sample holder significantly and cause damage and issues for the resist, which we will get back to. However a trick we came up with to alleviate some the radiation heat was to cover the sample holder in Aluminium foil as seen in Fig.13.b).

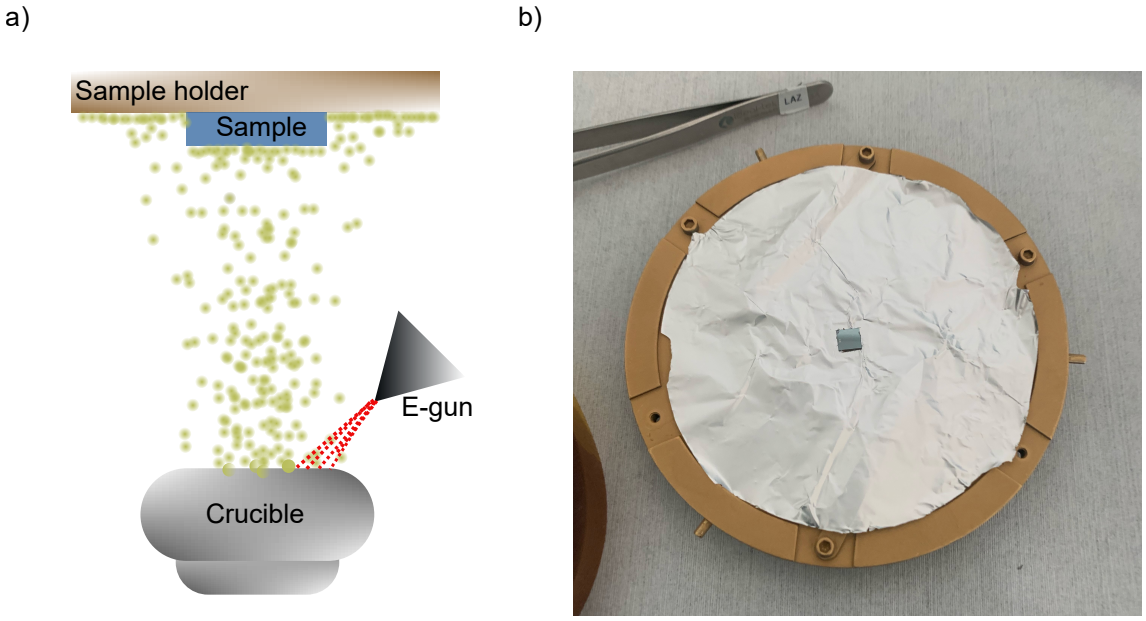

Figure 13: a) Cartoon illustration of the metal evaporation process. **b)** Sample holder wrapped in Aluminium foil to reflect excessive heating from the Platinum. Sample chip located in the middle.

3.1.3 Atomic layer deposition

As formerly mentioned our ohmic and gate layers are separated by a dielectric. While seemingly a very simple step, it is one of the most important steps of the fabrication for these types of multilayer devices.
A good dielectric allows us to separate the layers without electrically shorting them to each other and any flaws in the dielectric might ruin the device functionality. For this we have chosen Alumina (Al_2O_3) due to its dielectric constant $\kappa = 9.3$ being low enough to permeate electric fields through and into our device from the gate electrodes while having a relatively high breakdown voltage of 4-5V at the very thin films we are working with.
The Alumina is deposited globally on the chip with atomic layer deposition (ALD). ALD is a thin-film deposition technique which uses gas-phase reactants called precursors. Within the chamber the precursors are let in sequentially, slowly forming an extremely uniform dielectric, (atomic)layer by (atomic)layer. For Alumina ALD we use the precursor gas trimethylaluminium ($Al(CH_3)_3$) and simple H_2O vapor [45]. ALD deposition was done by first pre-baking an empty chamber at a high temperature. Then followed by a chamber conditioning round, which essentially means that we run a few layers of Alumina in the empty ALD chamber, to trap eventual contamination and condition the chamber before loading our sample. When the sample is loaded, we pump the chamber between 6 to 10 hours before depositing either 70, 80 or 90, cycles of Alumina at $250\,C^\circ$ in the chamber. Upon loading the sample we also load a witness chip, which is then used to measure the Alumina thickness, the thickness is measured with a digital ellipsometer at various angles which yielded measurements of roughly $5.5 \pm 0.5\,nm$ for 70 cycles, $6.5 \pm 0.5\,nm$ for 80 cycles, and $7.5 \pm 0.5\,nm$ for 90 cycles

3.1.4 Alignment markers

Every multi layer device starts with alignment markers. Alignment markers are used to consistently align your device patterns betwixt the various e-beam lithography steps. Choosing the correct material for the best markers is critical for achieving the best contrast during the marker alignment procedure in the exposure tool, and thus also the most precise alignment. Au (Gold) is commonly used because of its high atomic mass and hence high SEM contrast [46]. We however opted for 40 nm of Pt on top of a 10 nm Ti sticking layer. This choice was based on the fact that we have to anneal the ohmic contacts and superconducting structures of our devices at a temperature of 400 C° for 15 min. While the bulk melting temperature of Au may be 1064 C°, it would unfortunately deform and contract into globules upon 400 C° annealing at the micron length scales of our marker features. Pt has a considerably higher melting point of 1678 C°; and is also able to retain its shape during the annealing process.

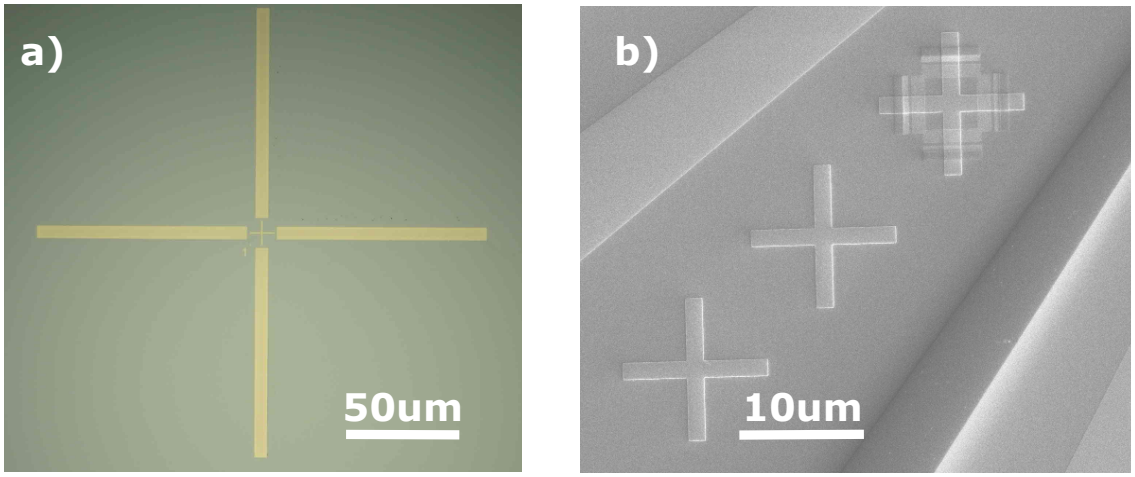

Figure 14: a) Optical photo of a global marker. The number under the left arm indicates which corner of the chip we are located at. **b)** Local marker surrounded by device gate fan-out. The patterns on the top marker indicate that it previously has been registered.

Two types of markers reside on the chip, one being the bigger global marker for initial alignment as in Fig.14.a) - located in the corners of the chip several mm from the active device region. The other being local markers as in Fig.14.b), located about 120 μm from the critical part of the device. The local markers are a crucial feature if one wishes to have sub 10 nm precision for alignment.

3.2 Superconducting PtGeSi leads and islands

The first step after alignment marks is the superconducting silicide PtGeSi leads and superconducting structures. The PtGeSi used in this thesis is made by diffusing a thin layer of Pt down into the Ge quantum well; resulting in a superconducting amalagamation of Pt, Si and Germanium with a critical temperature $T_c \approx 0.5\,K$ [27, 2].
The leads act as charge reservoirs and they extend all the way from the $200\,\mu m\ x\ 100\,\mu m$ bonding pads and directly into the nanoscale features of the device reaching 35-50 nm sizes. Whilst the superconducting island structures reside at the very center of the device spanning sizes between $100\,nm\ x\ 50\,nm$ to $450\,nm\ x\ 50\,nm$ as seen in Fig.11.a) and b).

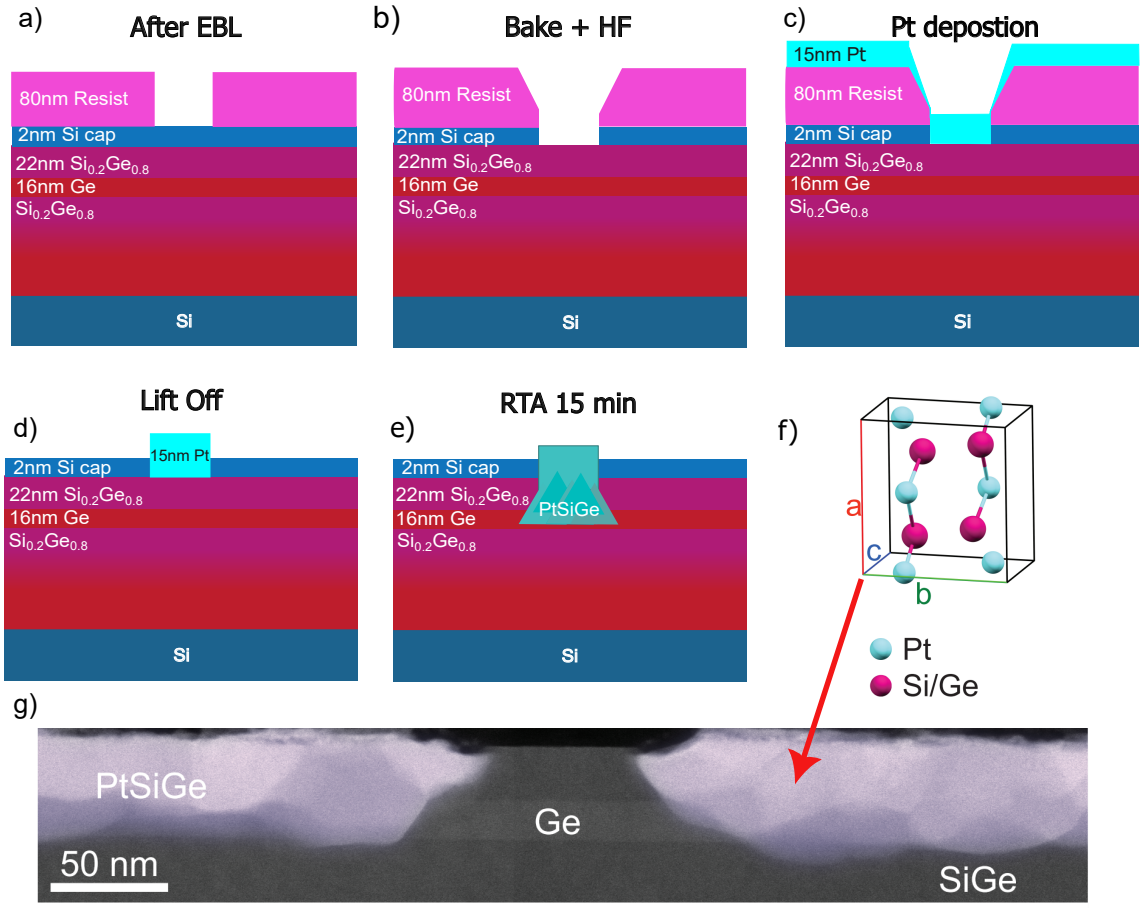

Figure 15: PtSiGe annealing process - not to scale. **a)** Heteretructure after EBL. **b)** Heterostructure post baking and HF dipping. Resist walls get deformed due to baking. If baking is excessive lift off will be compromised. **c)** E-beam evaporation of 15 nm Platinum. **d)** Lift off in Dioxolane. **d)** Annealing in pure Argon athmosphere for 15 min at 400C° causing defusion into Si/Ge. **f)** Crystal structure of PtSiGe as presented by A.Tosato et.Al in [2]. **g)** False coloured cross sectional TEM of PtSiGe structure as presented A.Tosato et.Al in [2]

The process starts by spin coating PMMA (A2), an e-beam lithography resist of thickness 80 nm at 4000 RPM and 60 s spin time. This resist is known for being resilient against hydroflouric acid (HF), which is used to etch away the 1-2 nm SiO_2 passivisation cap of our Ge/SiGe substrate. After e-beam lithography the sample is treated with a 10 s Buffered HF dip, and immediately (with in 5 min) transferred to a metal evaporation system and put under vacuum before a native oxide can regrow. 15 nm of Platinum is deposited, and followed by a rapid thermal anneal of 400 C° in an Argon atmosphere.

3.2.1 HF failure modes

The failure modes of this specific process were very high, and it took a long time to get it to a point that that was somewhat reproducible.
For the first iteration of devices the resist CSAR4 was used followed by a buffered HF dip of 5 s. Most devices came out well, but with the HF leaving a big shadow due to creeping Fig.16.b), however once in a while we would see large structure peeling similar but not as severe as in Fig.16.c). We however suspected that the first generation of devices did not yield superconductivity (due to measurements shown in chapter 5.1.1). Thus we suspected that the etching time played a role in that.

To fix this we upped the etching time to 10 s, this caused heavy HF bleeding underneath the areas which were not exposed, causing massive resist peels as seen in Fig.16.e) and breakdown of resist walls causing unwanted fusing between nanostructures. To combat this effect a pre-bake step of the CSAR4 recommended time (1 min at 145 C°) was introduced to reflow the resist hopefully preventing the HF from creeping under. The pre-baking, along with the deposition of platinum which happens under very high temperatures caused sidewall problems, leaving unwanted pieces of Pt around the edges of the entire design making it a non ideal approach as seen in and Fig.16.d).

We then introduced extra complexity to the device in the form of two leads to be able to probe the center island independently. Which was when it became evident that CSAR4 simply could not sustain its integrity after the process. We switched the resist to PMMA2, which gave problems in the beginning due to oxygen ashing before the HF dip. It is usually common to clean the chip after the development step Fig.12.b) using an oxygen plasma ash, it was however discovered that doing so compromises the integrity of the resist when also exposing the sample to HF, leaving broken resist walls and again unwanted fusing. After some tinkering, we found a recipe that worked: Develop, no ash, 10 s HF dip, pre-baking for 20 s at 100 C°, this yielded the result

in Fig.16.i), the features came out as designed with no HF bleeding.

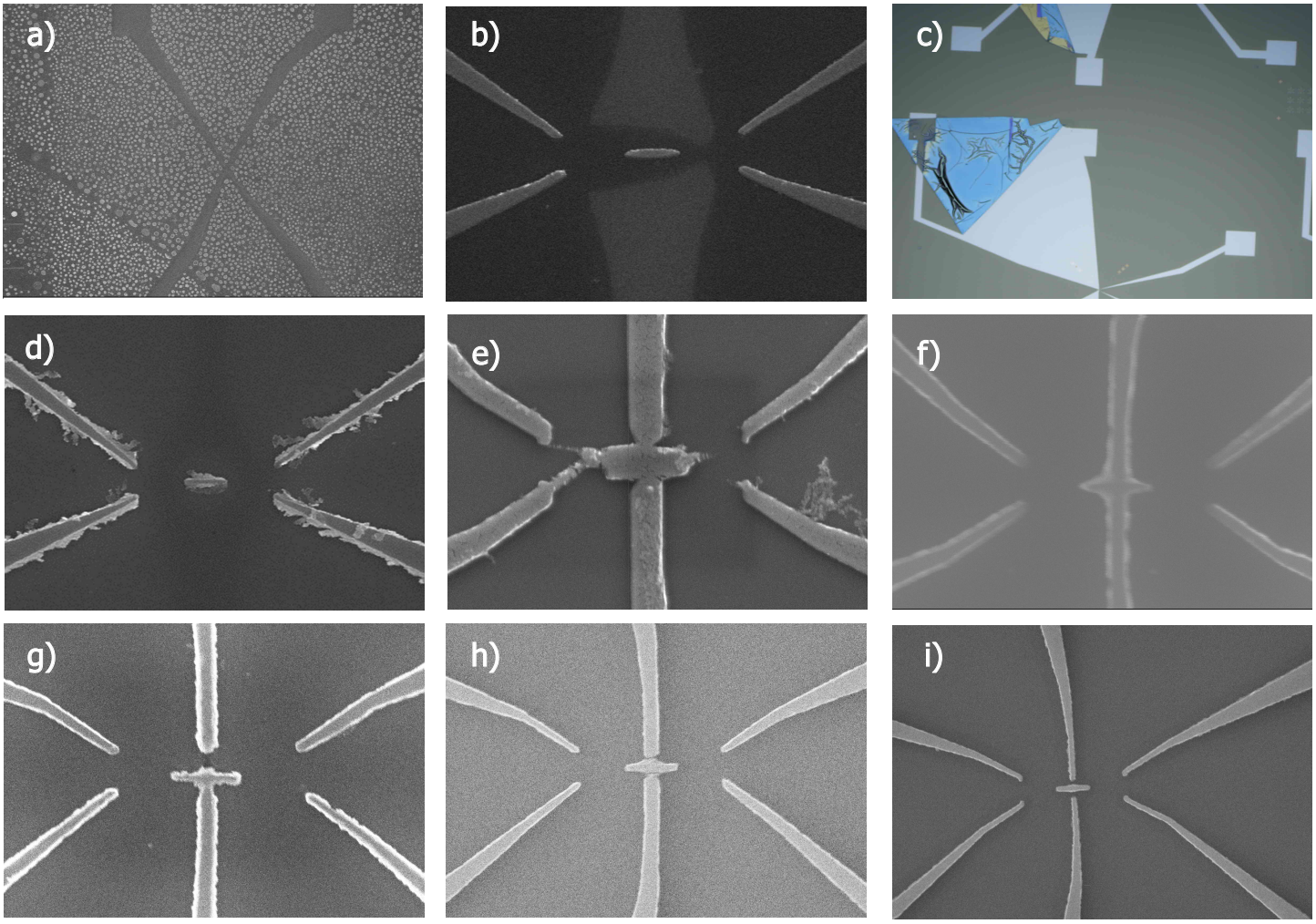

Figure 16: Failure modes of HF **a)** Too high HF concentration of 15%, usual buffered HF content is around 6%, resulting in a burned resist and ruined chip. **b)** CSAR4 - 30 s ash, and 20 s bake at 130 C°, HF through is present and seen as a shadow around the leads. **c)** Resist with no pre-bake, Causing the HF to bleed in under undeveloped structures ultimately peeling off the resist. **d)** CSAR4 - Baked at 130 C° for 120 s, 30 s ashing and 5 s HF dip. Resulted in Pt "hairs" due to the resist gap deforming and not lifting off properly. **e)** Adding more structure around the island in the middle - CSAR4 - 10 s HF dip, 30 s ashing, and bake for 20 s at 130 C° **f)** A2 - 10 s HF dip, 30 s ashing, no bake. **g)** A2 - 10 s HF dip, 30 s ashing, and bake for 60 s at 100 C°. **h)** A2 - 10 s HF dip, 30 s ashing, and bake for 10 s at 100 C° **i)** The optimal result - A2 - 10 s HF dip, no ashing, and bake for 20 s at 100 C°

3.2.2 Annealing

After the Platinum has successfully been deposited and lifted off, it will have to be annealed into the Ge/SiGe. The annealing of Pt into the heterostructure happens at 400 C°) in an a Argon atmosphere for 15 min. Upon optical inspection the devices done with CSAR4 and HF 5 s HF dip all had a dark grey colour which is seen in Fig.17.a), aswell as an extremely rough surface as seen in the darkfield optical image Fig.17.c).
The second generation of devices which all were done with PMMA2 and an HF dip of 10 s, annealed into a visibly lighter grey Fig.17.b), and had almost no visible surface roughness in dark field.

The devices HF dipped for 5 s we suspected of not showing superconducting properties, while the devices dipped for 10 s did. We assume that the Platinum does not fully integrate with Ge/SiGe when not etching long enough, thus retaining its properties as Platinum which does not superconduct on its own, but was still able to form ohmic contacts upon reaching the quantum well but not be superconducting.

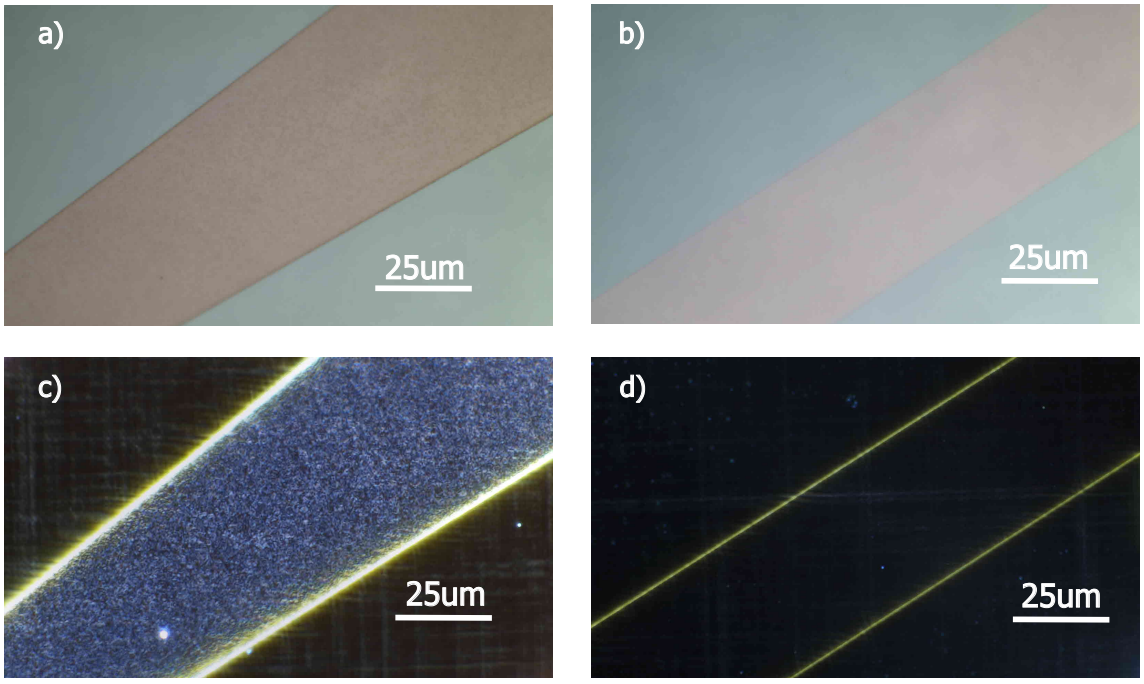

Figure 17: Optical comparisons of post annealing Pt. images were taken exactly the same time with same light settings. **a)** Optical image post annealing of Pt deposited on CSAR4 after 5 s HF dip. Measured devices showed no super conductivity. **b)** Optical image post annealing of Pt deposited on A2 after 10 s HF dip. Measured devices showed super conductivity.**c)** Dark field optical photograph of a) at 5 s image exposure time. **d)** Dark field photograph of b) at 5 s image exposure time.

3.2.3 Bonding buffers

Before any low temperature measurements are performed, the device must undergo wire bonding. Wire bonding is a process in which you connect the chip to a sample holder in the form of a printed circuit board (PCB), in order to probe the device electrically.
Wire bonding is a delicate process, in which a robotized arm brings down a fine thread of Aluminium onto a desired surface. The arm holds down the wire whilst stretching it with a set force, until an ultrasonic blast rubs the wire with the metal at the connection point - resulting in the wire and destination point fusing, due to the friction created.
This is now done from PCB to device-chip a multiplum of times, and while the aluminium thread may look small (25 μm in diameter), and movement of robotic arm smooth, the rubbing action at the chip's bonding pads carries enough power to press or break through several hundred nanometers of metal, insulating oxide and semiconductor.

Now imagine we apply a bias of a few μV over a source drain channel at base temperatures, no current would flow unless we accumulate charge with a gate electrode bridging semiconductor between the source and drain. Now further imagine the gate electrode being shorted to the conduction plane via the substrate by punching through the bonding pad. The instant you would accumulate charge underneath the gate electrode. The charges would travel up along the gate fan-out and straight to the gate's wirebond, due to the now massive potential drop from drain to gate electrode. Orders of magnitude larger than from source to drain. That is, hundreds of mV to V of potential being the normal operating ranges for gate electrodes contra the tens of μVs for source bias Fig.18.a). This will cause massive currents and unusable devices. The scenario is seen in Fig.18.b) and the usual current leakage in Fig.18.b) first measured with a positive bias (blue curve), and then a negative bias (orange curve) to determine that it is truly is leakage, if not the current would change sign. It is common that the accumulation voltage gets higher for each measurement hence the leakage starts later for the orange curve.

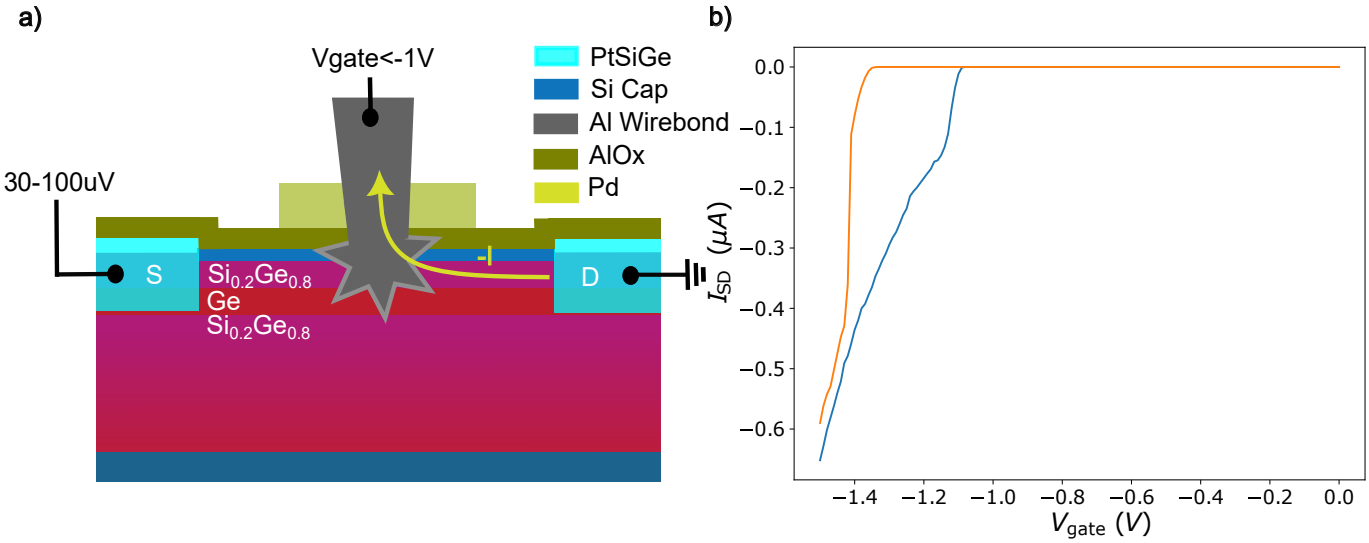

Figure 18: a) Cartoon illustration of how the gate electrode leakage occurs. **b)** Typical gate electrode leakage measurement, measuring current at the drain vs a gate. The blue curve was measured with a positive bias , the orange curve was measured with a negative bias. Measurements were taken right after each other.

Thus a strategy was needed to circumvent this problem. In the first attempt to solve this problem we etched trough the alumina at every bonding pad using aluminum echant Transene-D for 2 min at 53 $C°$, followed by a deposition of 300 nm Aluminium. The aluminium was however too soft and got got visibly destroyed upon wirebonding as see in Fig.19.a), again causing gate leakage. What in the end worked was etching the ALD away with Transene-D for 2 min at 53 $C°$ followed by a gate stack consisting of 50 nm Ti, 100 nm Au, 50 nm Ti and finally a layer of 100 nm Al. The idea being that Ti is a hard metal and will brace the impact from the wirebond through the soft Al, and if would break trough, it will be slowed down by the softer Au before again meeting hard Ti. This approach had us going from 50-75% substrate shorted gates to almost none. In the latest devices we made we additionally put down a 100 nm SiO_2 underneath all of the bonding pads for extra padding.

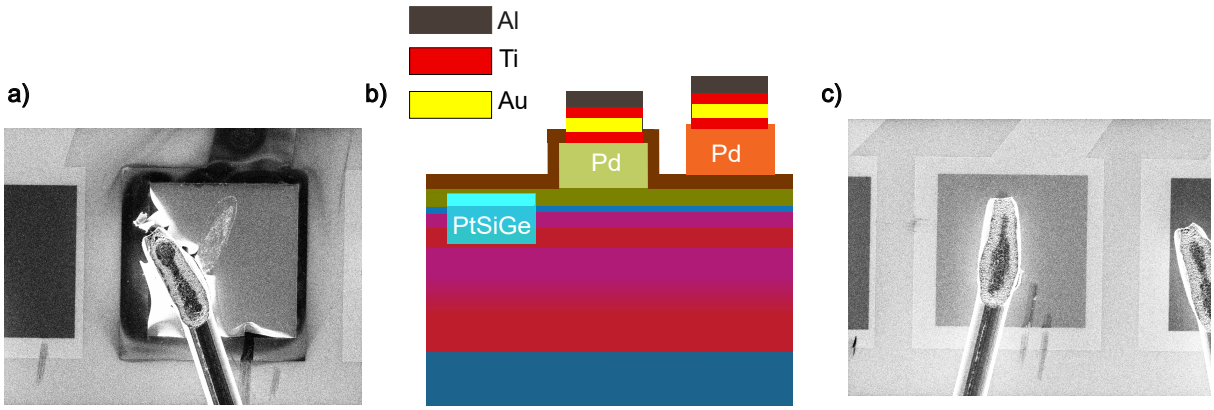

Figure 19: a) SEM micrograph of 5 nm Ti sticking layer and 300 nm Al on top of a gate electrode bondpad that has been wirebonded, demonstrating the damage a wirebond is capable of. **b)** New gate stack with 50 nm Ti, 100 nm Au, 50 nm Ti and 100 Al on top of it. **c)** SEM micrograph of the gate stack in b) on top of a gate electrode bondpad that has been wirebonded.

3.2.4 Fabrication summary

We presented fabrication techniques for fabricating advanced super-semi multilayer devices using Ge/SiGe and the superconducting amalgamate PtSiGe. We presented two big issues in the fabrication of succesful devices. One being the HF dipping times, causing resist wall failures, over etching and resist peeling. This was solved by optimizing resist, pre-bake times and omitting plasma ash cleaning. The second issue presented was wirebond induced gate electrode shortage which was solved by introducing metallic bonding protectors.

3.3 Experimental setup

We will in the following section briefly introduce the experimental setup, and the measurent techniques used.

3.3.1 Dilution unit

In this thesis all devices are measured in a BLUEFORS XLD dilution unit, capabale of reaching temperatures of around $\sim 17\,mK$ at the mixing chamber Fig.21.a) which our sample holder (usually called puck) is thermally connected to. The puck withholding the device is seen in Fig.21.c). The dilution unit utilizes a closed loop $He3/He4$ dilution cycle, which enables an endothermic reaction causing the mixture of $He3/He4$ to absorb thermal energy from its sourroundings, effectively making the surroundings cold [47]. The dilution is sectioned into several stages of various cooling powers and temperature stages as seen in Fig.21.a) These extreme temperatures are essential when doing quantum transport measurements to avoid thermal excitation of the quantum systems being measured. The unit is furthermore equipped with a superconducting vector magnet capabable of creating a magnetic field of 6 T in the z direction, 1 T in the x direction and 1 T in the x direction.

3.3.2 DC measurements

Superconducting transport measurements were done in a two terminal configuration using an Stanford Research Systems SR830 lock-in amplifier. The Lock-in amplifier mixes the lock-in signal with the signal that has been through the device under test, furthermore filtering the high frequency component away then amplifying the signal at room temperature with a Basel preamplifier before measuring the signal on the lockin input. By dividing the signal of the measured current with the applied AC excitation amplitude gives us the differential conductance dI /dV which we for short just write as G. We convert G into units of the conductance quantum $G_0 = \frac{2e^2 2}{h}$, where h is Planck's constant.

All DC signals applied to gate electrodes and ohmics are being sent along a DC loom (green line in Fig.21.a)) and are being generated using a QDevil QDACII which is a digital-to-analogue converter. The Drain is connected to Basel current preamplifier at room temperature and further a Agilent 34465A Agilent Digital multimeter (DMM) used for measuring voltage and current. The DC line resistance including cryo filters and QDevil sample holder motherboard is roughly $2.7\,K\Omega$

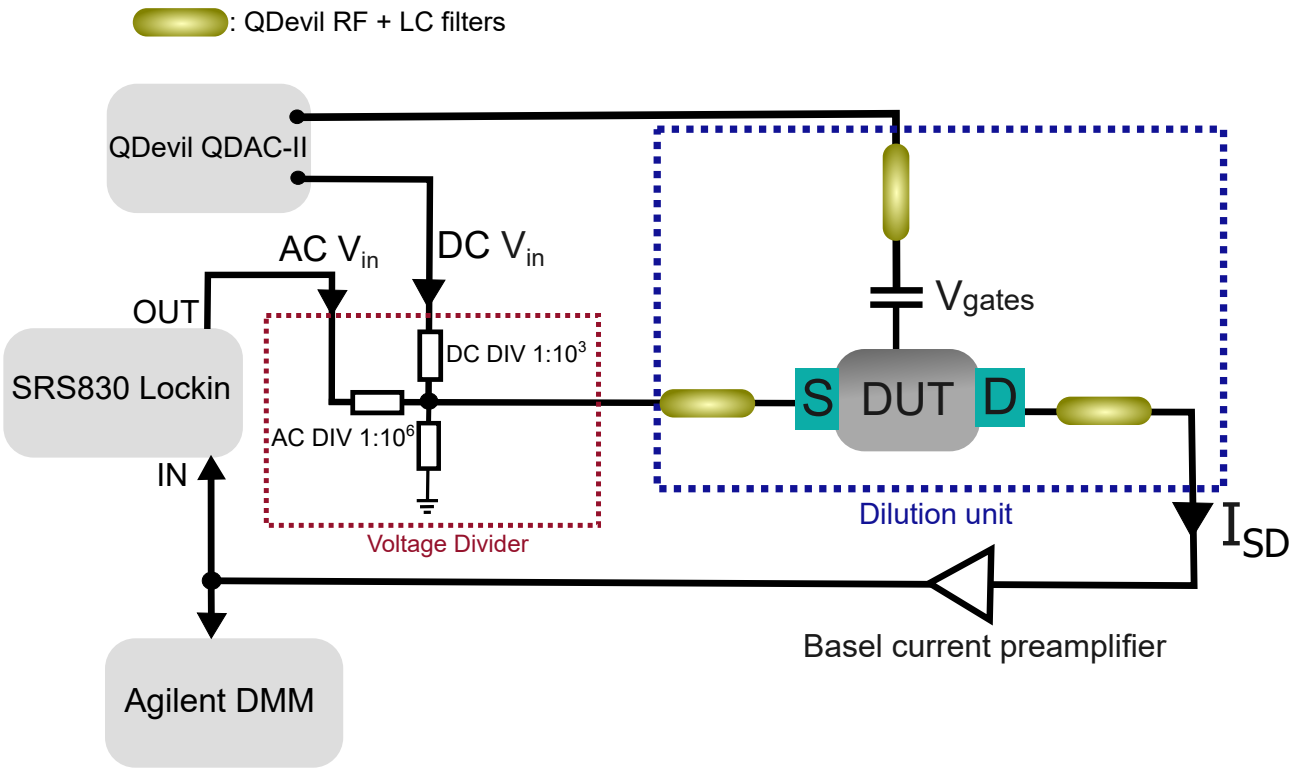

Figure 20: The DC setup used for taking two terminal bias spectroscopy measurements. Lockin and QDAC-II output goes via their respective voltage dividers to the source the device under test (DUT). The current is pre-ampflified at room temperature before being measured at the DMM and lockin inputs. DC gate electrodes are controlled via DC gate electrodes. In pure DC measurements the lockin is omitted and only the QDAC-II and DMM is used.

3.3.3 RF-Reflectometry

In this thesis we use radio frequency reflectometry for fast and sensitive measurements of our devices [48, 49]. As it allows us to measure our system at higher frequencies to avoid $1/f$ noise, which is prevalent in DC measurements. It also allows us to increase the speed of our measurements from around 300 ms pr. measurement point with the DC lock-in, to around 3, ms pr measurement point with reflectometry. The two tools we use for RF is either a UHF SRS860 Lock-in amplifier which is a lockin cabable of utilizing higher frequency excitation tones. The other is a 'Quantum machine multi-core Pulse Processing Unit' (OPX+) which is a powerful multitool, essentially being an arbitrary wave generator with a built in processor capable of signal mixing and demodulating (and many other things). We thus perform the RF measurements by employing homodyne detection, using the internal demodulation of the either the UHF SRS860 Lock-in amplifier or the OPX+, both of which can output their own RF probe tones. The drain

leads of our devices are connected to a LC tank circuit with a certain resonance frequenc (Seen in Fig.21.b).

$$f = \frac{1}{2\pi\sqrt{LC}}, \tag{3.1}$$

where L is the inductance of the surface mounted inductors, and C is the total capacitance to ground often called the parasitic capacitance. When fast changes in charge occurs, so does the resonance, phase and, most importantly the impedance of the system. This happens since off loading a charge or accumulating a charge causes some change in capacitance, this capacitance is commonly called the quantum capacitance C_q as it is usually associated with single electrons (holes) in charge sensing. Thus the frequency briefly changes as

$$f = \frac{1}{2\pi\sqrt{L(C + C_q)}} \tag{3.2}$$

and as mentioned so does the 'load' impedance Z_L[50] at the end of our resonator which is the at the device. The change in impedance affects the signal we are measuring since the load impedance governs the reflection at the device.

$$\Gamma_F = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.3}$$

where Γ_F is the reflection coefficient, from 1 to 0. Where 1 is full reflection and 0 is no reflection. Z_0 is the characteristic impedance in most systems $50\,\Omega$. We thus apply some probe tone at Tx Fig.21.a) with a frequency that matches that of the resonator, this signal gets attenuated and goes through the directional coupler, and reflects at the drain with some rate given by the reflection coefficient. The signal then gets amplified on the way up through Rx Fig.21.a) and enters either the UHF lock-in or the OPX+. Inside the UHF lock-in or the OPX+, the signal undergoes demodulation, which works by mixing the recieved signal with the original probe signal (reference signal). Mixing essentially means that he two signals get multiplied, creating a multitude of frequency products which we can remove with a low pass filter, only leaving a 'demodulated' DC voltage, which is also called homodyne detection.

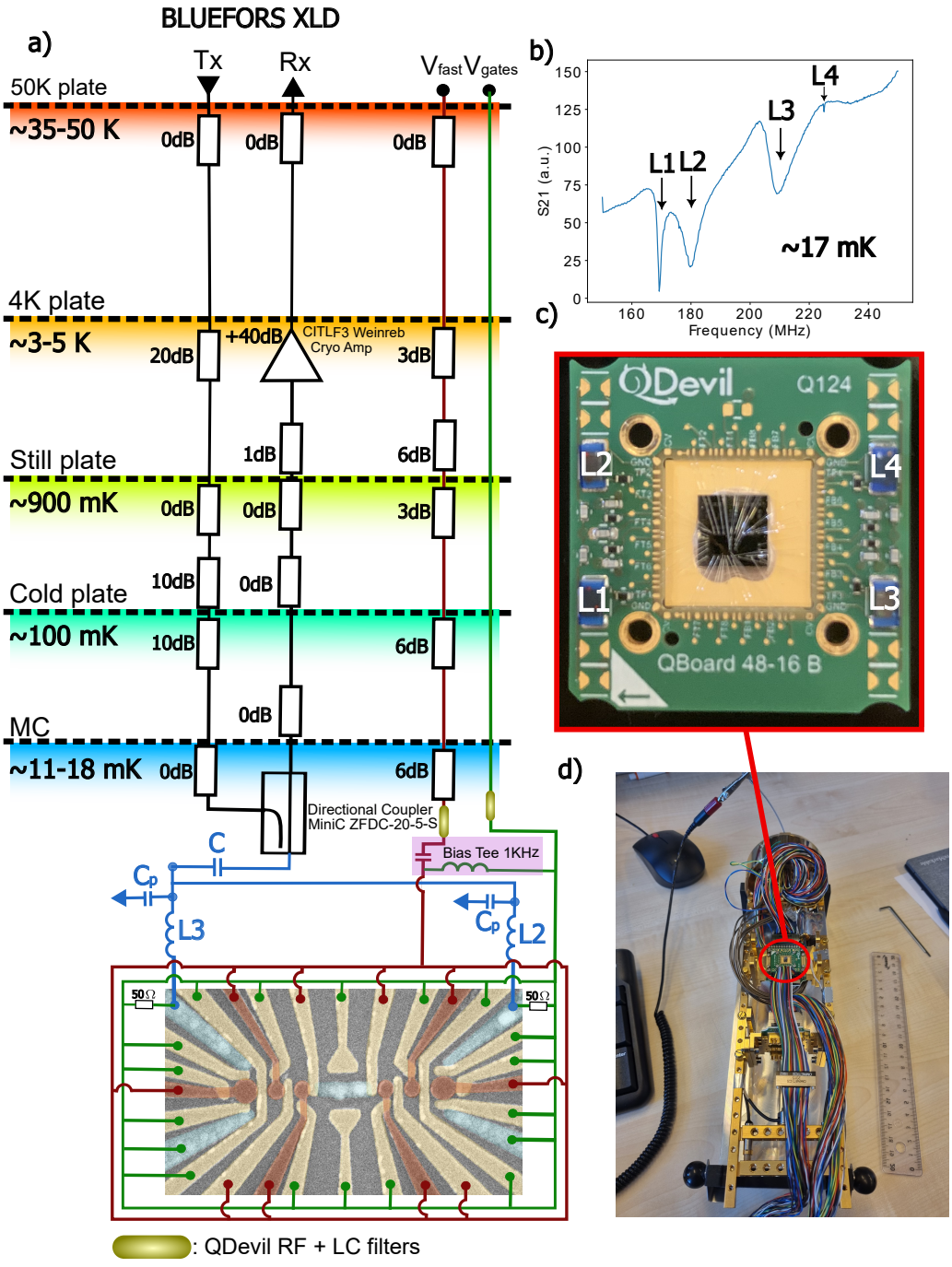

Figure 21: a) BLUEFORS XLD curcuit schematic. **b)** Four resonance frequencies belonging to the four inductors L1, L2, L3, and L4 seen on the sample holder in c) measured with the OPX+ at base temperature. L2 and L3 are connected to devices drains. **c)** QDevil QBoard-48-16B sample holder portraying a wirebonded chip. The four inductors have the indutance values L1=1200 nH, L2=820 nH, L3= 560nH and L4= 390nH, corresponding to to blue tank circuits seen in a).

4 Germanium/Silicon-Germanium quantum dots

4.1 Introduction

In order to eventually make semiconductor gate based qubits in our platform Ge/SiGe we have to be able to control quantum dots down to single hole occupation. We will in this chapter present the results we achieved. We will mainly be studying these systems to validate that we can fabricate quantum dot systems in which we can reach the single hole or at least few hole regime with charge sensing, charge compensation and radio frequency reflectometry techniques in order to eventually use them as qubits. The majority of the results we are about to present stem from the first device batch "QT443-Friendship.mk1" of the type seen in Fig.10, of which we fabricated two chips with a total of six devices. This batch suffered heavily from wirebond induced leakage, and the first four devices measured, had all gates leaking. We identified that the wirebonding must have caused the issues by screening all gates with needle probes before bonding, showing almost no gate leakage. We thus patched up the devices using 300 nm Aluminium bonding protectors as shown in chapter 3.2. This was however not quite enough protection but gave two devices which yielded the following quantum dot measurements.

4.1.1 Tuning the sensor dot

We start off simple by tuning the sensor dot. As the sensor dot will be a key component in current and reflectometry charge sening measurements. The sensor dot is slightly larger, about 150 nm where as the regular quantum dots we have are 100 nm. This is because we want a larger dot with smaller charging energy and more holes, such that it can act as a pseudo hole reservoir to the double dot as the model in Fig.4.). We start by accumulating holes from the reservoirs until we create a current pathway for our carriers going from the source to the drain. This is done by applying a voltage bias to the source and sweeping V_{B1}, V_{B2}, V_{P1}, and V_{SB} down with a negative voltage, until a current runs.

We then tune the barriers V_{B1}, V_{B2} and V_{SB} to a regime just before the channel turns on. In the Fig.22.b) we sweep the dot plunger V_{DP} allowing for successive coulomb oscillations. The coulomb oscillations retain their ΔV_P spacing for several 100 mV and show sharp well defined coulomb peaks. We furthermore see oscillations enveloped on top of our coulomb peaks, this we attribute to barrier oscillations meaning that there is a possible dot under one of the barriers somewhere.

Upon further playing around[3] with the sensor dot, we find a stable regime to do bias spectroscopy and obtain coulomb diamonds, this is seen in Fig.22.c) where successive diamonds are portrayed. From the coulomb diamonds we extract the charging energy E_c (red line in Fig.22.c) to be roughly $1\,mV$, which gets smaller the more holes we fill into our dot and larger the fewer holes we have. The black line in the highlighted diamond is the plunger gate difference ΔV_{p1}, using E_c and ΔV_{p1} we can extract the lever arm α, $\alpha = \frac{E_c}{\Delta V_{p1}} = \frac{1\,meV}{3.5\,meV} \approx 0.3$ which is comparable to hole quantum dots in Ge/SiGe in the literature [19].
The tilt of the coulomb diamonds is attributed to the dot being coupled stronger to one of the barriers.

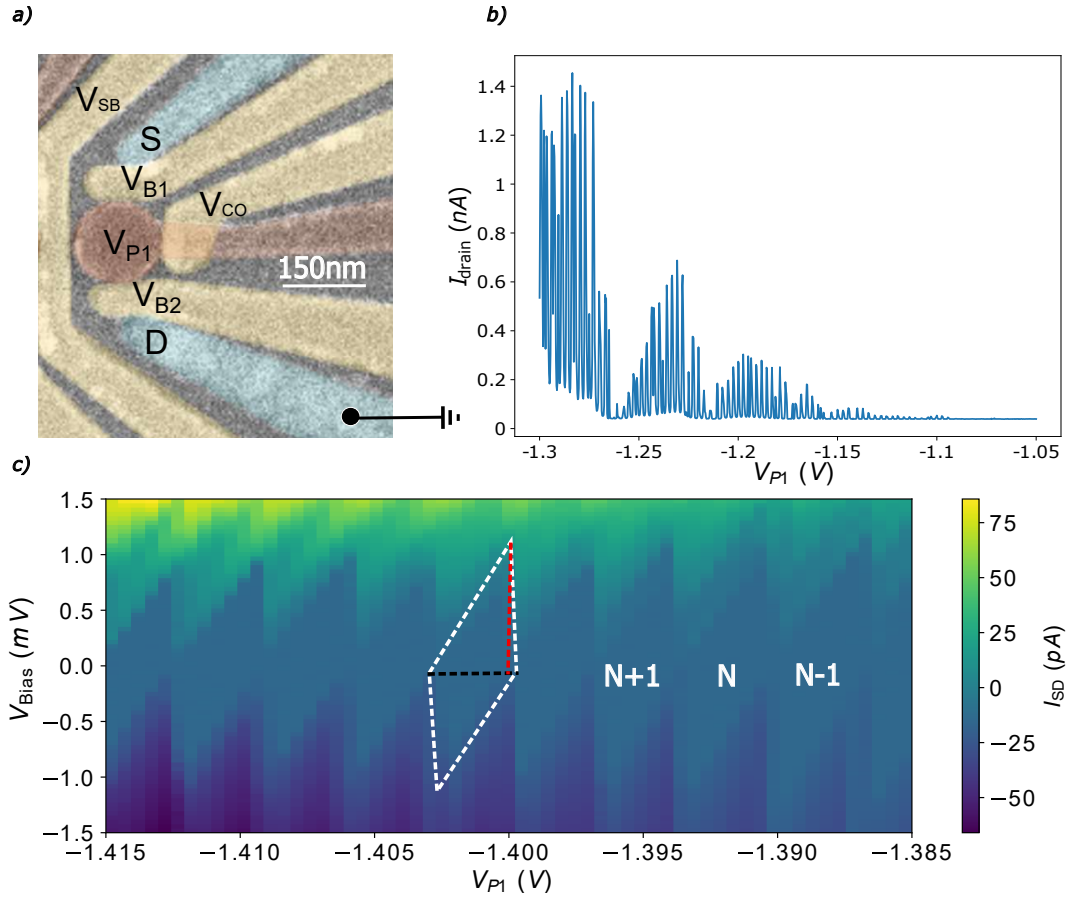

Figure 22: a) False colour SEM micrograph depicting the region of interest on our device. **b)** coulomb oscillations measured as current vs plunger gate voltage. **c)** Bias spectroscopy measuring current as a function of SD voltage vs plunger gate voltage. Highlighted diamond contains a black dashed line representing ΔV_{P1} and a red dashed line representing the charging energy E_c.

[3]When sweeping gates around, the channel turn-on voltage increases, hence the regime around -1.25 V in Fig.22.B) is pushed further up to -1.4 V as we see in Fig.22.c).

4.1.2 Charge Sensing

Upon tuning the sensor dot we can park the sensor plunger V_{P1} on the side of a coulomb peak and start accumulating the first dot setting the sensor barrier V_{SB} to a fitting regime and slowly sweeping the first dot plunger V_{D1} negative. Upon off loading a hole from the sensor dot into the neighbouring dot, an abrupt charge jump can be seen on the sensor peak. This happens due to the change in charge occupation on the sensor dot pushing the energy needed energy needed to re-supply the sensor with a hole from the reservoirs up. Depending on where you are situated on a coulomb peak the charge sensing event looks different as described in Fig.23.b), this is furthermore demonstrated in Fig.23.c) where we sweep V_{D1} and measure the current from S to D, showing the difference between sensing events going down a coulomb peak and up the next one (sweeping negative).

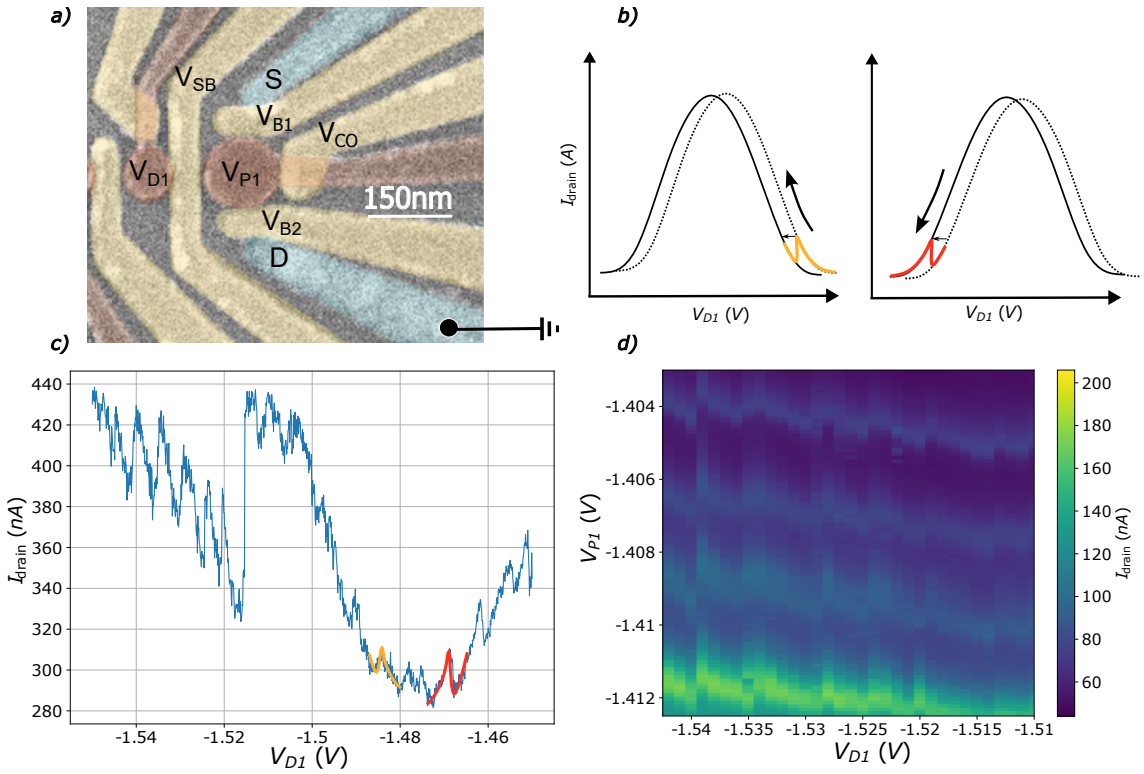

Figure 23: a) False colour SEM of the device region of interest. **b)** Cartoon drawing of a charge sensor Coulomb peak undergoing a charge sensing event. To the left: upon off loading a hole from the sensor to the neighbouring dot while going up a Coulomb peak. To the right off-loading a hole from the sensor to the neighbouring dot while going down a Coulomb peak. **c)** Charge sensing events measured in current as a function of the first dot plunger V_{P1}, colours correspond to the two events in the cartoon of c). **d)** Verifying charge sensing events measuring current as a function of V_{P1} and V_{D1}.

To verify that it indeed is a charge sensing event, we measure the current as a function of the sensor plunger vs the dot plunger as in Fig.23.d), this is done multiple times as random charge jumps and fluctuations can often imitate the behaviour.

4.1.3 Reaching the first hole

In Fig.23.c) we saw that sweeping the dot plunger V_{D1} changes the chemical potential of the sensor dot shifting it in voltage space which can obscure and cause unintended charge transitions. In an attempt to reach the first hole in a single dot we will now utilize linear charge compensation to increase the sensitivity of our sensor and remove the background. Charge compensation is a scheme that allows us to iteratively re-calibrate the sensor plunger voltage every time we sweep another gate in order to keep a target current. In addition to controlling the dot plunger V_{D1} with a DAC, we also add a low frequency lockin excitation of $5\mu V$ to the source. Measuring the differential conductance dI_{SD}/V_{SD} in units of the conductance quantum, as well as a regular DC current, both amplifed at room temperature by a Basel current pre-amplifier. The compensation works by updating the sensor plunger value V_{P1} for each measurement point x such that we keep a target conductance, this is done by using a feedback loop based on the following formula [51]

$$V_{P1}[x+1] = V_{P1}[x] - \beta \cdot i_S[x] - \Delta V_{D1} \cdot A_{C1} - \Delta V_{D1} \cdot A_{C2}, \tag{4.1}$$

Where β is the conductance coefficient in units of Ω which is there to correct the error current into a voltage. Then we have i_s which is the sensor error current, defined as $i_s = I_{meas} - I_0$ where I_{meas} is the measured current and I_0 is the target current. ΔV_{D1} is the dot plunger voltage step size. And the A_{Ci} are the cross capacitive coefficients for the sensor barrier (SB) and the dot barrier (DB) $A_{C1} = C_{P_1}/C_{SB}$ and $A_{C2} = C_{P_1}/C_{DB}$.

We thus set a target current in our code of $I_0 = 120\,nA$ by setting the sensor plunger to the voltage value corresponding to the red star in as Fig.24.c), we furthermore set the conductance coefficient to $\beta = 6M\Omega$. We can find the cross capacitance coefficients by sweeping the sensor barrier vs the sensor plunger and the dot barrier V_{DB} vs the plunger, and roughly extract their slopes $A_{C1} = 0.4$ - Fig.24.b) and $A_{C2} = 0.04$ - Fig.24.d).

gates [51].

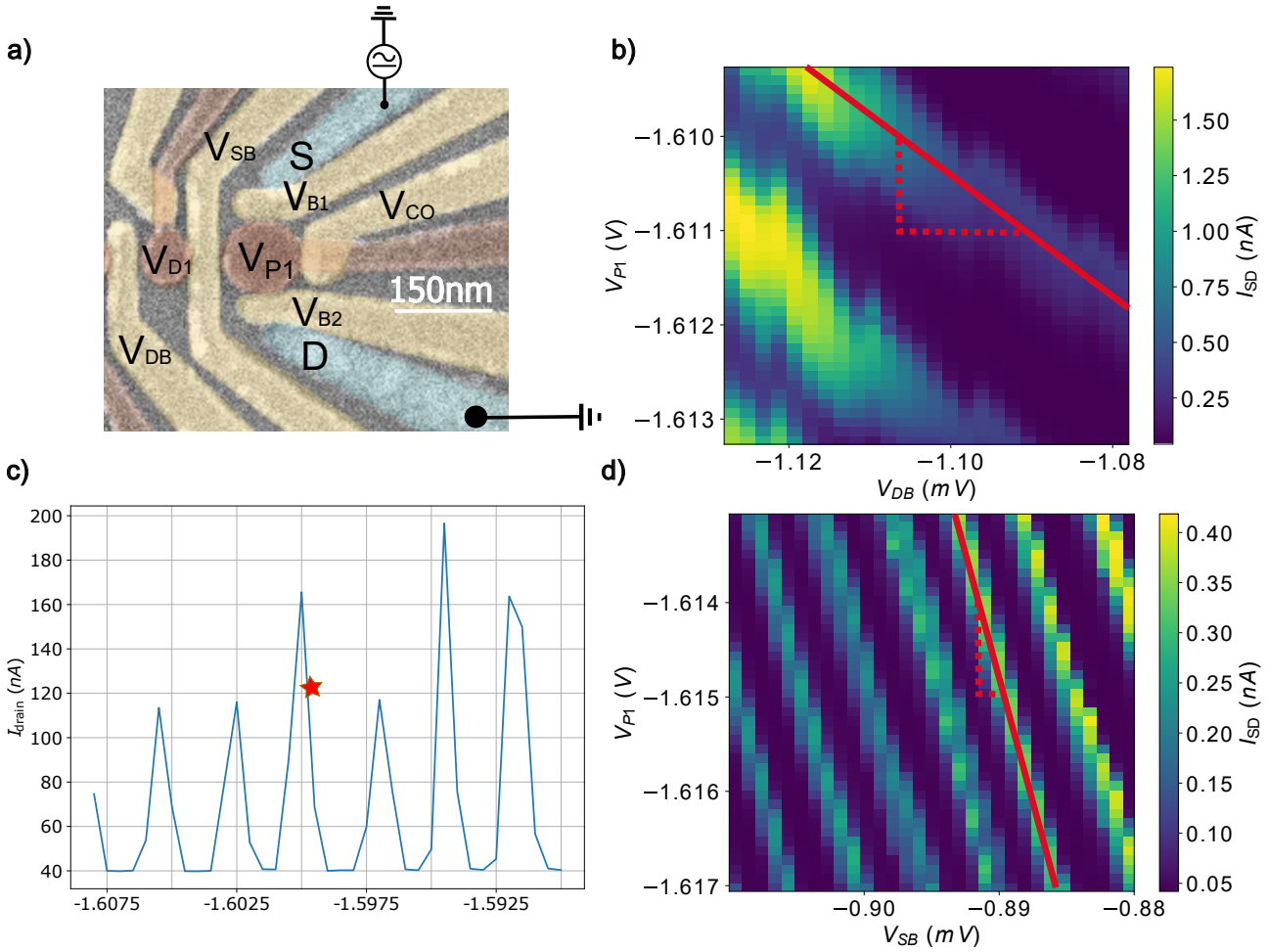

Figure 24: a) False colour SEM of the device region of interest. **b)** Charge transitions on the sensor dot measured in current as a function of V_P1 vs V_{DB}. **c)** Coloumb oscillations on measured in current as a function of plunger gate V_{P1}, red star indicates the target conductance I_0. **d)** Charge transitions on the sensor dot measured in current as a function of V_P1 vs V_{SB}.

Ultimately we can utilize the algorithm as a sweep parameter to hunt for the last hole. The algorithm runs simultaneously along the measurement, for every time a pixel is recorded it measures the conductance and corrects it to the target value by compensating on the sensor plunger. First off we find a regime that has many transitions Fig.25.a), and then slowly go positive with the dot plunger V_{D1} vs sensor barrier V_{SB} until we find no more charge transitions. What we think are the first charge transitions are seen in Fig.25.b). The noise seen in Fig.25.b) is when the algorithm drops of the sensor peak and can not find its way back. We attribute this to a very unstable sensor dot in this regime and possible barrier dots filling as well. Albeit the poor data quality we still believe that we are seeing the first transitions of quantum dot D1. A way to make the algorithm more robust, would be to use cross capacitive coefficients that also get updated for

each iteration, as well as including additional cross capacitance terms.

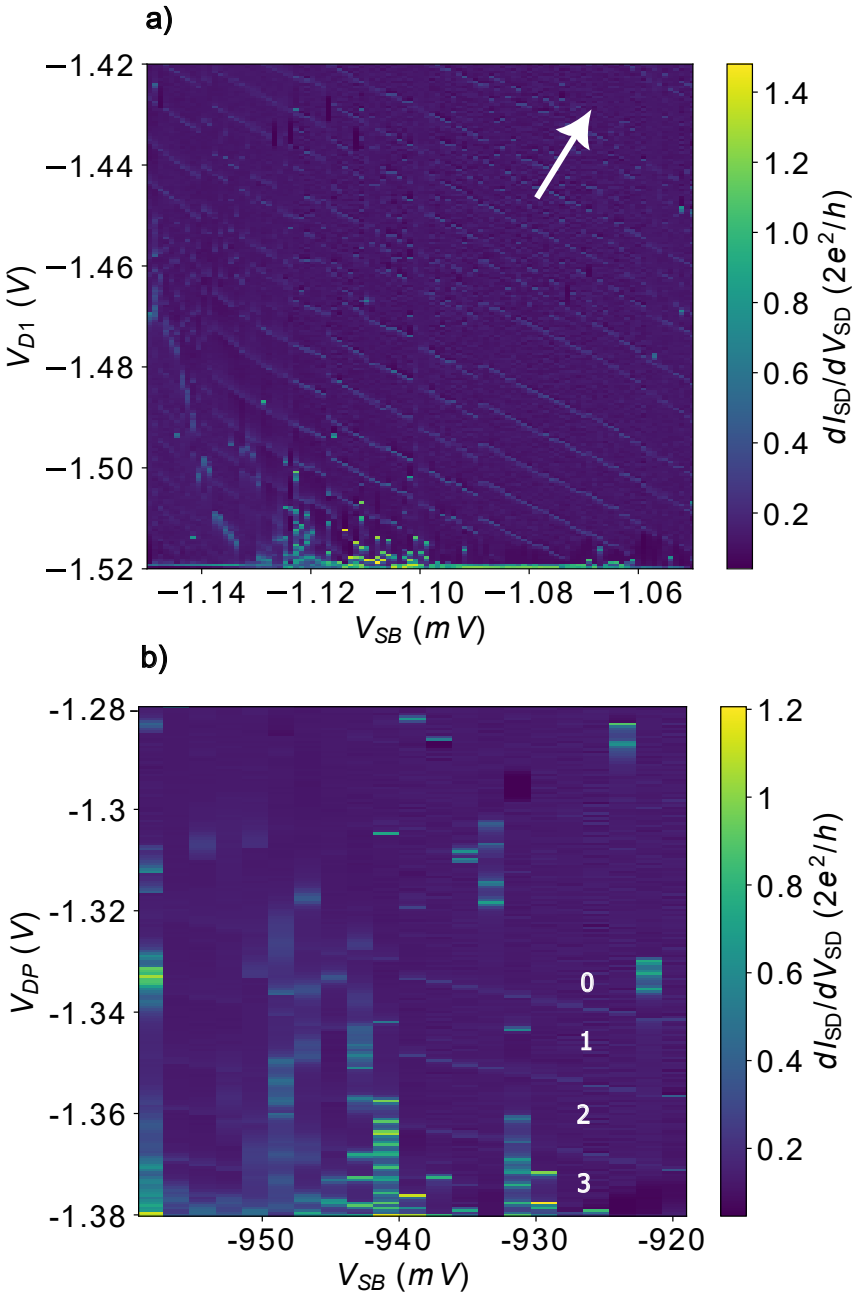

Figure 25: a) Compensated measurement of dI_{SD}/dV_{D1} as a function of V_{D1} vs V_{SB} in a regime with many charge transitions. By Moving towards positive gate voltage indicated by white arrow we can eventually reach a few hole regime. **b)** Compensated measurement of dI_{SD}/dV_{D1} as a function of V_{D1} vs V_{SB} obtaining what we think is the first 3 hole charge transitions. Plunger sensor was particularly unstable in this region, therefore the noise.

4.1.4 Reaching the first holes in a double dot

We will now tune up a double quantum dot using quantum dot D1 and D2 controlled by the plungers V_{D1} and V_{D2} as seen in Fig.26.a). The following measurements were done on a different device than the previous single dot measurements due to wirebond induced gate leakage prohibiting further progression. Now instead of use current charge sensing we will switch over to utilizing RF reflectometry charge sensing. The source and gates are controlled by the QDAC-II while the drain has a tank circuit connected as depicted in Fig.26.a). The tank circuit resonance frequency is $\approx 180\,MHz$ shown in Fig.26.c) For measuring the reflectometry signal we use a UHF SRS830 lock-in amplifier inputting a RF tone at UHF lock-in OUT going to the drain and reflecting back back through the circuit to UHF Lock in IN. The reflected signal gets mixed, demodulated, mixed and filtered before being amplified at room temperature.
We had multiple devices not having all gates intact due to the aforementioned bonding problems and for this particular device we did not have as sharp a sensor dot as we previously showcased. the best we could for this experiment was the sensor peak in Fig.26.b).

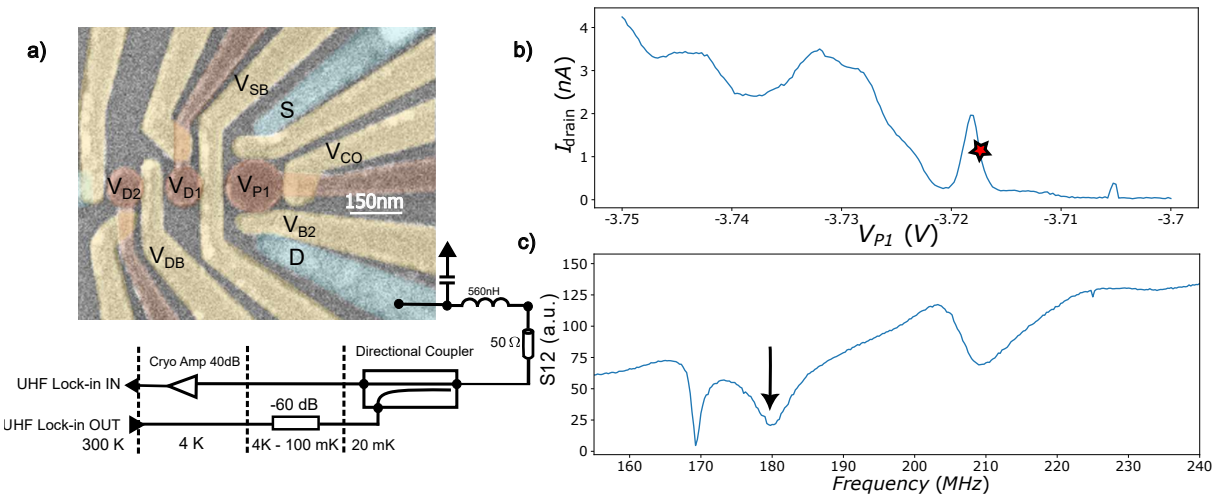

Figure 26: a) False colour SEM micrograph of the device region of interest with additional RF reflectometry circuit schematic connected to the drain. **b)** Current measured as a function of V_{P1}, red star depicts the chosen sensor peak. **c)** Reflected signal measured in arbitrary units. Black arrow indicates the resonance frequency of the tank circuit in a).

We proceed by tuning barriers V_{B1}, V_{B2}, V_{SB}, and V_{DB} to fitting regimes and sweep the plungers V_{D1} and V_{D2} versus each other to reveal a "honeycomb" double dot charge stability diagram Fig.27.a) where we have indicated where we think the first hole fillings are. Furthermore In Fig.27.a) where the white arrow is pointing, we see a charge transition. We attribute this charge transition to a stray quantum dot. We tested this by moving the barriers up and down in voltage, setting the dot barrier V_{DB} voltage +10mV up we moved the charge transition towards our double dot as seen in Fig.27.b) indicating that the spurious dot indeed is under the dot barrier. We tried various voltage settings to remove the stray dot under the barrier but we could not get rid of it, as raising the voltage too positive resulted in closing the channel. Thus we moved it as far as we could into out double dot region as seen in Fig.27.c), to clear the stability diagram in the few hole regime. Zooming in on the first transitions of Fig.27.c) we obtain Fig.27.d) which we believe is the first hole regimes of our double dot.

This particular system is a double dot in parallel with the sensor dot and the reservoirs, and we see in Fig.26.a),b) and c) that the charging lines of the second dot are very horizontal meaning that it is coupled less to our sensor dot. we furthermore see in Fig.26.a),b) and c) that the transitions (1,0), (2,0), and so forth are barely visible if at all, this is due to the first dot being empty, so even though there technically should be a filling of the second dot from the first, there is simply no hole to give from the first. This would be different for a double dot in series as it would just fill from the other reservoir instead.

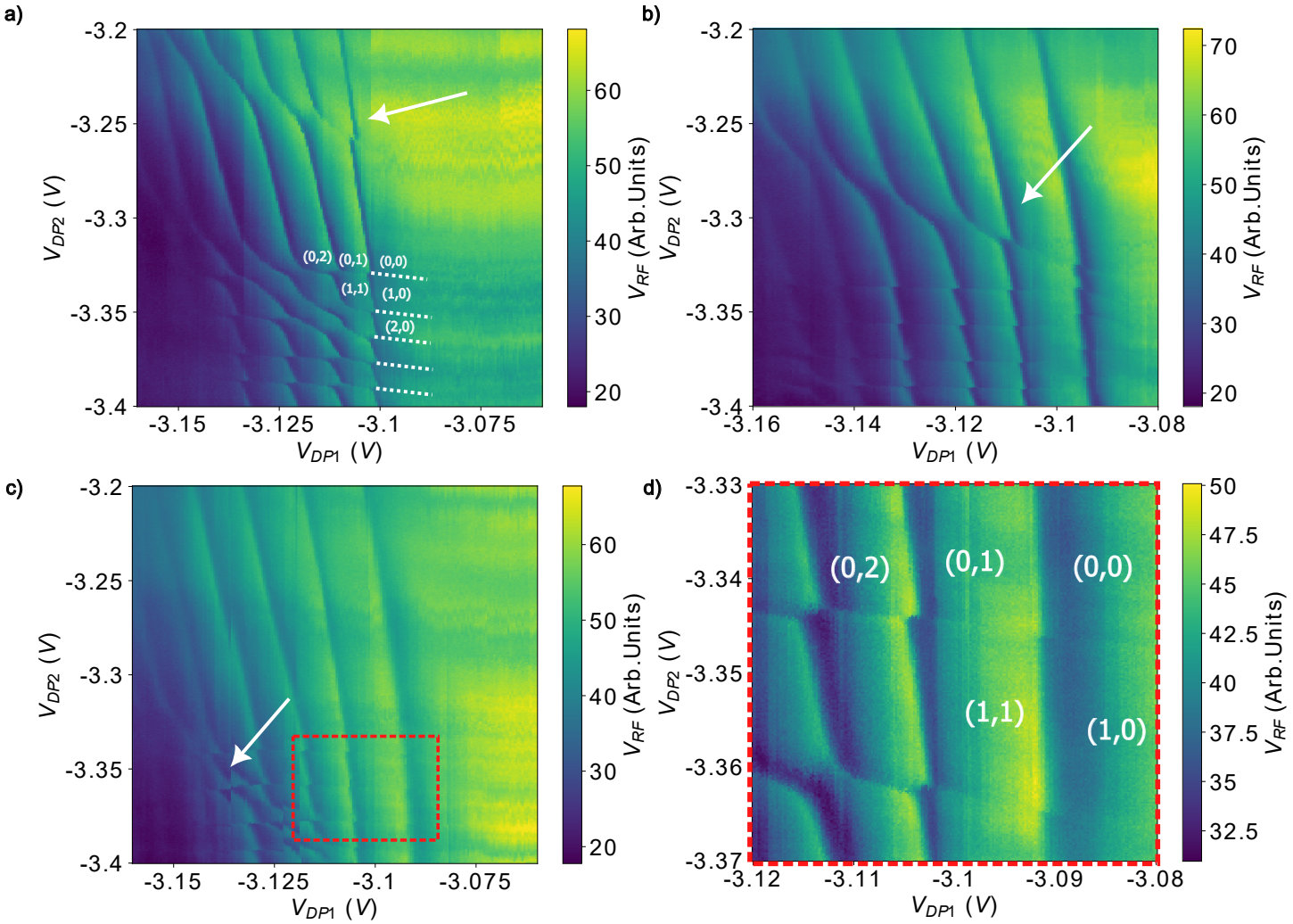

Figure 27: a) Double dot charge stability diagram with a stray dot underneath the dot barrier DB indicated by the white arrow. **b)** Retrace of the measurement in a), with V_{DB} being sligthly more positive (+10 mV). White arrows still points at the stray dot. **c)** Moving the stray dot into the doubledot. Red square corresponds to where the zoom in d) is from. **d)** Zoom of red square in c), with hole charge occupations denoted in white.

4.1.5 Summary

We managed to tune up a sensor dot and use it in DC charge sensing with and without gate electrode voltage compensation to reach the first hole. We furthermore used RF-reflectometry to perform charge sensing in order to reach the first holes in a double quantum dot. We struggled with stray dots under out gate electrodes which we hope to mitigate by making our gate electrodes less wide.

5 Platino-Germano-Silicide superconductor measurements

5.1 Introduction

In this chapter we will explore the superconducting properties of our exotic amalgamation of platinum, germanium and silicon. We will mainly do this by studying superconducting islands, junctions and proximitized quantum dots. The ability to integrate Ge/SiGe with a superconductor allows us to approach semiconductor quantum dot based qubits from a different angle, and possibly in future experiments enable long range coupling mechanisms as presented in the introduction [52, 23]. We will be looking at it with a phenomenological approach, in the sense of whether we actually can evoke the characteristic behaviour of superconducting devices using the PtSiGe amalgamate to make very small architectures we need to realize our experiment. The superconducting structures we have fabricated and implemented in the following measurements are as small as 40 nm. PtSiGe superconducting structures have not been studied at these scales except for micron sized junctions [2].

5.1.1 Suspicion of no superconductivity

When measuring the sensor quantum dots from the device batch "QT443-Friendship.mk1" we began suspecting that it did not yield superconductivity. We took multiple bias spectroscopy measurements measuring the differential conductance G as a function of bias voltage vs plunger gate V_{P1} as seen in Fig.28.a) and b), we however could not find the characteristic 4Δ gap when measuring a super quantum dot super system and we furthermore could not access the island in the middle due to gate leakage. While this is not sufficient proof for no superconductivity, we nonetheless still decided to fabricate the 2nd generation of devices "QT443-Freundschaft.mk2" Fig.29. All fabricated on the same QT443 wafer, with all the same fabrication methods as the "QT443-Friendship.mk1" devices in Fig.10. However this time we prolonged the HF dip to 10 s, contrary to the 5 s of the first generation batch. We also learned from the first generation that too wide barrier gates introduced unwanted stray quantum dots, thus we tightened the design from 50-60 nm gate widths to 35-40 nm gate widths. In addition to this we added two leads on each side of the superconducting island named O_{top} and O_{bot} in Fig.29, with each their barrier gate V_{B1} and V_{B2} Fig.29. This was done in order to probe the island independently from the rest of the device. Furthermore we added a top gate to the island V_{top} in Fig.29, in hope of being able to control energy levels in the superconductor. We furthermore incorporated both SiO_2 and $Ti/Au/Ti/Al$ bonding protectors as in chapter 3.2) helping greatly with the leakage problem.

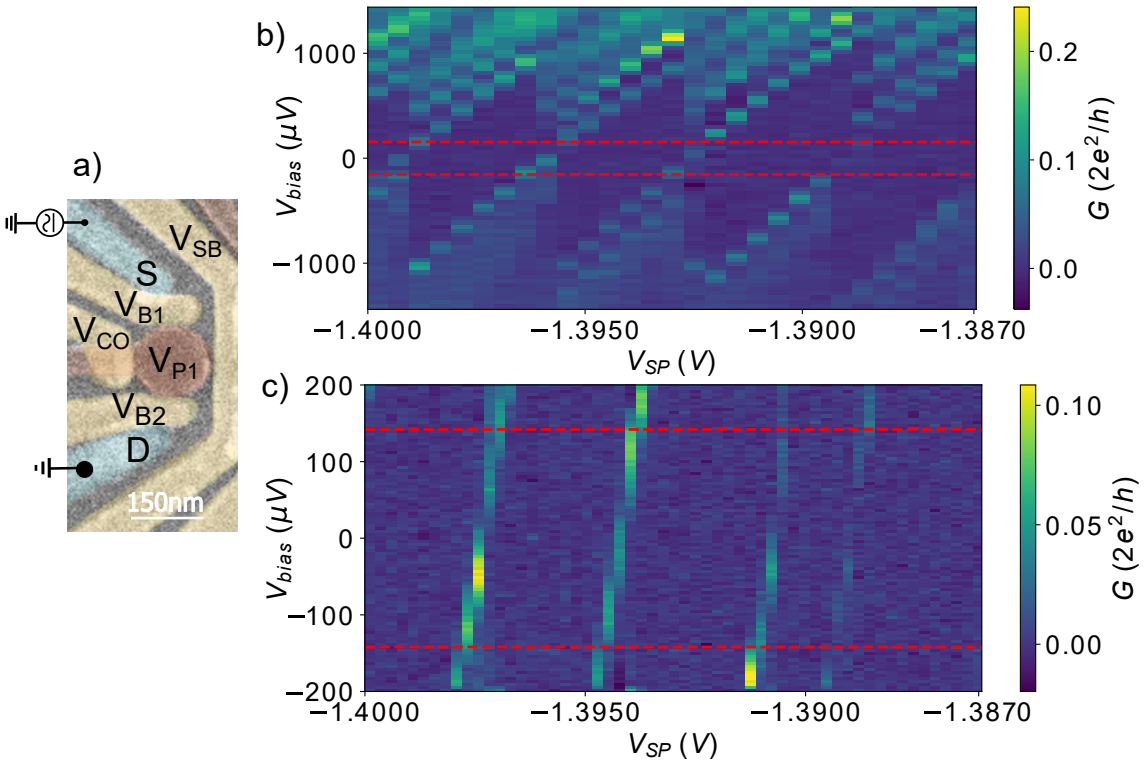

Figure 28: a) False colour SEM of the sensor dot and associated gates.**b)** Bias spectroscopy, measuring differential conductance G in units of $2e^2/h$ as a function of bias voltage and plunger gate voltage V_{P1}. Red lines indicate where 2Δ peaks should be in PtSiGe according to A.Tosato et al. in [2]. **c)** Zoomed in version of b).

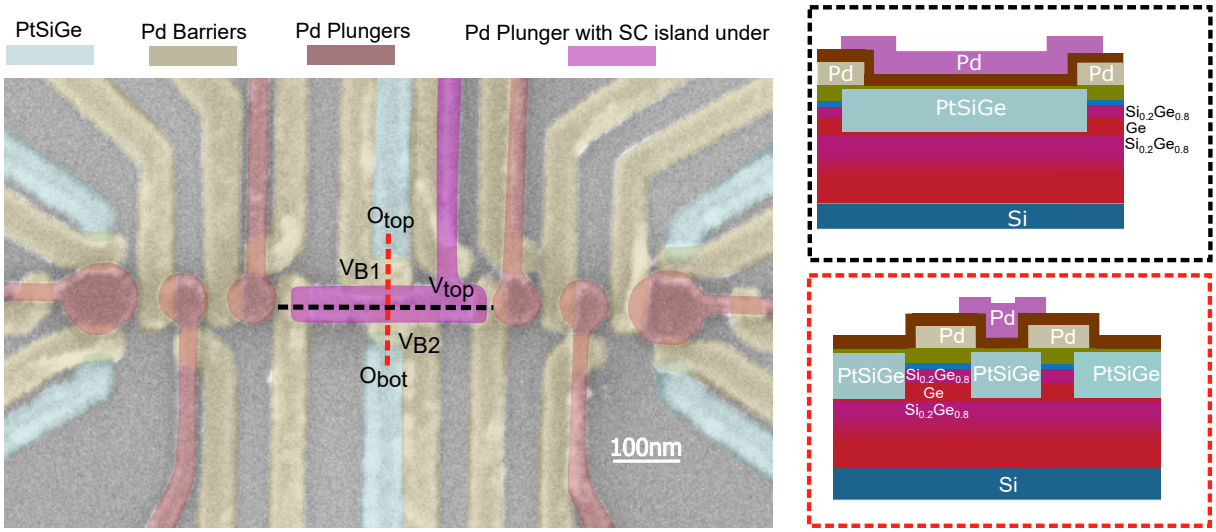

Figure 29: False colour SEM micrograph of Second generation 'Fruendschaft.mk2' device. Cartoons of the corresponding device line cuts in red and black can be seen on the right.

5.1.2 SNS

We will now explore the superconducting island in the configuration of a SNS junction as seen in Fig.6.a) and b). In the following measurements the source was connected to both a QDAC-II and a SR830 lockin ampifier with an excitation of 2.5 μV and probe tone of 17Hz. The barrier gates were all controlled with the QDAC-II. Current was measured with the DMM preceeded by a Basel current amplifier with a gain of 10^6 V/A as seen in Fig.20.
Ideally the system we see in Fig.30.a), would correspond to a SNSNS junction.
However due to either systematic (measured across 3 devices on the same chip) mis-alignment or EBL errors causing a short between the island and the drain. We were not able to probe it as a SNSNS junction.

Thus we measure it as an SNS system as seen in Fig.30.b). The barrier gates V_{B1} and V_{B2} in Fig.30.a) are ideally used to accumulate charge carriers in the semiconductor situated betwixt the island and the leads, letting a current run from source to drain. V_{B1} did not leak and was able to control the current flowing from source to drain. V_{B2} did not leak, but had however no control over the current, which would make sense if the island was shorted to the drain. We were thus able to form a SNS junction from the source to the now 'extended' drain simplified in Fig.30.b). Ultimately we saw that the top gate V_{top} was shorted to the island, as we measured a high negative current on the order of mA, when sweeping V_{top} to a negative voltage of around -40 mV.

In Fig.30.c) we perform energy spectroscopy measurements by sweeping the bias voltage versus V_{B1}, measuring the differential conductance G in units of $2e^2/h$ being the quantum of conductance. At a V_{B1} gate voltage of $\approx$-50 mV we see two differential conductance peaks situated at $\pm 155\,\mu V$ in Fig.30.c) and the line cut Fig.31.c). We interpret this as the characteristic SNS $\pm 2\Delta$ quasi particle peaks, corresponding to the situation to the right in Fig.6 where we have a single quasi particle current flowing. Dividing this with 2 we obtain 77.5 μV, which should have the same energy as the parent gap size of Δ. A value of Δ of this size would fit with previously measured values by A.Tosato et al. of around 71 μV [2].

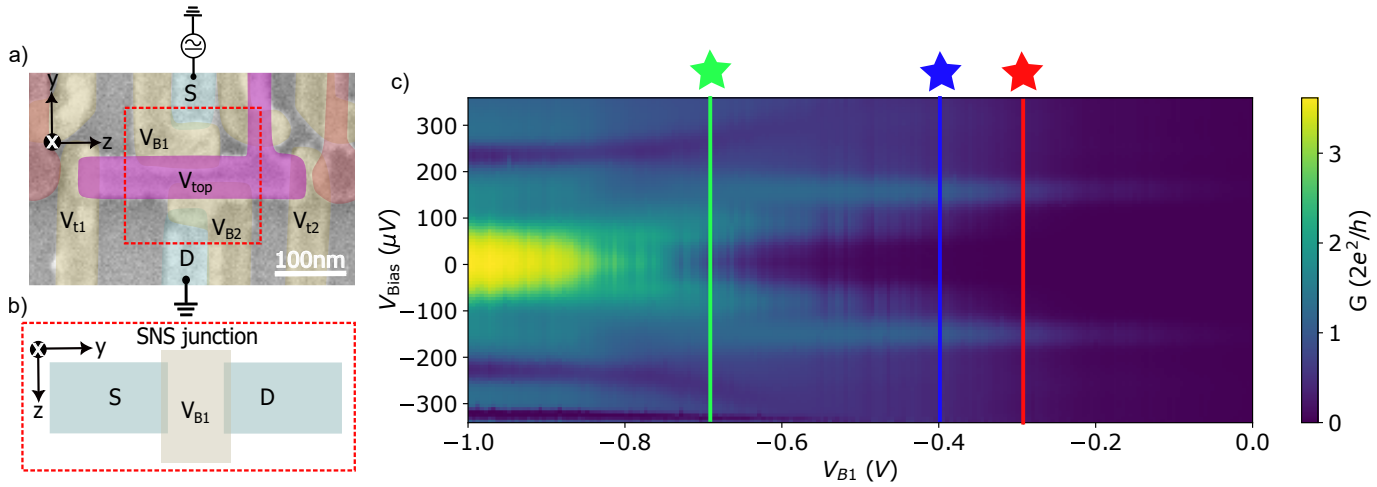

Figure 30: a) False colour SEM micrograph of the device zoomed in at the area of interest. V_{top} being the top gate, V_{B1} and V_{B1}, being the barrier gates, source and drain indicated as S and D. **b)** Cartoon schematic of device configuration. As V_{B1}, V_{top} are shorted to D in figure a), we thus have a SNS junction. **c)** Differential conductance G in units of conductance quanta measured with a lockin amplifier, with the y-axis being the source-drain bias controlled by the QDACII, the x-axis being V_{B1} also controlled with the QDACII.

Lowering the voltage on V_{B1} we see the emergence of two conductance peaks at $V_{Bias} = \pm 77\,\mu V$ in Fig.30.c) and Fig.30.b). Using $T_c \approx 0.5\,K$ from the literature [27, 2], we can compute that $\Delta = 1.764 \cdot k_b 0.5\,K \approx 76\mu\,eV$ giving us enough confidence to say that this is the second order multiple Andreev reflection as seen to the left in Fig.7 with an energy corresponding to that of the parent gap Δ in PtSiGe.

Upon pushing V_{B1} even further negative, we suspect that we open up for a small supercurrent at zero bias that becomes increasingly larger towards V_{B1}=-1 V as we open the channel more and more. seen in Fig.30.c) and Fig.31.a) green. Although to rigorously confirm that this is a supercurrent one would need to do a 4-terminal measurement and substract the exact line resistance, where as we only subtract the DC looms, Cryo filters and QDevil sample holder motherboard ($\approx 2.7\,K\Omega$). These measurements indicate that is it possible to maintain the coherence of the over the semiconducting link bridging the two superconductors. Meaning that the wavefunctions from the superconductors actually overlap with the semiconductor on a meaningful length scale. Which should be enough distance to couple a superconductor separated by a barrier gate to a quantum.

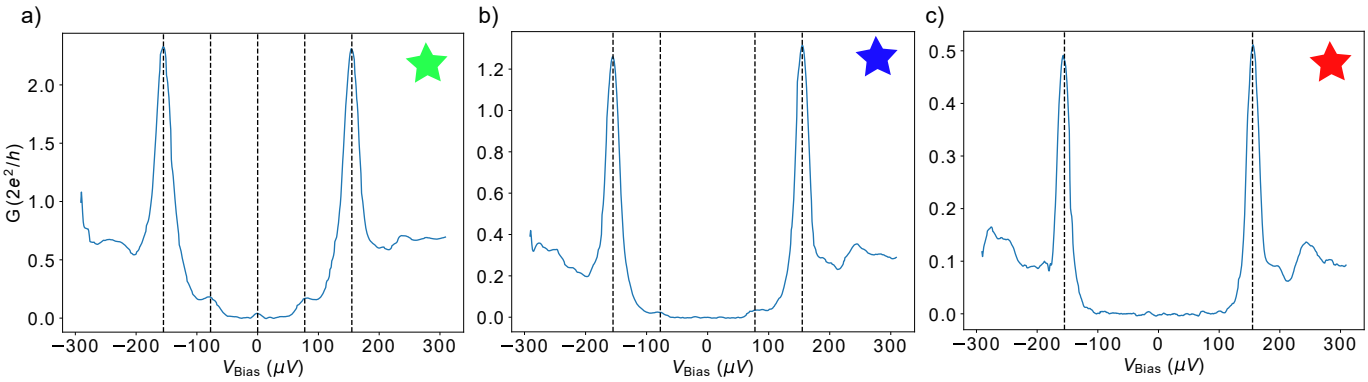

Figure 31: Bias spectroscopy measurements measured with lock-in amplifier across the junction. Each colour star corresponds to measurement taken with a higher resolution of the coloured linecuts in in Fig.30.c), setting V_{B1} to the voltage value of the coloured star. **a)** Lines at $4\Delta = 155\,\mu V$ **b)** Lines at emerging at the second order MAR at $2\Delta = 77\,muV$. **c)** Emergence of a zero bias peak.

5.1.3 SNS B-field sweeps

In order to investigate the magnetic field robustness of our superconductor we perform bias spectroscopy measurements while sweeping the magnetic fields in all three spatial directions. proceeding with the device and measurement configuration as in Fig.30.a) and b). We measure the differential conductance G, as a function of source drain bias vs magnetic field.
Parking V_{B1} at -0.65 V, leaving our parent gap resonances and a faint zero bias peak. By sweeping the magnetic field to 1 T in the X direction, which is out of plane with respect to the device Fig.32.a). The gap closes in at 0.5 T and vaguely persists to 0.7-0.8T, which is large compared to bulk Aluminium which has an in plane field tolerance of roughly 18-20 mT [53].
The parallel magnetic field in the y-direction, that is along the direction of the current flow of the junction, the gap closes in at 1 T Fig.32.b). While the magnetic field in the z-direction Fig.32.c), which is along the superconducting island, persists for more than 1 T.

This is in accordance to superconducting thin film measurements in magnetic fields, as the out of plane field will have a larger surface to pin and fill the superconductor with magnetic flux lines until the superconducting phase breaks down. While the parallel directions are more robust due to having their geometry minimized, thus avoiding flux pinning. Retaining superconductivity at such high magnetic fields gives us sufficient room to perform various spin qubit experiments [16], as spin qubit experiments usually need magnetic fields as a control parameter.

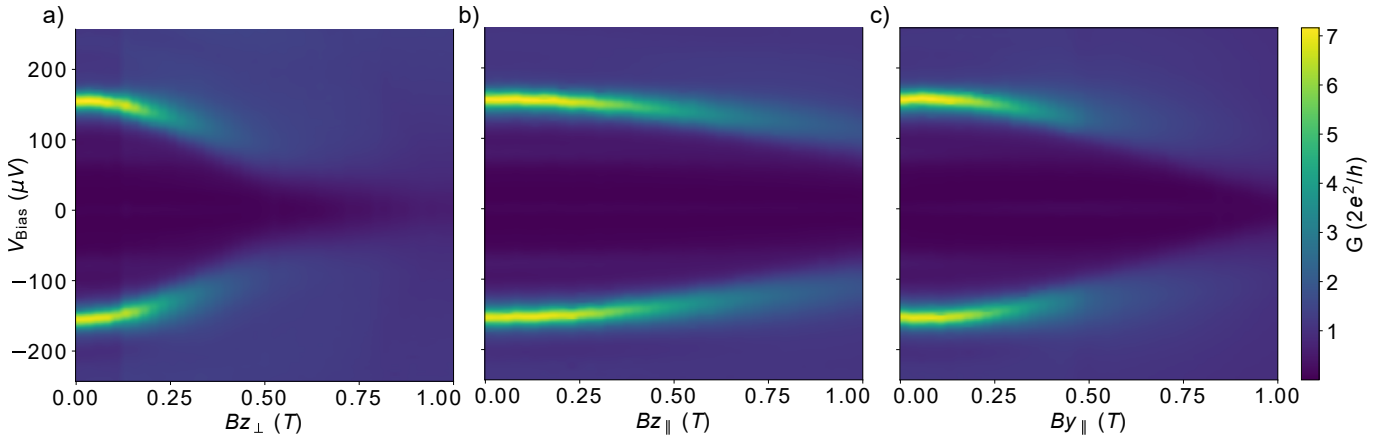

Figure 32: Bias spectroscopy, measuring differential conductance G in units of $2e^2/h$ as a function of bias voltage and magnetic field. Following the device configuration and spatial coordinate system of Fig.30.a). All three plots share the y-axis. **a)** Field pointing in the x-direction, i.e. out of plane. **b)** Magnetic field in the y-direction(parallel to the path of current). **c)** Field in the z-direction (parallel with the island).

5.1.4 MARs

The following measurements are done in the same configuration as in Fig.30.a) and b), same chip, but new identical device. This time V_{top} was not shorted to the island but had little to no effect on the current, V_{B2} still had no effect on the current what so ever. In Fig.33.a) we do a bias spectroscopy measurement of the differential conductance as a function of bias voltage vs V_{B1} pushing the barrier negative, reavealing multiple conductance peaks at what we we previously identified as 2Δ and Δ. However this time additional peaks reveal between the zero bias peak and 2Δ. We attribute this behaviour to multiple andreev reflection causing subgap conductance peaks. Taking a higher resolution line cut along the orange line reveals Fig.33.b) which shows the subgap conductance peaks. Inferring 2Δ to be $155\,\mu V$ we insert dashed lines in accordance to $eV = \frac{2 \cdot 155 \mu V}{N_{MARs}}$ with $N_{MARs} = 1, 2, .., 5$ too see whether our conductance peaks fit to the fractions of the gap size. We see in Fig.33.c) that $N_{MARs} = 1$, 2, $3\,and\,5$ line up at the "shoulder" of the conductance peaks at roughly
$155\,\mu V$, $77\,\mu V$, $52\mu V$ and $31\mu V$, where as $N_{MARs} = 4$ is in a dip. Whether the MAR resonance is located at a peak or a dip depends on the transparency τ of the junction, if the transparency is high the MAR is located in a dip, if it is low then it is located on a peak [40].

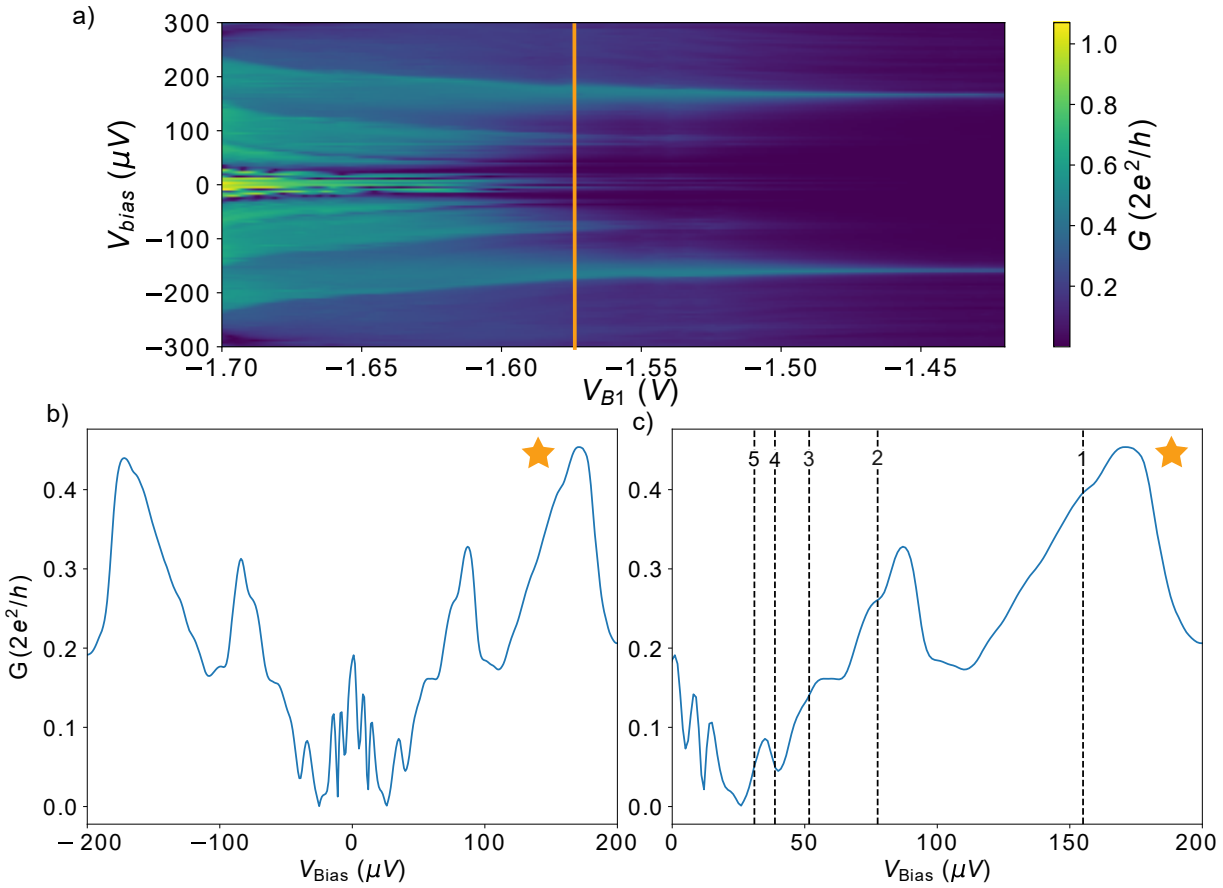

Figure 33: a) Bias spectroscopy at measuring the differential conductance G as a function of bias voltage V_bias vs barrier gate.**b)** Bias spectroscopy at $V_{B1} = -0.85\,V$, in units of differential conductance.**c)** Same measurement as in b) zoomed in from 0 to 200 μV bias. Dashed lines correspond to $eV = \frac{2\Delta}{N_{MARs}}$, $2\Delta = 155\,\mu V$ and $N_{MARs} = 1, 2, .., 5$.

The line cut would thus seem to be in a regime of intermediate transparency as our first three orders of MARs are still located on conductance peaks. As for the higher order MARs it is harder to determine where they belong. Going further towards zero bias in Fig.33.a) we see several conductance peaks hugging the zero bias peak. This we we do not fully understand as those peaks do not follow the spacing which MARs resonances usually do. We however attribute the zero bias peak to a supercurrent. A more systematic investigation of these nano sized junctions would be interesting, in order to validate whether a "dirty"[4] annealing process of Pt in Ge/SiGe could yield as good or close to as good transparency as is possible in InAs platforms with epitaxial Al.

[4]Whether the process is dirty is not known, for all we know the surface impurities could be burned or removed during the annealing process.

5.1.5 Superconducting island

In the following measurements we look at transport across the "island", which unfortunately was shorted to one of it's probe leads see Fig.34.a) including inset. Ideally it would be a piece of floating superconductor sometimes referred to as a Cooper pair box or Cooper pair island [54] where the first step would be to demonstrate even-odd occupation of the island, that is the sequential loading of first a hole, then a cooper pair, and so forth. This demonstration would should that we have some control over the island. However due to the shorted island this was not possible as the charging energy probably is infinitely small due to being shorted to the massive bottom lead O_{bot} in Fig.34.a). The measurement configuration seen in Fig.34.a) is the same as in Fig.20, using the lead denoted S as source and the lead denoted D as drain, creating a current path along the yellow line in Fig.34.a).

All gates in Fig.34.a) marked with a C are cut-off gates, and are used to prevent accumulation of charge carriers along the plunger gate fan outs, all cut off gates and V_{B2}, V_{B2}, and V_{top} were set to 0 V. All leads except for S and D were open. All plunger gates denoted P and barrier gates denoted B were slowly, one by one lowered to -1.5 V, allowing for step wise accumulation and inspection of leakage until reaching the tunneling gates V_{t1} and V_{t2}. V_{t2} however turned out to leak to the substrate at around -1.2 V, we thus had to help it accumulate and bridge a current path, by using the cutoff gate C_h. The two superconducting leads O_{top} and O_{bot} were both floating.

When sweeping the tunneling gates versus each other in fig.34.b) we see the emergence of a signal in a "elbow" style plot, where it is seen that V_{t2} needs less voltage to allow a current than V_{t1}, as it is being helped by C_h now. By parking the tunneling barriers V_{t1} and V_{t2} at the red star in fig.34.b) We obtain the bias spectroscopy plot in fig.34.c). In fig.34.c) we see a gap, it is however ill defined, with vague peak structure at multiple places. Doing the same but now parking the V_{t1}, and V_{t2} at voltages corresponding to the green star in fig.34.d) shows a slightly more defined gap starting $60 - 70\mu V$ but with more pronounced peaks toward $180\,\mu V$ as well. The lack of a well defined island make this data hard to analyze, although the presence of a gap along this 400 nm of superconducting strip (albeit the short to the lead) indicates some coherent processes are happening, which gives us a lower bound on our superconducting coherence length of 400 nm.

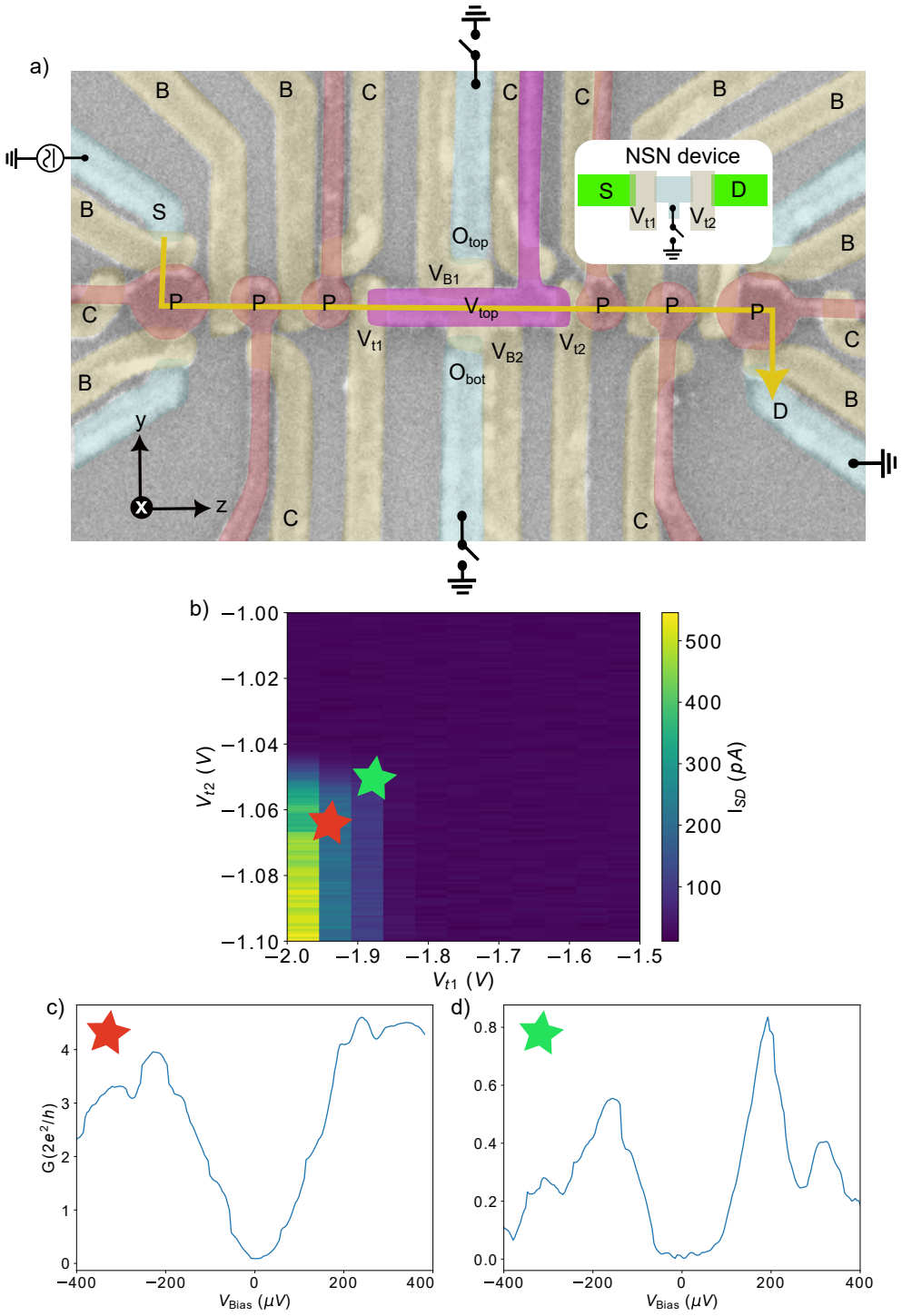

Figure 34: a) False colour SEM micrograph of full device. **b)** Elbow plot measuring current from S to D as a function of V_{t1} and V_{t2}. The Inset is a simplified cartoon of the device configuration. **c)** Bias spectroscopy measurement - differential conductance G in units of the conductance quanta as a function of SD bias at V_{t1} and V_{t2} set to the values of the red star in b). **d)** Bias spectroscopy measurement - differential conductance G in units of the conductance quanta as a function of SD bias at V_{t1} and V_{t2} set to the values of the green star in b).

5.1.6 S-QD-S

Different from the previous generation of devices, we now saw that we could not turn on our sensor dot channel when using a too low voltage bias. We figured that this was due the superconducting gap suppressing the conduction, meaning that superconductivity likely was present. This would now allow us to explore a superconductor quantum dot superconductor hybrid system, as the sensor dot is located in direct in vicinity to the two superconducting leads as the false colour SEM shows in Fig.35.a). We furthermore decided to investigate the system using RF-reflectometry. While RF-reflectometry is a standard technique in quantum dot and quantum information experiments [29], it is rarely used for superconducting transport measurements due to worries about power broadening and unwanted excitations. We however present the following data showing a hybridized quantum dot Fig.34.b), c), and d) measured using RF, showing well understood phenomena as we will explain.

The drain is connected to a tank circuit receiving an RF signal from the OPX+ output via port Tx as seen in Fig.35.a), the receiving signal is reflected at the device, to the OPX+ input via the Rx line in Fig.35.a). The bias as well as the all barrier gates are controlled by the QDAC-II. The plunger gate V_{P1} is connected to both the QDAC-II and a secondary OPX+ output channel in order to sweep the gate electrode fast (on the order of ms). When using the OPX+ we are limited by the sweep range of $\pm 500\,mV$ which is then further attenuated by 24dB. The signal after attenuation amounts to $\pm 30\,mV$. This means that 0 in Fig.35.b),c) and d) is some V_{P1} plunger value, and δV_{P1} is so to speak a virtual parameter that sweeps from $-30\,mV$ to $30\,mV$ around that point.
The input signal on the drain from the OPX+ would have a $3\mu V$ excitation voltage at the frequency 180 MHz matching the tank circuit. The OPX+ upon receiving the signal mixes it with the original tone and filter off the low frequency component, which means that we effectively use the OPX+ as a MHz lockin amplifier, measuring the in-phase magnitude in units of a demodulated voltage. Except we we now measure a change in reflected signal when the conductance changes. This means that when when the resonance frequency changes as a function of changes in capacitance, we lose signal.

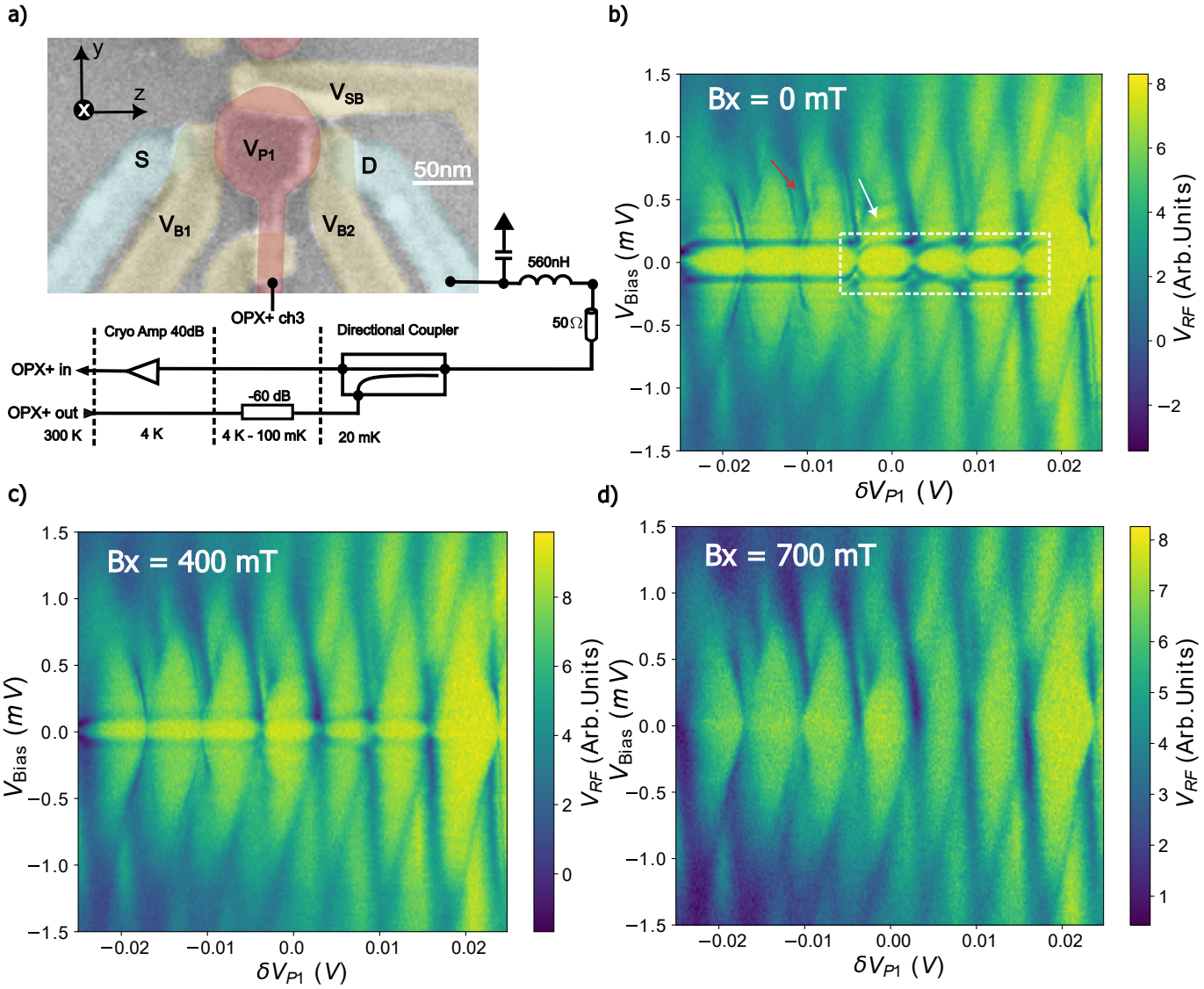

Figure 35: **a)** False colour SEM micrograph of the device region of interest. Reflectometry schematic connected to device drain. **b)** Couloumb diamonds at zero perpendicular magnetic field measuring S21 as a function of bias voltage vs virtual gate plunger. White arrow points to inelastic cotunneling lines. Brown arrow points to normal quantum dot excited states. The features in the dashed box correspond to Andreev proceeses in the YSR limit. **c)** Couloumb diamonds at 400 mT perpendicular magnetic field, measuring S21 as a function of bias voltage vs virtual gate plunger. **d)** Couloumb diamonds at 700 mT perpendicular magnetic field, measuring S21 as a function of bias voltage vs virtual gate plunger.

We then tune the sensor dot by setting the SD bias well above 2Δ in order to have single particle transport, then proceeding with accumulation using V_{P1}, and tuning the barrier gates V_{B1} and V_{B2} until reaching a regime of stable Couloumb oscillations.

By then doing bias spectroscopy measurements measuring the amplitude of the reflected signal versus the fast plunger gate $\pm 30\,mV$ having V_{P1} parked at $V_{P1} = -1.85V$ and the barriers parked at a finite voltage in the Couloumb regime we obtain Couloumb diamonds with roughly 1.5 meV charging energies with a clear $\pm 2\Delta$ gap inside them as seen in Fig.35.b). This we again attribute to the situation in Fig.6 to the right, except that the normal region is now a quantum dot with its own levels. We further more see various behaviour such as co-tunneling lines denoted by the white arrows Fig.35.b). These lines indicate that quasi particles can travel along the dot levels [55]. We also see classic exited states in the quantum dot denoted by a brown arrow in Fig.35.b) [26]. We furthermore see conductance features that bend within the gap, as seen in the white box in Fig.35.b). We attribute this to Andreev bound states at the interface between the leads and the dot. We can observe this in spectroscopy measurements when the superconductors chemical potential (μ_{SC}) of one lead aligns with an Andreev bound state, while the dispersion i.e. the rounding comes from hybridization between spins residing within the quantum dot and the excited quasiparticle states. This process involves an Andreev reflection at e.g. the drain which absorbs a hole-like quasiparticle and sends out an electron-like quasi particle (and ect. back and forth.), thus enabling a conductance [56]. We can furthermore ascertain that we are in the Yu-Shiba-Rusinov Andreev bound state limit, which means that our parent gap Δ is much smaller than our dot charging energies [57] .

By redoing the bias-spectroscopy measurements at different perpendicular field strengths we first see in Fig.35.c) that the SNS 4Δ gap slowly closes and only show the to the parent gap of 2Δ. Why it exactly closes to 2Δ we do not fully understand, but one explanation could be that one lead turn normal before the other, thus becoming a S-QD-N system. We furthermore retrieve the normal state Couloumb diamonds at 0.7 T in fig.35.d). We see this as a promising result as we want to be field resilient when doing spin qubit experiments. In addition to this, a proximitized quantum dot has not been shown in this platform ever before. Having field resilient proximitized quantum dots could potentially be an avenue to explore. Since having an elongated proximitized dot, acting as a coupler instead of a full superconducting island as we are doing now, would yield more on site tune-ability [58].

5.1.7 Summary

We demonstrated that we could fabricate superconducting nanostructures in Ge/SiGe using annealed platinum. We were furthermore able to tune an SNS junction between different transparencies and see possible signatures of a super current. We saw a promising and large magnetic field robustness as well as multiple Andreev reflections. We demonstrated hybridize a quantum dot with neighbouring superconductors. We were however not able to create a superconducting island due to fabrication errors, although we saw transport over the 400 x 50 nm strip shorted to the open lead. We were finally able to tune a first ever Ge/SiGe heterostructure - PtSiGe proximitized dot. This round of fabrication had minimal gate electrode leakage caused by wirebonding, the gate electrode leakage present was however attributed to a too thin ALD layer of 5 nm.

6 Conclusion

6.1 Conclusion

We thus conclude our work by summing up what we have done. We have designed and fabricated a device which shows crucial components to realize a superconducting island quantum dot coupler. We demonstrated single hole occupancy in Ge/SiGe quantum dots by forming sensor dots, single quantum dots and double quantum dots. We performed DC charge sensing with and without compensation techniques, as well as RF-reflectomery charge sensing. Furthermore, we fabricated nano-scale PtSiGe Superconducting structures that exhibit superconductor-semiconductor physics such as a superconducting gap, as well as a zero bias peak within the gap, attributed to a possible supercurrent. We also observe higher order MAR processes, indicating a SN interface capable of coherent processes. We furthermore managed to combine semiconductor dots and group IV superconductors by measuring hybrid behaviour in a single quantum dot using RF reflectometry and a fast operated gate electrodes. We managed to solve and mitigate crucial fabrication issues, namely wirebond induced gate leakage and prolonged HF etching as well as annealing of nanostructures. We however still have a long way to go if we are to realize the full coupler structure proposed, as we we need to demonstrate even odd occupancy for a superconducting island, tune and operate spin qubits as well as performing spin to charge conversion read out. And last but not least, assembling an entire device where all subcomponents work.

6.2 Outlook and next steps

Immediate next steps would include demonstrating a cooper pair box island capable of even-odd filling as well as demonstrating tuneability of the superconducting island in conjunction with fast gate electrode operation and actually assembling a full device. The Ge/SiGe platform has so far proven to be relatively easy to incoorporate with the superconducting amalgamate PtSiGe. The ability to couple very small footprint superconductors with a semiconductor that has high mobilities is rather unique, and could be used to fractional quantum hall experiments using superconductors, which previously has not been possible before.

References

[1] Martin Leijnse and Karsten Flensberg. “Coupling Spin Qubits via Superconductors”. In: Phys. Rev. Lett. 111 (6 Aug. 2013), p. 060501. DOI: 10.1103/PhysRevLett.111.060501.

[2] Alberto Tosato et al. “Hard superconducting gap in germanium”. In: Communications Materials 4.1 (Apr. 2023). DOI: 10.1038/s43246-023-00351-w.

[3] Yuri I. Manin. Computable and uncomputable (In Russian - Vychislimoe i nevychislimoe. Sovetskoye Radio, 1980.

[4] ”C. H. Bennett and G. Brassard.”. “"Quantum cryptography: Public key distribution and coin tossing"”. In: vol. 175. In Proceedings of IEEE International Conference on Computers, Systems and Signal Processing. IEEE, New York, 1984.

[5] David Deutsch. “Quantum theory, the Church Turing principle and the universal quantum computer”. In: The Royal Society of London. A. Mathematical and Physical Sciences 400 (1985), pp. 117–97.

[6] David Deutsch and Richard Jozsa. “Rapid solution of problems by quantum computation”. In: Proceedings of the Royal Society of London - Series A: Mathematical and Physical Sciences 439.1907 (1992), pp. 553–558. DOI: 10.1098/rspa.1992.0167.

[7] Daniel R. Simon. “On the Power of Quantum Computation”. In: SIAM Journal on Computing 26.5 (1997), pp. 1474–1483. DOI: 10.1137/S0097539796298637.

[8] Peter W. Shor. “Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer”. In: SIAM Journal on Computing 26.5 (Oct. 1997), pp. 1484–1509. DOI: 10.1137/s0097539795293172. URL: https://doi.org/10.1137percent2Fs0097539795293172.

[9] Seth Lloyd. “Universal Quantum Simulators”. In: Science 273.5278 (1996), pp. 1073–1078. DOI: 10.1126/science.273.5278.1073.

[10] David P. DiVincenzo. “The Physical Implementation of Quantum Computation”. In: Fortschritte der Physik 48.9-11 (Sept. 2000), pp. 771–783.

[11] M.A. Nielsen and I.L. Chuang. Quantum Computation and Quantum Information: 10th Anniversary Edition. Cambridge University Press, 2010.

[12] Morten Kjaergaard et al. “Superconducting Qubits: Current State of Play”. In: Annual Review of Condensed Matter Physics (2019).

[13] Colin D. Bruzewicz et al. “Trapped-ion quantum computing: Progress and challenges”. In: Applied Physics Reviews 6.2 (May 2019). DOI: 10.1063/1.5088164.

[14] Loïc Henriet et al. “Quantum computing with neutral atoms”. In: Quantum 4 (Sept. 2020), p. 327. DOI: 10.22331/q-2020-09-21-327.

[15] Sergei Slussarenko and Geoff J. Pryde. “Photonic quantum information processing: A concise review”. In: Applied Physics Reviews 6.4 (Oct. 2019), p. 041303. ISSN: 1931-9401. DOI: 10.1063/1.5115814.

[16] Guido Burkard et al. Semiconductor spin qubits. June 2023. DOI: 10.1103/RevModPhys.95.025003.

[17] Peter Stano and Daniel Loss. “Review of performance metrics of spin qubits in gated semiconducting nanostructures”. In: Nature Reviews Physics 4.10 (Aug. 2022), pp. 672–688. DOI: 10.1038/s42254-022-00484-w.

[18] Jun Yoneda et al. “A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%”. In: Nature Nanotechnology 13.2 (Dec. 2017), pp. 102–106. DOI: 10.1038/s41565-017-0014-x.

[19] W. I. L. Lawrie et al. “Simultaneous single-qubit driving of semiconductor spin qubits at the fault-tolerant threshold”. In: Nature Communications 14.1 (June 2023), p. 3617. ISSN: 2041-1723. DOI: 10.1038/s41467-023-39334-3. URL: https://doi.org/10.1038/s41467-023-39334-3.

[20] L. M. K. Vandersypen et al. “Interfacing spin qubits in quantum dots and donors-hot, dense, and coherent”. In: npj Quantum Information 3.1 (Sept. 2017). DOI: 10.1038/s41534-017-0038-y.

[21] Cécile X. Yu et al. “Strong coupling between a photon and a hole spin in silicon”. In: Nature Nanotechnology (Mar. 2023). DOI: 10.1038/s41565-023-01332-3.

[22] Veit Langrock et al. “Blueprint of a Scalable Spin Qubit Shuttle Device for Coherent Mid-Range Qubit Transfer in Disordered $Si/SiGe/SiO_2$”. In: PRX Quantum 4 (2 Apr. 2023), p. 020305. DOI: 10.1103/PRXQuantum.4.020305.

[23] Maria Spethmann et al. High-fidelity two-qubit gates of hybrid superconducting-semiconducting singlet-triplet qubits. 2023. arXiv: 2304.05086 [quant-ph].

[24] M. Lodari et al. “Lightly strained germanium quantum wells with hole mobility exceeding one million”. In: Applied Physics Letters 120.12 (Mar. 2022), p. 122104. ISSN: 0003-6951. DOI: 10.1063/5.0083161.

[25] W. I. L. Lawrie et al. “Spin Relaxation Benchmarks and Individual Qubit Addressability for Holes in Quantum Dots”. In: Nano Letters 20.10 (Aug. 2020), pp. 7237–7242. DOI: 10.1021/acs.nanolett.0c02589.

[26] T. Ihn. Semiconductor Nanostructures: Quantum States and Electronic Transport. OUP Oxford, 2010.

[27] Ch.J. Raub et al. “Superconductivity of some new Pt-metal compounds”. In: Journal of Physics and Chemistry of Solids 24.9 (1963), pp. 1093–1100. ISSN: 0022-3697.

[28] W. I. L. Lawrie et al. “Quantum dot arrays in silicon and germanium”. In: Applied Physics Letters 116.8 (Feb. 2020). 080501. ISSN: 0003-6951. DOI: 10.1063/5.0002013.

[29] Anasua Chatterjee et al. “Semiconductor qubits in practice”. In: Nature Reviews Physics 3.3 (Feb. 2021), pp. 157–177. DOI: 10.1038/s42254-021-00283-9.

[30] Giordano Scappucci et al. “The germanium quantum information route”. In: Nature Reviews Materials 6.10 (Oct. 2021).

[31] A. Stockklauser et al. “Strong Coupling Cavity QED with Gate-Defined Double Quantum Dots Enabled by a High Impedance Resonator”. In: Phys. Rev. X 7 (1 Mar. 2017), p. 011030. DOI: 10.1103/PhysRevX.7.011030.

[32] X. Mi et al. “Circuit quantum electrodynamics architecture for gate-defined quantum dots in silicon”. In: Applied Physics Letters 110.4 (Jan. 2017), p. 043502. ISSN: 0003-6951. DOI: 10.1063/1.4974536.

[33] J. M. Luttinger and W. Kohn. “Motion of Electrons and Holes in Perturbed Periodic Fields”. In: Phys. Rev. 97 (4 Feb. 1955), pp. 869–883. DOI: 10.1103/PhysRev.97.869.

[34] G.L. Bir and G.E. Pikus. Symmetry and Strain-induced Effects in Semiconductors. A Halsted Press book. Wiley, 1974. ISBN: 9780470073216.

[35] E. Marcellina et al. “Spin-orbit interactions in inversion-asymmetric two-dimensional hole systems: A variational analysis”. In: Phys. Rev. B 95 (7 Feb. 2017), p. 075305. DOI: 10.1103/PhysRevB.95.075305.

[36] W. G. van der Wiel et al. “Electron transport through double quantum dots”. In: Rev. Mod. Phys. 75 (1 Dec. 2002), pp. 1–22.

[37] Henrik Bruus and Karsten Flensberg.
Many-body quantum field theory in condensed matter physics: an introduction. English. United Kingdom: Oxford University Press, 2003.

[38] Michael Tinkham. Introduction to Superconductivity. 2nd ed. Dover Publications, June 2004. ISBN: 0486435032.

[39] M. Octavio et al. "Subharmonic energy-gap structure in superconducting constrictions". In: Phys. Rev. B 27 (11 June 1983), pp. 6739–6746. DOI: 10.1103/PhysRevB.27.6739.

[40] K. Flensberg, J. Bindslev Hansen, and M. Octavio. "Subharmonic energy-gap structure in superconducting weak links". In: Phys. Rev. B 38 (13 Nov. 1988), pp. 8707–8711. DOI: 10.1103/PhysRevB.38.8707.

[41] M. Kjaergaard et al. "Transparent Semiconductor-Superconductor Interface and Induced Gap in an Epitaxial Heterostructure Josephson Junction". In: Phys. Rev. Appl. 7 (3 Mar. 2017), p. 034029. DOI: 10.1103/PhysRevApplied.7.034029.

[42] David J Griffiths. Introduction to electrodynamics. Pearson, 2013.

[43] Guido Burkard et al. "Superconductor–semiconductor hybrid-circuit quantum electrodynamics". In: Nature Reviews Physics 2.3 (Jan. 2020), pp. 129–140.

[44] Jirovec.D Et at. "A singlet-triplet hole spin qubit in planar Ge". In: Nature Materials 20 (Aug. 2021), pp. 1106–1112.

[45] Véronique Cremers, Riikka L. Puurunen, and Jolien Dendooven. "Conformality in atomic layer deposition: Current status overview of analysis and modelling". In: Applied Physics Reviews 6.2 (Apr. 2019), p. 021302. ISSN: 1931-9401. DOI: 10.1063/1.5060967.

[46] K Kanaya and S Okayama. "Penetration and energy-loss theory of electrons in solid targets". In: Journal of Physics D: Applied Physics 5.1 (Jan. 1972), p. 43. DOI: 10.1088/0022-3727/5/1/308.

[47] Pobell .F. Matter and Methods at Low Temperatures. Springer, Berlin, Heidelberg., 1996.

[48] D. J. Reilly et al. "Fast single-charge sensing with a rf quantum point contact". In: Applied Physics Letters 91.16 (Oct. 2007), p. 162101.

[49] Véronique Cremers, Riikka L. Puurunen, and Jolien Dendooven. "Conformality in atomic layer deposition: Current status overview of analysis and modelling". In: Applied Physics Reviews 6.2 (Apr. 2019), p. 021302. ISSN: 1931-9401. DOI: 10.1063/1.5060967.

[50] David M Pozar. Microwave engineering; 3rd ed. Hoboken, NJ: Wiley, 2005.

[51] C. H. Yang et al. "Dynamically controlled charge sensing of a few-electron silicon quantum dot". In: AIP Advances 1.4 (Oct. 2011), p. 042111. ISSN: 2158-3226. DOI: 10.1063/1.3654496.

[52] Martin Leijnse and Karsten Flensberg. "Coupling Spin Qubits via Superconductors". In: Phys. Rev. Lett. 111 (6 Aug. 2013), p. 060501. DOI: 10.1103/PhysRevLett.111.060501. URL: https://link.aps.org/doi/10.1103/PhysRevLett.111.060501.

[53] Sandor Caplan and Gerald Chanin. "Critical-Field Study of Superconducting Aluminum". In: Phys. Rev. 138 (5A May 1965), A1428–A1433. DOI: 10.1103/PhysRev.138.A1428.

[54] Jie Shen et. al. "Parity transitions in the superconducting ground state of hybrid InSb–Al Coulomb islands". In: Nature Communications 9.1 (Nov. 2018). DOI: 10.1038/s41467-018-07279-7.

[55] Silvano De Franceschi et al. "Hybrid superconductor–quantum dot devices". In: Nature Nanotechnology 5.10 (Oct. 2010), pp. 703–711. ISSN: 1748-3395. DOI: 10.1038/nnano.2010.173.

[56] Eduardo J. H. Lee et al. "Spin-resolved Andreev levels and parity crossings in hybrid superconductor–semiconductor nanostructures". In: Nature Nanotechnology 9.1 (Dec. 2013), pp. 79–84. DOI: 10.1038/nnano.2013.267.

[57] Anders Jellinggaard et al. "Tuning Yu-Shiba-Rusinov states in a quantum dot". In: Phys. Rev. B 94 (6 Aug. 2016), p. 064520. DOI: 10.1103/PhysRevB.94.064520. URL: https://link.aps.org/doi/10.1103/PhysRevB.94.064520.

[58] Alberto Bordin et al. Crossed Andreev reflection and elastic co-tunneling in a three-site Kitaev chain nanowire device. 2023. arXiv: 2306.07696 [cond-mat.mes-hall].

A Appendix A - Recipes

A.1 Markers

- Preparation of bare chip - 10 min Acetone soak, sonicate 5 min in IPA. Blowdry 1 min with N^2 gas.
- Ash 4 min in O_2 Atmosphere.
- Dry 2 min on 115 C° hotplate.
- Spin coat CZAR13, 4000RPM for 60s. Bake 150 s on 185 C° hotplate
- Exposure 125 kV Elionix E-beam lithography system - 10 nA with a dose of 260 $\mu C/cm$ using 260nm ZEP520 on Si PEC.
- Development - 50 s Gentle stirring in Amyl-Acetate (Pentyl-Amyl-acetate) followed by 1 min IPA rinse to stop development.
- Ash 60 s in O_2 Atmosphere
- Deposition AJA2 - To avoid excess baking of the resist due to thermal radiation, the whole stage is masked with Aluminum foil except for a square in the middle dedicated for the chip. Furthermore the current is ramped with 1mA pr. 2 s. We then deposit a 5 nm Titanium sticking layer, followed by 40 nm Platinum. Upon ramp down the stage is turned away from the evaporation target.
- Liftoff - Place in Di-Oxolane for 2 hrs. Proceed liftoff with sonication at lowest power and higest frequency for 5 min, transfer to new Di-Oxolane and repeat.
- Rinse in IPA, transfer to a small beaker of IPA inspect with optical microscope while submerged in IPA. If Resist remains, sonicate in Di-oxolane at highest frequency and lowest power for 1 1, repeat inspection until clear of resist.

A.2 PtGeSi leads and islands

- Spin coat PMMA2 resist, 4000 RPM for 60s, bake 90 s at 185 C°.
- Exposure with Elionix 125kV E-beam lithography system, 0.1 nA with a dose of 710 $\mu C/cm^2$ using 100nm PMMA on Si PEC.
- Development - Gently stirred in 60 s MBIK, rinse 60 s in IPA to stop development.

- Postbake at 100 C° for 20 s.
- Remove substrate oxide cap - 10 s HF (Hydroflouric acid) followed by 2 times 10 s MQ rinse in 2 seperate MQ beakers. finish with a 5 s IPA dip.
- Transfer to AJA metal evaporation system in less than 10min. To avoid excess baking of the resist due to thermal radiation, the whole stage is masked with Aluminum foil except for a square in the middle dedicated for the chip. Furthermore the current is ramped with 2mA pr. 2 s. Deposit 15nm of Pt. Upon ramp down, the stage is turned away from the evaporation target.
- Liftoff - Place in Di-Oxolane for 2 hrs. Proceed liftoff with sonication at lowest power and higest frequency for 5 min, transfer to new Di-Oxolane and repeat.
- Rinse in IPA, transfer to a small beaker of IPA inspect with optical microscope while submerged in IPA. If Resist remains, sonicate in Di-oxolane at highest frequency and lowest power for 1 1, repeat inspection until clear of resist.
- Diffusion - Bake for 15 min at 400° in RTA (Rapid Thermal Annealer) in an Argon atmosphere.

A.3 Bonding buffers

- Spin coat two layers of CZAR13 resist, 4000 RPM for 45 s, bake first layer for 60 s at 185 C°, and the second layer for 120 s at 185 C°.
- Exposure with 125 kV Elionix E-beam lithography system - 10 nA with a dose of 420 $\mu C/cm^2$
- Development - 60 s Gentle stirring in Amyl-Acetate (Pentyl-Amyl-acetate) followed by 1 min IPA.
- Deposition - 200 nm SiO_2, followed by 10 nm Ti, again followed by 40 nm SiO_2 AJA evaporation system. Spreading the electron beam significantly.
- Liftoff - Place in Di-Oxolane for 2 hrs. Proceed liftoff with sonication at lowest power and higest frequency for 5 min, transfer to new Di-Oxolane and repeat.
- Rinse in IPA, transfer to a small beaker of IPA inspect with optical microscope while submerged in IPA. If Resist remains, sonicate in Di-oxolane at highest frequency and lowest power for 1 1, repeat inspection until clear of resist.

A.4 Paladium gates

- Spin coat CZAR4 resist, 4000 RPM for 60 s, bake 150 s at 185 C°.
- Exposure with 125 kV Elionix E-beam lithography system - 0.5 nA with a dose of 220 $\mu C/cm^2$ using a bias of -2nm for the first gate layer, and 0.5 nA with a dose of 240 $\mu C/cm^2$ for the second gate layer.
- Development - 50 s Gentle stirring in Amyl-Acetate (Pentyl-Amyl-acetate) followed by 1 min IPA.
- Ash 30 s in O_2 Atmosphere
- Deposition - 5 nm Titanium sticking layer, followed by 29 nm Palladium for the first gate layer, and 35nm palladium for the second gate layer using AJA metal evaporation system.
- Liftoff - Place in Di-Oxolane for 2 hrs. Proceed liftoff with sonication at lowest power and higest frequency for 5 min, transfer to new Di-Oxolane and repeat.
- Rinse in IPA, transfer to a small beaker of IPA inspect with optical microscope while submerged in IPA. If Resist remains, sonicate in Di-oxolane at highest frequency and lowest power for 1 1, repeat inspection until clear of resist.