MSc Thesis

Quantum point contacts with complex gate geometry in high-mobility GaAs

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Submitted: May 22, 2023

Acknowledgements

Abstract

In this study, we investigate the versatility of complex gate geometry quantum point contacts (QPCs) fabricated on GaAs/AlGaAs heterostructures, for enhanced control and manipulation of electron transport. By carefully designing and optimizing the QPCs, we aim to have precise control over key parameters, including channel length, type of confinement, disorder, and local electron density. This parameter exploration enables us to delve into fundamental phenomena in electron transport and expand our understanding of quantum confinement effects.

The primary objective of this project is to operate these complex QPC devices in the quantum Hall regime and employ them for tunneling experiments. In the quantum Hall regime, QPCs offer the unique capability to locally manipulate edge channels by controlling the tunnelling probability between counter-propagating edge channels. Moreover, the generalization of QPC designs holds promise for their integration as building blocks in more intricate devices, such as interferometers. The ability to fine-tune QPC parameters opens up opportunities for creating complex architectures and exploring novel transport phenomena.

This study focuses on the fabrication and characterization of two main complex gate geometries. By systematically investigating different QPC designs and their associated parameters, our goal is to gain deeper insights into how the confinement potential of QPCs influences their transport properties, especially in the quantum Hall regime. By understanding and controlling electron transport in QPCs, we can harness their potential for improved performance and explore interesting phenomena in the field of quantum devices.

Contents

List of Figures

Chapter 1

Introduction and Motivation

A good introduction to the motivation for this thesis project would be the statistical study carried out in [1]. Here, the researchers investigate the conductance properties of one-dimensional (1D) quantum wires. More specifically, they studied transport through 256 nominally identical split gates fabricated on the same GaAs/AlGaAs heterostructure chip. By using two multiplexers, they were able to isolate each of these split gates, and measure its transport properties. An important thing to note down is that all of these devices were measured in the same cooldown, under the same experimental conditions. Despite the devices being nominally identical, [1] and measured in exactly the same way and conditions, they did not exhibit the same behaviour.

Even though the main focus of this work is centered around variations in the 0.7 anomaly among these split gates, we can come to some important conclusions regarding the parameters that influence the transport properties of this ensemble of devices.

The researchers initially measured the 1D conductance curve for every split gate, as shown in Figure 1.1(a), and noted down two critical voltages for each channel, the definition voltage V_d, and the pinch off voltage V_p. The definition voltage V_d, is the gate voltage where the system goes from being two-dimensional (2D) to 1D and the ballistic channel is formed. The pinch off voltage is the voltage at which the split gate fully blocks the channel. Intuitively, we understand that both V_d and V_p must depend on the local electron density [2]. If the density is higher, the definition voltage would be more negative, as we would need to push harder to get rid of the extra electrons underneath the gates, and vice versa. Indeed the relation between the definition voltage and the electron density n_{2D} is the following:

$$|V_d| = \frac{edn_{2D}}{\epsilon} \tag{1.0.1}$$

where e is the electron charge, d is the distance from the surface to the 2DEG

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[1] All devices went through the same fabrication process, the design is the same, consequently they are expected to be nominally identical up to nanoscale variations due to fabrication.

and ϵ is the permittivity of the material between the surface and the 2DEG. A similar argument goes for the pinch off voltage. As seen in Figure 1.1(b), the definition voltage (and consequently the local electron density because of equation 1.0.1) varies significantly between the different split gate sites.
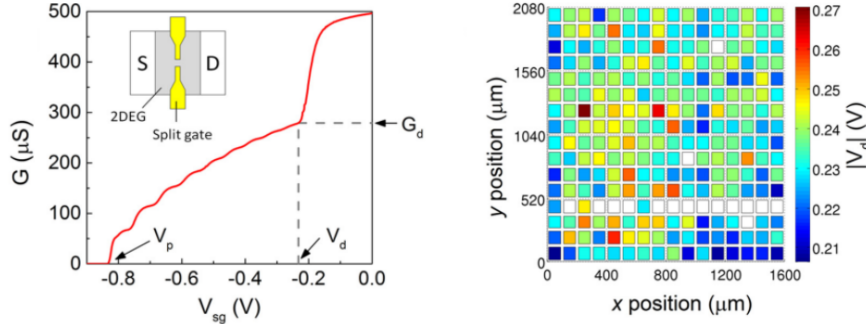
Figure 1.1: (a) Conductance across a split gate, as a function of the applied gate voltage on the split gate, inset: how one split gate device looks like. (b) Definition voltage extracted from (a), for each of the 256 split gate sites. Figures obtained from [1].

The main observation is that the devices exhibit different electrostatic behaviour, and this is primarily attributed to variations in the local 1D potential of each split gate. Several factors could contribute to the variability of the 1D potential among these devices, including nanoscale variations due to fabrication, or the presence of impurities and defects inside the channel.

The crucial aspect that motivates our work, is that not only the electrostatics, but more importantly the transport properties of QPCs are highly dependent on the specific characteristics of the 1D potential. We realize that numerous parameters play a role in determining the 1D potential. It follows naturally that we seek methods to manipulate these parameters, granting us ultimate control over the 1D potential profile of a ballistic channel.

A few groups have focused their efforts on doing that by adding gate complexity to their designs, to study the dependence of QPC transport properties to specific parameters. Some of these include the length [3], [4], potential shape [5] and local electron density of the channel [6]. It is worth noting that only recently have advances in electron beam lithography and deposition tools in academic cleanrooms enabled multi-layer complex gate geometries, with unprecedented control over the 2DEG potential.

One of the reasons why we would like to gain ultimate control over the potential, is to be able to shape it in a regime of interest, where some interesting phenomena appear. This could be to study many body physics effects such as the 0.7 anomaly, the zero bias anomaly or even realizing even denominator fractional quantum Hall states in the constriction. Such effects have proven to be sensitive to the specifics of the QPC potential.

In this work, we test two different complex gate geometry QPC [2] designs, which are fabricated on GaAs/AlGaAs heterostructures. With our designs, we opt to control parameters such as the length of the channel, the width of the constriction, as well as the type of confinement, the location of the channel (to have the ability to shift the constriction around in real space to avoid a possible defect or impurity), and finally the local electron density of the channel. By obtaining control over these parameters, one could study the phenomena mentioned above in much greater detail and extent.

A second reason as to why QPCs need to be generalized, is to use them as building blocks in more complex devices such as interferometers. In the quantum Hall regime, a QPC can locally manipulate edge channels by controlling the tunnelling probability between counter-propagating edge channels. The ultimate goal for this project is to operate our complex QPC devices in the quantum Hall regime and perform such tunneling experiments.

Chapter 2 provides an exploration of the theory surrounding quantum point contacts, the integer and fractional quantum Hall effects, and their combined study where QPCs are operated within the quantum Hall regime. This is followed by Chapter 3, which motivates and describes the two main designs that were fabricated and characterized in this thesis. These designs consist of the 3×3 pixelated channel design, as well as two simplified versions, that share similar properties to the 3×3. These are called the 3×1 and 3×2 designs.

In Chapter 4, we take a brief detour to delve into the technical aspects of this work, looking into the basics of fabrication and discussing some experimental methods. Finally, Chapters 5 and 6 present the measurement results obtained during the characterization of the designs mentioned in Chapter 3, providing an analysis of their properties.

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[2]Or 1D ballistic channel geometries in the variable length case.

Chapter 2

Theory

"Semiconductor technology has developed considerably during the past several decades. [...] One key ingredient of the LSI technology is the development of the lithography and microfabrication. The current minimum feature size is already as small as 0.2μm [...]. The next generation of devices is highly likely to show unexpected properties due to quantum effects and fluctuations"

These words were written 25 years ago [7]. The advancements in science and technology that happened ever since are impressive. Today, the minimum feature size that one can achieve with lithographic techniques has dropped to sub 10 nm, allowing us to probe physics that was inaccessible back then.

The combination of modern lithographic technology, and advancements in semiconductor heterostructure crystal growth technologies such as MBE, have produced a playground of very interesting structures that include quantum wires, quantum dots, antidots, interferometers and Quantum Point Contacts (QPCs). In such mesoscopic devices as they are called, the feature sizes are small[1], and we cannot deny the wavelike nature of electrons anymore. A number of fundamental quantum effects originate from this wavelike nature of electrons. For instance, there is the Aharonov-Bohm effect, the quantum Hall effects, and most importantly for us in this thesis is the quantization of conductance in integer steps of $2e^2/h$.

We are interested in systems where one can define a one-dimensional ballistic channel or a QPC. There are many platforms available to study QPCs, a relatively more novel example being graphene [8], but more relevant to this thesis is the two-dimensional electron gas of a GaAs/AlGaAs heterostructure, where QPCs where first demonstrated, i.e. [9].

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[1]Small enough to obey quantum mechanics, but not atomic physics.

2.1   Two-dimensional electron gas

An important system where quantum effects can be observed is the two-dimensional electron gas (2DEG). There are two basic systems where 2DEGs are realized.   One of them is the Si MOSFET (Metal Oxide Semiconductor Field-Effect Transistor). The other system, which is highly utilized in this work, is modulation doped GaAs/AlGaAs heterostructures, where an electron quantum well is formed close to the interface of these two materials. Note that 2DEGs of the latter kind represent the cleanest solid state platform available to experimentalists[2].
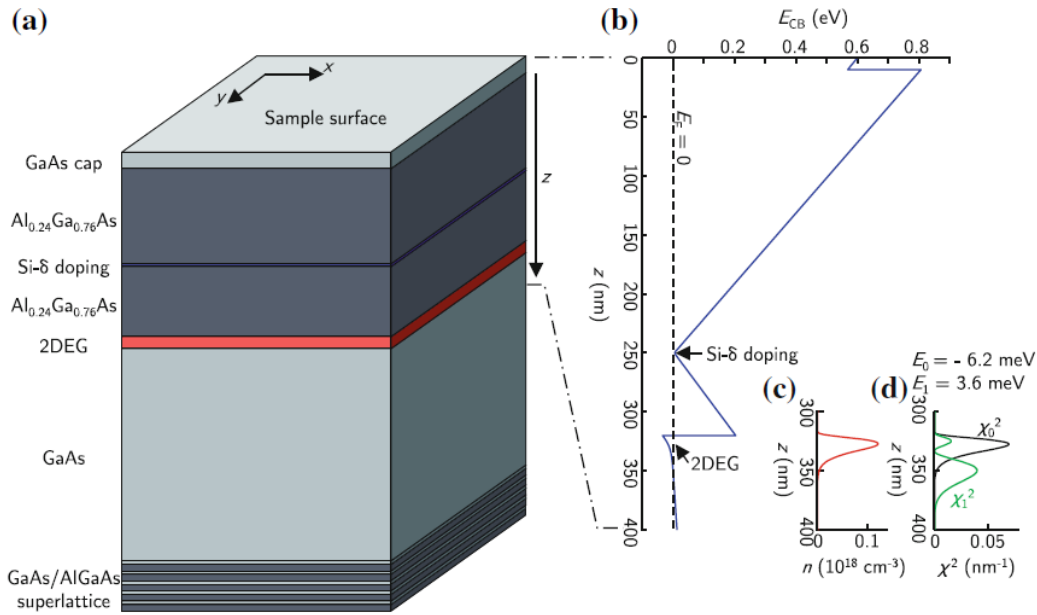
Figure 2.1: (a) Material stack for modulation doped GaAs/AlGaAs heterostructure, (b) Conduction band edge, obtained from numerical self-consistent solution of Schrödinger-Poisson equations, (c) Electron density and (d) square of two lowest energy subband wavefunctions, both as a function of z. Figure adapted from [10].

Suppose as in Figure 2.1(a), we have a type I [3] heterointerface, where the material on top is AlGaAs, and the bottom one is intrinsic GaAs. In combination with this heterointerface, a technique called modulation doping is used. A sheet (or thin volume) of Si donors is placed in the AlGaAs side, at a distance from the heterointerface between the two semiconductors. Because of the conduction band offset, it is energetically favorable for the donor electrons to move away from the AlGaAs side which has a bigger band gap, to the GaAs side with the smaller band gap.

Therefore, an internal electric field will be created, and directed from the non-neutralized donors in the AlGaAs to the additional electrons in the GaAs. This field is also responsible for the band bending shown in Figure 2.1(b). This

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[2]According to [10] published in 2015.

[3]As defined in [11].

continues until equilibrium is reached, where the Fermi levels line up. During this process, a triangular quantum well is formed in the GaAs layer. The electrons that are trapped in this potential well form the 2DEG, and should have a very high mobility in the x-y plane, since they move within the GaAs which is free of dopant impurities [4]. Evidently, electron mobilities in GaAs/AlGaAs are very high compared to MOS structures. Furthermore, by patterning metallic gates on the surface of such heterostructures, one can electrostatically control the shape of the 2DEG, as we will see in the following section.

2.2 Conductance quantization in quantum point contacts

QPCs are fundamental building blocks for many experiments in mesoscopic physics, not to imply that they are not interesting systems on their own; quite the opposite. One way to experimentally realize them is in 2DEGs. The 2DEGs that this work is based on are formed in GaAs/AlGaAs heterostructures. To form the simplest QPC, it is necessary to pattern two metallic gates on the surface of the heterostructure, forming a split gate structure shown in Figure 2.3(a). By applying a negative voltage on this pair of gates, the 2DEG underneath them is depleted from electrons, and what remains is a narrow channel connecting two large electron reservoirs. In 1988, two independent groups, Wharam et.al [12] and van Wees et al. [9], studied QPCs for the first time using a split gate in a GaAs 2DEG, at zero magnetic field. It was a surprising result that the conductance showed a step like behaviour, being quantized in integer steps of $2e^2/h$ with respect to the applied gate voltage on the split gate, as depicted in Figure 2.2.
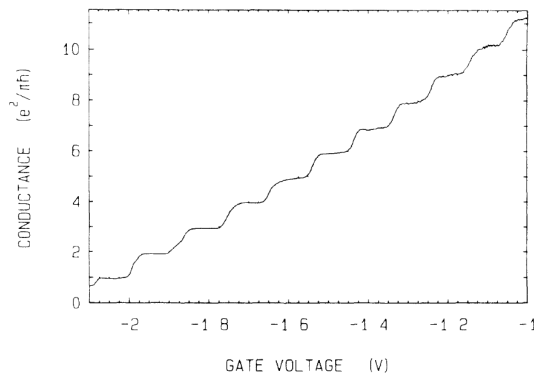
Figure 2.2: Conductance quantization in a simple split gate device on GaAs. Figure adapted from [9].

More than 30 years have passed since the first realization of QPCs, and they are still widely used and studied in experiments. In this section, we discuss the transport properties of a QPC at zero magnetic field, and see how a simple

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[4]It is well known that impurity scattering is one of the main limiting factors in carrier mobility, especially in low temperatures.

non-interacting electron model can explain the conductance quantization. Before
continuing, I should warn that this non-interacting electron model is not sufficient
to explain everything. Some anomalies appear in the conductance, such as the
famous 0.7 anomaly (see Figure 2.2), and cannot be described within this model.
Electron-electron interactions need to be considered, and a sufficient explanation
about the origin of this effect is still lacking. Some experimental attempts that
utilize more complex QPC structures to study the 0.7 anomaly are found in [5], [4].

(a)   (b)
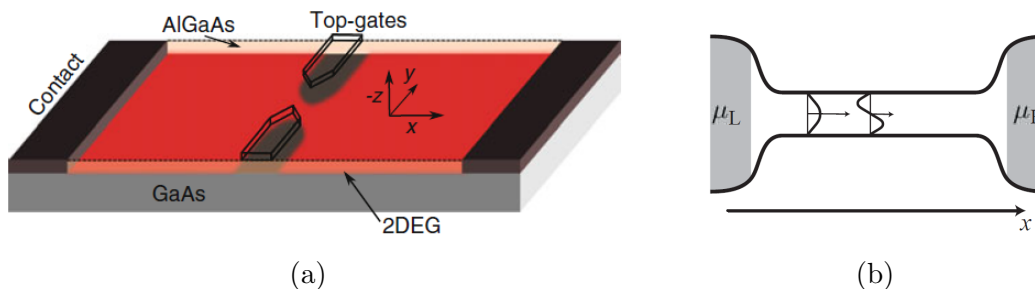
Figure 2.3: (a) GaAs heterostructure, with patterned metallic split gate on the
surface. By applying a negative voltage on the split gate, the 2DEG underneath
them is depleted, forming a 1D channel, (b) Modelling a QPC as a 1D channel
connected to two electron reservoirs. Figure (a) is adapted from [10], while (b) is
taken from [11].

We can model a quantum point contact as a one dimensional channel that
connects two electron reservoirs, with corresponding chemical potentials μ_L to the
left and μ_R to the right, as depicted in Figure 2.3(b).

To observe conductance quantization, the first condition is that the channel
should be sufficiently narrow. In other words, the width should be comparable to
the Fermi wavelength for electrons, $w \sim \lambda_F$, such that quantization can occur in the
y-direction indicated in Figure 2.3(a). The number of transverse quantized modes
that can fit in the channel at any given width, is exactly equal to the integer N that
precedes the conductance quantum of $2e^2/h$.

$$G = N\frac{2e^2}{h} \tag{2.2.1}$$

With the first condition we satisfy the *1D* in *1D ballistic transport*. To also
satisfy the word ballistic, the electrons need to travel without any energy loss in
the x-direction. This brings us to the second condition, which is that the mean free
path of electrons l_e[5], must be much larger than the length of the channel, $L \ll l_e$,
such that electrons travelling from one reservoir to the other will not experience any
inelastic collisions inside the wire.

The following ansatz is considered for the wavefunction [11]:

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[5]The average distance an electron can travel before scattering off impurities or defects.

$$\psi_{n,\mathbf{k}}(\mathbf{r}) = \chi_n(y)\frac{1}{\sqrt{L}}\exp^{ik_x x} \tag{2.2.2}$$

In equation 2.2.2, condition one for quantization in the y-direction is represented by the transverse modes of the wire $\chi_n(y)$[6]. The second condition of long mean free path is included in the assumption that the x-direction is infinitely long, and electrons travel as plane waves. The energy dispersion along the x-direction is assumed to be parabolic:
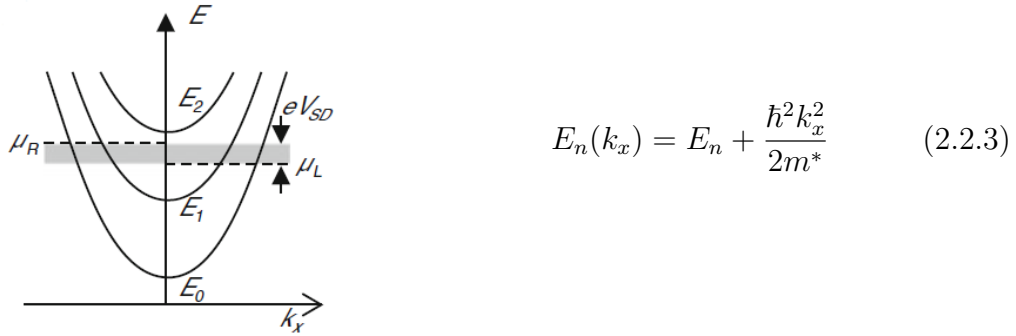
Figure 2.4: Parabolic dispersion as a function of k_x.

$$E_n(k_x) = E_n + \frac{\hbar^2 k_x^2}{2m^*} \tag{2.2.3}$$

where E_n is the energy of the nth subband due to quantization in the y-direction. Suppose a voltage bias $|e|V_{SD} = \mu_R - \mu_L$ is applied between the left and right electron reservoirs. In this case, only the electrons with k_x inside the bias window will contribute to the current. Electrons originating from the reservoir to the left have a positive k_x and are called right movers, and similarly electrons coming from the right reservoir are left movers owning to their negative k_x. The goal is to calculate the current through the wire, created by the movement of these energetically available electrons.

The differential current density of mode n and wavevector k_x is written as:

$$d\mathbf{j}_{n,k_x}(\mathbf{r}) = -\hat{\mathbf{x}}g_s\frac{|e|}{h}|\chi_n(y)|^2\frac{\partial E_n(k_x)}{\partial k_x}dk_x \tag{2.2.4}$$

where g_s denotes spin degeneracy. To obtain the total current through the wire, we need to integrate over the left and right movers that are energetically allowed to move because they are included in the bias window. Note that a summation is also performed over all occupied modes n.

$$I_{tot} = \left(\sum_{n_{occ}}\int_{k_x>0}d\mathbf{j}_{n,k_x}\right) - \left(\sum_{n_{occ}}\int_{k_x<0}d\mathbf{j}_{n,k_x}\right) \tag{2.2.5}$$

[6]More strictly the term $\chi_n(y)$ should be $\chi_n(y,z)$ since we also have confinement in the z direction, however for simplicity let us assume that $\mathbf{r} = x\hat{x} + y\hat{y}$, since the z and x-y Hamiltonians are separable.

The electron reservoirs are described by the Fermi-Dirac distribution. Since the electrons that create the current originate from these reservoirs, they also obey the Fermi-Dirac distributions f_R, f_L of their corresponding mother reservoir. The integrals in 2.2.5 can be re-written with the integration to be over energy.

$$I_{tot} = g_s \frac{|e|}{h} \left(\sum_{n_{occ}} \int_{E_n}^{\infty} dE \left[(f_L(E - \mu_L) - f_R(E - \mu_R)) \right] \right) \qquad (2.2.6)$$

Finally, in the linear regime where the applied source-drain bias is very small ($|e|V_{SD} \ll K_B T$), the spin degeneracy is two, and at the zero temperature limit we come to the formula for conductance quantization.

$$G = \frac{I_{tot}}{V_{SD}} = 2\frac{e^2}{h}N, \qquad T \to 0 \qquad (2.2.7)$$

All the above are valid for transmission through an ideal quantum wire. Due to simplified assumptions, the energy eigenvalues E_n were independent of the spatial distribution of the wire. Realistically, this is not the case. Both the width and confinement potential are dependent on x, and the solutions to the Schrödinger equation become more complex. Now for the electrons in the bias window, there is a finite probability of transmission and reflection through the QPC. For both the left and right movers, there is a probability of transmission through the QPC, $T_n(E)$ and a corresponding probability for reflection $1 - T_n(E)$. After taking this into account, we come to another form for 2.2.7, the Landauer formula. Proof of equation 2.2.8 can be found in several textbooks [11],[10].

$$G = \frac{I_{tot}}{V_{SD}} = 2\frac{e^2}{h} \sum_n T_n(E_F), \qquad T \to 0 \qquad (2.2.8)$$

2.3 Quantum Hall effects

2.3.1 Integer Quantum Hall effect (IQHE)

"The birthday of the quantum Hall effect can be fixed very accurately. It was the night of the 4th to the 5th of February 1980 around 2 a.m. during an experiment at the High Magnetic Field Laboratory in Grenoble."[13]

Klaus von Klitzing's research at the time included characterization of the electronic transport of silicon field effect transistors. For this, Hall bar devices were provided by G.Dorda and M. Pepper. These 2DEG systems were cooled down to 4.2K and exposed to high magnetic fields [14]. The result can be summarized in one of the most famous experimental curves in condensed matter physics:
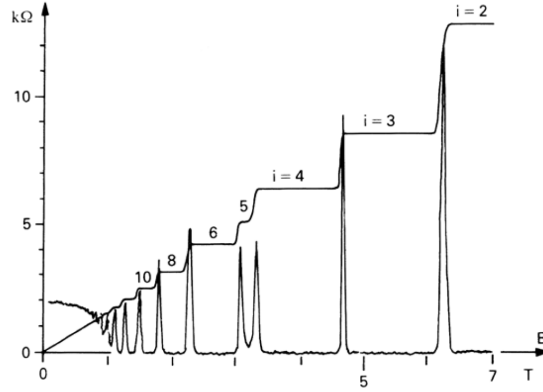
Figure 2.5: Integer quantum Hall effect discovery.

The transverse (or Hall) resistance exhibits a steplike behaviour at higher fields,

$$\rho_{xy} = \frac{1}{\nu}\frac{h}{e^2} \qquad (2.3.1)$$

where ν is an integer ($\nu = i$ in Figure 2.5). In the magnetic field regions where plateaus occur in ρ_{xy}, the longitudinal resistance ρ_{xx} settles to zero. Because of the two dimensional nature of the system, the resistance and conductance become 2×2 tensors. One can show that whenever the field value is such that the Hall resistance is parked on a plateau ν, the transverse Hall resistance and conductance are both zero simultaneously,

$$\rho_{xx} = \sigma_{xx} = 0, \quad \text{if } \rho_{xy} \neq 0 \qquad (2.3.2)$$

Vanishing conductance is characteristic of an insulating state. In turn, we would call a material with zero resistance a perfect conductor. We see that our intuition is not very helpful when trying to understand the high magnetic field behaviour of a 2DEG.

In the following, we will study the IQHE through the edge state picture. When the system has finite dimensions $L_x \times L_y$, it is found that the current going through the system is carried by counter-propagating edge states that intersect the Fermi level.

In the low magnetic field limit, in-plane electrons move in circles due to the perpendicular magnetic field. As the magnetic field is further increased, there is a point where an electron will only be able to perform few circles before scattering and losing all of it's momentum ($\omega_c \tau \gg 1$). The kinetic energy of the electron will then become quantized into discrete energy levels; the so-called Landau levels. To calculate them, one has to solve the Schrödinger equation for an electron in an external magnetic field:

$$\left(\frac{(\mathbf{p} + |e|\mathbf{A})^2}{2m^*}\right)\psi(x,y) = E\psi(x,y) \qquad (2.3.3)$$

Typically, a Landau gauge is chosen for the vector potential, $A_y = Bx\hat{y}$. Because the Hamiltonian commutes with the momentum operator in the y

direction, we can consider an Ansatz solution of the following form for the wavefunction:

$$\psi_k(x, y) = e^{iky} f_k(x) \tag{2.3.4}$$

The eigenvalue problem takes the final form:

$$\left(\frac{p_x^2}{2m^*} + \frac{1}{2} m^* \omega_c^2 \left(x + \frac{\hbar k}{|e|B} \right)^2 \right) f_k(x) = E f_k(x) \tag{2.3.5}$$

This Hamiltonian corresponds to a shifted harmonic oscillator in the x-direction, with oscillation centers $x_0 = -\hbar k / |e|B$. The eigenenergies of the problem represent the Landau levels, and are given by:

$$E_n = \hbar \omega_c (n + \frac{1}{2}) \tag{2.3.6}$$

where $n = 0, 1, 2...$ is the Landau level index. The wavefunction is described by the wavevector k. The Landau level energies are independent of k, this makes them highly degenerate. The degeneracy of the Landau levels n_L, is equal to the number of flux quanta that pierce through the system:

$$n_L = N_\Phi = \frac{\Phi}{\Phi_0} \tag{2.3.7}$$

where $\Phi_0 = h/e$ is defined as the flux quantum. Finally, the filling factor represents the ratio between the number of electrons in the system divided by the number of flux quanta:

$$\nu = \frac{N_e}{N_\Phi} \tag{2.3.8}$$

The Landau level description ignores the existence of physical boundaries, however the resistance behaviour observed in Figure 2.5 is a consequence of the system having a finite size. The confining potential causes the Landau levels to bend upwards towards the edge of the sample as shown in Figure 2.6(a).

Whenever the Fermi level lies in between two Landau levels, the bulk is insulating due to the presence of the gap in the bulk $\hbar \omega_c$. The edges on the other hand show a completely different behaviour. Because of the Landau level bending, each level that is below the Fermi level crosses the Fermi energy twice, once on each side of the sample. These two intersection points represent 1D conducting channels that emerge at the edges of the system. These two edge channels for each LL are counterpropagating at the opposite sides of the sample, and as they are separated by a macroscopic distance, backscattering is entirely absent. Since the bulk is insulating, no current can run through it, and in the edge picture, the current can only run through these edge channels.

The question we have answered so far is: Why do the R_{xy} plateaus have the integer value that they do? It is because that integer value corresponds to the number of LLs that intersect the Fermi energy, which in turns corresponds to how many conducting edge channels exist in the system. However, this picture does not

explain why resistance exhibits plateaus; and why these plateaus extend over a range
of magnetic field. To understand this we need to consider how disorder influences
the system.

(a)   (b)
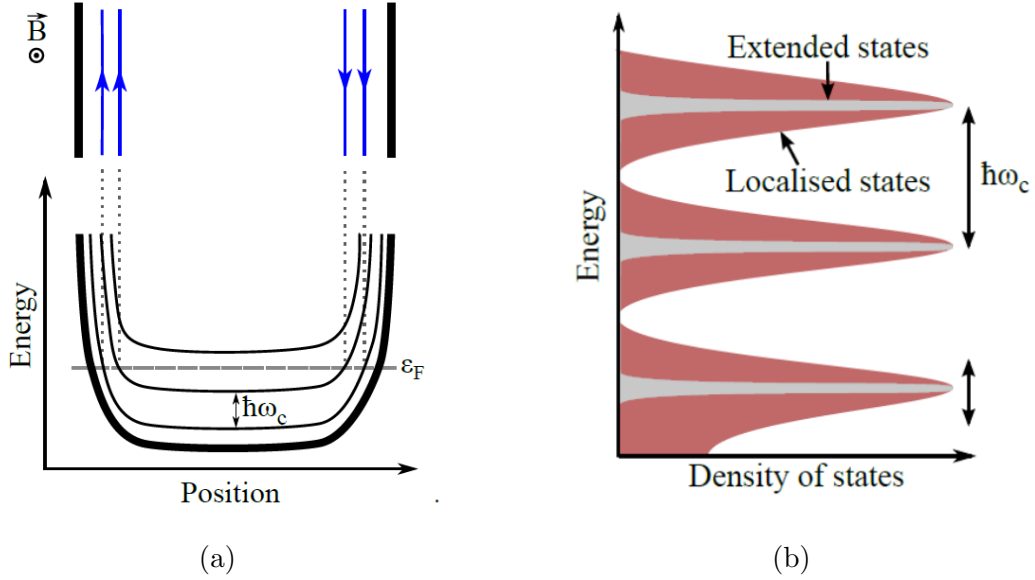
Figure 2.6: (a) Landau levels bend upwards due to the confinement potential of
the finite sample. Counterpropagating edge states are formed on both sides of the
sample, whenever the Fermi level intersects the LLs. (b) Landau levels broaden
because of disorder; the quantum states now comprise of extended states that carry
the current through the sample, and localised states. Figures adapted from [15].

We start from a free 2DEG, characterized by a continuous density of states
(DOS), resembling that of a metal. Subsequently, we introduce a perpendicular
magnetic field; this results in the DOS to become discrete, forming the LLs, which
at a first glance are assumed to be flat. However, this assumption does not accurately
reflect the complexity of the system in reality. Our samples are inherent to random
disorder, and in the presence of such disorder, the energy spectrum of the LLs
broadens. The quantum states of the system now comprise of extended and localised
states. Extended states spread through the sample, and carry the current across the
device. Localised states on the other hand are, well, localised. They are restricted in
some small region in space, usually trapped around maxima or minima of the spatial
potential that varies within the sample. Since these states cannot move, they do
not contribute to the current.

To understand how the plateaus are formed, consider the following: Suppose
that all extended states in a given LL are filled, and the magnetic field is decreased,
with fixed electron density in the system. The degeneracy of the LLs decreases, but
rather than jumping to the next LL, localised states in the tails of the DOS curve
are populated. Since these states do not contribute to the current, the resistance or
conductance does not change over a range of magnetic field, until the next extended
states are reached. For more details on the IQHE the reader is referred to [16] as a
qualitative source, and [17] for a deeper mathematical approach.

2.3.2   Fractional Quantum Hall effect (FQHE)

The fractional quantum Hall effect (FQHE), much like the IQHE, emerges in two-dimensional electron systems subject to a strong perpendicular magnetic field at low temperatures.   The difference between the IQHE and FQHE is that electron-electron interactions become important in the latter.

The strong interactions originate from the Coulomb repulsion between electron. Under normal circumstances, this interaction is weak, and the electrons behave as non-interacting particles.   In strong magnetic fields, the interaction energy between electrons becomes comparable to their kinetic energy. The strong interactions lead to the formation of correlated states, where the electrons organize themselves collectively to minimize the overall energy of the system.   These correlated states are characterized by the appearance of energy gaps, which correspond to the incompressible states observed in the FQHE.

In their experimental observations, the IQHE and FQHE are identical, except for the value of the quantized Hall resistance $R_{xy} = h/fe^2$, with the difference being that f is now a fraction. In 1982, Tsui, Stormer and Gossard [18] exposed their 2DEG to very high magnetic fields, aiming to force all electrons to the lowest LL. With their kinetic energy being quenched, it would be entirely the Coulomb repulsion determines their state.
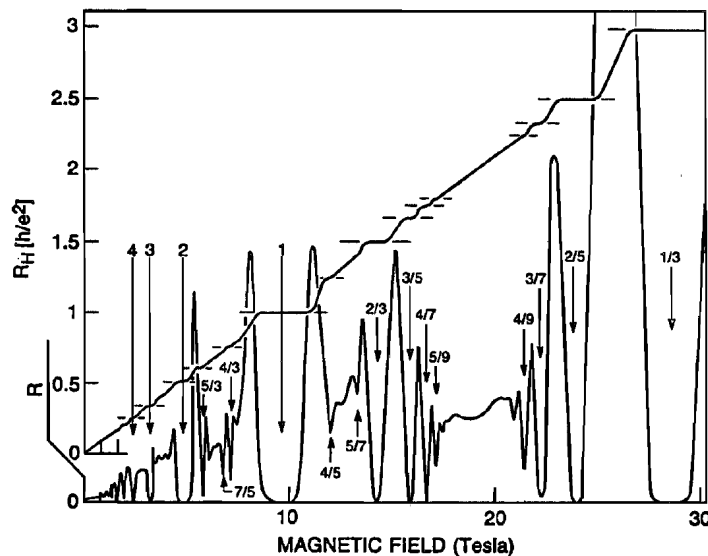
Figure 2.7: Fractional quantum Hall effect. Some integers and fractions are indicated in the longitudinal resistance minima. Adapted from [19].

One theoretical framework used to explain the FQHE is the composite fermion (CF) model proposed by Jain [20].

"The motivation for the CF theory came from the following observation: If you mentally erase all numbers in Fig. 1 (Figure 2.7 for us), you will notice that it is impossible to tell the FQHE from the IQHE." [21]

In this proposed unifying framework, each electron in the 2DEG binds to two magnetic flux quanta, transforming it into a composite particle, or a "composite fermion" (CF). In other words, it is suggested that fractional quantum Hall effect electrons can be understood as a manifestation of the integer quantum Hall effect of composite fermions.
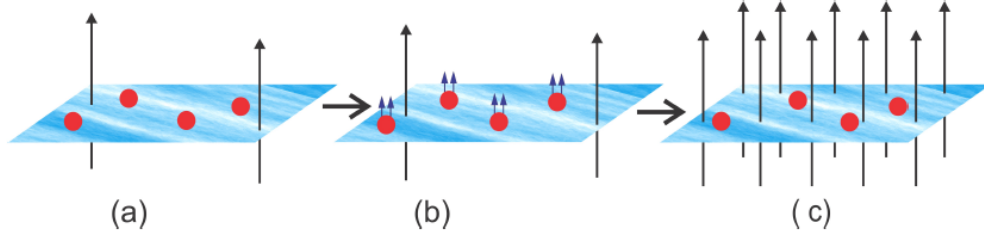
Figure 2.8: Deriving the FQHE from the IQHE through composite fermions. (a) Begin with an integer quantum Hall state at $\nu^* = n$, (b) Attach two magnetic flux quanta to each electron, to convert them to CFs, (c) Spread the flux quanta out to obtain electrons in a higher magnetic field. If the energy gap closes from (b) to (c) then a fractional quantum Hall state at $\nu = n/(2n+1)$ is formed. All quantities indicated by a star(*) correspond to CFs. Figure adapted from [21].

The intuitive idea that Figure 2.8 illustrates is as follows, where all quantities corresponding to CFs are indicated by a star (*). We begin with the IQHE with non interacting electrons, at $\nu^* = n$ in a magnetic field $B^* = \rho\Phi_0/\nu^*$, where ρ is the electron density. Then we attach two flux quanta to each electron, that now becomes a composite fermion. By adiabatically smearing the fluxes attached to the electrons, such that they become part of a unified magnetic field, we obtain electrons moving in an enhanced magnetic field $B = B^* + 2\rho\Phi_0$. This is identified as the real applied magnetic field, and as long as the energy gap closes during this transition, it implies that the filling factor takes the following values:

$$\nu = \frac{n}{2n+1} \tag{2.3.9}$$

Composite fermions form their own Landau-like levels, called Λ levels (ΛLs), in the reduced magnetic field, and fill ν^* of them. Thus the lowest Landau level effectively splits into these ΛLs. For more details on the FQHE the reader is referred to [22] for a review of the FQHE, and to [17] for a mathematical and in-depth approach.

2.4 Quantum point contacts in the quantum Hall regime

In section 2.2, we showed that at zero magnetic field, in a 1D ballistic channel, conductance is quantized in integer steps of $2e^2/h$. When a magnetic field is switched on, the conductance plateaus gradually become wider and flatter, as seen in Figure

2.9. When we enter the quantum Hall regime, the conductance plateaus are no longer a measure of transmitted transverse modes originating from a reservoir. The new transmission modes of the system are due to the formation of Landau levels. In the quantum Hall regime, whenever the Fermi level is parked in-between two LLs, the bulk is insulating, and the counterpropagating edge states are carrying the current across the sample. Thus, the only modes that are available are the edge states, and they must necessarily go through the QPC.
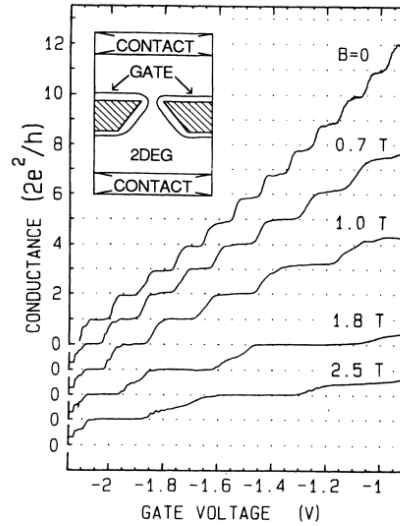
Figure 2.9: Effect of perpendicular magnetic field applied to a QPC, defined in a GaAs 2DEG. Figure adapted from [23].

At a constant magnetic field value, by making the gate voltage on the split gates of a QPC more negative, we can control the transmission and reflection of the edge channels, as is graphically shown in Figure 2.10. In Figure 2.10(a), there are two edge states ($\nu = 2$) in the system, and backscattering is suppressed because of the macroscopic spatial separation of these counterpropagating states. As the split gate voltage becomes more negative, the counterpropagating edge states come closer and closer, and backscattering is introduced. Further decreasing the gate voltage results in one of the edge states to be fully transmitted, while the other is fully backscattered. This of course is the easy cartoon example for integers. Things are more complicated when fractional states are included, where compressible and incompressible regions are formed within the channel. Some examples of such experiments, of QPCs in the fractional regime include [6], [24].
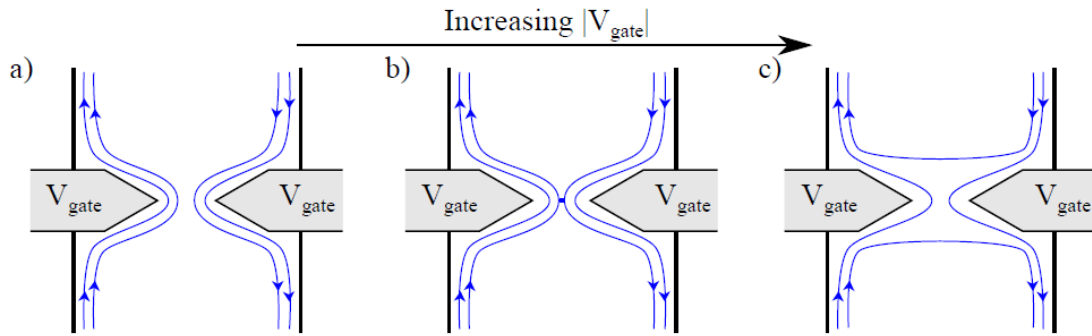
Figure 2.10: (a) Bulk parked at $\nu = 2$, where two edge states exist. (b) As the QPC gates become more negative, backscattering is introduced, (c) One of the edge states is fully backscattered, and the other is fully transmitted. Figure adapted from [15].

Chapter 3

Complex Gate Geometry QPC Designs

3.1 3×3 design motivation

The main focus of the project is to find complex gate geometry QPC [1] designs, that allow us to control all parameters that influence their transmission properties. Furthermore, in-depth understanding and precise control of QPC confinement and QPC transmission properties, are crucial for interference and tunneling experiments within the quantum Hall regime. Ultimately, our aim is to gain a thorough understanding of how to effectively tune the potential in this specific regime of interest.

As mentioned in Chapter 1, numerous parameters can potentially influence the transport properties of a QPC. While certain factors, such as nanoscale variations in gate fabrication, are beyond our control, we wish to control the rest. As a reminder, some of those include the length and width of the channel, channel density and potential shape, as well as disorder that has an unforeseen effect on the properties of the channel.

In theory, even a simple split gate has the potential to selectively allow certain states pass through it. As a consequence, it should have the ability to locally manipulate Hall edge channels, by controlling the tunnelling probability of the counterpropagating edge channels. While this is true for numerous influential studies conducted within the research community, it is important to note that it is not always the case.

It is not guaranteed that we can always see interesting fractional states in a simple split gate QPC. The reason is that with only two gates available, there are not enough parameters that we can experimentally vary to probe the system. This observation is highlighted in this study [6], where the $\nu = 3/2$ even denominator

---

[1]In the case of length tunable QPCs we can't call them QPCs anymore, a more correct term is quantum wires or 1D ballistic channels.

state is only observed in the device featuring a center gate for controlling the QPC potential, as illustrated in Figure 3.1. Conversely, it is absent in a simple split gate device fabricated on the same material. This is just an example that underlines the critical role of the QPC potential in realizing fractional Hall states.
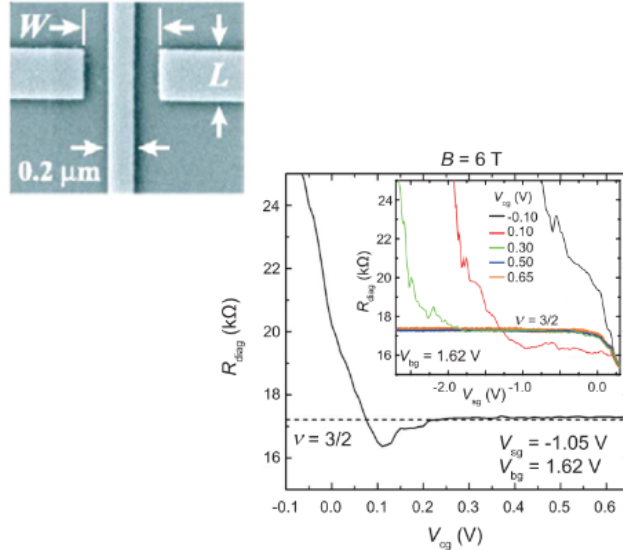
Figure 3.1: The top left corner shows the device, which is a split gate with an additional center gate, and the data plot shows that for positive center gate voltage, the diagonal resistance converges to the $\nu = 3/2$ state. Figures adapted from [6].

This inherent sensitivity of fractional edge states to QPC geometry, motivates us to create more knobs through gate complexity, that allow us to control the QPC potential. In the following sections, I introduce our initial design, which is referred to as the 3×3 design, and there are two generations of such devices. This thesis focuses on the investigation of the second generation of 3×3 devices.

3.1.1 First Generation: Single layer design

To motivate the second generation of the 3×3 devices, we look at the results from the first generation. The device shown in Figure 3.2 was fabricated and studied by Bertram Brovang and Torbjørn Rasmussen during their master's thesis work [25], [26]. This device consists of two distinct sets of gates: the outer gates, depicted in blue, which create a wide channel when subjected to highly negative voltages, and the remaining gates forming a 3 by 3 array known as pixels. The purpose of the pixels is to divide the large square channel into a grid-like arrangement of 9 gates. The goal of their thesis work was to implement an optimization algorithm, that autonomously tuned the pixels in the best voltage configuration, with conductance quantization as the optimization criterion.

An example of the voltage configuration that the algorithm converged to is found in Figure 3.2(b). It was very counter-intuitive how the final configuration of

voltages resulted to conductance quantization. They attributed this to the connector lines of the middle pixels, causing an effect that couldn't be fully comprehended.

The first design that the current thesis is concerned with is an evolution of this single layer design, and attempts to eliminate this connector problem. We will from now on refer to this design as "the Swiss cheese design" and it is described in the following section.

<table>
<tr><td>(a)</td><td>(b)</td></tr>
</table>
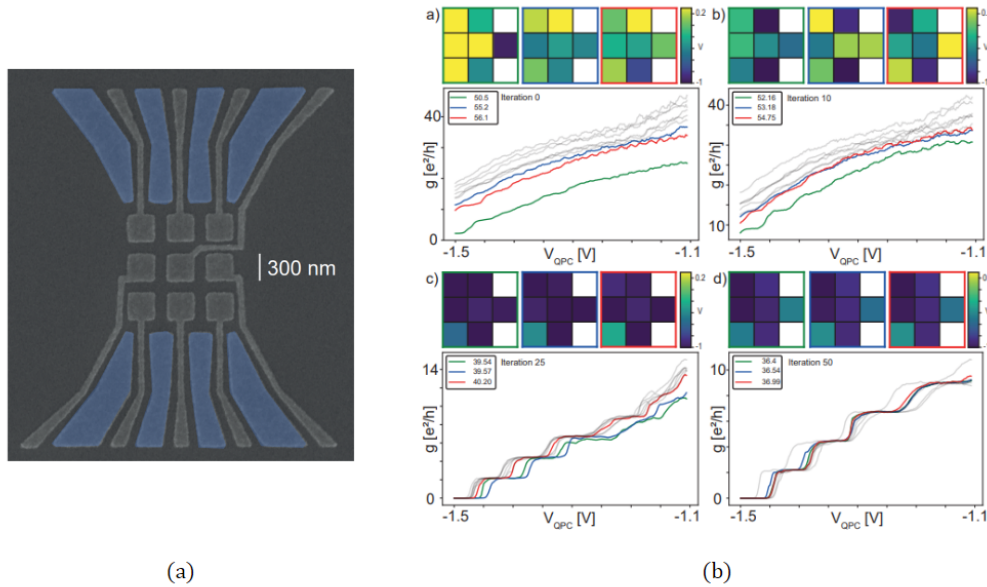
Figure 3.2: (a) False color SEM of single layer 3 by 3 design. The blue gates correspond to the outer gates that are negatively biased to form a channel, and the remaining 9 gates are called pixels, (b) Results from applying optimisation algorithm, both (a) and (b) adapted from [25].

3.1.2 Second Generation: Swiss cheese design

It is very hard to design a 3 by 3 grid-like array of gates in a single layer, without having the connector lines that route the middle row go through other pixels. As a result, when the middle row pixels are energized, the connectors will be as well, and this will have an effect on the operation of the rest of the pixels. For example, if a negative voltage is applied to the middle left pixel in Figure 3.2, then its connector line will block the 2DEG to the pixel below it. As a consequence, with the single layered design, the 9 pixels cannot be controlled independently as needed.

The obvious solution is to make these connectors as thin as possible, such that their effect could be minimized, but this causes practical problems in fabrication. Thinner gates below 30nm are very hard to consistently achieve in deep 2DEGs, because they tend to break [2]. This lowers the fabrication success yield, and

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[2]Tall resist is needed for deep 2DEGs, to fully cover the etched mesa and outer gates. This will become evident in Chapter 4. With tall resists, the aspect ratio has to be very big to achieve thin gates, and what happens is that very often the resist walls collapse.

ultimately, even if a perfect thin-connector device could be achieved in fabrication, the electric field of the connectors would still be experienced by the 2DEG. That is because the 2DEGs we use are quite deep, typically below 200nm, and the electric field lines of the connectors would spread to a bigger area by the time they reach the 2DEG.

We decided to try a different approach to solve this problem; this was to include an additional layer of gates in the design, that would effectively screen the middle row pixel connectors. The idea is taken from simple electrostatics, when we place a piece of metal over another, the electric field of the piece on top will be screened by the metal on the bottom, and thus the 2DEG laying underneath won't experience the electric field of the screened gates.

The first gate layer of the design can be found in Figure 3.3a, and it consists of three big gates. The top and bottom gates are called outer gates, and are used to form a channel. The middle gate is called the screening gate, and it has 9 holes[3], owning to the Swiss cheese name. This gate acts as a mask for the second layer of gates, and the 2DEG will only see any gate that falls inside a hole. A HfO_2 layer is then deposited, to electrically isolate the first layer from the second layer of gates, the pixel gates, which are shown in black in Figure 3.3b. The idea is that the connector lines are now screened by the screening gate, and the pixels can be operated independently.

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[3]The slits are there for liftoff purposes.
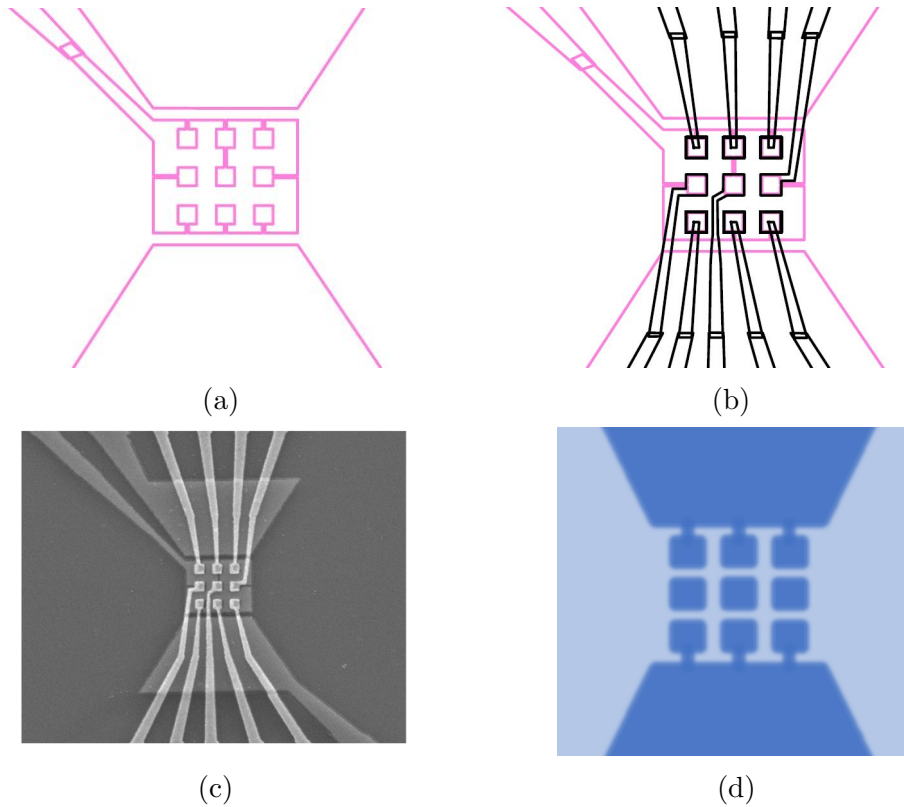
Figure 3.3: Swiss cheese design. (a) First gate layer, (b) Full design including both gate layers, (c) SEM of final device, (d) Qualitative picture of how the potential landscape is expected to look like at the 2DEG level, when the outer gates and pixel gates are activated, light blue is free 2DEG and dark blue are areas where the 2DEG is depleted.

To demonstrate the flexibility of this design, Figure 3.4 shows some examples of how some parameters can be controlled in operation. The length of the channel can be controlled by activating more or less pixels in any two rows, as shown in Figure 3.4a. The width can be chosen to be equal to the distance between a first row and third row pixel (or pixels), as shown in the left picture in Figure 3.4b, or between adjacent rows, in the case that D and G are used as one effective gate versus pixel A. The density or shape of the potential can also be manipulated, for instance by using pixels D and E in the example of Figure 3.4c. By making D and E positive, the saddle point potential is expected to become deeper, and the conductance plateaus more pronounced [27], [28].

Finally, the channel can be shifted around in space, as demonstrated in Figure 3.4d. There are measurement techniques [10] that allow us to visualize the potential landscape of the channel, by identifying clear signatures of disorder and localization. Through these kind of measurements, we can decide which channels are good or bad, and shift the channel accordingly.
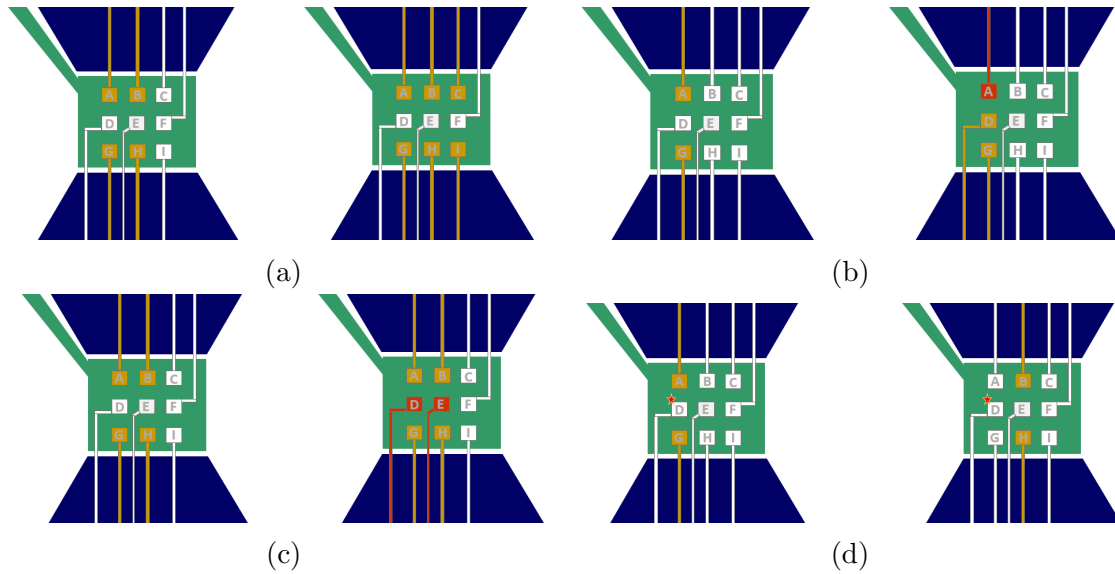
Figure 3.4: Demonstration of length, width, density and channel location control in operation. The outer gates (dark blue) are parked at a very negative value to form a big channel. The screening gate (green) is grounded. A white pixel is at 0V, while yellow and red means activated at a negative voltage. (a) Varying the length of the channel, (b) Changing the width, (c) Controlling the density of the channel, (d) Shifting the channel way from the defect/impurity (red star).

Figure 3.4 only includes some examples of the multiple gate configurations that can be achieved with this design, therefore this design seems to be promising in realizing more generalized and flexible quantum wires and QPCs. The first chip fabricated and measured in this thesis consisted of 6 Hall bar mesas, with a Swiss cheese device in the center of each mesa. The chip is called SCQPC∅, and results are discussed in chapter 5.
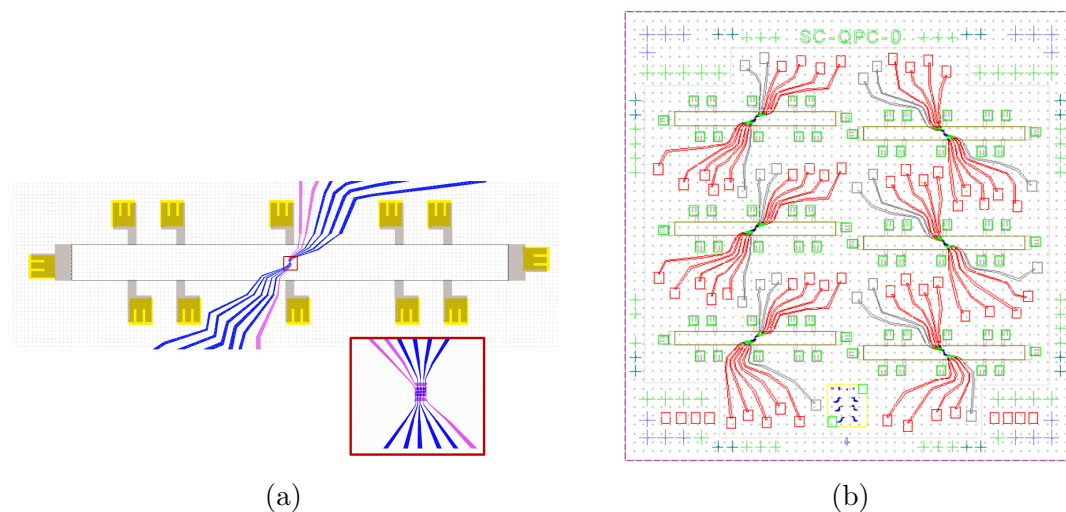
Figure 3.5: (a) Isolated Hall bar with Swiss cheese 3×3 design in the center, (b) SCQPC∅ chip layout.

3.2 3×1 and 3×2 designs

After measuring the Swiss cheese device of Figure 3.3, it was very clear that the screening gate had much more of an effect than expected. Even though some 1D channels could be formed (see Chapter 5), the device was unable to prove the point of the project, namely that we can control the 1D potential with a complex device better than with a simple split gate or split gate with a center gate.

However, the failure of the Swiss cheese device did not disprove the basic idea of using one layer of gates to screen away gate pieces that we don't want the 2DEG to see.

This led to another generation of devices, the 3×1 and 3×2 devices shown in figures 3.6 (a),(b). The potential we hope to get for these devices is shown in figures 3.6 (c),(d). The first layer purple gates are there for screening purposes, and again act as a mask for the second layer gates.

The inspiration for designing the 3×1 device is mostly to avoid disorder. To do this, the device has the functionality to laterally shift the channel to three positions. The 3×2 device is an evolution of the 3×1, that also allows for in-situ variation of the length of the channel.

Results and discussion of measurements performed on the 3×2 device can be found in Chapter 6.
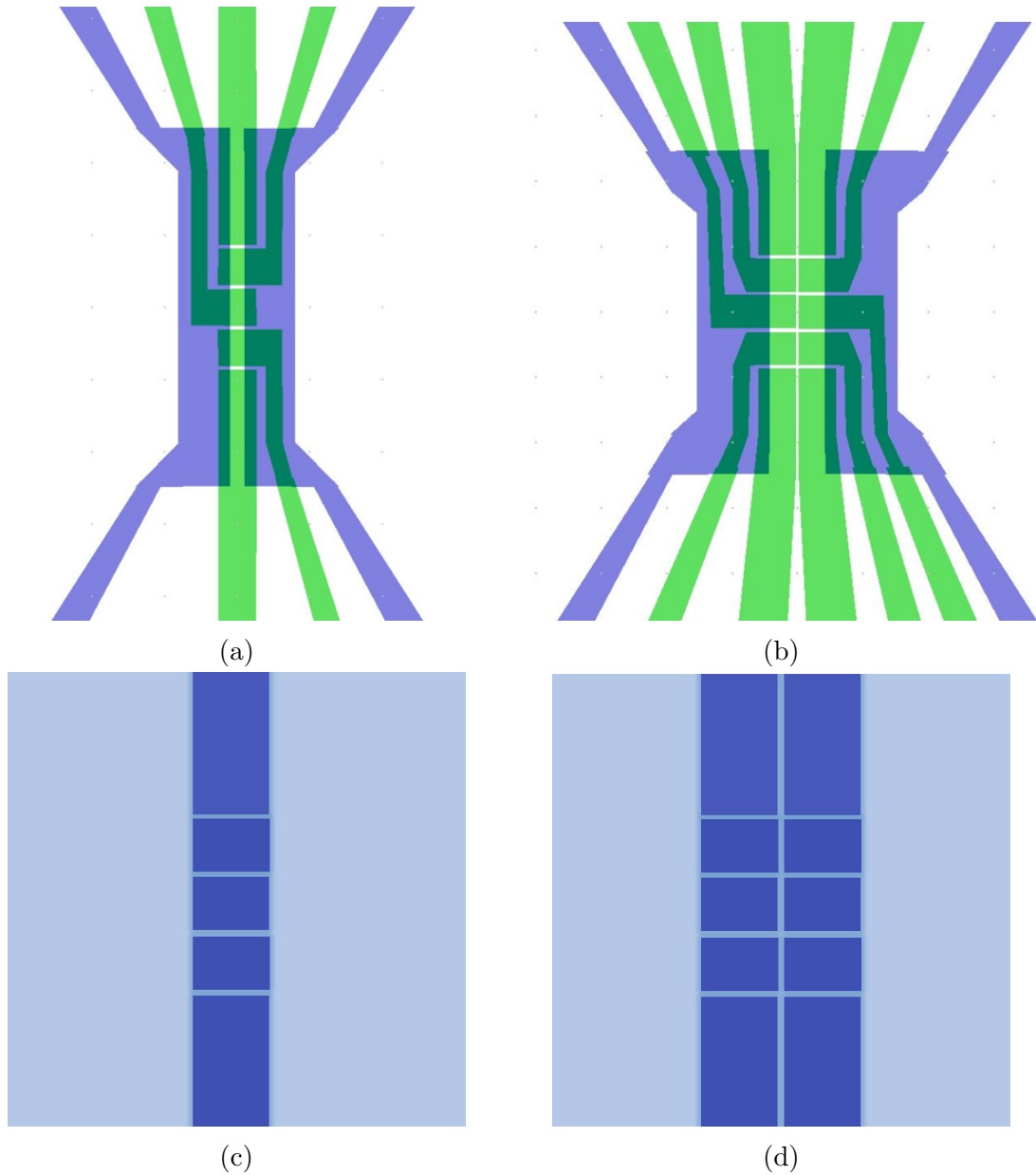
Figure 3.6: (a) 3×1 design and (b) 3×2 design. In both, the purple gates are in the first layer and green gates are in the second layer, (c) and (d) show an expected qualitative drawing of the potential landscape at the 2DEG level, for devices (a) and (b). Light blue is ungated 2DEG and dark blue is when the second layer gates are activated to a negative voltage.

3.3 Interferometer designs

The interferometer designs shown in this section were fabricated for the work done in thesis [29], and are not part of the current thesis. The QPC project that my thesis is concerned with was part of a bigger FQHE group, where interferometers were the other big branch of study.
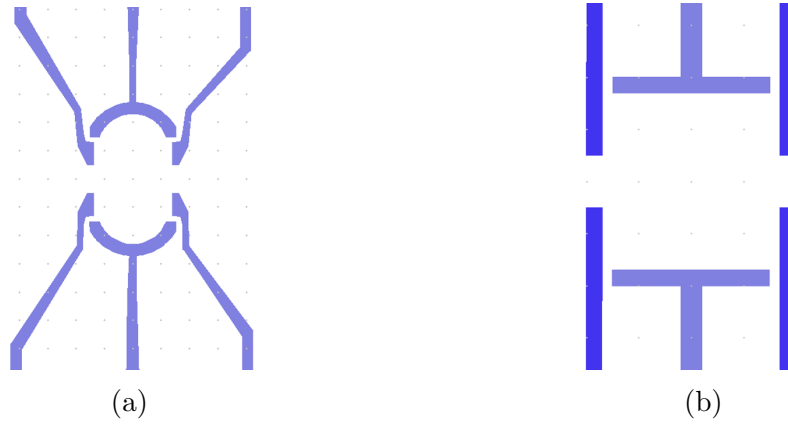
Figure 3.7: (a) Single gate layer interferometers.
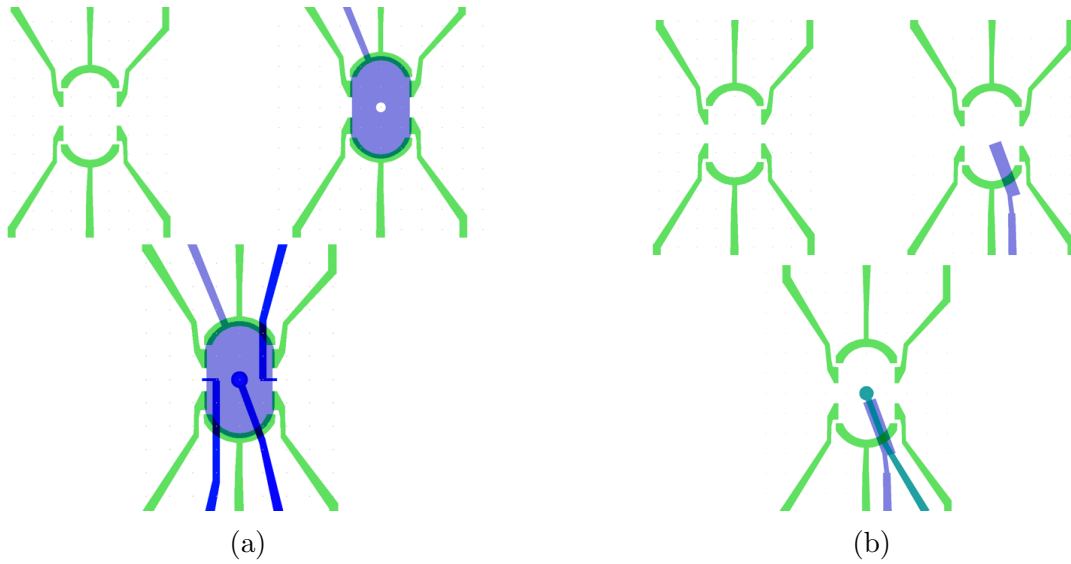
Figure 3.8: Triple gate layer interferometers.

An essential motivation behind our goal to achieve complete control of the confinement potential in complex QPCs within the fractional quantum Hall regime, is their potential integration into interferometers in the future.

There are two single gate layer interferometers, one with curved plunger gates and a squared version with flat plungers. Those are depicted in Figure 3.7, and they were measured in [29], mainly to study the material before moving on to the more interesting experiments that take place with the triple gate layer devices, depicted in Figure 3.8. With the triple layer design shown in 3.8(a), the existence of the second layer gate, the screening gate, allowed for the addition of helper gates in the QPC channels. Additionally, since we realize in section 4.1.1 that gating GaAs reduces the local mobility, an alternative washboard design shown in Figure 3.8(b) was implemented, to have less gate overlapping the interferometer region, while maintaining the antidot gate.

All four interferometers have 500nm wide QPCs, and were fabricated to have

both a $3\mu m^2$ and a $8\mu m^2$ area. While I contributed to the design of these devices, and fabricated them, interferometer measurements will not be discussed in this thesis.

Chapter 4

Materials, Fabrication and Methods

4.1 GaAs Material Study

Two GaAs wafers were used in this work, and they are shown in Figure 4.1. The 3×3 Swiss cheese device was fabricated on the MF1 wafer shown to the left, while the 3×1 and 3×2 devices were fabricated on wafer MF3 to the right.

(a) MF1   (b) MF3
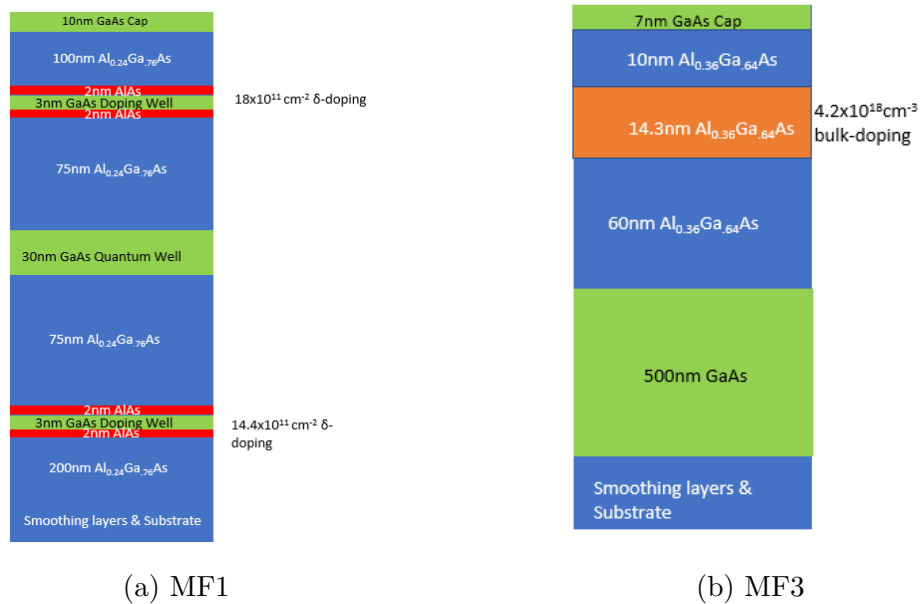
Figure 4.1: Two GaAs wafer stacks that were used in this thesis.

Table 4.1 shows the estimated electron density and electron mobility for these two wafers.

Wafer	300mK Mobility ($10^6 cm^2/Vs$)	300mK Electron Density ($10^{11}/cm^2$)
MF1	15.6	2.86
MF3	4.67	1.37

Table 4.1: MF1 and MF3 estimated electron density and mobility.

When looking at the Hall scans shown in Figure 4.2, we can see that because of the high electron density in wafer MF1, we cannot access the interesting fractions that lie between $\nu = 2$ and $\nu = 1$, since our limitation is that our magnet can only go as high as 6T in the z-direction.

On the other hand, wafer MF3 can go all the way up to $\nu = 1$, and shows two fractions in the bulk, namely 4/3 and 5/3.
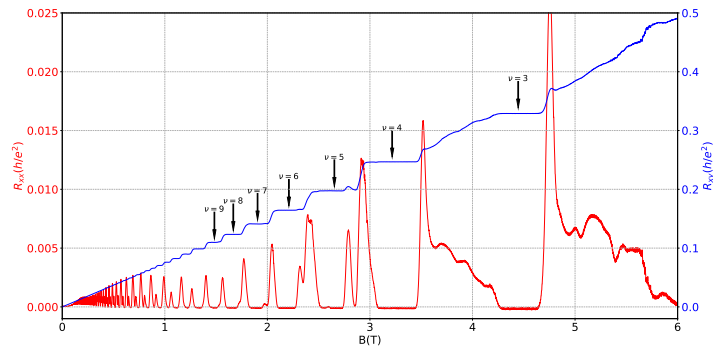
(a) MF1
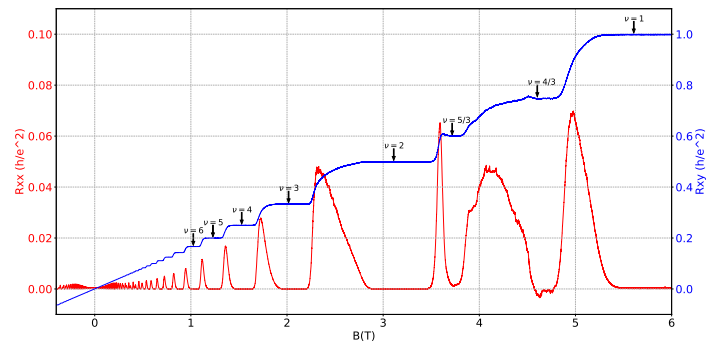
(b) MF3

Figure 4.2: Hall scans obtained for the two wafers. These measurements were taken as a collaborative effort between the current thesis and thesis [29].

4.1.1 Gating GaAs
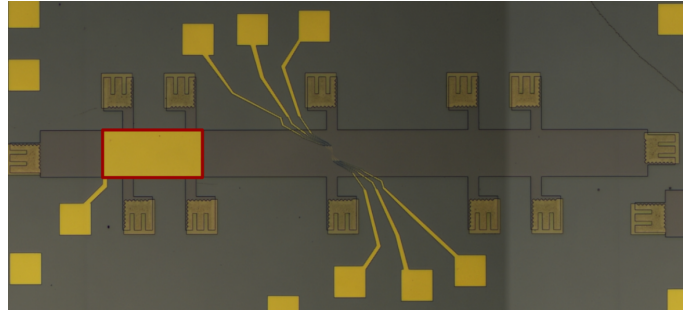
(a)
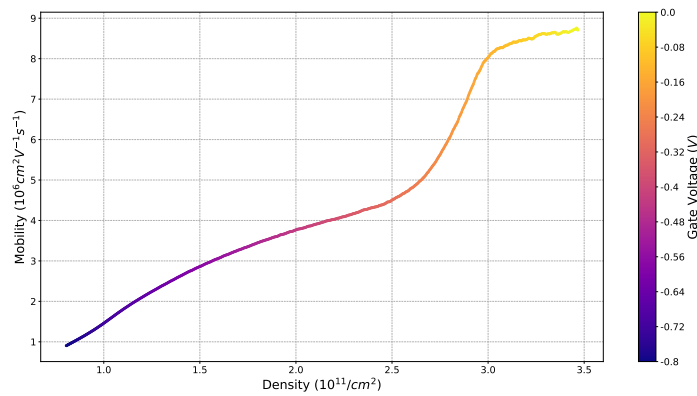
(b)
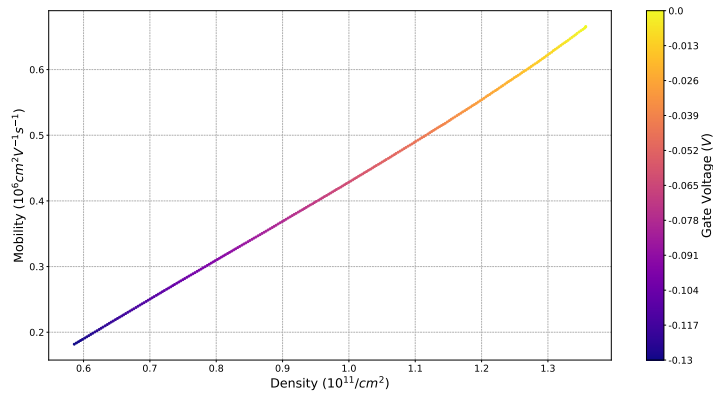
(c)

Figure 4.3: (a) Top gate on the left side of a Hall bar shown with a red frame, (b) MF1 wafer, gate effect on electron density and mobility, (c) MF3 wafer, gate effect on electron density and mobility. Figures (b) and (c) were taken as a collaborative effort between the current thesis and thesis [29].

To further characterise the wafers, a top gate was placed on the left side of the Hall bars to measure the mobility and density in terms of the applied gate voltage. As a reference, the mobility and electron density were also measured on the right

side of the mesa which is ungated. Table 4.2 shows the measured mobility and electron density on the ungated side of the mesa.

Wafer	Measured Mobility($10^6 cm^2/Vs$)	Measured Density($10^{11}/cm^2$)
MF1	22.8	3.19
MF3	3.74	1.43

Table 4.2: Ungated mesa measured electron mobility and electron density for wafers MF1 and MF3.

By comparing the values in Table 4.2, which show the measured electron density and mobility in both wafers on an ungated region, with figures 4.3(b) and (c), we can see a clear reduction in the mobility, even when the gate is at 0V. In wafer MF1, the mobility of the gated region is almost 3 times lower than the mobility in the ungated region at 0V gate voltage. Similarly, in wafer MF3 the mobility of the gated region is almost 5 times lower than the mobility in the ungated region at 0V gate voltage. The electron density in both wafers is roughly the same, when comparing the gated and ungated regions.

4.2   Electron Beam Lithography (EBL)

Electron beam (e-beam) lithography was used in all fabrication steps for the chips fabricated during this thesis. It is a powerful technique for creating nanostructures with features as small as a few nanometers. A fun and simple illustration on some basic concepts of EBL can be found in [30],[31]. They are highly recommended to understand the very basics of e-beam lithography.

The technique works by moving a highly focused electron beam over a sample to write out a pattern designed with suitable CAD tools. The pattern is recorded in a layer of resist, that is deposited onto the sample before the exposure by spin coating. After spin coating, the chip is baked on a hotplate for some appropriate amount of time, the longer the bake the stronger the molecular bonds in the resist will become. When the electron beam hits the resist, it induces a change to it's molecular structure and solubility.

Following the exposure of some areas to the electron beam, the resist is developed in a suitable solvent. This will selectively dissolve either the exposed or unexposed areas of the resist, depending on the resist's polarity. In this work positive electron beam resist is always used. With this type of resist, the exposed areas are those that dissolve in the developer, leaving behind a 3D realization of the CAD design.
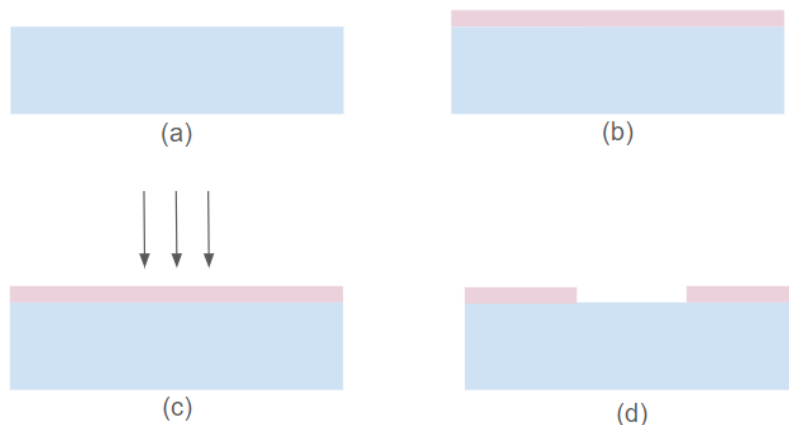
Figure 4.4: Steps that repeat for every exposure. Vertical cross section of chip. Blue indicates the substrate and pink is the resist. (a) Clean substrate, (b) Spin suitable resist and bake, (c) Exposure, (d) after development.

This sequence of steps (Clean-Resist-Expose-Develop) are shown in Figure 4.4, and are common for every fabrication step. The next steps are determined based on what we want to make. This could be the mesa, where chemical processing follows, or it could be ohmics/metal gates where metal evaporation comes after. The following section is intended for a reader with minimal to zero fabrication experience, and it shows a simplified overview of how a GaAs chip is fabricated starting from a blank chip. For a more advanced reader, a very detailed and technical recipe including tips and tricks can be found in Appendix A.

4.3 GaAs fabrication decoded

When learning how to fabricate on GaAs/AlGaAs heterostructures, there are two main skills one has to acquire. The first one is how to dose test metal gates, or in other words how to fine tune a recipe to bring their designs to life. The second one is more straightforward, namely how to prepare the chip to accommodate these designs by etching the mesa and adding ohmic leads to the chip. The following subsection goes through the latter, and the art of dose-testing can be found in subsection 4.3.2.

4.3.1 From chip to device

When a GaAs wafer or a piece of a wafer is received, the first step is to take it to the cleanroom and inspect it under the microscope. The whole wafer is then coated in a layer of resist, typically an ebeam MMA or PMMA resist and then stored in a Nitrogen cabinet awaiting cleaving. The chip size is typically chosen to by 5×5 mm and can be cleaved at the manual or automatic scribers.

In order to fabricate more complex nano devices, it is necessary to perform multiple lithographic and processing steps, requiring a careful alignment of subsequent layers. For this, alignment marks need to be patterned on the chip. These define the chip's frame of reference, and are used when exposing multiple elements on the chip such that they are properly aligned with respect to each other.

The next order of business is to define the mesas. These are nothing more than isolated islands in the chip inside which the 2DEG exists, but not around them. These could have any shape depending on the experiment, in our case we pattern Hall bars on all the chips, as demonstrated in Figure 4.5.
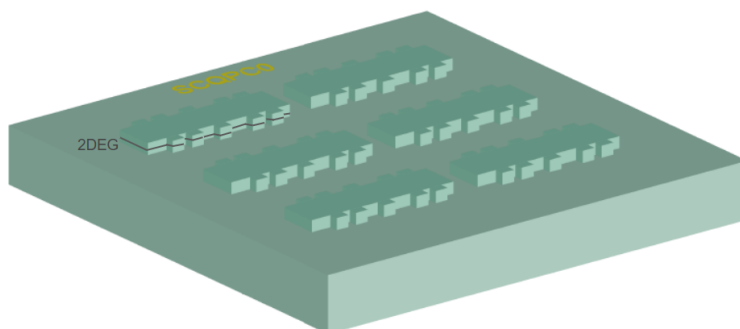
Figure 4.5: Chip after mesa etching, here 6 Hall bar mesas are defined. The 2DEG is shown as an example in the top left mesa as a grey line.

A wet etching process is followed to pattern the mesas on the chip, and the process is shown in Figure 4.6. After spinning and baking the PMMA resist, all the areas *around* the mesas are exposed. The areas exposed by EBL will then dissolve in the developer. In this way we wash away the resist around the mesas, and the substrate is left unprotected, so when it is dipped in the etching solution those bare GaAs areas will be dissolved vertically. After development the chip is hard baked on a hotplate to make the resist more resistant to wet chemical etching, and reduce the undercut that can occur during this process.

We then prepare the etching solution and insert the chip inside for some appropriate amount of time that depends on the strength of the solution. The goal is to etch the substrate around the mesas at least 50nm below the 2DEG level [1], in order to isolate the mesas from each other. Before doing this on the chip intended for the experiment, it is recommended to do some etching tests on an outer piece of the wafer to determine the appropriate etching time. Finally the remaining resist on the chip is removed with another solvent and the result should look like Figure 4.5.

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[1]We aim for at least 50nm below the 2DEG, because depending on how the etchant hits the chip, some mesas will be etched deeper, some less, and we definitely want to go below the 2deg in all mesas.
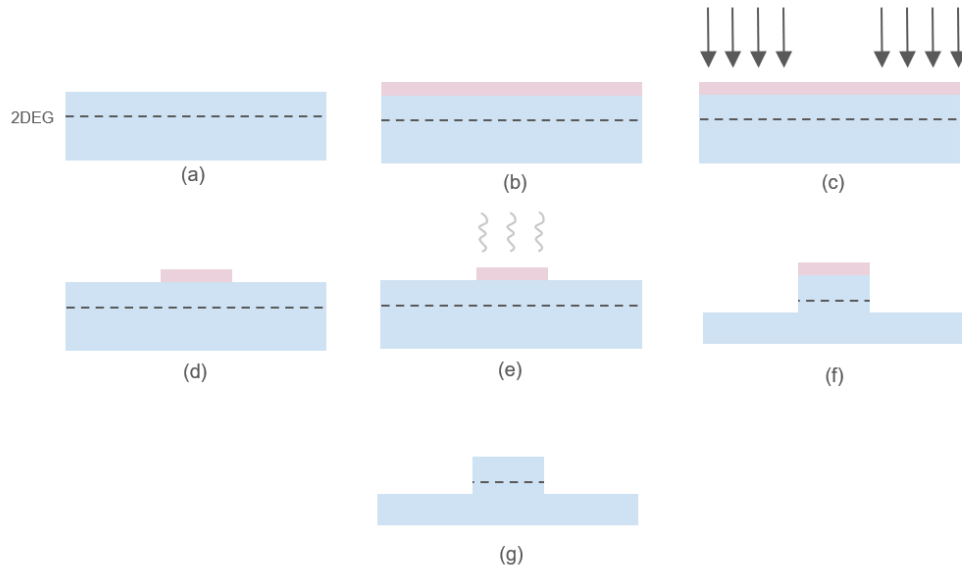
Figure 4.6: Defining the mesa steps. Vertical cross section of chip. (a) Starting from a clean chip (blue), (b) spin resist (pink) over the chip and bake, (c) expose areas around the mesa, (d) after development, (e) hard bake, (f) after etch, (g) after stripping resist.

We are interested in performing transport experiments that will take place inside the 2DEG, so we need a way to connect the 2DEG with the outside world. This is done by diffusing some leads from the surface into the wafer to reach the 2DEG. They are called ohmics (short for ohmic contacts) which are used to bias and measure the 2DEG.

To do this, we follow the process shown in Figure 4.7. Just as for the mesa, the substrate is covered in resist, and the areas where the ohmics will be placed are exposed and subsequently developed. Then in the AJA2 chamber, the chip is bombarded with Ar plasma to remove material to some desired depth, and a stack of metals is evaporated. After removing the excess resist, the chip goes through a process called Rapid Thermal Annealing (RTA), where it gets heated to a very high temperature of 450C° for one minute. This diffuses the metal through the substrate, creating ohmic contacts that reach to the 2DEG.
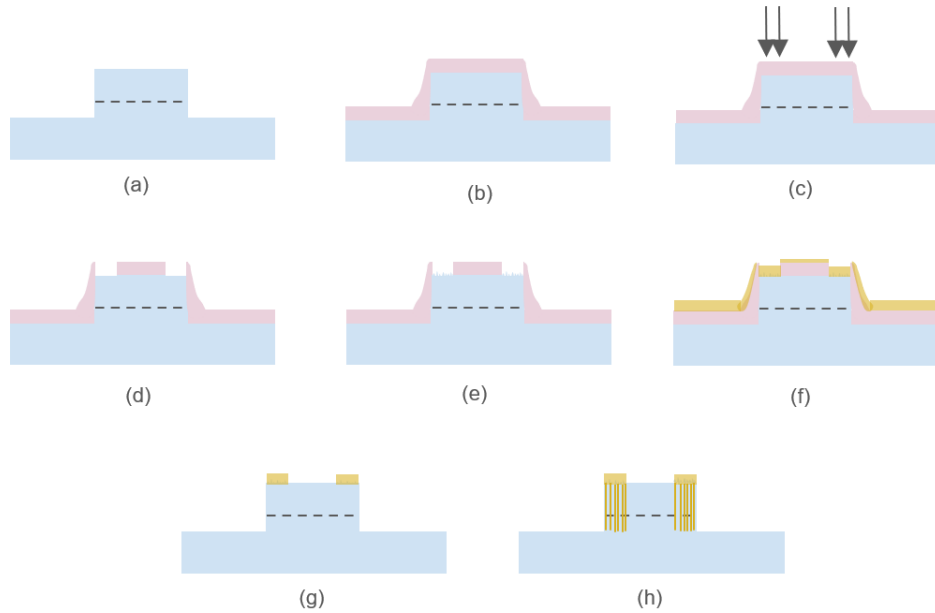
Figure 4.7: Ohmic Annealing steps. Vertical cross section of chip. (a) starting from a clean substrate (blue) with mesas defined (b) spin resist (pink) over the chip and bake, (c) Expose areas where ohmics will go, (d) after development, (e) after ashing and ion milling, (f) after Ge/Pt/Au evaporation, (g) after stripping the resist (h) after diffusing the ohmics (RTA).

Now that we have access to the 2DEG, we can start thinking about pattering gates on the substrate surface. Typically one designs their device using a CAD software, and depending on the limitations of the design, a suitable fabrication recipe is chosen to pattern the gates. More details on how to fine tune a recipe to produce the correct gate design can be found in the following section.
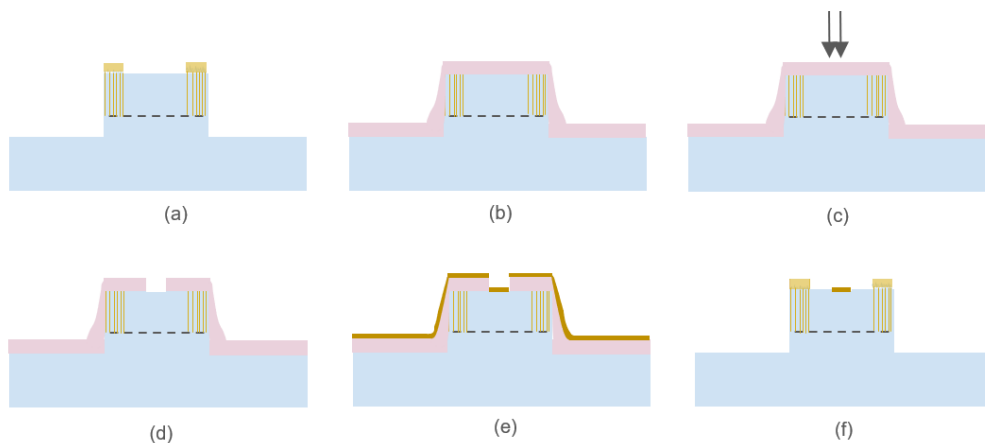
Figure 4.8: Inner/fine gate patterning. Vertical cross section of chip. (a) starting from a clean substrate (blue), (b) spin resist (pink) over the chip and bake, (c) expose gates, (d) after development, (e) after metal evaporation, (f) After liftoff.

There are two steps in fabricating gates. The first is patterning the fine (or

inner) gates, which is in essence the design of the device and is typically in the range of a few microns. However, to gain electrical control of these gates, they have to fan out and eventually become bond pads. These fanned out gates are called outer gates and are fabricated after the fine gates as an additional fabrication step.

To fabricate the fine gates, the common procedure of clean-resist-expose-develop shown in Figure 4.4 is followed. The next step is evaporating a stack of Ti/Au[2]. After liftoff [3], the excess metal and resist are removed leaving behind a 3D realization of the design. The same process is followed for the outer gates, with the difference being that more metal is evaporated to ensure that they climb the mesa without breaking.

When a gate design is multilayered, an insulating layer needs to be grown in-between the layers to ensure that they are electrically isolated. In this fabrication process, an insulating oxide layer of HfO_2 is grown in a chamber through a process called Atomic Layer Deposition (ALD). This method generates high quality and high breakdown point thin oxide films.

4.3.2   Dose testing gates

When faced with the task of realizing a new gate design, the conventional thing to do is to start from a well established recipe that people in the group typically use, and try to make it work for the design through a dose-bias test. In the exposure parameters of the recipe, there should be a parameter called dose which is measured in units of $\mu C/cm^2$. This critical parameter is nothing more than a measure of how many electrons there are per unit area of exposure. The dose range is highly dependent on the type of resist and substrate that are being used, but many parameters determine the exact dose needed to create a pattern. Some of these parameters include e-beam forward scattering through the layers of resist, back scattering from the substrate and resist thickness and processing history.

Since the dose is a measure of 'how charged' the electron beam is per unit area of exposure, it is often translated into another parameter called dose time. This is a quantity measured in $\mu s/dot$ and can be calculated through dose calculators. In essence, it shows how long the electron beam sits at each pixel of the pattern before moving on to the next.

The other parameter that is important to test is the bias. When exposing a pattern, the dimensions that will come out on the chip can vary from the ones in the design. Features are usually exposed bigger due to electron scattering during the exposure [4]. To compensate for this there is no need to go back to the design

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[2]Titanium helps the gold stick to the surface.

[3]This is a common term in nanofabrication. Liftoff is the process where the chip is placed in a solvent that dissolves the resist after metal evaporation. Along with the resist, the excess metal will be removed. See Figure 4.8.

[4]How much the design spreads out also depends on the current being used, the effect is usually more prominent at higher currents.

and re-scale everything, the bias parameter can change the size of the pattern to counteract this effect.
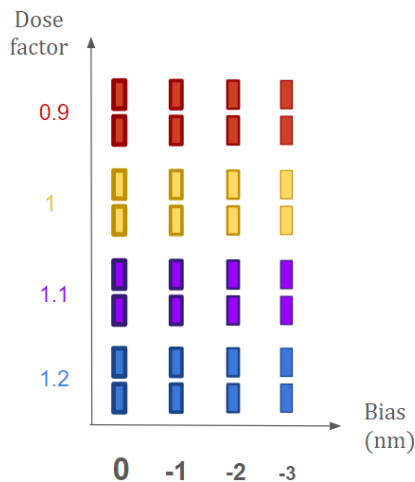
Figure 4.9: Dose-Bias array. The vertical axis shows a change in the dose factor in integer steps of 0.1, and the horizontal axis represents the bias in integer steps of -1nm.

The dose-bias test is designed in a software called Beamer. The design goes through two loops to create the dose bias array shown in Figure 4.9. The first one creates the row, where the Bias module is applied. The second is formed through the module ChipPlace. This assigns a dose factor to each row. A dose factor of one corresponds to the base dose that the fabber has to supply to Beamer in the form of dose time [5]. When starting from a given recipe, I would use the dose given in the recipe as the base dose (dose factor 1), and play around that with dose factors between 0.8 to 1.2. Each row now corresponds to a new dose which is equal to dose factor $\times$ base dose.

After exposing this array, an SEM inspection is performed and the best dose-bias element that is closest to the design dimensions is selected. To be safe, it is good to inspect the closest neighbors of the best element as well. The dimensions might not be exactly spot on, but it is important to at least see that they produce a correct looking pattern with no lithographic shorts. This is important because after performing the dose test if there is a time gap between the dose test and fabrication of the real chip, the Elionix dose can shift through time due to tool degradation. This dose shift is the main reason why a dose test is needed in the first place.

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[5]When knowing the dose one can calculate the dose-time through a dose calculator on the design computers.

4.4 Fridge modifications

In an attempt to reach lower electron temperatures, a QDevil copper powder filter was installed on a loom of DC lines at an Oxford dilution refrigerator.

The filter was placed in series with the pre-existing RC filter of that specific loom. The filter was screwed with stainless steep screws on the mixing chamber plate of the fridge, and was further connected to the mixing camber plate through oxygen free copper wires, to increase thermal contact.

To test the effect of the copper powder filter, a GaAs wafer previously measured in the same fridge was loaded again, and a Hall scan was performed after the filter installation. As shown in Figure 4.12, the green curve corresponds to no added filtering, and the cyan curve is the same measurement after the copper powder filter was installed. There seems to be no improvement in the appearance of more fractions.

In further attempts to cool down the sample even more, a copper braid was used to thermalise the cavity of the chip carrier. As shown in Figure 4.11, the copper braid is connected to the top of the puck that thermalizes through the mixing chamber, to the cavity of the daughterboard. The blue curve in Figure 4.12 corresponds to a measurement done on the same sample after the copper powder filter was installed and the copper braiding was implemented. Again no improvement can be seen in the realization of more fractions.

(a)   (b)
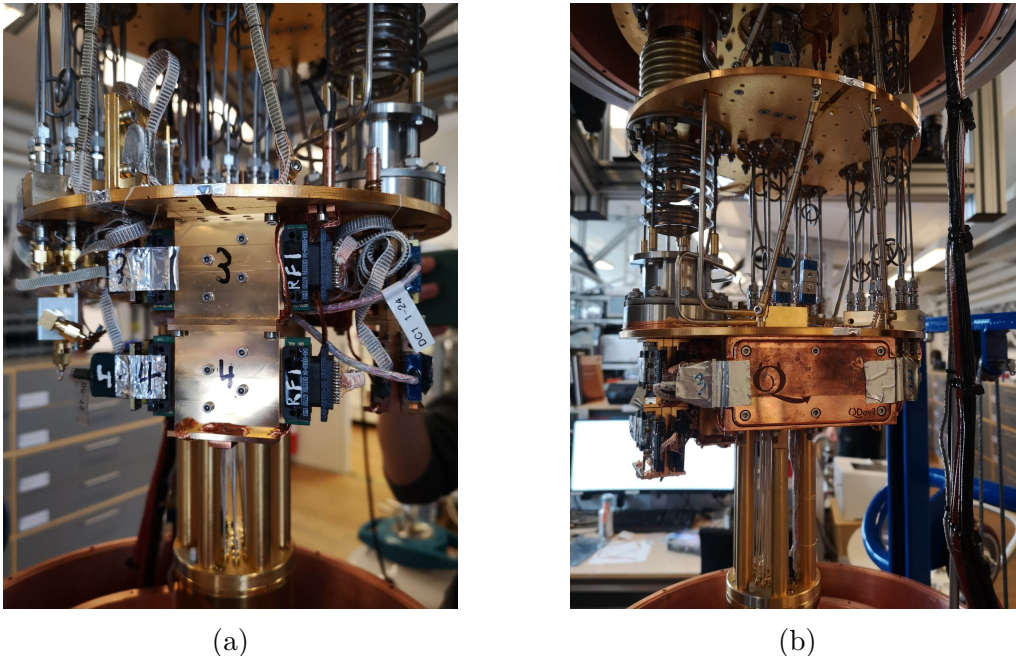
Figure 4.10: (a) Pre-existing RC filters on looms 3 and 4, (b) QDevil copper powder filter connected in series to the existing RC filter on loom 3.
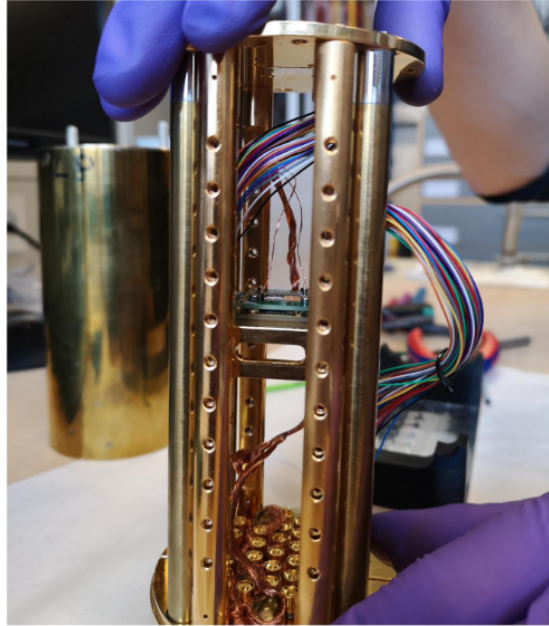
Figure 4.11: Copper braid going from the top of the puck which engages to the mixing chamber, to the cavity of the daughterboard.
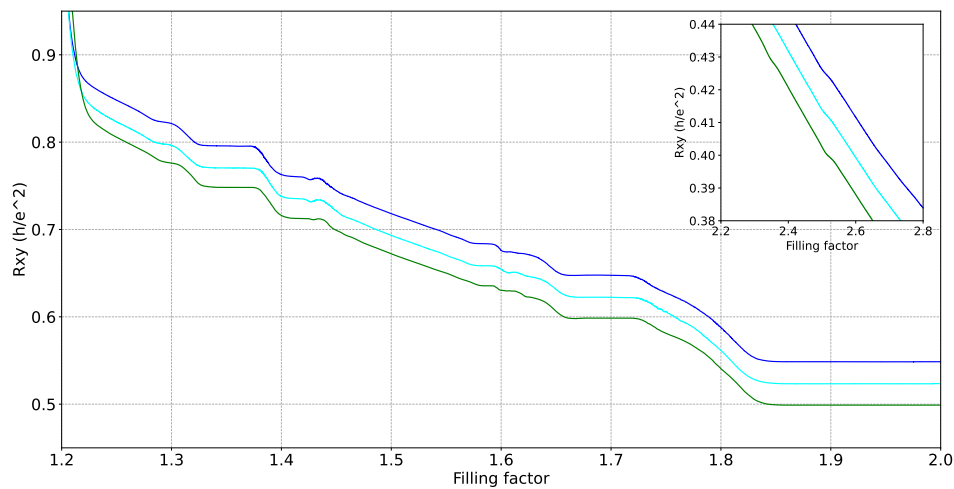
Figure 4.12: Hall scan of the same Pfeiffer GaAs chip in T9. Green is with no added filtering, cyan is with copper powder filter added, and blue is with both copper powder filter and a copper braid from the top of the puck to the daughterboard. R_{xy} is shown as a function of the filling factor. Data taken as a collaborative effort between the current thesis and thesis [29]. The curves are vertically shifted for clarity.

4.5 Device characterization at base temperature

For any newly bonded device there is a checklist of tests that have to be performed at base temperature before it can be called fully functional and ready to perform experiments on. The first is to measure the I-V curve for all ohmics in the range of ± 1mV. The I-V should of course be linear and the resistance of each ohmic when the rest are grounded should ideally be below 20kΩ.

Then the gates need to be leak checked. There are two sources of leakage. The first is a short, meaning that two gates are touching and as a result they can only be operated as one gate. Shorts can be caused lithographically, there could be a floating piece of metal that was not lifted off properly that shorts them together, or if the gates are in different layers it indicates that there are gaps in the oxide layer.

Shorts show up very easily by hooking up a Keithley with zero voltage bias on a gate on the break out box[6], while all the rest are grounded. If a current in the range of a few nano amperes appears when the gate is floated this indicates that the specific gate is shorted to something. To identify what it leaks to, the rest of the gates are floated one by one until the current disappears. It should disappear when it's leaking partner(s) is(are) floated.

The other type of leakage is leakage between gates from electrons tunneling between two gates that have a very thin dielectric layer between them, just like an NIN junction. This leakage current depends exponentially to the gate voltage applied. It is not uncommon for a very small leakage current of 10s of pico amperes to exist when a gate is activated. A red flag is raised when a gate is leaking nano amperes of current when it is activated.

After verifying that no gates leak, it is necessary to check that they are connected. To check this, a very small current of a few nano amperes is applied across the device and the gates are energized according to the device design. The goal is to see that when each gate is activated there is a current drop, signaling that that gate has some effect on the 2DEG.

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[6]The reason why a current can be detected even at zero applied voltage is because there exists a very small voltage difference when connecting the Keithley to the breakout box, because the ground of the Keithley is different than the ground of the fridge.

Chapter 5

Swiss Cheese QPC characterization

The device studied in this chapter is shown in Figure 5.1. We measure the four point conductance across the device, and try to manually tune different channels.
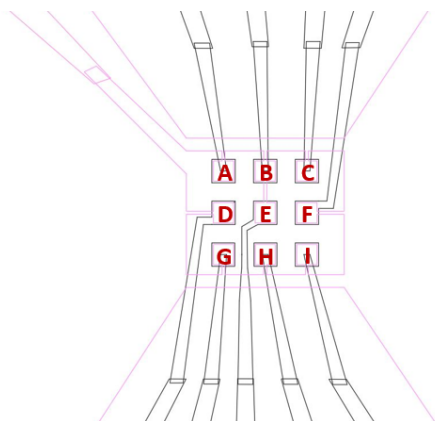
Figure 5.1: Device studied in this chapter, the pink gates are in the first layer, and the black gates, the pixels, are in the second layer and renamed as letters between A and I.

5.1 Experimental setup and initial tuning

Sample SCQPC∅ was loaded in a dilution refrigerator and cooled down to 15-25mK. For the middle left device of chip SCQPC∅, the device characterization checklist in section 4.5 was followed. All the ohmics were connected with reasonable valued resistances. Furthermore no gates were leaking, however pixel D was not responsive. We assumed that the connection broke off at some point. Nonetheless, the device was measured and results are shown and discussed in the following sections.

The initial goal for this device was to try to manually tune some good channels,

with the criterion for a "good" ballistic channel being conductance quantisation in integer steps of $2e^2/h$.
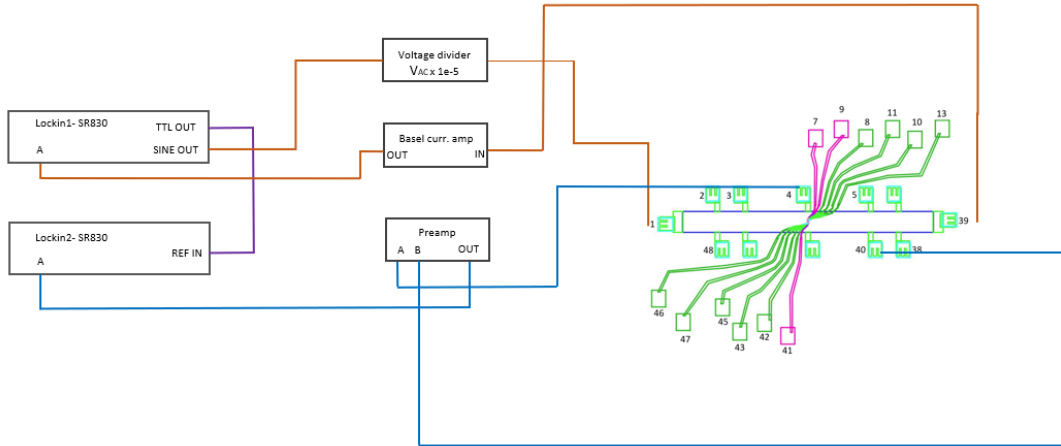
Figure 5.2: Voltage biased four point conductance measurement setup. A constant voltage bias is applied between contacts 1 and 39, and the resulting current is amplified and measured. The voltage drop across the device is measured between contacts 4 and 40. The two lockins are slaved to the same frequency.

The circuit shown in Figure 5.2 was used to measure the four point conductance of the device. For this device geometry, there are two types of tuning, the rough and fine tuning.

The rough tuning is simply to form a channel with the outer gates (top and bottom gates). To to so, they are scanned from zero volt to a very negative voltage such that the 2DEG underneath them is fully depleted. The sign of fully depleted 2DEG under a gate is that when ramping the gate voltage, the conductance saturates. This is depicted in Figure 5.3(a).

Now that a channel is formed in between the outer gates, as seen in the cartoon picture of Figure 5.3(b), fine tuning follows, where the inner gates are manually tuned to achieve conductance steps. In all that follows the outer gates are always parked in their depletion voltage, and only the inner gates are changed in different configurations.

As can be seen from Figure 5.3(a), at the saturation point of the outer gates, the conductance measured across the channel is very high, around $70G_0$. This is because the channel is very wide, around 1μm. Initially the idea was to keep the screening gate grounded and only play with the pixel gates to fine tune the channel potential. This could not be done in practise, because activating the pixels would cause no change to the conductance, if we started scanning them with $70G_0$ conductance going through the channel. This is because they are very small compared to the width of the channel[1], as seen in Figure 5.3(b). If some of those pixels were activated

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[1] This is because of lithographic requirements, see Chapter 3.

and not all of them together, no change was seen in the signal.
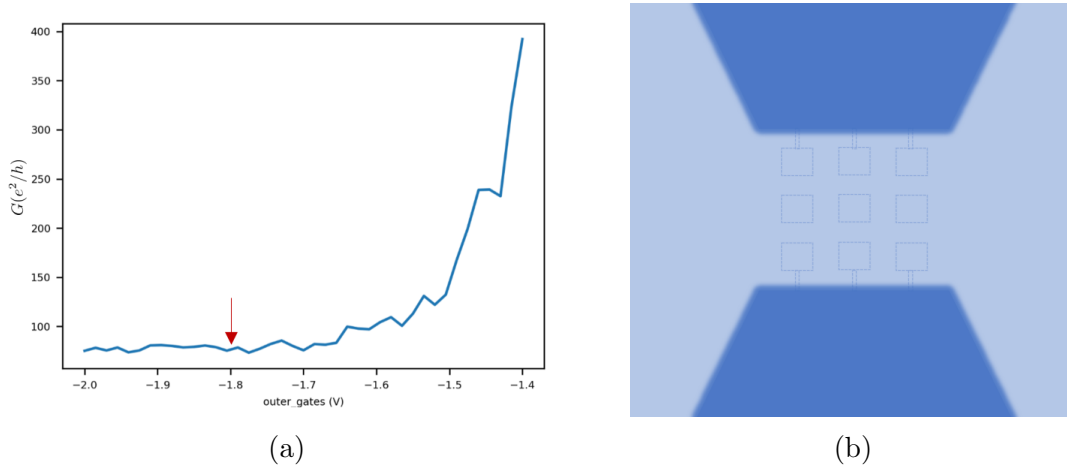
Figure 5.3: (a) Park outer gates at their saturation point -1.8V, (b) Qualitative drawing of the 2DEG potential. The 2DEG underneath the outer gates is fully depleted (dark blue), and a channel is formed in between them. Light blue indicates free 2DEG.

To make the effect of the pixels visible, the screening gate needed to be activated in all measurements, and parked at a negative voltage to reduce the conductance going through the channel.
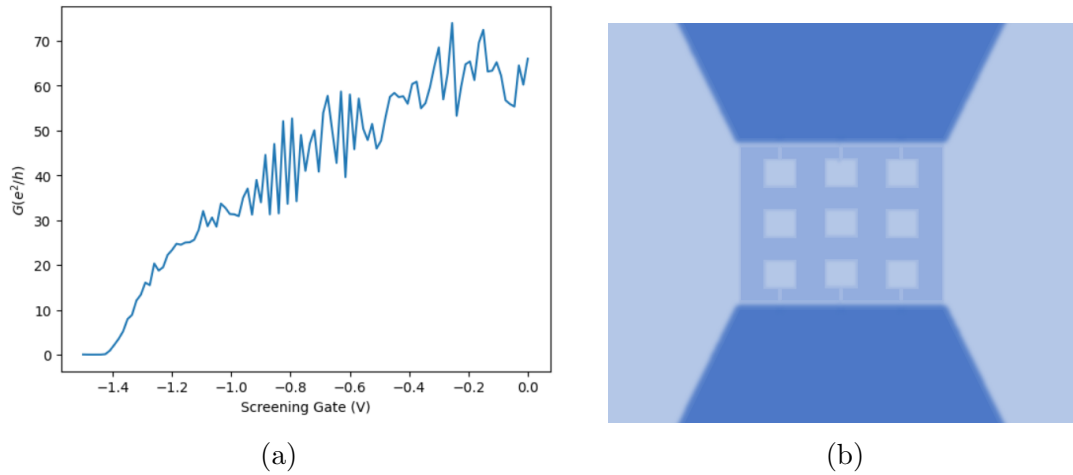
Figure 5.4: Figures (b) is a qualitative drawing of the 2DEG potential. Light blue is free 2DEG, dark blue is depleted electron gas and middle blue indicates a potential in between where 2DEG still exists. (a) Screening gate scan corresponding to potential configuration of (b).

Figure 5.4(a) shows a scan of the screening gate, when the pixels are at zero volt and the outer gates are saturated. This corresponds to the potential picture in Figure 5.4(b). A value for the screening gate was chosen based on this curve, to begin tuning the pixels from an initial conductance value less than $70G_0$. Then, the effect of the pixels was visible, however a negative potential background was created

as shown in Figure 5.4(b), and was always present due to the necessity to use the screening gate.

5.2 Results

In Figure 5.5(a), the top and middle row pixels (A,B,C,D,E,F) were parked at their saturation point. Then, pixel H was scanned for different screening gate voltages, and as seen in Figure 5.5(b) the screening gate voltage has a significant effect on the quality of the steps.

| (a) | (b) |
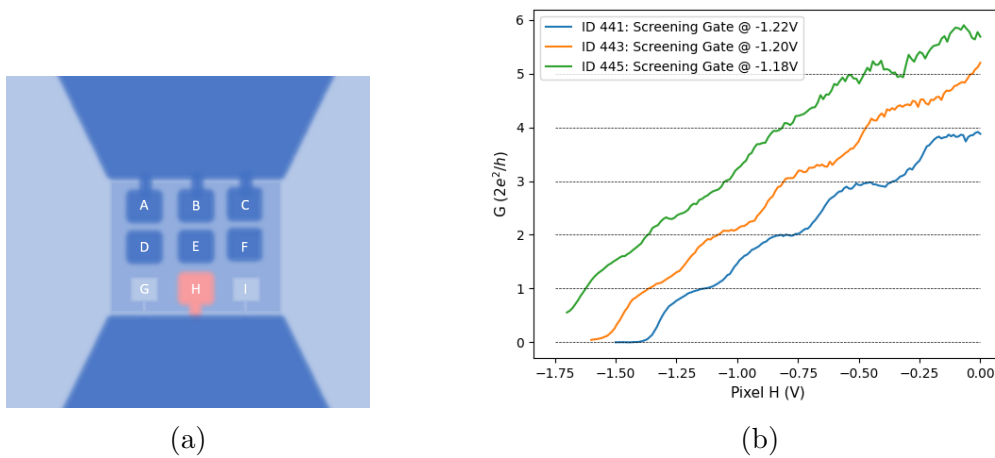
Figure 5.5: Figure (a) is a qualitative drawing of the 2DEG potential. Dark blue is depleted 2DEG, medium blue is a voltage in between where 2DEG still exists, light blue is free 2DEG. Pixel H which is being scanned is shown in pink. Pixels A,B,C,D,E,F are saturated, (b) Conductance curve as a function of the voltage on pixel H, for different voltages on the screening gate.

After realizing the importance of the screening gate voltage, a new channel was investigated, between pixels B and H. That is shown in Figure 5.6(a). A 2D scan was performed with gates BH as one axis and the screening gate as the other, with the goal of creating a QPC in between B and H with these pixels, and to find the sweet spot for the screening gate voltage for this channel, just as 5.5(b).

It was very surprising to see that the steps very clearly appear as a function of the screening gate, since the idea was to use the pixels to form the channels, not the screening gate. The reason why we believe this happens is discussed in detail in the next section. The reader is encouraged to bypass the following measurements straight to the Discussion section before returning back. The final measurements are slightly challenging to understand without realizing how the channel is formed.
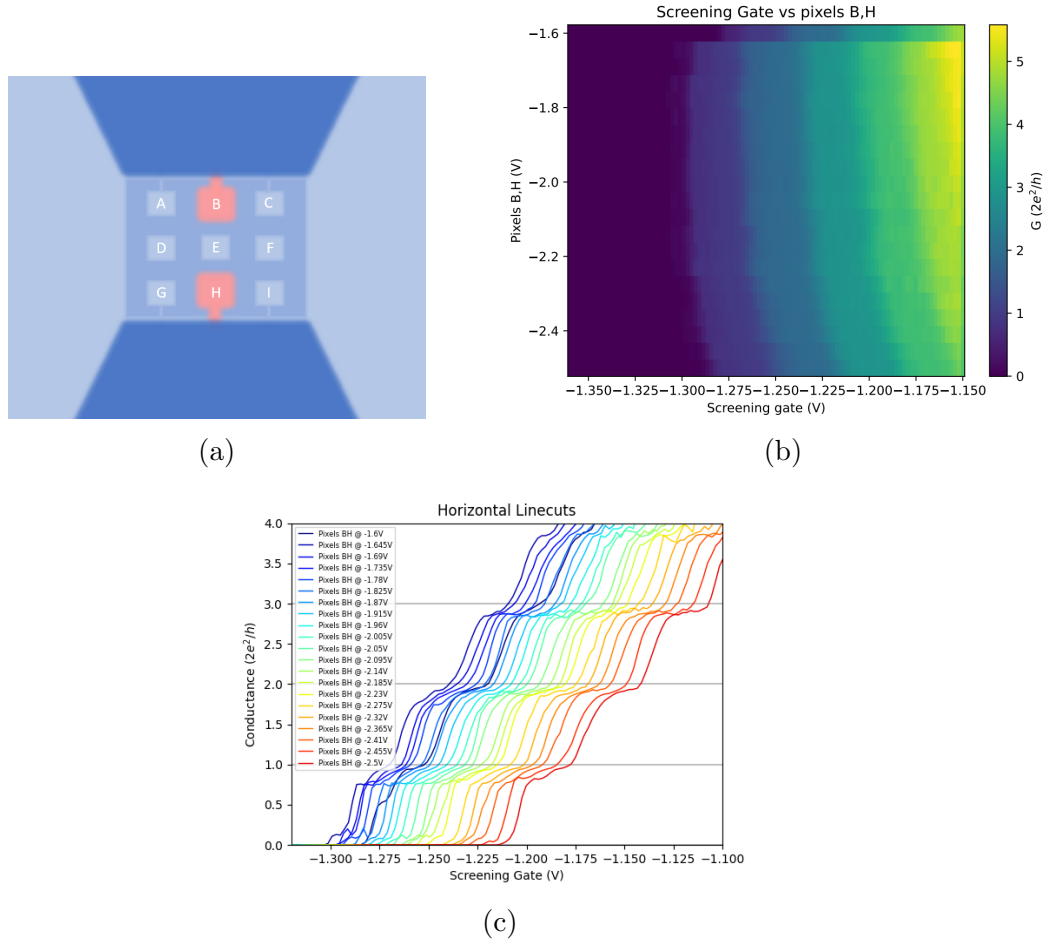
Figure 5.6: (a) Qualitative drawing of potential landscape in 2DEG. Dark blue is depleted 2DEG, medium blue is a voltage in between where 2DEG still exists, light blue is free 2DEG, and the gates in pink are being scanned together. Configuration where BH is scanned versus the screening gate, (b) 2D plot of BH pixels versus the screening gate, and the conductance is measured (c) Horizontal linecuts of (b), curves are shifted for clarity.

Even though it is not obvious, what the attempt described in Figure 5.6 shows is that we can form QPCs under one pixel at a time, with pieces of the screening gate acting as "virtual" QPC split gates.

To confirm this, QPCs were successfully formed under pixels B,H,E,F. The forementioned pixel's voltage was varied, and we expect that if the channel shifts in voltage space as a response to the pixel's applied voltage value, that the channel is indeed formed underneath that pixel.

As an example, data for channels formed under pixels E and H is shown in Figure 5.7. The voltage of the pixel under which the channel is believed to be forming is varied. This is represented by the colormap in the plots. We can see that the conductance curves shift in voltage, as the pixel over the channel is varied.

(a)

(b)

(c)

(d)
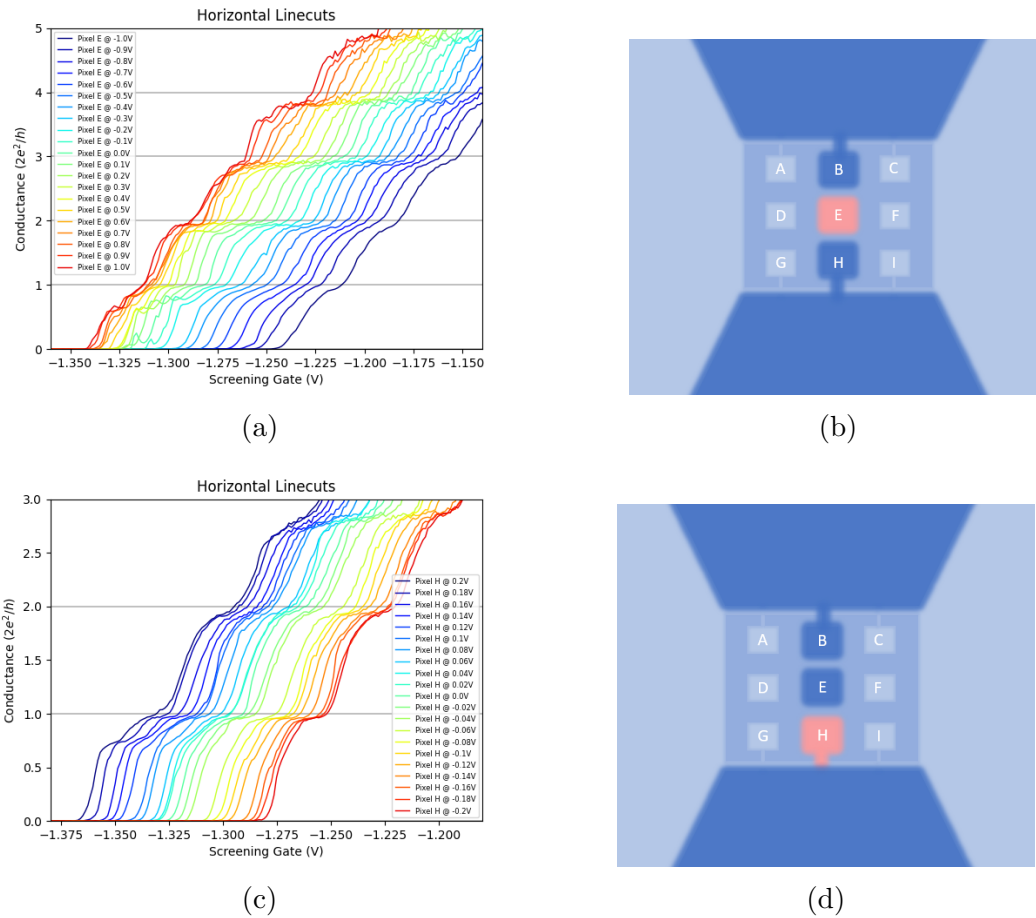
Figure 5.7: (a) and (c) are qualitative drawings of the 2DEG potential. Dark blue is depleted 2DEG, medium blue is a voltage in between where 2DEG still exists, light blue is free 2DEG. Pink indicates under which pixel the channel is formed. (a) Screening gate scan for different pixel E voltage values, (b) voltage configuration used for (a). (c) Screening gate scan for different pixel H voltage values, (d) voltage configuration used for (c). The curves are not shifted.

5.3 Discussion
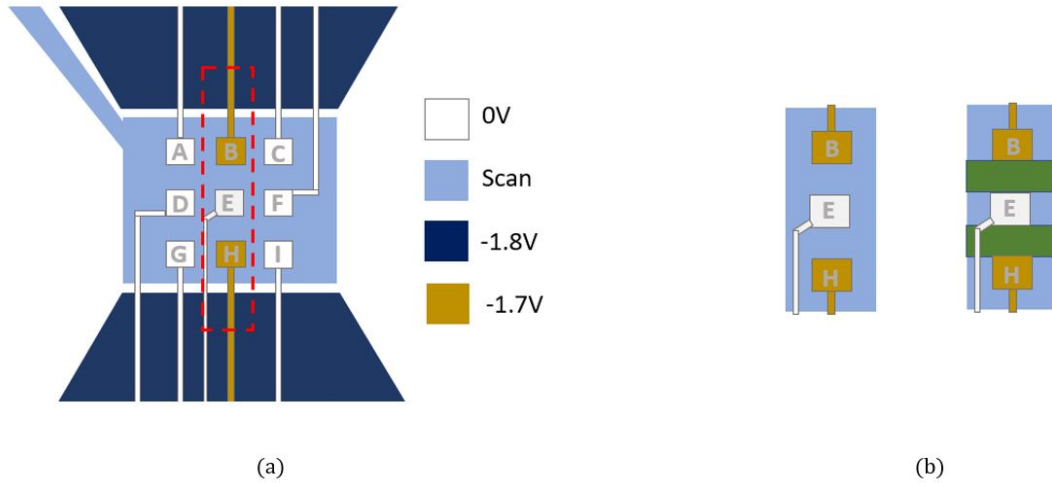
Figure 5.8: (a) Voltage configuration for the scan shown in 5.7(a). Pixels B and H are depleted, making sure that the only 2DEG that goes from left to right goes between B and H. (b) Focusing on the middle column of the device, the only thing that exists between B and H, is chunks of the screening gate (green) and pixel E.

As seen in Figure 5.6(c), the steps appear as a function of the screening gate. This was a surprising result, and an explanation of how we believe this happens is graphically shown in Figure 5.8. Pixels B and H are parked at saturation, such that they block the 2DEG from left to right at the top and bottom sides of the channel. Now we make sure that the only path for the 2DEG between left and right is between pixels B and H. The important thing to notice here is that the screening gate is also activated at a quite negative voltage, and the only possible explanation as to why the steps appear as a function of the screening gate is that two pieces of the screening gate inside the channel, namely the green pieces shown in Figure 5.8(b), act as virtual split gates, and form a channel between them, under pixel E.

Our theory could be proven correct if we performed a scan of the screening gate, for different voltage values on pixel E [27]. If there is a shift of the conductance curve as pixel E changes, then the channel is indeed under pixel E, because pixel E acts as a top gate modulating the density of that channel. The result of such a measurement is shown in Figure 5.7(a). The first thing to notice is that the curve shifts as E is changed, as expected. The more positive E is, the higher the electron density inside the channel, thus the pinch off point of the screening gate should be more negative. This is indeed the case. As a verification, Figure 5.7(c) shows the result of creating a channel under pixel H, and again we see the curve shifting with the voltage on pixel H, as expected.

Finally in both figures 5.7 (a) and (c), we can see a trend for the 0.7 anomaly. It seems to be more prominent at positive voltage on pixel E, and slowly washes away as pixel E becomes more negative. The same is true for pixel H. While it is not within the scope of this thesis to study the 0.7 anomaly, we can refer the reader to relevant literature. Some studies have found no dependence of the 0.7 anomaly

to the local electron density of the channel [32], while other suggest that that the barrier shape, rather than density, is the primary factor governing the conductance of the 0.7 structure [33].

In principle we can form a QPC under every pixel since they are all sandwiched in between two pieces of the screening gate. This was tried and successfully achieved for pixels B,H,E,F.

However, since with this device we could only shift the channel under one pixel at a time, we could not demonstrate that using a complex device over a simple split gate can indeed shape the confinement potential in any way needed. To prove this, new designs were considered and measurements on those can be found in the next chapter.

Finally, let us discuss future possible directions if one would wish to attempt a two-layered pixel-gate design again, such as the 3×3 device, or even N$\times$N. The problem with this device is that there is too much screening gate, and because the pixels are too small compared to the channel, nothing could be done without activating the screening gate. In terms of the design, if one wishes to make these two-layered design again, what we learned from this device is that the holes need to be bigger so that the gates are indeed close enough to pixelate the channel. This is graphically shown in Figure 5.9(b), where the holes are big enough such that the pixels make up the channel. However in practise this is extremely hard to achieve, since there will be no space left in between the pixels to route out the middle pixel.

(a)   (b)
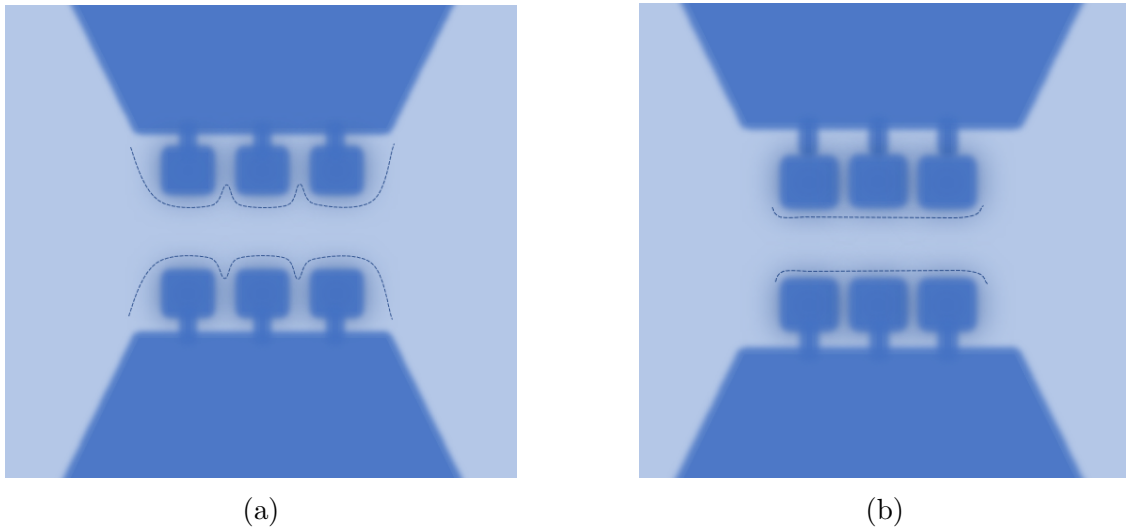
Figure 5.9: Qualitative drawing of 2DEG potential. Dark blue is depleted 2DEG, light blue is free 2DEG. (a) What happens in the device we measured, because the holes in the screening gate are too far apart, (b) Ideal case, if the screening gate holes were bigger.

All the roads lead back to the single layered design. There, the only problem was that the connector lines of the middle pixels had an odd effect on the 2DEG. To eliminate that problem one could try fabricating air bridges as shown in Figure 5.10 to connect the middle row gates. The dimensions needed for these air bridges are

between 500-700 nm, and can be successfully fabricated as seen in Figure 5.10(c). Such air bridge gates are also used in graphene based QPC devices (5.10(b)).

(a)

(b)

(c)
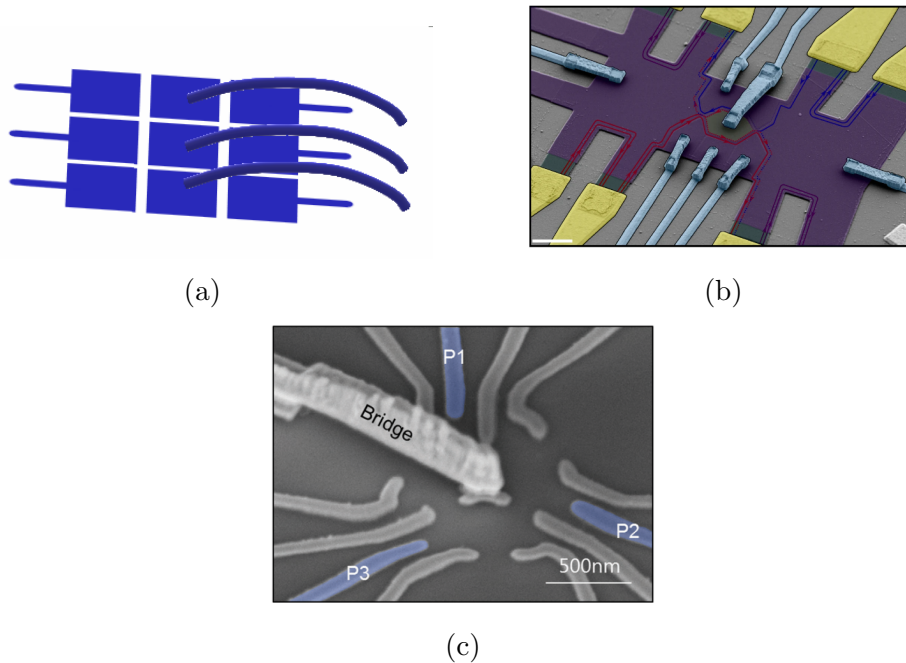
Figure 5.10: (a) How air-bridge gates could potentially eliminate the connector problem mentioned in Chapter 3, and keep the 3×3 design single layered , (b) Figure adapted from [34], how bridge gates are used in graphene based devices. (c) Adapted from [35], where an air bridge of dimensions comparable to the ones needed for the 3×3 device is successfully fabricated.

Lastly, it is important to address the issue of the lack of simulation tools. When we decided to pursue a multilayered design, we encountered a noticeable absence of self-consistent simulators capable of accommodating such configurations. While there are numerous accurate and widely-used simulation tools available that demonstrate the influence of gates on the 2DEG [2], these simulations are limited to single-layered designs. What they lack is a way to incorporate metal screening into the simulation calculations. Although recently such simulations are being developed in COMSOL, they were not accessible to us at the beginning of the project. Had we been able to utilize such a tool, it might have potentially predicted that the hole size was too small, enabling us to make appropriate adjustments to the direction of the project.

Chapter 6

3 × 2 QPC characterization

The device under investigation in this chapter is depicted in Figure 6.1(a). As a reminder, the 3×3 Swiss-cheese design was characterized in Chapter 5, and the main result was that with that specific gate design, we could not achieve the flexibility we wished for. The screening gate had much more of an effect than expected, however there was no uncertainty in the fact that the screening gate achieved it's main objective; which is to screen the connectors of the pixel gates. We exploit this property in designing the device depicted in Figure 6.1, and we characterized it in this chapter.

Figure 6.1(b) shows the gates the 2DEG should experience after screening takes place. In all that follows, only the right column of the device shown in blue in Figure 6.1(b) was operated, with the grey gates in Figure 6.1(b), as well as the purple screening gates in Figure 6.1(a) kept grounded.

(a)   (b)
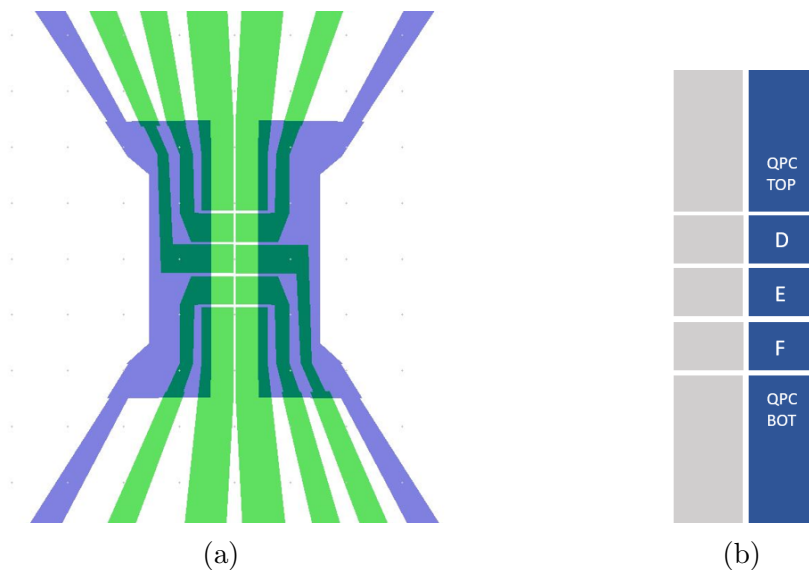
Figure 6.1: (a) Device under investigation in this chapter, (b) Only the right column is operated, indicated in blue in this qualitative drawing, that shows the gates that the 2DEG is expected to see after screening takes place.

6.1   Experimental setup

The setup being used in the following measurements is shown in Figure 6.2, and additionally, a magnetic field was applied perpendicular to the sample, to bring us to the quantum Hall regime. All measurements were performed in a dilution refrigerator of estimated base temperature 25mK.
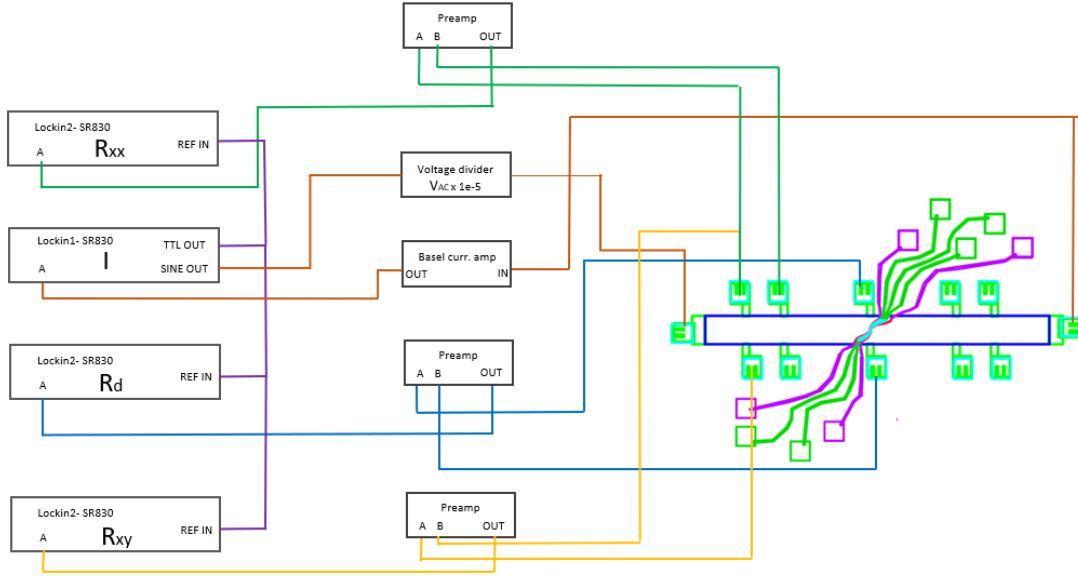
Figure 6.2: Voltage biased four point conductance measurement setup. A constant voltage bias is applied between the outer contacts (orange loop), and the resulting current is amplified and measured. Further, the diagonal resistance (R_d), longitudinal resistance (R_{xx}) and transverse resistance (R_{xy}) are measured. All four lockins are slaved to the same frequency of 17Hz.
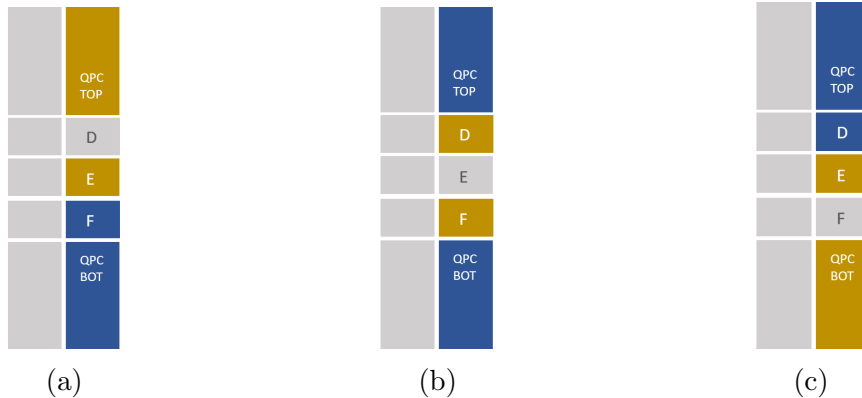
Figure 6.3: Laterally shifting the channel, (a) under pixel D (top channel), (b) under pixel E (middle channel), (c) under pixel F (bottom channel). Gray gate means kept at 0V, blue means parked at saturation, -0.5V, and the two yellow gates in each figure indicate the two gates that are used to form a channel between them.

This device is unique in the sense that we can laterally shift the channel in three different locations, by applying appropriate voltages on the gates. This is another

potential application of a complex or pixelated quantum point contact: the ability to spatially move the wavefunction of an edge state, with potential applications in their braiding and in topological quantum computation. Figure 6.3 graphically shows that for this device the channel can be chosen to live under pixel D, E or F. The width of each pixel is 500nm, and the length is 400nm.

6.2   Results

In this chapter, preliminary results of quantum Hall tunneling experiments performed in the device depicted in Figure 6.1 can be found. For the reason that we do not fully understand the behaviour of this device, due to time limitations during measurements, I chose to separate the data from the discussion, to prevent biasing the reader with any possible interpretation we might have.

6.2.1   Bulk properties

A Hall scan is taken to characterize the bulk. This is shown in Figure 6.4. In this figure, we can identify the integer plateaus up to $\nu = 2$, and two fractions, namely 5/3 and 4/3.[1]
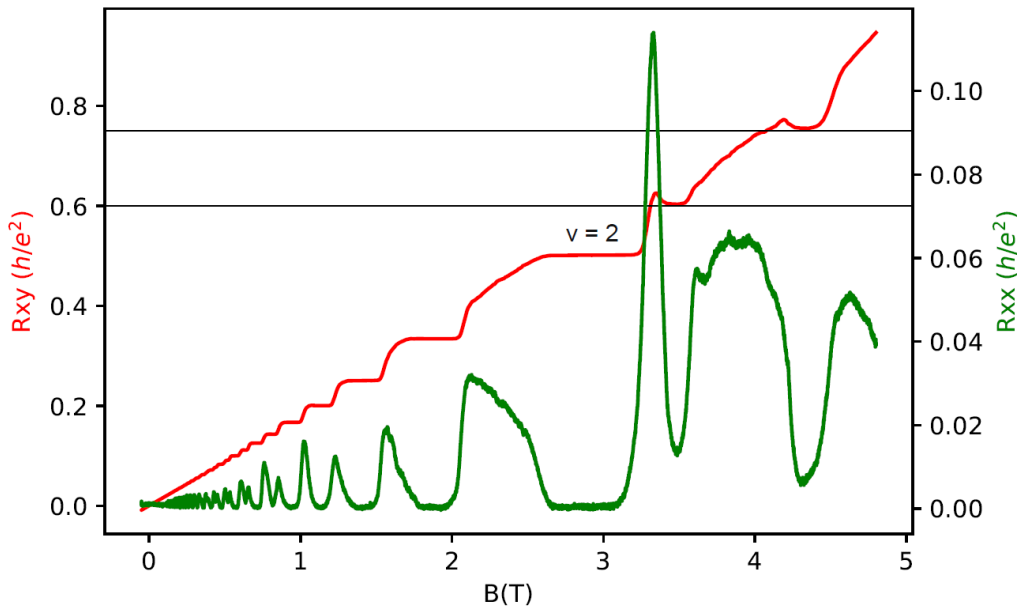
Figure 6.4: Hall scan. The R_{xy} curve is drawn in red while the R_{xx} is shown in green.

In the measurements that follow, we choose to park the bulk at a constant filling factor of $\nu = 2$. To choose a magnetic field value along the $\nu = 2$ plateau, we

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[1]We are able to reach $\nu = 1$ close to 5.8T, however it is not shown in this Hall scan due to the magnet overheating at high fields.

park the QPC top and bottom gates at their depletion voltages, -0.5V, and search for a field value where $R_d = R_{xy} = \frac{1}{2}\frac{h}{e^2}$. This field value was found to be 2.8T.

We form the three channels shown in Figure 6.3, and measure the diagonal resistance across the device, to determine which edge modes, if any, are transmitted through the QPCs.

6.2.2   Bottom channel

(a)   (b)

(c)   (d)
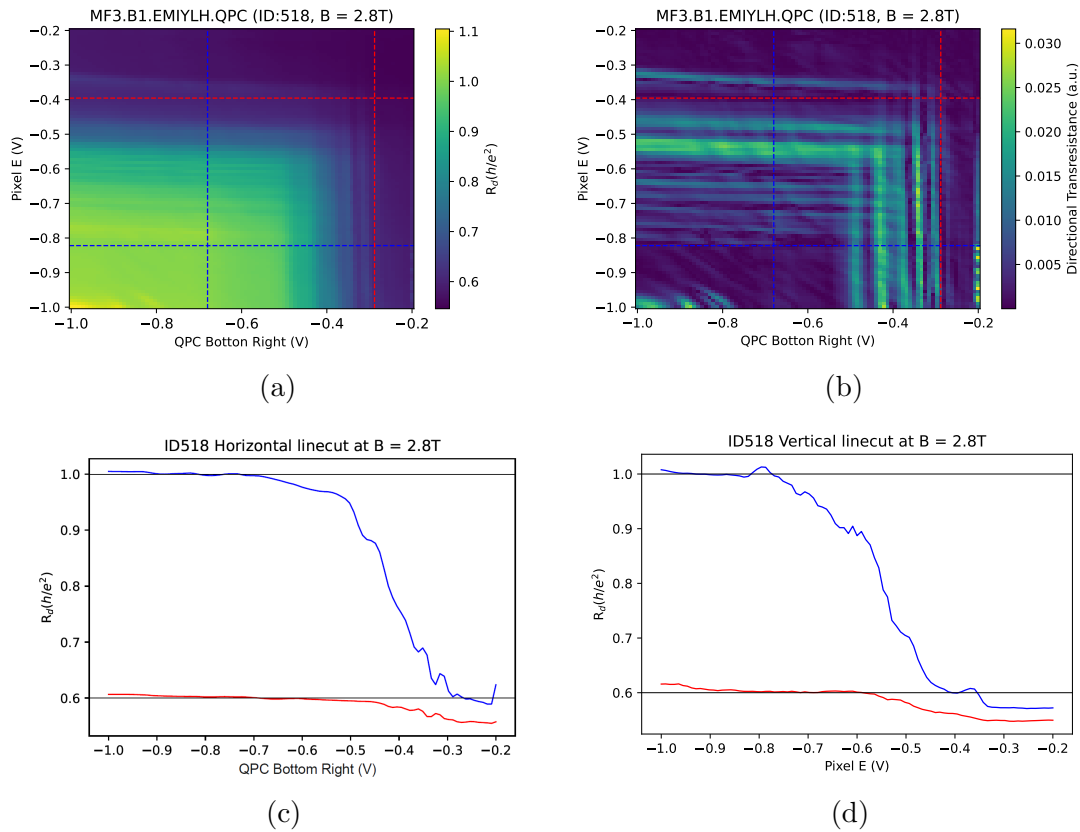
Figure 6.5: (a) Pixel E versus QPC Bottom gate, colormap represents the diagonal resistance R_d. (b) Pixel E versus QPC Bottom gate, colormap represents the transresistance, which is the numerical derivative of R_d along the diagonal, (c) Horizontal linecut of (a) along the red and blue horizontal lines, (d) Vertical linecut of (a) along the red and blue vertical lines.

As shown in Figure 6.3(c), we park pixel D at the same voltage as QPC top, and we use gate QPC bottom and pixel E to form a channel in the bottom part of the device. A measurement of the diagonal resistance, as a function of these two gates, can be found in Figure 6.5(a). The directional transresistance [2], or transresistance for short, is shown in Figure 6.5(b), to help us identify any flat regions.

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[2]This is the numerical derivative of R_d in the diagonal direction of 45°, plotted in arbitrary units, because we only care about the colorscale to help us identify flat features, and not the actual value of the transresistance.

When taking horizontal and vertical linecuts of 6.5(a) along the red and blue lines, the resistance converges to 0.6 and 1, in both directions. This is shown in figures 6.5(c) and (d), where the blue and red lines correspond to linecuts along the blue and red lines in Figure 6.5(a).

6.2.3   Top channel
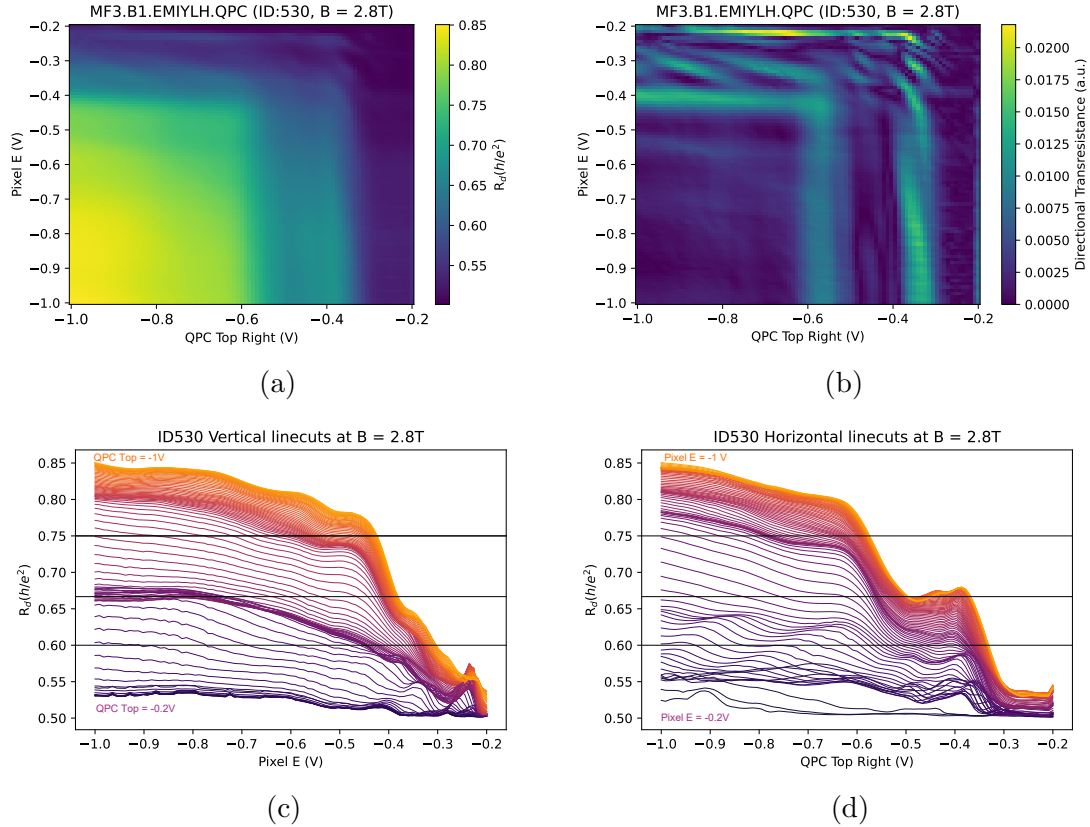
Figure 6.6: (a) Pixel E versus gate QPC top gate, colormap represents the diagonal resistance R_d. (b) Pixel E versus gate QPC top gate, colormap represents the transresistance, numerical derivative of (a) along the diagonal, (c) Vertical linecuts of (a), (d) Horizontal linecuts of (a).

Similarly, to form a channel at the top part of the device, we park pixel F at the same voltage as QPC bottom, as shown in Figure 6.3(a). The diagonal resistance as a function of these two gate voltages is found in Figure 6.6(a), and the corresponding transresistance in Figure 6.6(b). Figures 6.6 (c) and (d) show horizontal and vertical linecuts of (a). In these waterfall plots, as an example take Figure 6.6(c), dark purple corresponds to low magnitude gate voltages on gate QPC Top, and orange corresponds to the more negative values of gate QPC Top. The same argument is true for the colorscale of Figure 6.6(d) and the value of pixel E.

From the vertical linecuts in Figure 6.6(c), we can identify that many lines converge towards $R_d = 2/3R_0$. Many lines bunched up together in Figure 6.6(c)

signify a plateau in 6.6(d), at the same value. From these two waterfall plots, we can identify that feature $R_d = 2/3R_0$ is enhanced.

6.2.4 Middle channel

(a)   (b)
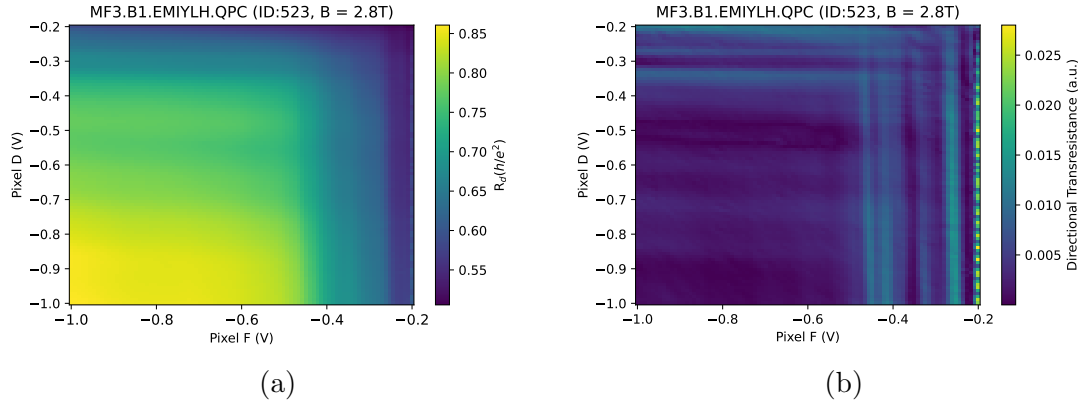
Figure 6.7: (a) Pixel D versus pixel F, colormap represents the diagonal resistance R_d. (b) Pixel D versus pixel F, colormap represents the transresistance, numerical derivative of (a) along the diagonal.

Finally, to form a channel in the middle of the device, we park QPC top and QPC bottom at their depletion voltage, as shown in Figure 6.3(b). Then, we use pixels D and F to form a channel between them. After reviewing the horizontal and vertical linecuts of Figure 6.7, we cannot identify any convergence towards a plateau in the diagonal resistance.

6.3 Simple QPC results

The same wafer was used to fabricate interferometers for another project [29]. The device is shown in Figure 6.8(a). The left QPC, which is just a simple split gate, was operated in the same regime as the device in Figure 6.1. The purpose of these measurements, is to compare the data of a simple QPC on the same material, with the data of a more complex, top gated design, such as the 3×2.

The bulk is parked at $\nu = 2$, and the top versus bottom QPC gates are scanned from zero volt. The diagonal conductance across the device is measured, and can be found in Figure 6.8(b). When taking a horizontal and vertical linecut of (a), we can see from figures 6.8(c) and (d) that conductance converges to $\nu = 2, 1, 0$.

(a)

(b)

(c)

(d)
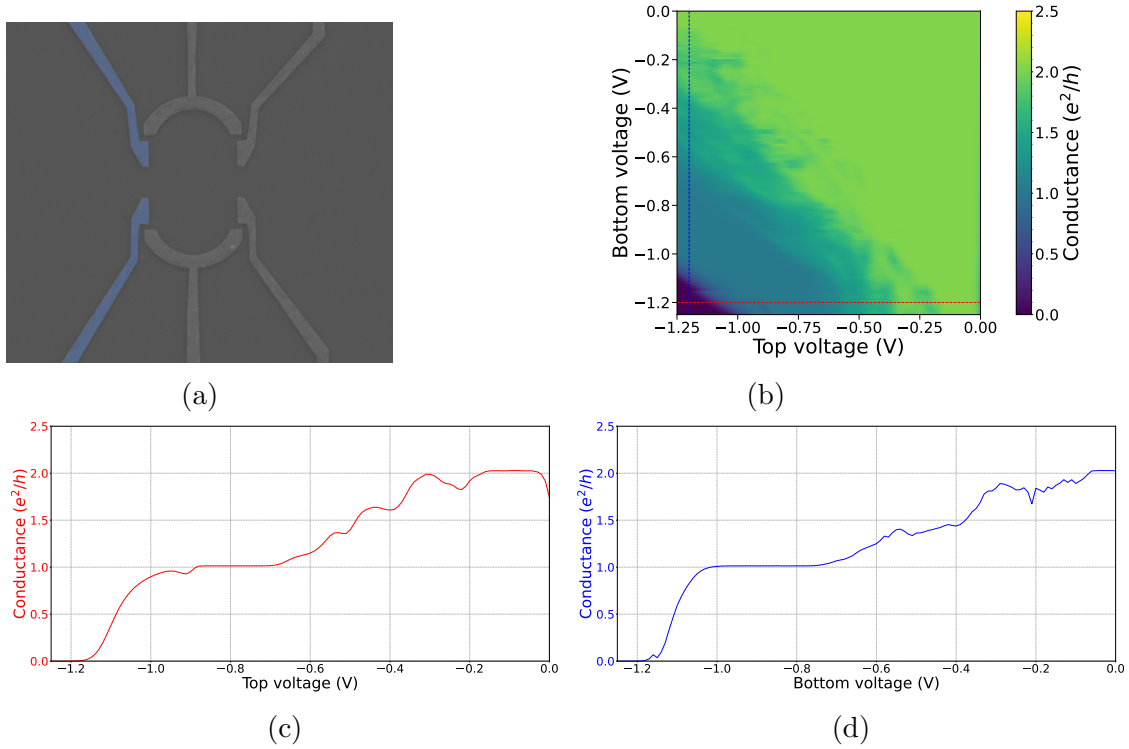
Figure 6.8: (a) Interferometer device fabricated on the same material as the 3×2 device of Figure 6.1. We use the left QPC shown in blue. (b) Diagonal conductance G_d as a function of the top and bottom QPC gates, (c) and (d) are linecuts of (b) along the red and blue lines.

6.4   Discussion
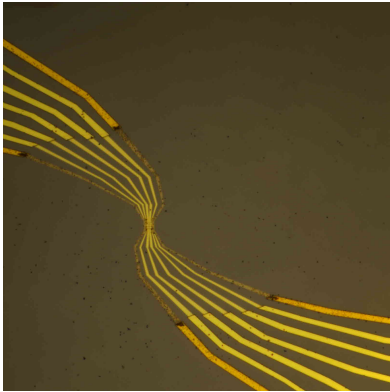
Figure 6.9: HfO$_2$ dots caused by oxide layer deposition between the first and second layers of gates.

Before commenting on the results, it should be noted that on this chip there was a fabrication problem, related to the HfO$_2$ layer grown between the first and second layer of gates. As seen in Figure 6.9, some small black dots were created in the ALD, and they are localized close to the first layer gates[3]. After performing EDS analysis on them, we have concluded that these dots are excess HfO$_2$ of unknown origin. We believe that some exist inside the channel as well, under the second layer gates. Such surface defects could localize charges underneath the gates, leading to reduced mobility in the channel.

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[3]One can find more information on these HfO$_2$ abnormal growth in Appendix A, under the alias 'popcorns'. Note that in this device, the popcorns are much more sparse and do not swallow the gates, as seen in the pictures in the Appendix.

The data presented in section 6.2 are preliminary results achieved within a limited time frame. Due to the time constraints, we didn't fully exploit the voltage space that this devices has to offer, and similarly were not able to perform a more careful study the observed features. As a result, we can only comment on what we see in the existing data, and speculate on what some features might be.

In the bottom channel data, we can see that when taking linecuts in both the horizontal and vertical directions, the diagonal resistance converges to 0.6 and 1. These two numbers correspond to filling factors 5/3 and 1 respectfully, which we also identify in the bulk material. These plateaus could be resistance plateaus originating from an edge state of that filling factor being transmitted through the QPC, or they could be saturation curves.

Another comment is that in Figure 6.5(b), the transresistance shows some faint diagonal lines that span the background of the whole figure. Diagonal transconductance, or transresistance peaks, in such gate versus gate maps are believed to originate from localization in the channel, as explained in [36]. Another thing they could be are charge jumps in accidental quantum dots. However, the very prominent horizontal and vertical bright lines in the transresistance are not explained in any literature we have come across. One possibility is that the flat features in between the bright lines, are resonance plateaus due to disorder or impurities, and the bright peaks just signify the change from one such plateau to the other. The next measurement plan would be to retake these gate versus gate maps, at different magnetic fields and temperatures. Impurity and disorder induced effects have a different expected behaviour, as a function of the magnetic field and temperature, compared to fractional quantum Hall states.

In the top channel, from the collective behaviour of the linecuts taken in the vertical direction (figure 6.6(c)), we can see many lines collectively converging towards $R_d = 2/3R_0$. This corresponds to a filling factor $\nu = 3/2$. Further study is needed to understand this feature. If it is the $\nu = 3/2$ fractional state, it should also stretch in magnetic field scans for constant gate voltage values. Such measurements were not performed, and are crucial to gain an in-depth understanding of the data. Another parameter to be checked again is temperature; this 3/2 feature is expected to disappear with increasing temperature, if it is indeed a fractional plateau. However, if it is localization related, it should not care about the temperature as much as a fractional state would.

Finally, in the middle channel, there are no plateauing features in the horizontal and vertical linecuts. If most of the features that we observe in the other two channels are localization related, this indicates that this channel is relatively clean, since no distinct diagonal bright lines appear in the transresistance.

Taking into consideration all the forementioned observations, the main conclusion that we come to is that having the ability to shift the channel laterally is achieved with this device. This attribute proves to be highly valuable for the device. From the data presented for each channel, we can conclude that all three channels behave differently. The disorder and localization background seems to be different in all three channels; and the possible resistance plateaus that each

channel exhibits are different. In the top channel we can see that there might be an enhanced feature around $\nu = 3/2$. On the other hand, in the bottom channel we can see that there could be some feature at $\nu = 5/3$ and $\nu = 1$. In the middle channel, no features are highlighted.

Lastly, we discuss the simple QPC data shown in Figure 6.8. We can see that a split gate QPC, fabricated on the same material, transmits integers $\nu = 2, 1, 0$, but nothing in-between, at least for this particular QPC in this particular measurement. What is evident here is that there are no added degrees of freedom to tune it further. More gates could potentially help in the appearance of transmitted fractions. Additionally, from the conductance figure we can identify some diagonal features that could be attributed to localisation. The data comparison indicates that the 3×2 device indeed behaves differently, compared to a simple split gate. Whether the differences are advantageous or not needs to be investigated further.

In this work [36], the authors compare self-consistent simulation results of a simple split gate QPC, and a QPC with a center gate. They come to the conclusion that the latter device with a center gate has a wider incompressible region of constant density in the channel for the states $\nu = 2, 1, 1/3$, compared to the simple QPC. At the same time, a larger incompressible region makes it more likely that a disorder potential fluctuation could create a localisation inside the incompressible region.

Consequently, from their results we can conclude that our devices, owning to their unique geometry of always having a center gate over the channel, are more prone to localization in the channel. This could explain the diagonal bright peaks in the bottom and top channels.

Chapter 7

Conclusions and Outlook

In this thesis, we have successfully fabricated two complex gate geometry quantum point contact, or one-dimensional ballistic wire devices in GaAs. Our motivation for complicating what would normally be a straightforward split gate device, is due to it's inherent limitation in tuning the channel's potential. Various parameters, including unpredictable factors like disorder, have a significant impact on the transmission properties of QPCs. Particularly in the fractional quantum Hall regime, the states are extremely sensitive to the device's geometry.

To gain better control over these parameters, we employ a technique of pixelating the active channel with gates. This approach allows us to have more knobs to turn, enabling fine-tuning of the confinement potential of QPCs. A noteworthy addition to our devices is the introduction of an extra layer of gates, which increases the dimensionality of our design by one. These additional gates serve a dual purpose: firstly, they screen any metal that falls over them, preventing undesired interactions between excess gate pieces and the 2DEG, and secondly, they serve as a mask for the second layer of gates, allowing us to form more intricate gates in hard to reach locations.

Additionally, we conducted low-temperature characterization of both devices. During the evaluation of the 3×3 device, we discovered that the inclusion of the screening gate was effective in resolving the connector issue. However, it introduced an unexpected complication. The gate was very big, almost spanning the entirety of the channel, resulting in it having a much stronger impact. Continuous operation of the gate at a negative voltage led to the creation of a negative potential background between the pixel gates. Unfortunately, with this particular device, we were unable to demonstrate the main objective of our project, which is to establish the superiority of a complex gate geometry device over a simple split gate device. Nevertheless, this experience served as inspiration for the development of the most recent generation of devices.

Let us now delve into the latest findings from the characterization of the 3×2 device. Through the operation of a single column within the device, we obtained preliminary data of QPC tunnelling experiments within the quantum Hall regime. One important feature of this device is its capability to laterally shift the channel

in three different locations. This feature allows us to navigate away from regions with clear signs of disorder. Furthermore, a top gate is positioned above each lateral position. This unique configuration opens up possibilities for future investigations into the impact of top gates on the QPC potential, and specifically on the how they affect the formation of incompressible regions within the channel. Regarding our measurements, we were able to observe certain features that provide a promising outlook, encouraging further in-depth examination in future studies.

One significant limitation that became evident over the past year is the absence of predictive simulations, specifically tailored for multilayered gate designs. Even though the absence of such a tool has sharpened our intuition, self-consistent simulations capable of accurately modeling how the gates influence the 2DEG would have greatly assisted us during the device design process, particularly in determining optimal gate dimensions. Access to such multilayered simulations, that include metal screening effects, could have resulted in more targeted device designs.

For instance, in the case of the 3×3 device, simulations could have predicted the influence of the screening gate beforehand. Furthermore, in our latest 3×1 and 3×2 devices, simulations could have shed light on potential occurrence of accidental dots. The narrow spacing between the pixels increases the likelihood of unintentional dot formation, and indeed, in certain measurements, we have observed indications that some accidental dots may have formed.

Lastly, we will discuss the introduction of the screening layer in our devices. We are confident that the screening layer effectively fulfills its primary purpose, which is to screen specific parts of the gates in our design. However, with the incorporation of an additional gate layer, we require another layer of HfO_2 in between the gate layers to electrically isolate them. Consequently, the second layer gates, which are the primary gates influencing the 2DEG, are laying over a double HfO_2 layer.

It is known that HfO_2 layers are susceptible to defects, which can serve as charge traps and potentially modify the electronic properties of the device by localizing charges. These defects become particularly relevant in the context of the fractional quantum Hall regime, and double HfO_2 means double trouble. The main challenge we face in the 3×2 device lies in distinguishing genuine fractional states from localization signatures, which may arise due to these charge traps.

Appendix A

Fabrication Recipes

A.1   Device SCQPC∅

Material: MF1 (M5-30-18.1)

General Cleaning

It's a good practise to clean the chip before every process:

- Acetone (5 min)
- IPA (2 min)
- Blowdry

1. Substrate Cleaning

- 1-3 Dioxolane (15 min)
- Acetone (5 min)
- IPA (2 min)

2. First Alignment Marks

Metal alignment marks are needed for exposing the mesa, ohmics and new set of alignment marks, since the ohmic annealing will destroy these marks. At least four sets of marks should be exposed in this stage.

- General cleaning

- Spin PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 2 nA, 60um
Exposure conditions	WF = $600\mu m$ 60K dots Dose = 720 $\mu C/cm^2$ Dose time = 0.36 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Metal Deposition in AJA:

    - Ti (5nm, Rate = 1Å/sec)
    - Au (100nm, Rate = 1Å/sec for the first 20nm, then increase to 2Å/sec)

- Liftoff: Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

Note: In most cases 50nm of Au is enough for alignment marks, however since very tall resist stacks are used in this recipe I found the visibility during alignment to be very poor with less Au.

3. Mesa

- General cleaning

- Spin PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 $\mu s/dot$

Beamer	PEC: GaAs PMMA 200nm
	Uniform Clearing

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Post Bake @ $115°C$ for 2 min

- Etching Solution: MilliQ : H_3PO_4: $H_2O_2(30\%)$ (150:15:3 mL), Stirrer speed 2

- Etch time 188 sec (Average etch depth = 342nm)

- Vigorously rinse in MilliQ for 60 sec

- Resist strip in Acetone for 10 min, IPA 2min, blowdry

Notes: We found that the etching quality depends on the timing of adding the chemicals in the solution, so this diagram can be referred as to how to prepare the etching solution.

Figure A.1: Mesa etchant preparation timing

Once the etching solution is prepared, the chip is placed at the bottom of the beaker close to the stirrer. If the 2DEG is deep (say more than 200nm) the chip is moved around 90° every 30 seconds. If the 2DEG is shallower then the chip can be moved around 90° every 10 seconds.

4. Ohmics

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 μs/dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clearing

- Develop in MIBK:IPA (1:3) for 45 sec, then in IPA for 10 sec, blowdry vertically

- Ash for 1 min

- RF Milling at AJA2, run recipe FF_SHIV_RF_ETCH_30_50W_2MIN

- Metal Deposition in AJA2:

  - Ge (60nm, Rate = 1Å/sec)
  - Pt (30nm, Rate = 0.5Å/sec)
  - Au (120nm, Rate = 1Å/sec)

- Liftoff in 1-3 Dioxonale for at least 1hr. Squeeze acetone on chip, check at microscope , rinse with IPA and blowdry

- Ash for 1 min

- Rapid Thermal Annealing (RTA)

  - Forming Gas N2/H2
  - Recipe: ML_450C_1m

5. First Dielectric Deposition: ALD1

- General cleaning

- Ash for 2 min

- Material: HfO_2, 125 cycles ($\sim$ 15nm)

- Prebake

  - Bake chamber at 250°C for 2hrs
  - Bring chamber temperature back to 90 °C before placing chip

- Conditions

  - Temperature = 90°C
  - Nitrogen = 90sccm
  - Hf pulse time 0.2sec, 180sec pulse purge
  - Water pulse time 0.5sec, 180sec pulse purge

6. Second Alignment Marks

Same recipe as alignment marks 1.

7. First Layer Fine Gates

- General cleaning

- Spin PMMA A3 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 100 pA, 40um
Exposure conditions	$WF = 150\mu m$ 60K dots Dose = 700 $\mu C/cm^2$ Dose time = 0.4375 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (3nm, Rate = 1Å/sec)
  - Au (15nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane ideally overnight. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

8. First Layer Outer Gates

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 500pA (40um) and 20nA (250um)

Exposure conditions 500pA, 20nA	WF = $300\mu m$, $600\mu m$
	60K dots , 20K dots
	Dose = 700 $\mu C/cm^2$, 700 $\mu C/cm^2$
	Dose time = 0.35 $\mu s/dot$, 0.315 $\mu s/dot$
Beamer 500pA, 20nA	PEC: GaAs PMMA 200nm, Optimal Contrast, GaAs PMMA 200nm, Uniform Clearing

- Develop in MIBK:IPA (1:3) for 55 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1min

- Metal Deposition in AJA1 with 60rpm rotation:

  - Ti (10nm, Rate = 1Å/sec)
  - Au (400nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

9. Second Dielectric Deposition: ALD1

Same recipe as first dielectric deposition.

10. Second Layer Fine Gates

- General cleaning

- Spin Csar 13 @ 6000rpm, CR1 spinner Process 8: Program 13 (custom - anyone can mess with this)

  - 1/3: Ramp to 500rpm, 10 sec
  - 2/3: Ramp to 6000rpm, stay 60 sec
  - 3/3: Ramp to 0rpm, 10sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 100 pA (40um)
Exposure conditions	WF = $150\mu m$
	60K dots
	Dose = 290 $\mu C/cm^2$
	Dose time = 0.18 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in n-Amyl Acetane for 60 sec (don't stir), then IPA for 10 sec (stir slowly), blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (5nm, Rate = 1Å/sec)
  - Au (32nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

11. Second Layer Outer Gates

Same recipe as first layer outer gates.

A.2 Device A3.MF3.LARSER.FQHI_2

Material: MF3 (M5-19-15.1)

1. Gallium Removal

- Spin resist on the wafer to protect the front side - any thick resist

- Bake it on a CR wipe for a few minutes on the hotplate otherwise the Ga will melt on the hot plate

- Take some aluminum foil and wrap the hot plate, it should lay very straight

- Place the wafer on the foiled hotplate, with the backside touching the foil to melt the Ga

- After a minute, take the wafer and flip it on a CR wipe, so that the front face touches the wipe and the backside is facing up

- Take many Ga removal swabs and a medium beaker with DI water, dip the swab in the water and wipe away the Ga. Found it best to do this not with the tip f the swab but with the two flat sides. Some Ga should come off but it cools down very fast

- Once no more Ga can be removed, place it back on the foil and repeat the process until most as much Ga as possible can be removed

2. Substrate Cleaning

- 1-3 Dioxolane (15 min)

- Acetone (5 min)

- IPA (2 min)

3. First Alignment Marks

- General cleaning

- Spin PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 2 nA, 60um
Exposure conditions	WF $= 600\mu m$
	60K dots
	Dose $= 720\ \mu C/cm^2$
	Dose time $= 0.36\ \mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Metal Deposition in AJA:

    - Ti (5nm, Rate = 1Å/sec)
    - Au (100nm, Rate = 1Å/sec for the first 20nm, then increase to 2Å/sec)

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

4. Mesa

- General cleaning

- Spin PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF $= 600\mu$m 20K dots Dose $= 700\mu C/cm^2$ Dose time $= 0.315\ \mu s/$dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clearing

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Post Bake @ $115°C$ for 2 min

- Etching Solution: MilliQ : H_3PO_4: H_2O_2(30%) (150:15:3 mL), Stirrer speed 2

- Etch time 80 sec (Average etch depth $=$ 136nm)

- Vigorously rinse in MilliQ for 60 sec

- Resist strip in Acetone for 10 min, IPA 2min, blowdry

Notes: Detailed notes on the etching process can be found in the recipe found in A.1. Since this 2DEG is shallower the chip was rotated 90° every 10sec.

5. Ohmics

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF $= 600\mu$m 20K dots Dose $= 700\mu C/cm^2$ Dose time $= 0.315\ \mu s/$dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clear

- Develop in MIBK:IPA (1:3) for 45 sec, then in IPA for 10 sec, blowdry vertically

- Ash for 1 min

- RF Milling at AJA2, run recipe FF_SHIV_RF_ETCH_30_50W_2MIN

- Metal Deposition in AJA2:

    - Ge (60nm, Rate = 1Å/sec)
    - Pt (30nm, Rate = 0.5Å/sec)
    - Au (120nm, Rate = 1Å/sec)

- Liftoff in 1-3 Dioxonale for at least 1hr.Squeeze acetone on chip, check at microscope , rinse with IPA and blowdry

- Ash for 1 min

- Rapid Thermal Annealing (RTA)

    - Forming Gas N2/H2
    - Recipe: ML_450C_1m

6. Dielectric Deposition: ALD1

- General cleaning

- Ash for 2 min

- Material: HfO_2, 125 cycles ($\sim$ 15nm)

- Prebake

    - Bake chamber at 250°C for 2hrs
    - Bring chamber temperature back to 90 °C before placing chip

- Conditions

    - Temperature = 90°C
    - Nitrogen = 90sccm
    - Hf pulse time 0.2sec, 180sec pulse purge
    - Water pulse time 0.5sec, 180sec pulse purge

7. Second Alignment Marks

Same recipe as alignment marks 1.

8. First Layer Fine Gates

- General cleaning

- Spin PMMA A3 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 500 pA, 40um
Exposure conditions	WF = $150\mu m$
	60K dots
	Dose = 700 $\mu C/cm^2$
	Dose time = 0.0875 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- No ashing

- Metal Deposition in AJA:

    - Ti (4nm, Rate = 1Å/sec)
    - Au (16nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane ideally overnight. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

9. First Layer Outer Gates

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 500pA (40um) and 20nA (250um)
Exposure conditions 500pA, 20nA	WF = $300\mu m$, $600\mu m$
	60K dots , 20K dots
	Dose = 700 $\mu C/cm^2$, 700 $\mu C/cm^2$
	Dose time = 0.35 $\mu s/dot$, 0.315 $\mu s/dot$
Beamer 500pA, 20nA	PEC: GaAs PMMA 200nm, Optimal Contrast, GaAs PMMA 200nm, Uniform Clearing

- Develop in MIBK:IPA (1:3) for 55 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1min

- Metal Deposition in AJA1 with 60rpm rotation:

  - Ti (10nm, Rate = 1Å/sec)
  - Au (215nm, Rate = 1Å/sec for first 50nm, 2Å/sec for the rest))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

A.3   Device A1.MF3.LARSER.FQHI_3

Material: MF3 (M5-19-15.1)

1. Gallium Removal

Same as A3.MF2.LARSEN.FQHI_2 recipe.

2. Substrate Cleaning

- 1-3 Dioxolane (15 min)

- Acetone (5 min)

- IPA (2 min)

3. First Alignment Marks

- General cleaning

- Spin PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 2 nA, 60um
Exposure conditions	WF = $600\mu m$
	60K dots
	Dose = 720 $\mu C/cm^2$
	Dose time = 0.36 $\mu s/dot$

Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Metal Deposition in AJA:

  - Ti (5nm, Rate = 1Å/sec)
  - Au (100nm, Rate = 1Å/sec for the first 20nm, then increase to 2Å/sec)

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

4. Mesa

- General cleaning

- Spin PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 μs/dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clearing

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Post Bake @ 115°C for 2 min

- Etching Solution: MilliQ : H_3PO_4: H_2O_2(30%) (150:15:3 mL), Stirrer speed 2

- Etch time 80 sec (Average etch depth = 136nm)

- Vigorously rinse in MilliQ for 60 sec

- Resist strip in Acetone for 10 min, IPA 2min, blowdry

Notes: Detailed notes on the etching process can be found in the recipe found in A.1. Since this 2DEG is shallower the chip was rotated 90° every 10sec.

5. Ohmics

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 μs/dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clear

- Develop in MIBK:IPA (1:3) for 45 sec, then in IPA for 10 sec, blowdry vertically

- Ash for 1 min

- RF Milling at AJA2, run recipe FF_SHIV_RF_ETCH_30_50W_2MIN

- Metal Deposition in AJA2:

    - Ge (60nm, Rate = 1Å/sec)
    - Pt (30nm, Rate = 0.5Å/sec)
    - Au (120nm, Rate = 1Å/sec)

- Liftoff in 1-3 Dioxonale for at least 1hr.Squeeze acetone on chip, check at microscope , rinse with IPA and blowdry

- Ash for 1 min

- Rapid Thermal Annealing (RTA)

    - Forming Gas N2/H2
    - Recipe: ML_450C_1m

6. First Dielectric Deposition: ALD1

- General cleaning

- Ash for 2 min

- Material: HfO$_2$, 125 cycles ($\sim$ 15nm)

- Prebake

- Bake chamber at 250°C for 2hrs
- Bring chamber temperature back to 90 °C before placing chip

- Conditions

  - Temperature = 90°C
  - Nitrogen = 90sccm
  - Hf pulse time 0.2sec, 180sec pulse purge
  - Water pulse time 0.5sec, 180sec pulse purge

7. Second Alignment Marks

Same recipe as alignment marks 1.

8. First Layer Fine Gates

- General cleaning

- Spin PMMA A3 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 500 pA, 40um
Exposure conditions	WF = 150μm 60K dots Dose = 700 $\mu C/cm^2$ Dose time = 0.0875 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (4nm, Rate = 1Å/sec)
  - Au (16nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane ideally overnight. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

9. First Layer Outer Gates

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

- Exposure

Elionix 100kV	Current: 500pA (40um) and 20nA (250um)
Exposure conditions 500pA, 20nA	WF = $300\mu m$, $600\mu m$ 60K dots , 20K dots Dose = 700 $\mu C/cm^2$, 700 $\mu C/cm^2$ Dose time = 0.35 $\mu s/dot$, 0.315 $\mu s/dot$
Beamer 500pA, 20nA	PEC: GaAs PMMA 200nm, Optimal Contrast, GaAs PMMA 200nm, Uniform Clearing

- Develop in MIBK:IPA (1:3) for 55 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1min

- Metal Deposition in AJA1 with 60rpm rotation:

    - Ti (10nm, Rate = 1Å/sec)
    - Au (215nm, Rate = 1Å/sec for first 50nm, 2Å/sec for the rest))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

10. Second Dielectric Deposition: ALD1

Same recipe as first dielectric deposition.

11. Second Layer Fine Gates

- General cleaning

- Spin EL9 @ 4500rpm for 45sec, then A2 @ 4500rpm for 45sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 100 pA (40um)

Exposure conditions	WF = $150\mu m$
	60K dots
	Dose = 770 $\mu C/cm^2$
	Dose time = 0.4812 $\mu s/dot$
Beamer	PEC: GaAs PMMA 200nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45sec (don't stir), then IPA for 10 sec (stir slowly), blowdry vertically

- Ash for 1min

- Metal Deposition in AJA:

    - Ti (5nm, Rate = 1Å/sec)
    - Au (45nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

12. Second Layer Outer Gates

Same recipe as first layer outer gates, but evaporate 225nm of Au instead.

13. Third Dielectric Deposition: ALD1

Same recipe as first dielectric deposition.

14. Third Layer Fine Gates

- General cleaning

- Spin EL9 @ 4000rpm, then PMMA A4 @ 4000rpm

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 100 pA (40um)
Exposure conditions	WF = $150\mu m$
	60K dots
	Dose = 608 $\mu C/cm^2$
	Dose time = 0.38 $\mu s/dot$

Beamer	PEC: GaAs PMMA 200nm, Optimal Contrast

- Develop in MIBK:IPA(1:3) for 450 sec (don't stir), then IPA for 10 sec (stir slowly), blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (5nm, Rate = 1Å/sec)
  - Au (100nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

15. Third Layer Outer Gates

Same recipe as first layer outer gates but evaporate 235nm of Au instead.

A.4 Device B1.MF3.EMILYH.QPC

Material: MF3 (M5-19-15.1)

1. Gallium Removal

Same as A3.MF2.LARSEN.FQHI_2 recipe.

2. Substrate Cleaning

- 1-3 Dioxolane (15 min)

- Acetone (5 min)

- IPA (2 min)

3. First Alignment Marks

- General cleaning

- Spin PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 2 nA, 60um
Exposure conditions	WF = $600\mu m$ 60K dots Dose = 720 $\mu C/cm^2$ Dose time = 0.36 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Metal Deposition in AJA:

  - Ti (5nm, Rate = 1Å/sec)
  - Au (100nm, Rate = 1Å/sec for the first 20nm, then increase to 2Å/sec)

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

4. Mesa

- General cleaning

- Spin PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 $\mu s/dot$
Beamer	PEC: GaAs PMMA 200nm Uniform Clearing

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1 min

- Post Bake @ 115°C for 2 min

- Etching Solution: MilliQ : H_3PO_4: H_2O_2(30%) (150:15:3 mL), Stirrer speed 2

- Etch time 80 sec (Average etch depth = 136nm)

- Vigorously rinse in MilliQ for 60 sec

- Resist strip in Acetone for 10 min, IPA 2min, blowdry

Notes: Detailed notes on the etching process can be found in the recipe found in A.1. Since this 2DEG is shallower the chip was rotated 90° every 10sec.

5. Ohmics

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 45 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 20 nA, 250um
Exposure conditions	WF = 600μm 20K dots Dose = $700\mu C/cm^2$ Dose time = 0.315 μs/dot
Beamer	PEC: GaAs PMMA 200nm Uniform Clear

- Develop in MIBK:IPA (1:3) for 45 sec, then in IPA for 10 sec, blowdry vertically

- Ash for 1 min

- RF Milling at AJA2, run recipe FF_SHIV_RF_ETCH_30_50W_2MIN

- Metal Deposition in AJA2:

  - Ge (60nm, Rate = 1Å/sec)
  - Pt (30nm, Rate = 0.5Å/sec)
  - Au (120nm, Rate = 1Å/sec)

- Liftoff in 1-3 Dioxonale for at least 1hr.Squeeze acetone on chip, check at microscope , rinse with IPA and blowdry

- Ash for 1 min

- Rapid Thermal Annealing (RTA)

    - Forming Gas N2/H2
    - Recipe: ML_450C_1m

6. First Dielectric Deposition: ALD1

- General cleaning

- Ash for 2 min

- Material: HfO_2, 125 cycles ($\sim$ 15nm)

- Prebake

    - Bake chamber at 250°C for 2hrs
    - Bring chamber temperature back to 90 °C before placing chip

- Conditions

    - Temperature = 90°C
    - Nitrogen = 90sccm
    - Hf pulse time 0.2sec, 180sec pulse purge
    - Water pulse time 0.5sec, 180sec pulse purge

7. Second Alignment Marks

Same recipe as alignment marks 1.

8. First Layer Fine Gates

- General cleaning

- Spin PMMA A3 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 500 pA, 40um

Exposure conditions	WF = 150μm
	60K dots
	Dose = 700 $\mu C/cm^2$
	Dose time = 0.0875 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in MIBK:IPA (1:3) for 45 sec, then IPA for 10 sec, blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (4nm, Rate = 1Å/sec)
  - Au (16nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane ideally overnight. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

9. First Layer Outer Gates

- General cleaning

- Spin EL9 + EL9 + PMMA A4 @ 4000rpm for 60 sec

- Bake @ 185°C for 2 min after each layer

- Exposure

Elionix 100kV	Current: 500pA (40um) and 20nA (250um)
Exposure conditions 500pA, 20nA	WF = 300μm, 600μm
	60K dots , 20K dots
	Dose = 700 $\mu C/cm^2$, 700 $\mu C/cm^2$
	Dose time = 0.35 $\mu s/dot$, 0.315 $\mu s/dot$
Beamer 500pA, 20nA	PEC: GaAs PMMA 200nm, Optimal Contrast, GaAs PMMA 200nm, Uniform Clearing

- Develop in MIBK:IPA (1:3) for 55 sec, then IPA for 10 sec, blowdry vertically

- Ash for 1min

- Metal Deposition in AJA1 with 60rpm rotation:

  - Ti (10nm, Rate = 1Å/sec)
  - Au (215nm, Rate = 1Å/sec for first 50nm, 2Å/sec for the rest))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

10. Second Dielectric Deposition: ALD1

Same recipe as first dielectric deposition.

11. Second Layer Fine Gates

- General cleaning

- Spin Csar 9 @ 4000rpm

- Bake @ 185°C for 2 min

- Exposure

Elionix 100kV	Current: 100 pA (40um)
Exposure conditions	WF = $150\mu m$ 60K dots Dose = 200 $\mu C/cm^2$ Dose time = 0.125 $\mu s/dot$
Beamer	PEC: GaAs PMMA 100nm, Optimal Contrast

- Develop in n-Amyl Acetane for 60 sec (don't stir), then IPA for 10 sec (stir slowly), blowdry vertically

- No ashing

- Metal Deposition in AJA:

  - Ti (5nm, Rate = 1Å/sec)
  - Au (45nm, Rate = 1Å/sec))

- Liftoff Leave in 1-3 Dioxolane for at least 2 hours. Then squeeze acetone on chip, inspect at microscope, IPA rinse, blowdry

12. Second Layer Outer Gates

Same recipe as first layer outer gates but evaporate 225nm of Au instead.

A.5 General tips and tricks

Disclaimer: This section troubleshoots many problems that I encountered during fabrication, however when I claim something, it doesn't mean it's a general rule or good practise that should be followed. These are just notes on my

experience that might be helpful to someone. Fabrication is full of superstition, and so are (some of) these notes:)

Pictures

Take pictures of every step, many things can go bad in fab very fast and very easily, the only way to know what caused a problem is to have before and after pictures of every step, both in bright and dark field.

How to inspect a chip after liftoff at the microscope

Take the chip out of 1-3 Dioxolane and place at the bottom of a clean plastic beaker [1] and while holding down with the tweezers, squeeze acetone through the acetone bottle on the chip until you see most of the gold disappear from the surface. This should be done very quickly, the chip shouldn't be exposed to air before final approval.

You could have a second clean plastic beaker and move the chip to the second beaker when the acetone level is close to the surface of your chip. Again this process has to be done quickly. Always keep the chip in liquid until inspection because if the chip is exposed to air the metal dries out on the surface and you don't have a chance to fix something.

Prepare a curved lens with IPA under the microscope and place the chip inside to inspect (5X-10X max). Check dark field mostly to see if there are any stuck pieces of metal where they shouldn't be. Once it's fine squeeze some IPA on top for a few seconds and then blow dry vertically with N2.

Development: Stirring vs no stirring

Generally when developing small structures like the first or second layer fine gates, I found better results when *no stirring* was performed during development and just holding the chip in the developer for that amount of time. When stirring was performed for these small structures I noticed some resist walls collapsing, especially in the second layer fine gates where a very big aspect-ratio was required. This effect disappeared when I stopped stirring. However I did stir slowly when moving to IPA for 10 seconds to make sure the developer was gone and the structures didn't overdevelop and spread to the sides. In bigger structures such as outer gates, ohmics and the mesa, since there is no danger of fragile resist walls collapsing *stirring* is encouraged while developing.

How underdevelopment looks

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[1] wouldn't suggest using CR glass beakers, they are shared among many people and is an easy contamination source - use your own glass or just plastic
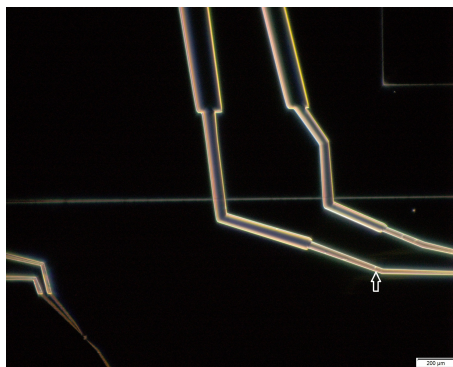
Figure A.2: Example of how under-developed resist looks like in dark field

A 500pA current is used to expose the finer outer gates, while 20nA is used for the rest (climb mesa and bond pads). As a rule 5um wide gates and above can be exposed with 20nA, so when the gates reach that size its good to switch current to make exposure faster (however be careful if the gates are close to each other, then 20nA might be too high). Since all these parts are exposed at the same time, they are developed together. The 500pA parts need more time to develop than the 20nA so when I followed the 45second recipe for development, it worked fine for the 20nA areas but not for the 500pA areas. The tiny white dots are a sign of underdevelopment. I increased the time to 55seconds and they went away. It is not good to underdevelop gates as they might break at points and be disconnected.

Resist Problem - Metal sticking on sidewalls
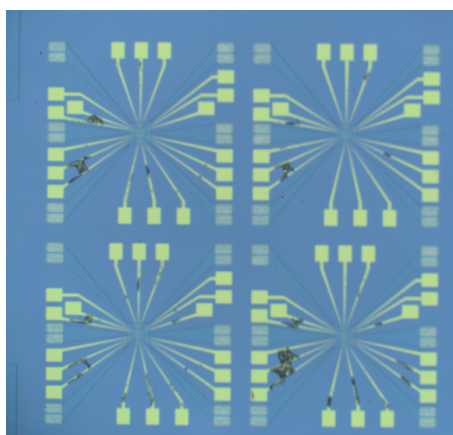
Figure A.3: Gold from second layer fine gates evaporation sticking on the sides of the first layer outer gates after liftoff

For this chip the the first layer fine gates and outer gates were patterned, and then a HfO_2 layer was grown. To achieve fine features in the second layer fine gates A2 was used. Since A2 has a thickness of around 50nm, it wasn't able to fully cover and protect the first layer outer gate sides, that's why metal is sticking there. The outer gates are around 150nm thick. To fix this, A3 which is around 100nm was used, and the issue was solved.

For my chip my mesa height was around 350nm, so for my second layer inner gates I had a hard time since I was looking for a resist that is thick enough to fully protect the mesa walls and the first layer outer gates so that metal wouldn't stick, but also at the same time I had to get features around 30nm in the second layer fine gates. I think this is called aspect-ratio, the resist needed to have a big aspect ratio. I decided to go with csar13 @ 6000rpm which gives around 300nm. This seems to have worked well in protecting the mesa and first layer, and after a lot of trial and error despite its height it was able to give great resolution and fine features.

Generally I would suggest to think about the topography of the chip when choosing a resist. The resist should be tall enough (again there is no exact measure of how tall is tall enough, testing might be needed. But for sure if 50nm resist is not tall enough to cover 150nm tall gates, and 100nm resist is enough, this is one data point to consider).

Spin Coating

For multi-layer spin coating (ohmics for example) it's possible to try spinning the chip without any resist, pause the setting and deposit the resist while it's spinning. Then continue the program. This might help if the edges are very tall and it causes very low visibility in mark registration.

How much metal to evaporate to climb mesa

Generally the rule is to evaporate metal such that the thickness of the outer gates is the height of your etched mesa + 50nm to ensure the gates are connected as shown in the picture below:
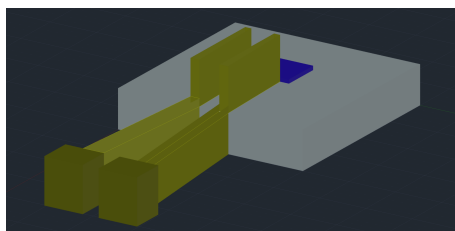
Figure A.4: Outer gates climbing mesa

The mesa heights may vary depending on the etching quality. Taking many scans on the profilometer to see how much the mesa height varies is good, and then make sure that the metal will climb even the tallest parts of the mesa.

Elionix misalignment of 50nm order

Misalignment of the order of 50nm was observed between the two layers of the SCQPC0 design. This was eliminated when I waited for at least half an hour after conditioning the beam. This allows the current to stabilize and also the stage to thermalize inside the main chamber before exposure. The process is to load the chip and condition the beam, wait for half an hour and then move pattern and continue.

Misalignment of this order is only important for very fine features such as the first and second layer fine gates where 100pA is used. For bigger features 30 minute wait is not necessary, 15 minutes is enough.

Elionix mark registration

If something happens and some marks are lost (maybe a corner breaks off), other marks can be used to form a reference frame. The set of four marks doesn't necessarily need to form a rectangle. On one chip the corner broke off and I lost all marks on the top left side, I managed to complete the exposure by using two marks from the top right side as marks C and D.

Cold development (CD)

As a general rule, cold development works with higher doses than room temperature development. I tried both cold development of PMMA and CSAR resists.

PMMA: I started using cold development for PMMA A3. For MilliQ water I initially used the one in the squeeze bottle in the HF bench. I then learned that nobody knows where that water comes from, and if it even is MilliQ or DI water, so my results wouldn't be reproducible if I continued using that water. Then I tried using tap MilliQ water. This made things very bad, the edges of my gates were very rough and ugly. Other people experienced similar things with cold development using the tap MilliQ, so we decided to stop using CD and stick with room temperature development of PMMA, MIBK:IPA (1:3) @ RT since it has many advantages over the CD. First of all it is reproducible, you will always get the same results. Also you can very good resolution and fine features with it, as a rule I found that after a dose-bias test A2 RT development can give fine features of around 20nm, and similarly A3 @ RT can give fine features of around 30nm. For fine features like this i suggest not stirring while developing (read section above).

CSAR: Only tried once with cold n-Amyl Acetane and rince in cold IPA. Didn't work for me since I didn't know that CD needs higher doses, but RT CSAR development with n-Amyl Acetane works fine.

Overall after trying out all possible combinations I find that room temperature development of these two resists is the safest way to go, with no trade offs. The results are reproducible and 20-30nm features can easily be achieved with correct resist thickness choice.

ALD 1 chamber contamination + steps

The chamber for the SCQPC0 fabrication run was baked at 150deg for half an hour to clean it. This is not enough as abnormal growths and dots were observed after the second oxide layer on this chip. Two more dummy chips show similar dots after the ALD-same process and recipe, but not it doesn't show up in all of our tries. For example, it doesn't show up after the mesa ALD so we have to conclude that this contamination is random. Also when placing a witness chip remember to deep clean it very good as this can be another source of contamination, and also ash for

2 minutes. Follow the next steps to overcome this problem:

- Ash before for 2 minutes, to make sure you get rid of anything organic

- Bake chamber at 250deg for 2 hours before loading

This fixed the issue temporarily, but then it appeared again. We still don't understand how it is created. We believe it is substrate related to GaAs, or at least the pieces that we use. It also only appeared on the second layer of ALD, meaning when there already was one layer on the chip they became obvious after deposition of the second layer. This is how they look in SEM, and we concluded after EDS analysis that they are abnormal growths of HfO_2.
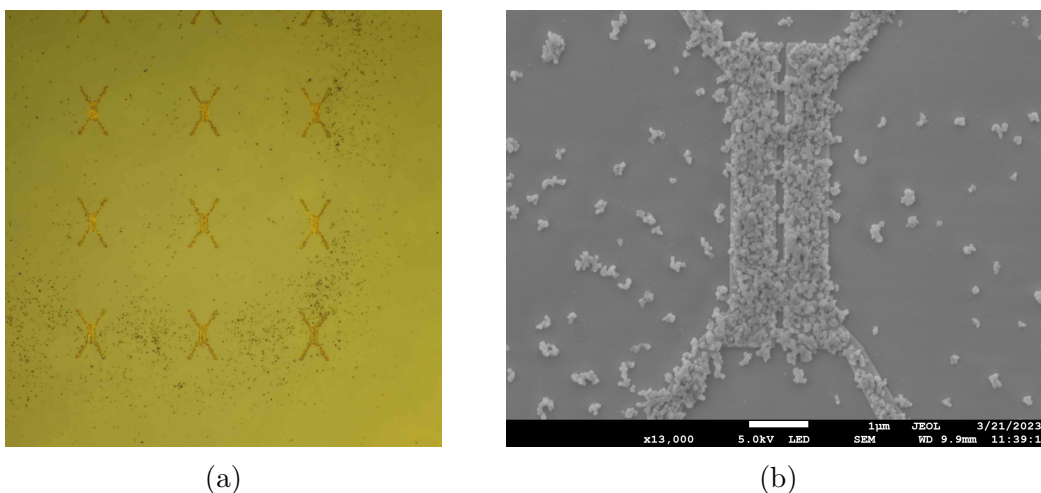
(a)   (b)

Figure A.5: How the ALD dots aka popcorns look like. They are not only localized around the gates, they span several microns.

Carbon tape stuck on the backside of the chip

It is common to test the ohmics of a chip at the probe station to check if they are conductive before continuing with the fabrication run. This can be done with and without carbon taping the chip to the probe station, however if the chip slides a lot when engaging the needle, carbon tape can be used. Since Ga removal was done on the backside of these chips, the backside was generally a bit rough; this resulted in a large amount of carbon tape to stick to the backside of the chip after testing at the probe station.

First aid step 1 is to soak a CR wipe with acetone and wipe the backside of the chip in zig-zag movements to remove excess carbon tape, but in the case that a piece of tape is stuck to the backside, this is not effective. When I came across this problem, I took the chip to the cleanroom and soaked it in acetone. This was a huge mistake, because the carbon tape dissolved into small pieces in acetone and climbed on the topside of the chip and the surface looked black and dirty, the chip was effectively garbage.

I made the problem even worse by sonicating the chip. So somehow the top side of the chip needed to be cleaned. The solution is as follows: the cleanroom has some expensive fabric wipes that are only used to clean chambers. Fold the fabric wipe in the middle and soak it in IPA (turns out that IPA is better in dissolving carbon tape than acetone). Then gently flip the chip such that the front side touches the soaked wipe and spray more IPA over it. Then very gently rub the surface of the chip on the soaked IPA wipe, making sure you don't rub in the same area of the wipe. Repeating this a few times should do the trick.

All in all, to remove carbon tape from the backside of the chip before you mess up the top side, I would suggest to get one of those expensive fabric wipes, soak it in IPA, place the chip top side up on the wipe, and gently rub the backside on the wipe. Try not to move in the same wipe area many times and drown the chip in IPA every few seconds because it vaporizes fast.

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