Quantum Phase Transitions in Josephson Junction Arrays

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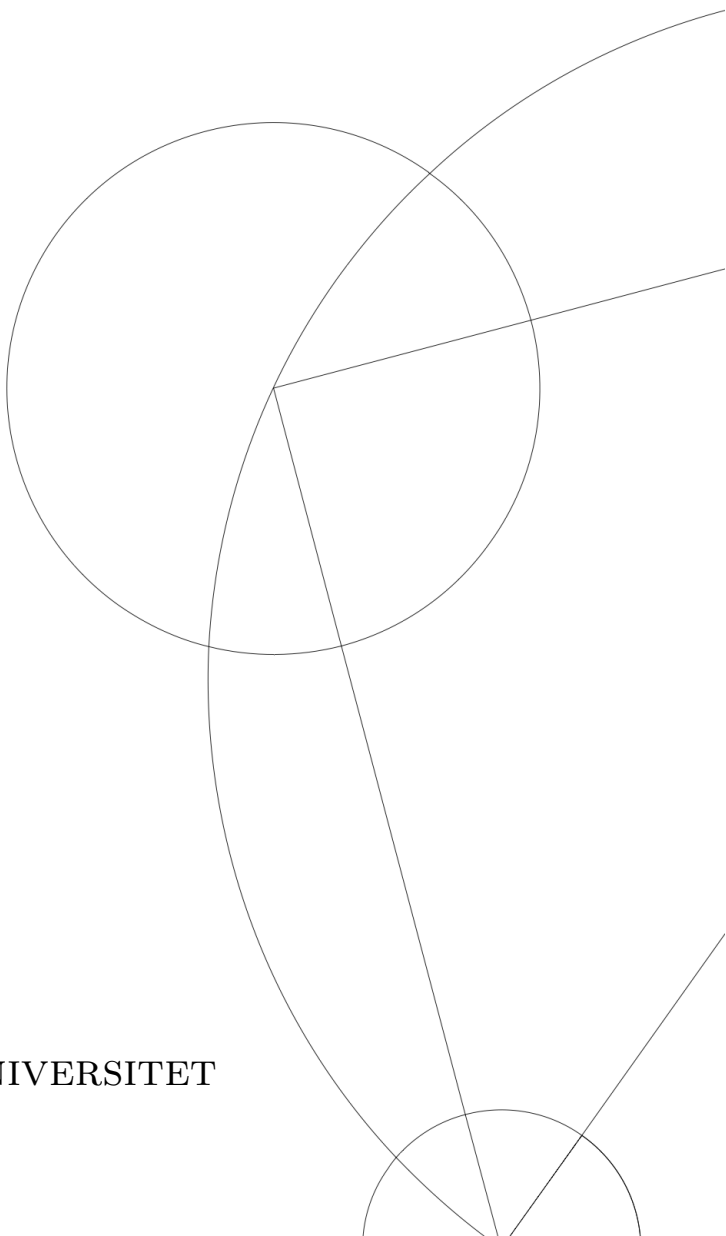

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Abstract

In this thesis we present a new design of semiconductor-superconductor two-dimensional Josephson junction array. The array is a square lattice of islands formed as crosses. This exposes the heterostructure material, which makes it possible to control the charge carrier density of the 2DEG by two gate potentials. The two gates allows fine tuning of competing characteristic energy scales in the array. We show that the array can be tuned into distinct regimes which significantly changes the dynamics of the array. We show that this material is a perfect platform to study an electric field driven superconductor-to-insulator quantum phase transition. We present data of the SIT in all of the characteristic regimes of the device, and we show that the prevalence of low-temperature resistance saturation is directly tunable by the gate potentials and by frustration. Furthermore we investigate the Berezinskii-Kosterlitz-Thouless (BKT) transition as a function of frustration and we show, that the the curvature of the resistance lines significantly depends of frustration. Finally we propose improvements to the design of the the frame gate layer which hopefully in the future allows for even better measurements of the SIT and BKT transitions.

Contents

1 Introduction

For the past 50 years, the physics of 2-dimensional superconductivity have puzzled physicist due to a complicated competing interplay between charge localization effects and the superconducting parring mechanism [38]. A huge amount of experiments on low-dimensional systems have been conducted with the goal of explain a plethora of unanswered questions: How is superconductivity destroyed by external parameters such as magnetic flux or electric fields? Can the system be driven out of superconductivity to the insulating state by introducing disorder? Do undiscovered states of matter appear in the phase transitions? Historically the majority of such experiments have been performed on thin superconducting films [10], [18]. Such films can be categorized by the type of disorder present in the system. The term "disorder" refers to random potential present in the system. The inhomogeneities of the potentials can have different length scales. Systems with variations of the random potentials on atomic scales are called uniform or homogeneous systems. If the length scale of disorder in the system is larger than the atomic length scale, the system is called granular [17]. More recently a new platform to study two-dimensional superconductivity has become popular namely the Josephson junction array. Over the last couple of decades fabrication techniques have become better which has made it possible make more complicated devices such as arrays. A huge advantage of fabricated Josephson arrays, is simply the fact that most parameters (such as physical dimensions of the superconducting islands) can be varied and chosen to desired values. Josephson junction arrays are artificially created materials hence such materials are well characterized. This is directly opposite to for instance the granular superconducting films where the Josephson coupling strength between granules are described by a distribution [3]. The Josephson junction array is a perfect system to study a plethora of physical phenomena such phase transitions (both classical and quantum) and vortex dynamics [16]. An unique feature of Josephson junction arrays is observed when a perpendicular magnetic field is applied namely frustration effects. As will be seen in section 5, due to the periodicity of arrays, the structures in the data of magnetic field sweep on arrays are much richer than for thin superconducting films.

Plenty of research has already been done on Josephson junction arrays. In this thesis however, we present measurement on a new design of the array. The device under investigation is a dual gated semiconductor-superconductor hybrid. This gives us huge amount of control of the electrostatic potential we can apply on the array which allows us to change the ratio of characteristic and competing energy scales in the system.

This device will serve as the experimental platform to study the superconductor to insulator (SIT) quantum phase transition. Due to the device being double gated, our available parameter space is very large: We have two gate potentials and a perpendicular magnetic field at our disposal. We took advantage of this by investigating the SIT at as many different combinations of the external parameters as possible. We quickly realized that multiple features in the data significantly change as a function of the external parameters. This thesis is a phenomenological description of these features.

1.1 Outline of the thesis

In this thesis we present results of a series experiment aimed at gaining a deeper understanding of the SIT quantum phase transition in Josephson junction arrays. However we quickly realized that instead of having a direct transition from the superconducting to the insulating phase, we observed a " metallic" phase characterized by low-temperature resistance saturation. This will be discussed in more details in section 5. Furthermore we observed that the classical phase transition to the superconducting phase behaved differently for different magnetic field strength. This feature is discussed in section 6.

In the next section the most important theoretical concepts are introduced for the reader. In section 3 the design of the device and design improvements are presented. Furthermore the measurement setup and the general low temperature techniques we have been using are presented. In section 4 we present a sequence of results where each of the available external parameter individually are tuned and their effect on the dynamics of the array is discussed. All our SIT measurements are shown section 4.

The data analysis and discussion of a BKT transition and the anomalous metallic phase are presented in section 5 and 6. Finally a conclusion of the project and of our observations are presented in section 7.

2 Fundamental concepts

In this chapter the theoretical background for the thesis is introduced. The review starts with a brief recap of superconductivity and the basic concepts of the Josephson junction and goes further to describe the most important physics of Josephson junction arrays.

2.1 The 2-dimensional electron gas

Semiconductors are characterized by the so-called band gap energy between the valence band and the conduction band. The conduction energy of InAs is less and the conduction band energy of $In_{0.81}Al_{0.19}As$ i.e. there is a mismatch in band gaps. Junction of semiconductors with uneven band gaps are called heterostructures. Due to the difference in conduction band energies, a quantum well is formed in the growth direction. This confinement potential "freezes out" one degree of freedom by quantizing the energy levels in the growth direction. The energy levels of the quantum wells are well described by the energy levels of the infinite square quantum well [23]

One of the most desired properties of the 2DEG, is the ability to gate the device. With a electrostatic potential we are able to tune the charge carrier density in the 2DEG. The tuneability of carrier density has been a very important tuning parameter in this project.

2.2 Superconductivity

According to the theory of superconductors presented by Bardeen, Cooper and Schrieffer (BCS), below a critical temperature T_C, the fermionic ground state becomes unstable against a phonon mediated attraction between electrons near the Fermi surface with opposite momenta and spin. Such a pair is called a Cooper pair. The attractive potential between two fermions is referred to as the pairing potential. The total spin of Cooper pairs is zero which means they are bosonic particles. It turns out that the the ground state of the BCS hamiltonian is a coherent state of Cooper pairs [8]. It can be shown that the paring potential causes the energy dispersion relation of the ground state to become gapped i.e. there is a minimum energy requirement to excite the coherent state. The gap in the excitation spectrum also causes an energy gap in the density of states in the superconductor. Below the energy gap, the density of states of quasiparticle is zero.

This coherent wave function is characterized with a complex order parameter. The order parameter has a phase ϕ and an amplitude which is related to the Cooper pair density: $\sqrt{n_s}$:

$$\Psi(r) = |\Psi(r)|e^{i\phi} \tag{1}$$

Where $|\Psi(r)|$ is the local density of superconducting charge carriers and $\phi(r)$ is the superconducting phase. The order parameter describes the entire condensate of Cooper pairs and is therefore a macroscopic wavefunction of the superconductor.

2.3 Andreev reflection and the proximity effect

The system under investigation is a superconductor-semiconductor hybrid. Therefore the normal-superconducting interface has to be taken into account. It turns out that a special reflection process occurs, the so-called Andreev reflection or retroreflection. Consider an electron with energy less than the superconducting gap. Due to the gap, no single electron states are available hence no transmission through the interface is allowed. Furthermore, it cannot be scattered normally because no scattering potential is present at the interface. Instead, a Cooper pair can be created in the superconductor by taking an additional electron near the Fermi surface of the normal material. This vacancy in the normal material is referred to as a "hole". The incoming electron is retroreflected as a hole with opposite spin and momentum at the N-S interface. This effectively transfers two electrons from the normal material to the superconductor in the form of a Cooper pair. The model described above can be extended to include a non-zero amplitude of normal scattering by adding a potential at the

interface. The so-called BKT model introduces a delta function potential at the NS interface [30].

The process described above resulted in adding a Cooper pair to the superconductor condensate. A Cooper pair from the the condensate and leak into the normal material and diffuse a short distance. Effectively the pairing potential from the superconductor does not abruptly stop at the NS interface can leak into the normal material with decaying amplitude. The characteristic length scale of this decay is the coherence length of the Cooper pairs [26].

2.4 Josephson junction basics

A Josephson junction consists of two superconducting leads separated by a layer of non-superconducting, the so-called weak link. Examples of Josephson junction are the superconductor-insulator-superconductor (SIS) junction where the weak link is a insulating material or a superconductor-normal-superconductor where the weak link is a metal (SNS) (More types of junctions exists [31]). It was discovered by Brian Josephson that a current can flow between the superconducting leads even without a potential difference. This phenomenon is hence called the Josephson effect. It originates from the coherent tunneling of Cooper pairs between the superconducting leads.

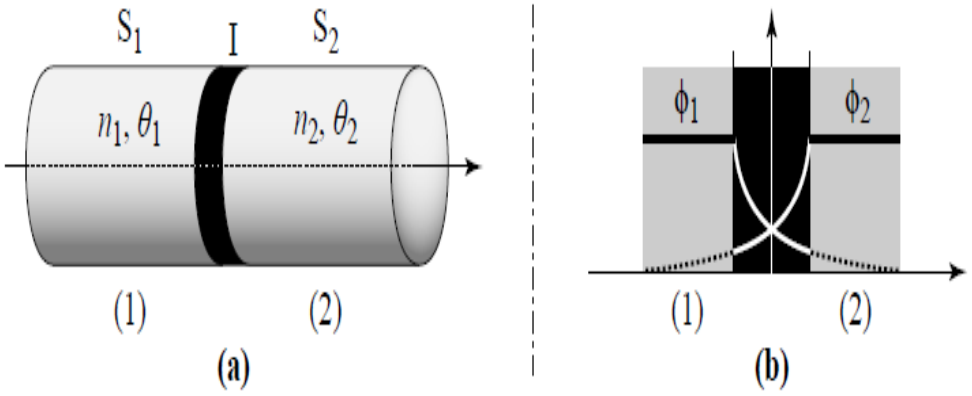

Figure 1: **a)** A schematic of a SIS junction [30]. Each superconducting lead is characterized by the macroscopic wavefunction. **b)** The overlap over wavefunctions leads to non-zero probability of Cooper pair tunneling.

A schematic of a SIS junction is shown in figure 1. Each superconducting lead is described by the wavefunction in equation 1. The wavefunction of the right lead can extend into the left lead and vice versa. This causes a non-zero probability of Cooper pair tunneling between the leads. Josephson derived that the current flowing between the two leads is given as:

$$I = I_c \cdot \sin(\phi_2 - \phi_1) \tag{2}$$

Where I_c is critical current which is the the maximal dissipationless current sustained by the junction. It is not a potential difference but a phase difference that drives the supercurrent. Even though the tunneling current is dissipationless, there is still energy stored in the junction. The Josephson junction in figure 1 can be thought of as a molecule with a binding energy resulting from the wave function overlap. This "binding" energy of the Josephson junction is the so-called Josephson coupling energy. The Josephson energy represents the junction coupling strength. It plays an extremely important role in the measurements shown in this thesis [32].

When an external magnetic fields is applied it interacts with the Josephson junctions via. its vector potential. It is well known from introductory electromagnetism, that there exists no unique vector potential for a given magnetic field. In order to select a specific vector potential to work with for a given magnetic field, one has to choose a specific gauge. The superconducting phase and the vector potential obeys a set of gauge transformations. All physical quantities have to be independent of the

gauge choice . A gauge invariant phase difference between two superconducting islands is therefore introduced:

$$\gamma_{ij} = \phi_i - \phi_j - \frac{2\pi}{\Phi_0} \cdot \int_i^j \vec{A} \cdot d\vec{r} \tag{3}$$

If a constant potential difference applied across the junction, it can be shown that the phase difference grows linearly as a function of time:

$$\frac{d\Phi}{dt} = \frac{2\pi}{\Phi_0} V \tag{4}$$

Where $\Phi_0 = \frac{h}{2e}$ is the flux quantum. It is seen that time evolution of the phase difference causes dissipation in the junction since it. This is a very important equation is used to explain the resistive behavior of arrays.

So far only the dissipationless supercurrent has been accounted for (eq. 2). But the Josephson junction consists of two separates pieces of metal. A capacitive current is given as $I = C \cdot \frac{dV}{dt}$. Inserting equation 4 gives the following expression:

$$I_C = \frac{\hbar C}{2e} \frac{d^2\phi}{dt^2} \tag{5}$$

2.5 Josephson Junction Arrays

Understanding the basics of single Josephson junction, one can go further to derive equations that describe the dynamics of an array of Josephson junctions. A Josephson junction array is made up of an ordered pattern of superconducting islands. Adjacent islands are weakly coupled by Josephson interactions. The lattice pattern investigated in this thesis is a square array. Each islands are weakly coupled to four adjacent islands.

The hamiltonian of the array is constructed simply by summing the junction potential energies (The capacitive and Josephson binding energy) for all junctions in the array. The following Hamiltonian is obtained:

$$H = \frac{1}{2} \sum_{<ij>} C\left(\frac{\hbar}{2e}\right)^2 \left[\frac{d}{dt}(\gamma_{ij})\right]^2 - J \sum_{<ij>} \cos(\gamma_{ij}) \tag{6}$$

Where the summation is over nearest neighbors. The first term is the energy required to add additional charge to an island and the second term is the Josephson tunneling energy between adjacent islands. This model is usually referred to as the quantum phase model (QPM). The reason for this is the fact that the superconducting amplitude on each island is not included. This hamiltonian only takes the superconducting phase into consideration. It is seen in the Hamiltonian in equation 6 that there is a competition between the Cooper pair tunneling term and the charging energy term. These two characteristic energies determine the dynamics of the array namely the Josephson energy E_J and the charging energy E_C. The former energy scale determines the strength of the Josephson coupling and the later determines the energy cost of adding additional charge to single island. The $\frac{E_J}{E_C}$ ratio is a important parameter which separates the array into two regimes: A classic and quantum array. Arrays are classified as being classical when $E_C << E_J$. In the classical limit a global phase coherence can be established and the array is superconducting. In the opposite limit $E_J << E_C$ the system becomes a Mott insulator due the large charging energy [16]. This results in a localization of Cooper pair on each island. It can be showed that the Hamiltonian of classical arrays is isomorphic to the two-dimensional XY-model. The fact that Josephson arrays are believed to be a physical realization of the XY-model has made it a heavily investigated topic, both experimentally and theoretically.

In the classical limit,the Josephson energy is dominating. Hence the charging energy term in the Hamiltonian can be ignored. The hamiltonian in equation 6 is reduced to the following:

$$H = -J \sum_{<ij>} \cos(\phi_i - \phi_j - \frac{2\pi}{\Phi_0} \cdot \int_i^j \vec{A} \cdot d\vec{r}) \tag{7}$$

This Hamiltonian has the same for as the so-called XY-model (the cosine can be written as a dot product of two two-dimensional unit vectors $S_i \cdot S_j$). The Hamiltonian in equation 7 is used to introduces the very important concept of vortices.

Every island in the array is characterized by its superconducting phase. It is seen in expression of the superconducting order parameter 1 that the phase is defined modulo 2π. Summing the phase difference across junctions in any closed path there must give $2\pi n$ with n begin an integer. Consider the hamiltonian 7 without an applied magnetic field (A = 0). It is clearly seen that the energy of the array is minimized by making the superconducting phase equal on all the islands. This phase configuration simultaneously satisfy the following condition:

$$\sum_{closedpath} \cos(\phi_i - \phi_j) = 2\pi n \tag{8}$$

For n = 0. The ground state configuration of the phases is shown in figure 2 All the phases are equal. We now search for phase configuration that satisfy 8 for n = 1. This phase configuration is shown in figure 2. A vortex (antivortex) is an excitation in the phase configuration such that the sum of all phase difference along a closed loop is 2π (-2π) [21].The vortex core is not necessarily located in the plaquette center as shown in figure 2. Phase configurations with other vortex core locations exists. The energy of every configuration is different. The energy differences between every configuration represent a potential landscape in which the vortices are moving. Stationary vortices are located in local minima in this potential. It is seen in equation 4 that a frozen vortex does not generate a voltage across the array. However vortices can be depinned by a biasing current or by thermal fluctuations. Free vortices in the array causes a voltage to appear.

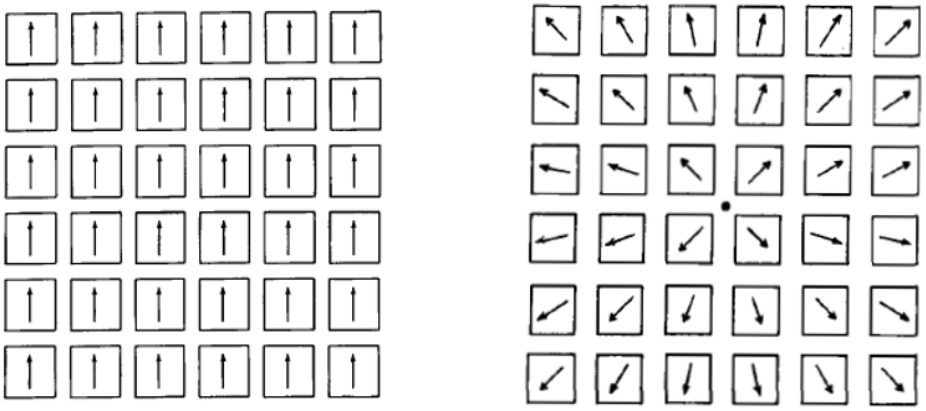

Figure 2: **a)** The ground state phase configuration. Every phase is aligned. **b)** The ground state phase configuration with a single vortex injected into the array. The phases have rearranged such that they cancel the additional phase term from the vector potential [31].

2.5.1 Magnetic field

The magnetic field introduces an additional phase difference A_{ij} across the junctions. The sum of A_{ij} around the four junctions in a plaquette is related to the applied flux though the plaquette [21]:

$$\sum_{plaquette} A_{ij} = \frac{2\pi BS}{\Phi_0} = 2\pi f \tag{9}$$

Where B is the applied flux and S is the plaquette area. f is referred to as the frustration parameter and is defined as the applied flux divided by the flux quantum. Consider the scenario of applying a single flux quantum across the entire array. The sum of all phase difference for for all the junction in the array is therefore 2π. The ground state of the energy is no longer the uniformly distributed

configuration shown in figure 2. However it is seen in the Hamiltonian that the energy of the system can be reduced if the phase difference adjust to cancel the phase gained from the vector potential. This configuration is shown in figure 2.

When a magnetic field is applied, the field penetrates the Josephson junction array by creating vortices similar to a type-II superconductor [28]. The major difference between JJa's and homogeneous type-II superconductors is the spatial configurations of vortices. In type-II superconductors the vortex lattice is triangular (The so-called Abrikosov lattice). The vortex lattice in Josephson arrays are more complicated since the spatial configuration of the vortex lattice in JJa's depends on the frustration parameter f [36]. Vortex lattices in JJa's is discussed in later sections.

2.5.2 Temperature

At non-zero temperature, vortices can be injected into the array if the thermal energy fluctuations are large enough. It can be shown that the energy cost of a single vortex excitation of the ground state phase configuration is the following (This is formally done by Taylor expanding the cosine in equation 7 and take the continuum limit. The field configuration which corresponds to a minima in the Hamiltonian is the vortex solution [33]):

$$E_{vortex} - E_0 \propto \pi E_J \ln(\frac{L}{a}) \tag{10}$$

Where a is the distance between islands and L is the width of the entire array. For large arrays, the energy cost of adding a single vortex is enormous. The probability of observing a single vortex in the array can be estimated by using the change in free energy by injecting a single vortex in the Boltzmann distribution:

$$P \propto \left(\frac{L}{a}\right)^{2-\frac{\pi E_J}{k_B T}} \tag{11}$$

For large arrays the probability is virtually zero until the exponent in equation 11 becomes zero at which the probability immediately increases to unity. The temperature at which this happens is defined as the Berezinskii-Kosterlitz-Thouless (BKT) temperature:

$$T_{KT} = \frac{\pi E_J}{2k_B} \tag{12}$$

This is the lowest temperature at which free vortices can be found in infinitely large arrays. At temperatures below the BKT temperature, thermal fluctuations do not generate free vortices due to the large energy cost. However, it can be shown that the energy cost of injecting a bound pair of two vortices with opposite sign is significantly lower than injecting a single free vortex:

$$E_{Pair} = 2\pi E_J \ln(\frac{r}{a}) \tag{13}$$

Where r is the distance between the vortex cores. If the distance between the vortex pair is less than the system width, the energy is significantly lower a single thermally injected vortex. As the temperature is increased from below, more and larger vortex pairs are generated. At the BKT temperature, thermal fluctuations become large enough to break the largest vortex pairs and create free vortices.

2.6 The BKT transition

Above the BKT temperature free vortices are present in the array which causes the array to be resistive. Below the BKT temperatures, all vortices are bound and the array is superconducting. At the BKT temperature a phase transition occurs between a resistive phase and the superconducting phase. Continuous phase transitions are characterized by diverging correlation length at the critical point [35]. It can be shown that the vortex correlation length for the XY-model is the following:

$$\xi = ae^{\left(\frac{b}{T-T_{BKT}}\right)^{\frac{1}{2}}} \tag{14}$$

For temperatures $T > T_{BKT}$. a and b are constants. The correlation length determines the average distance between free unbound vortices. At the BKT temperature, the correlation length is infinite indicating that there are no free vortices in the array.

The correlation length is used to derive an very important expression for the array resistance as a function of temperature. The resistance of the array is proportional to the density of free vortices which is proportional to 1 over the average distance between free vortices squared i.e. ξ^{-2}.

$$R(T) = ae^{-b\left(\frac{E_J}{T-T_{BKT}}\right)^{\frac{1}{2}}} \tag{15}$$

The function is defined for temperatures above the BKT temperature. For $T > T_{BKT}$ and R(T) = 0 for $T < T_{BKT}$. This expression is extremely important and is extensively in the data analysis section. Equation 15 has been derived from the Hamiltonian in equation 7. So far it has been assumed that the coupling strength (i.e. the Josephson energy) remains constant as a function of temperature. Therefore the temperature in equation 15 is can be replaced with a reduced temperature (defined as $\frac{T}{E_J}$):

$$\tilde{T} = \frac{2\pi k_B T}{\Phi_0 i_c(T)} \tag{16}$$

A more detailed discussion about the BKT phase transition and the temperature dependence of the array resistance is presented in a later section.

2.7 Quantum phase transitions

For classical phase transitions the system is driven through its critical point by the temperature. At the critical point the ground state fundamentally changes which often can be seen as diverging characteristic length scales. This is seen in the vortex correlation leg nth (eq. 14). The driving parameter of a quantum phase transition is however not the temperature. The SIT in Josephson junction array is an example of a quantum phase transition. A quantum phase transition can occur if the temperature is low enough such that quantum fluctuations are dominant. Quantum fluctuations is the driving the system through it critical point. If thermal fluctuations are much larger than quantum fluctuations, then the phase transition is purely classical.

Quantum fluctuations originates from the Heisenberg uncertainty principle and are present even at absolute zero. The Heisenberg uncertainty at play in Josephson junction arrays is the following:

$$[\phi_i, Q_j] \propto \delta_{ij} \tag{17}$$

The phase of the order parameter and charge are conjugate variables. Superconductivity on each island is governed by the local pair amplitude, but global superconductivity of the array is only achieved when a phase coherent path through the array is established [37]. Strong fluctuations in the phase prevents the establishment of phase coherence across the array. Global superconductivity remains as long as the following correlator approaches a non-zero value for $\mathbf{r} \to \infty$.

$$G(\mathbf{r}) = < \psi(\mathbf{r})\psi(0) > \tag{18}$$

Enhancing the quantum fluctuations of the phase can lead to suppression of superconductivity. In our experiments, this is achieved by increasing the frame gate voltage. This increases the E_C/E_J ratio which localizes charge. This mechanism of destroying superconductivity due to phase fluctuations is called "the Bosonic scenario". It is seen in the 18 that it is possible to suppress superconductivity if the modulus of the order parameter vanishes. This is the "fermionic scenario". Instead of localization of Cooper, it is electronic excitation that is responsible for the suppression of superconductivity [29].

3 Device fabrication and experimental setup

The design of the device and the electron transport measurement setup are presented in this section. Common low temperature techniques are discussed as well as the most important principles such as the lock in amplifier and 4-terminal measurement.

3.1 Superconductor-semiconductor hybrid

The fabrication and designs of the devices have not been a part of this master project. When I joined the project, the chip had already been fabricated, bonded and loaded in the dilution refrigerator. The main focus of this thesis is the electronic transport properties of the Josephson junction arrays. This being said, during the measurements we very quickly found flaws in the design of the arrays and we have new design proposals. This will be be discussed in later sections.

The device under investigation is a two-dimensional superconductor-semiconductor hybrid heterostructure. The wafer was grown by the Manfra group at Purdue university and the fabrication of the device was done by Sangeeth Kallatt in the clean room of center of quantum devices at University of Copenhagen. The heterostructure was grown on an insulating InP substrate. The layer structure of the quantum well (the so-called stack) and the electron wave function are shown in figure 3. The electronic properties the quantum well has previously been studied by Shabani et al. [25]. They studied the properties of the near surface quantum well as a function of varying the surface layer thickness (d) and calculated the electron wavefunction of the 2DEG electron carriers. The thickness of the heterostructure surface layer the devices in this project is 7nm.

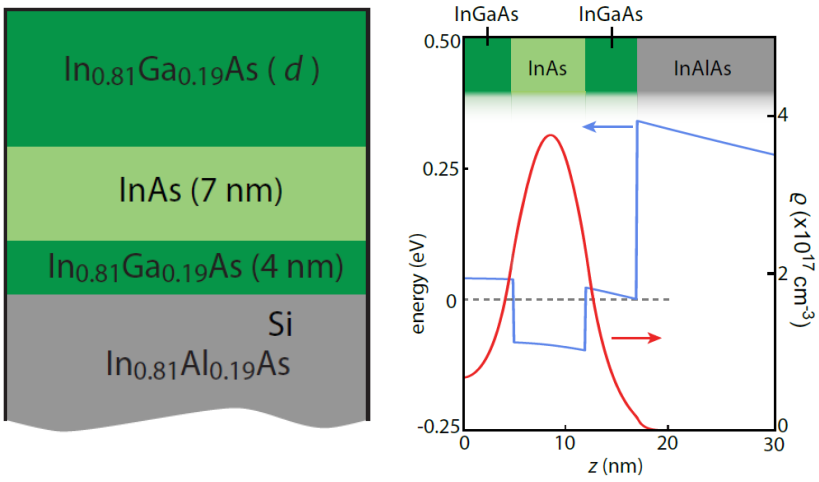

Figure 3: Left to right: **a)** The stack and quantum well of the devices under investigation. **b)** The electron wave function in quantum well [25].

On top of the stack, an 5nm aluminum layer has been grown. The aluminum layer have been grown using molecular beam epitaxy. This method allows the growth of highly homogeneous layers and very clean interfaces between the heterostructure and the aluminum. A clean interface is important to enhance the proximity coupling. When the device is cooled to temperatures below 1.8K, the aluminum becomes superconducting. Due to the proximity effect, the superconducting pairing potential decays into the quantum well.

Enhancing the proximity coupling comes with a cost. In order to improve the proximity coupling between the superconducting aluminum layer and the 2DEG, the charge carriers must be near the surface which decreases the carrier mobility. The electron mobility of the heterostructure was also measured by Shabani et al. The electron mobility is not very high since the quantum well is close to the surface which causes the surface scattering rate to be high. In order increase the proximity

coupling to the 2DEG, the electron wavefunction must reach the aluminum layer. It is seen in figure 3 b) that the electron wavefunction does extend into the surface.

3.2 Device fabrication

The entire chip consists of 12 Hall bars with varying plaquette areas, junction widths and lengths. The array is made of aluminum islands shaped as a cross. The array consists of junctions placed in a regular square lattice. In this project we have been conducting experiments of two different devices. An overview of the two arrays under investigation is shown in figure 4.

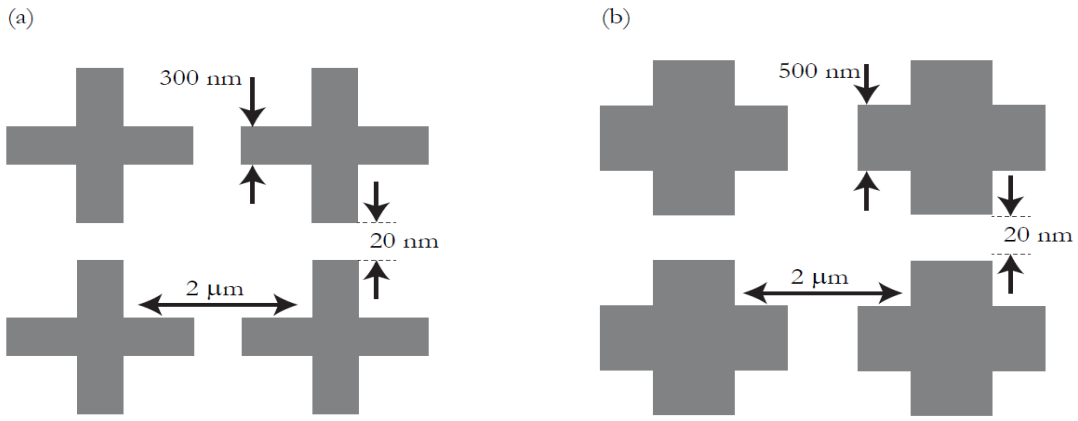

Figure 4: **From left to right: a)** The only difference between the two arrays is the width of the junctions. This device is referred to as C2. **b)** The width of the junction is increased to 500nm. This device is referred to as D3. The plaquette area is 2x2μm^2 for both devices.

The following section is a brief summary of the fabrication procedure. The initial step of the chip preparation is the mesa patterning. The chip is spin coated with resist and the mesa pattern is defined using e-beam lithography. All mesas are shaped as Hall bars. The etching of mesas consist of multiple steps. The aluminum layer must first be removed which is done using aluminum etchant. A separate etchant is used for the mesa etch (solution of water, citric acid, phosphoric acid and hydrogen peroxide). It is important to make sure the mesa etch is deep enough to the insulating area of the wafer to prevent leaking conduction paths between the mesas. Afterwards the resist used for mesa patterning is removed. The next step is the fabrication of the aluminum islands. Between every layer, the chip is always spin coated with resist and e-beam lithography is used for the patterning of the array itself. Removing parts of the aluminum layer makes it possible to gate the device since the electric field lines form the gate can no longer be screened by the aluminum.

The novelty of our experiment is the fact that the device is dual gated. A schematic of the Josephson junction array is shown in figure 5. The two gate layers are made of Gold and titanium (Au/Ti). To prevent currents through the gate layer to the device and to ensure a purely capacitive coupling, a dielectric layer is deposited. The dielectric medium between the gate layer and the aluminum surface consists of a 40 nm aluminum oxide layer. The dielectric is deposited using atomic layer deposition (ALD). The gate layers are deposited using e-bream evaporation. The sequence at which the two gates layers are deposited is very important. The frame gate layer must be placed underneath the top gate layer. The electric field from the top gate is screened by the field lines from the frame gate. This configuration of the two gates makes it possible to tune the Josephson energy with the frame gate only and make it independent of the top gate voltage.

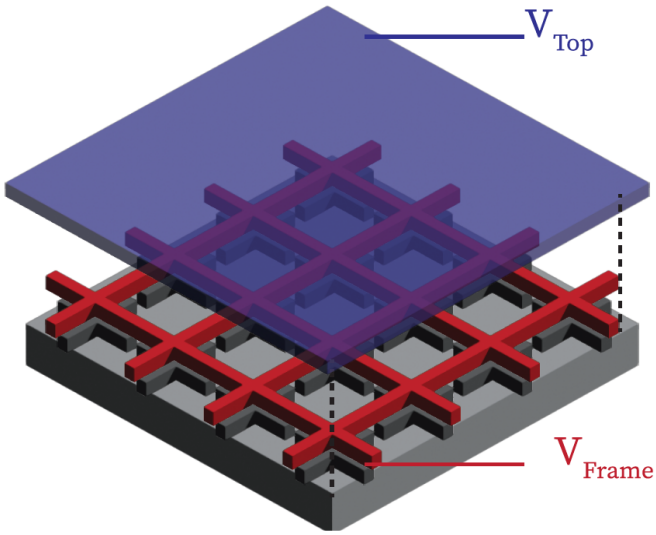

Figure 5: The general design of every device on the chip. The array consists of the aluminum island formed as a cross. The first gate layer is frame gate which controls the electrostatic potential across the junctions. The final layer is the top gate which applies a potential on the exposed 2DEG.

3.2.1 Chip Wire bonding and loading

After fabrication, the chip is glued to a sample holder on a daughterboard. The chip must be be electrically connected to the daughterboard. This is done by wire bonding the leads of the device to bond pads located on the edges of the daughterboard. The wire bonding is achieved using special bonding equipment. The material used for the bonding is gold. Afterwards the daughterboard is connected to a motherboard which is placed inside a puck. The puck is loaded into the cryostat from the bottom using a special designed loader which has its own vacuum chamber. The puck is placed in this chamber. The vacuum chamber of the loader is then vacated using a scroll and turbo pump. When the pressure in the loader vacuum chamber is comparable to the pressure of cryostat vacuum can, the chamber is opened and the puck is screwed onto a cold finger. This brings the sample in thermal contact with the mixing chamber plate. Coaxial cables are connected to the break out box and are used to connect measurement instruments to the setup.

3.3 Measurement techniques

In order to study quantum mechanical effects, the temperature of the system under investigation has to be low. This is due to the large difference in energy scale between quantum and thermal fluctuations at high temperatures. The energy scale for quantum mechanical phenomena much lower than the energy scale of thermal energy. The thermal energy is of order $k_B T$, hence the temperature has to be significantly lower than room temperature. We achieve low temperatures using a ^{3}He/^{4}He dilution refrigerator. We use a Oxford Instruments Triton 400 cryostat which is a pulse tube dry refrigerator. The base temperature is 15mK.

All of our experiments have been conducted using two methods of biasing: Voltage and current bias. Voltage bias was used to measure zero bias differential resistance of the device whereas current biasing was used to measure the critical current of the device. Voltage biasing consists of applying a voltage the source ohmic of the device. AC and DC voltages are combined through a voltage divider. The voltage divider is used to down scale the voltage generated by the connected voltages sources. This allows for more fine tuning of the voltage and can give higher resolution than what is possible with the voltage source. The AC voltage is divided by 10000 and the DC voltage is divided by 1000. The DC voltage was generated using either Yokogawa or a Qdevil qdac. The current going out of the

device was preamplified using an IV-converter (Basel Precision Instruments). The preamplification gain was set to 1e8. The longitudinal voltage was preamplified by a factor 1000 using a home-built voltage preamplifier.

A 4-terminal setup was used to measure the voltage drop across the sample and between ohmics on the sides of the Hall bar. The device under investigation is superconducting. Therefore it is very important to be able to measure very small resistances. The principle behind a 4-terminal measurement is to separate the probing circuit and the driving circuit such that no current is running in the sensing circuit. The impedance of a voltmeter is very high. Therefore no current is running through the sensing circuit hence there is no voltage drop across the wire contacts. The voltage drop across the drive leads are not seen by the sensing leads. Unfortunately the lowest resistance we can measure in the setup is 3Ω even when the device should be superconducting. We do not know the reason for this.

A slightly different measurement setup was used when current biasing the sample. The voltage was not applied directly to the ohmic. Instead a 10Mω resistor was put in series for the DC voltage and a 1Mω resistor of the AC voltage. This ensures that the entire voltage drops across the resistor. The current through the device is therefore approximately constant. When current biasing the sample, one has to be very careful to make sure, that the resistance of the sample itself is lower than the 10MΩ resistor on the DC line. If the resistance of the device becomes of similar value as the resistor, a significant voltage is dropped across the sample which may damage to the sample.

The magnetic field has been produced by a superconducting (6, 1, 1) vector magnet. We have only used very small magnetic field strength. We used a Keithly Source meter to fine tune the magnetic field.

Typical low-temperature experiments consists of measuring currents and voltages with very low amplitudes. Such signals can easily be buried in noise. Lock-in amplifiers are used to drastically enhance the noise to signal ration. Lock-in amplifiers can detect AC signals with very small amplitudes. The principle of lock-in amplifiers is called phase-sensitive detection [1]. Noise components of the detected signal with frequency different from the lock-in reference frequency, are significantly attenuated. The lock-in generates an internal reference sine signal with a fixed frequency Ω_{ref}, phase θ_{ref} and amplitude V_{ref}. This reference signal is used to excite the experiment. This causes the response of the system to be frequency modulated with the reference frequency θ_{ref}. The expected output signal of the experiment is hence a sine wave with the same frequency θ_{ref} plus additional noise signals at frequencies different from the reference frequency. The phase-sensitive detection (PSD) consists of mixing the reference signal and the output signal. Mathematically this operation generates the product of the two cosine waves. The resulting out of the PSD is the following:

$$V_{PSD} = \frac{1}{2}V_{sig}V_{ref}\cos((\omega_{sig} - \omega_{ref}) + \theta_{sig} - \theta_{ref}) + \frac{1}{2}V_{sig}V_{ref}\cos((\omega_{sig} + \omega_{ref}) + \theta_{sig} + \theta_{ref}) \quad (19)$$

The PSD generates two AC signals. For signal frequencies $\omega_{sig} \approx \omega_{ref}$, the first cosine become a DC signal and the second cosine becomes a high frequency AC signal. A low pass filter is used to remove the high frequency part hence the resulting out after the PSD is a DC signal. Noise components with frequencies far away from the reference signal is attenuated by the low pass filter since both cosines in eq. 19 become high frequency signals. The PSD output for noise components with frequencies close to the reference frequency is low frequency AC signal. The low pass filter time-constant determines the attenuation of such signals. The lock-in amplifier determines the phase difference $\theta sig - \theta_{ref}$ by adding a second PSD with a 90 degree phase shift of the reference signal.

All transport measurements have been performed using a combination of multiple Stanford research system lock-in model SR860 and SR830. The voltage drop across the sample and the current running through the device are both measured with lockin amplifiers. Dividing the voltage by the current (remember to include the preamplification factors), one obtains the differential resistance i.e. the slope of the IV characteristic of the array. Implicitly we are assuming that the IV-curve of the array is anti-symmetric around zero bias and that the slope around zero bias is approximated well

as a linear function. In that case the differential resistance and the absolute resistance of the device is approximately identical. The amplitude of the lockin excitations determines the precision of the derivative of the IV-curve. A large amplitude might generate less noisy signals, but sacrifices resolution. We used a 5μV AC excitation for all our SIT measurement.

The lockin excitation frequency is set to a rather low value of 3.14 Hz. The reason for this is due to the C2 device behaving as a low pass filter. The amplitude of the current was significantly attenuated when the lockin frequency was increased to higher values. The low pass filter characteristic was not significant in device D3 so the lockin frequency was set to 27.3 Hz.

4 Results

In this chapter all the conducted measurements on the chip are presented. The entire available parameter space is explored and the effect on the device of each of the tuning parameters is analyzed.

4.1 Preliminary measurements

Before actual experiments of each device on the chip can start, it is necessary to investigate which devices are working as intended and which have defects from the fabrication. Fabrication of nanostructures is difficult and complicated, and errors in the fabrication process can easily happen. The quality of each device are systematically checked by doing a handful of simple measurements.

The preliminary measurement consists of checking for leaking conduction pathways. The first measurements were gate leakage test. This measurement is conducted to find faulty gates and to map out the available gate space. The gate layers and the array are separated by a aluminumoxide dielectric layer. Bad ALD growth of the dielectric layer may cause a leaking current from the gate plates to the array. The test consists of sweeping the gate voltage while measuring the current. The quality of the probes must also be checked. A significant problem that often arises is the probe pinching off. The gate voltages are swept while the phase of the voltage probes are measured. Probe pinch-off is observed as a 90 degree phase shift.

The preliminary measurements on the chip has reduced the available number of devices from 12 to only two. The majority of the electron transport measurements have been done on device C2 and D3. The different geometry of these two devices makes it possible to directly compare the data of the two devices and investigate the effect of changing the dimensions of array parameters such as junction width and plaquette area. Furthermore it allows us to check the validity of unexpected features appearing in the device. If the same feature appear in multiple devices, it is easier to argue that new physics is going on.

4.2 Normal state resistance

The available parameter space for our device is vast. It is important to investigate the effect each of our tuning parameters have on the device. This section focuses on the effects of the top and frame gates. The two gates allows us to independently adjust the electrostatic potentials in the junctions and the plaquettes and give enormous tuneability of the charging and Josephson energies.

The first experiment on each device is measuring the normal state resistance (temperature is 2K) as a function gate voltages. The gate maps of device C2 and D3 are shown in figure 6. The maps have been obtained by setting the frame gate voltage sweep as the inner loop in qcodes and the top gate voltage sweep as the outer loop. Very early on in the project it was observed, that sweeping the top gate voltage causes hysteretic behavior. This hysteretic behavior is much less pronounced when sweeping the frame gate. The device is very large so probably a huge amount of metastable states that are very close in energy exists. Every time the top gate potential is swept, the array my settle in slightly different ground states.

The behavior of the array significantly depends on the gate potentials. The combined effect of the two gate potentials allow us to tune the array into different regimes each of which have unique behavior.

The frame gate potential allows us to tune the conductance through the junctions and hence is directly related to the Josephson energy. The driving parameter of the quantum phase transition is the ratio of the two the junction energy and the charging energy of the array. Hence the frame gate potential is our main driving parameter in the quantum phase transition from the superconducting phase to the insulating phase.

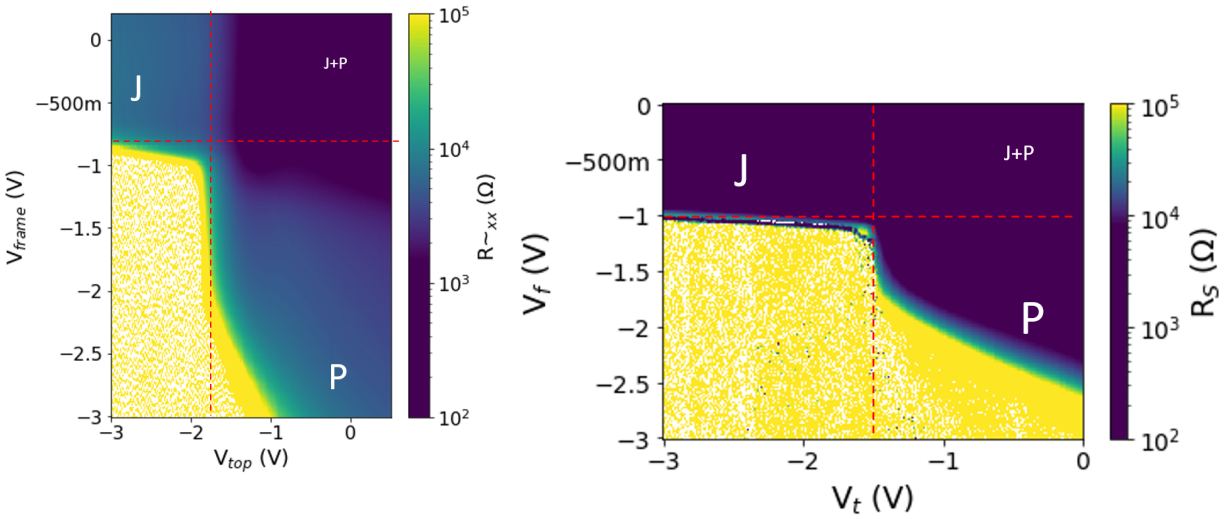

Figure 6: The figures shows the resistance of the device as a function top-gate and frame gate-voltages. The maps was measured at 2 K. The map on the left/right is the gate map of device C2/D3.

The top gate controls the fermion density in the plaquettes of the unit cell in the array. The exact effect of the fermion density in the plaquettes on the quantum phase transition is unclear, but it has been suggested that it can be modeled as reservoir of low lying fermionic excitations which acts as a dissipative bath for the superconducting order parameter [2].

The first noticeably feature is the areas of decreasing resistance in the gate scan of device C2 shown in figure 6. There are vertical and horizontal "band" of less resistance which is present at top gate voltage -0.75V and frame gate voltage -1.7V. We suggest this feature might be due to a mobility peak in the 2DEG. The mobility peak indicates that interface scattering can be suppressed. This is consistent with the fact that the quantum well is close to the aluminum interface. Shabani et al. were able to increase the mobility of the 2DEG carriers by increasing the thickness of the quantum well surface layer. This burrows the quantum well further from the surface and hence decreases surface scattering. We are able to push the quantum well further away from the surface by applying an electric potential.

The main features in the both gate maps is the clear separation of gate space into different areas. There are four different regimes in the device. The first is the "puddle regime" which occurs when the top gate is slightly energized (voltage near zero) and the frame gate is highly energized (large negative voltage). The area in gate space is shown with the letter P in figure 6. In the puddle regime the fermion density in the plaquettes is large while the highly energized frame gate significantly decreases the conductance through the junctions. In this regime the transport of electrons goes around the junctions through the plaquettes.

The second regimes is the "junction regime". The area in gate space is marked with a J. The top gate is highly energized which depletes the plaquette density and makes conductance through the puddles very small. The frame gate voltage is near zero which makes the Josephson junction energy very high. In this regime the junctions are fully open and the majority of carrier transport happens through the junctions.

The third regime is a complicated area where both gates are slightly energized, but neither are set to an extreme value. It is shown as a J+P marker in the gate space map. This is a very complicated regime so we decided not to investigate this regime.

The last regime is the insulating area. In the yellow area, both the gates are highly energized. Conduction paths through the plaquettes and through the junctions are all closed.

A key feature in the gate-gate maps for both devices is the presence of two different slops of the insulating area. The vertical red dashed line indicates the first slope. The general shape of the yellow

insulating area is a sharp corner followed by another area with a less steep slope. The corner occurs at the point in gate space where the junctions are fully closed and the puddle conductance channels are just about to open. Starting from the intersection of the two red dashed lines, going more negative on the frame gate doesn't change the array resistance since the junctions already are closed off and the majority of conductance occurs through the plaquettes. This is true until the second slope occurs. At this point the frame gate significantly increases the resistance. We believe this feature can be prevented by changing the frame gate design. The current and a newly proposed design are showed in figure 7.

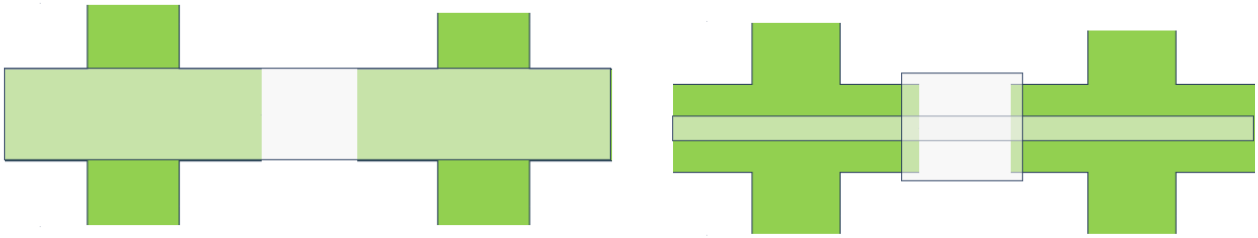

Figure 7: **From left to right. a):** The current design of the frame gate. The width of the frame gates is the same as the junction width. **b)** The new design of the frame gate. The width has been reduced except for the area between the junctions.

In the current design of the arrays, the frame gate width is the same as the width of the underlying aluminum layers. Slight misalignment of the frame gate layer makes it possible for the electric field lines of the frame gate to reach the heterostructure since they are no longer screened by the aluminum layer. At high frame gate voltages, this causes the frame gate to effectively pinches off the both the junction conductance and the puddle conductance. This is the reason for the second slope in the gate-gate maps. We therefore propose to make the changes shown in figure 7. The width of the frame gate layer has been reduced such that it no longer matches the width of the underlying aluminum layer. The width of the frame gate above the junction itself remains the same. The new design significantly reduces the possibility of puddles conduction pinch-off by the frame gate. Devices with these design changes have already been fabricated, and measurements have been conducted by Luca Felix Banszerus. Gate-gate maps of the devices have been obtained and the second slop has indeed disappeared.

4.3 Critical current

The gate maps reveal the array behavior when the aluminum is normal (at 2K). At base temperature (15mK) the different regimes are characterized by their critical current. The measurement is conducted by applying a DC biasing current to the source probe. If the applied current exceeds the critical current of the array, a voltage drops across the sample, since part of the current becomes dissipative. The critical current of device C2 was measured at different gate space configurations at base temperature (15mK).

The differential resistance maps are shown in figure 8. The two plots on the left side show the differential resistance of the array as a function of sweeping the top gate voltage. The frame gate is held constant at V_f = -0.6V i.e. the junctions are open and the top gate is swept from 0.5V to -5.5V. This gate sweep can be visualized in the gate map of device C2 (Figure 6) as a horizontal line at $V_f = -0.6V$ from the J+P regime to the junction regime. It is seen that the differential resistance is largely independent of the top gate potential in the range 0.5V to -1.25V. Increasing the top gate voltage in the interval between -1.25V and -5.0V drastically increases the critical current of the array. The top gate voltage controls the fermion density in the plaquettes. We suggests that the dramatic increase in critical current is rooted in the inverse proximity effect. The inverse proximity effect is a suppression of the superconducting gap near the surface between a superconductor and a reservoir of fermionic excitations. When the top gate voltage becomes very large, the fermion density in the puddles become very low. This reduces the inverse proximity effect, which causes the critical

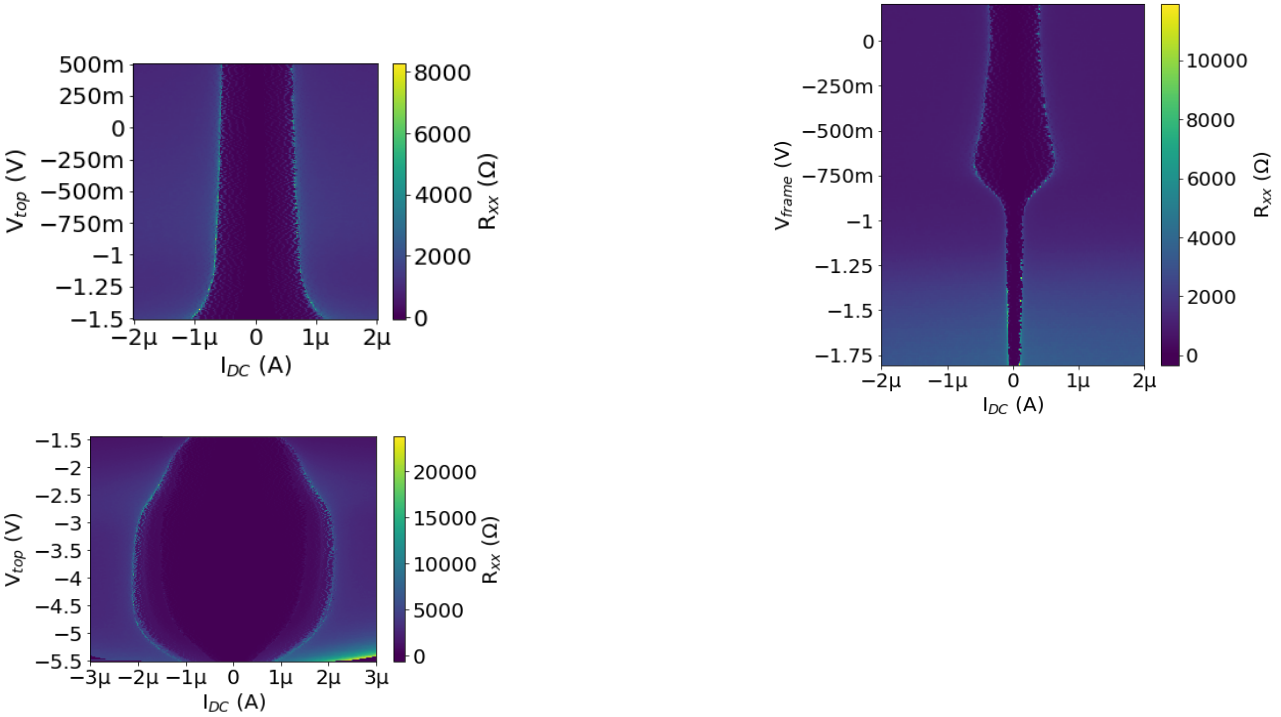

Figure 8: The critical current measurements have been taken at 15mK.

current to increase. The critical current significantly decreases at top gate voltages above -5.0V. This is probably due to an unintended cross capacitance between the top gate and the 2DEG underneath the frame gate. At such large voltages, the electric field lines from the top gate effectively pinches off the conductance through the junctions.

The figure on the right side shows the differential resistance as a function of the frame gate at fixed top gate voltage V_T=0.5V. The line cut in the gate map is the vertical line at V_T=0.5V going from the J+P region to the puddles region. The critical current is significantly smaller due to the large fermion density in the plaquettes. In the frame gate interval $V_f = 0V$ to -0.75V the critical current slightly increases. At higher frame gate voltages, the junctions are closed off and the critical current almost reaches zero.

The critical current scans strongly suggests, that the plaquette fermion density significantly suppresses superconductivity of the array. The magnitude of the critical current in the puddles and junction regimes are very different. The magnitude of a supercurrent going through the plaquettes is significantly reduced due to the inverse proximity effect.

4.4 Combination gate

Knowing we have multiple regimes in the array, we would like to sweep along a path in gate space that connects the two regimes, and investigate the features of the resistance lines along this path as a function of temperature. We were inspired by the Ambegaokar relation which makes a connection between the normal state resistance of a Josephson junctions and its Josephson energy. Hence the chosen paths in gate space were iso-resistance lines. Contour lines were found in the gate map shown in figure 6. The frame and top gate voltage combinations along the contour line was coded into a single sweeping parameter in qcodes. This “combination” gate map sweep was performed at multiple temperatures in the interval 20mK to 1.9K. The resistance lines as a function of temperature along the contour line at 10kΩ is shown in figure 9. The key feature is the fact that the resistance lines are clearly divided into two regions. In the junction regime the resistance lines become superconducting at much higher temperatures than the the lines in the puddle regime. In fact, the resistance lines

in the puddle regime do not become superconducting at all. The separation of resistance lines in the two regimes reaffirms the fact that the fermion density in the plaquettes are able to suppress superconductivity.

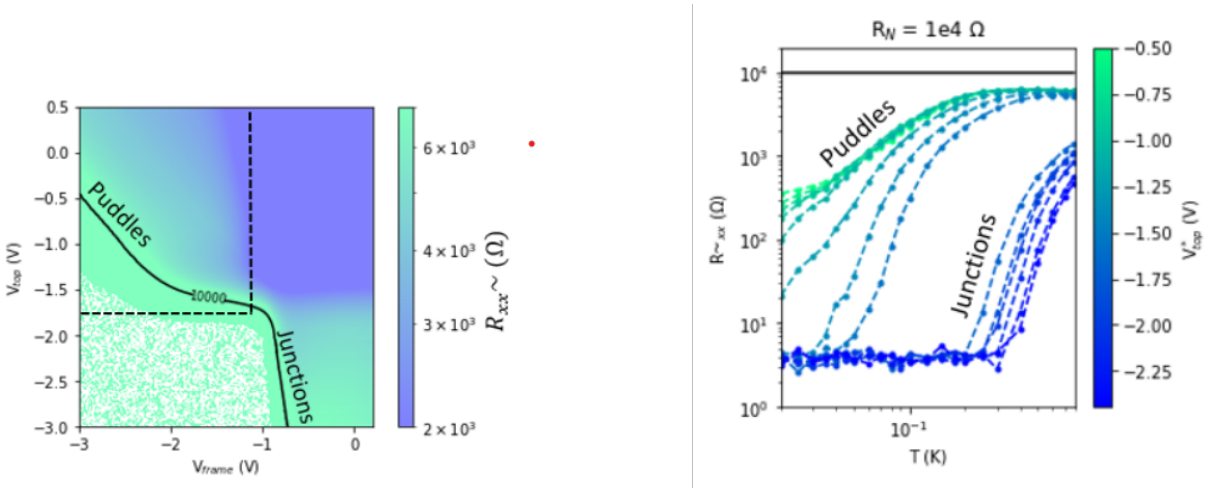

Figure 9: Left to right: **a)** A resistance iso-line at $R = 10^4\Omega$ was found in the gate-gate map of device C2 **b)** The combination gate was swept at multiple temperatures. A clear separation between resistance lines in the two regimes is seen. The colorbar has nothing to do with the voltage of neither the top or frame gate but shows an arbitrary sweeping parameter.

4.5 Magnetic Field Scan, Frustration

The final tuning parameter at our disposal is the magnetic field. Due to the plaquettes in the array we except periodic oscillatory behavior in the sheet resistance which is a unique feature for Josephson junctions array. In this section the response of the device to a magnetic field sweep is discussed. The behavior of each device was investigated in the puddle and junction regimes. The magnetic field is positioned perpendicular with respect to the plane of the array. No in-plane magnetic field was ever applied for any of the measurements.

The data of the magnetic field sweep for device C2 and D3 are shown in the figures 11 and 10. The magnetic field and temperature dependence on the sheet resistance was measured at different positions in gate space. The experiment was conducted by sweeping the magnetic field at constant temperature. The same sweep was performed for multiple temperatures in the interval 20mK to 1,8K. This makes it possible to probe the stability of the ground state against thermal fluctuations. The most stable ground state is pushed out of superconductivity at higher temperatures than less stable ground states. The data is shown in 10. This presentation of the data allows one to see very small frustration features. Another presentation of the data is seen in 10. The sheet resistance is plotted as a function of temperature and magnetic field strength. This representation makes it very easy to see the effect of the two gate potentials on the magnetic field sweeps. Furthermore the BKT temperature is more easily identified. In this section the BKT temperature is referred to as the temperature at which the array becomes superconducting. This is not the exact definition since single vortices injected by the magnetic field might still have enough energy to overcome the pinning potential energy [21] I use the term BKT to indicate the temperature at which the array becomes resistive.

The behavior of the array for magnetic fields sweeps significantly depends on the position in gate-space. The sweeps were performed in all three regimes (junction, puddles and j+p regimes) and are showed in figure 10. The first picture a) shows the data for the device D3 in the junction regime i.e the top gate voltage is $V_t = -3.0V$ and the frame gate voltage is $V_f = -0.9V$. As a function of the magnetic field, the sheet resistance is oscillatory which is the main characteristic feature of JJa's. It is difficult to identify the zeroth peak but it located at $B = 0.66mT$ and the integer peak periodicity

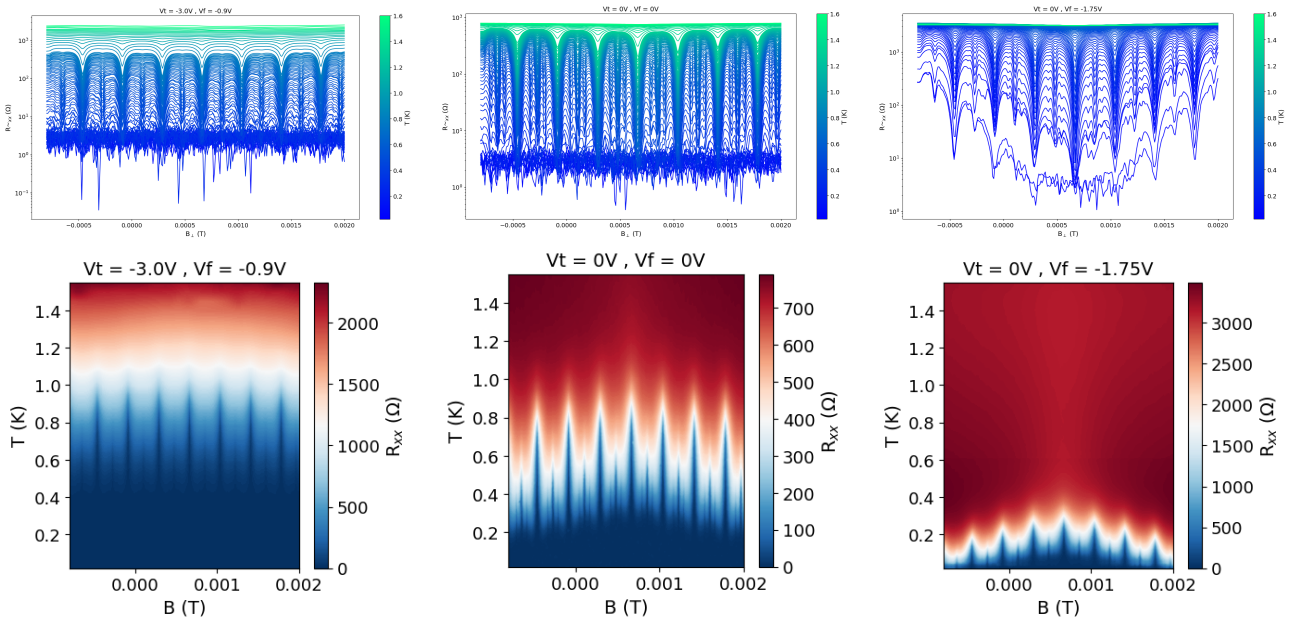

Figure 10: **From left to righta)** The magnetic field scan of device D3 in the junction regime. **b)** The puddle+junction regime. **c)** The puddle regime.

is $375\mu B$.

The most striking feature of the scan is the fact, that the data is perfectly periodic. The BKT temperature of all the integer peaks are the same at 1K. The half frustration peaks are observed between the integer peaks and their BKT temperature has been reduced to approximately 700mK. This clearly suggests that ground state at integer frustrations are more stable against thermal energy fluctuations compared to the ground state at half frustration. Very small dips in resistance can also be seen at frustration f = 1/3 are seen in figure 10. The sequence of most pronounced frustration peaks is therefore f = 0, f = 1/2 and f = 1/3.

Now the position in gate-space is changed to the J+P regime i.e. both the top gate and frame gate voltages are set to 0V. The data is shown in figure 10 b). Two remarkably features are seen. Firstly the BKT temperature of all frustration peaks have decreased. Secondly the magnitude of the decrease in BKT temperature is not the same for all frustration peaks i.e. the periodicity has become modulated. We are referring to this modulation as the envelope function. Frustration peaks at higher magnetic field strengths are more easily suppressed by thermal fluctuations. Surprisingly the 1/3 frustration peaks have become more pronounced in this regime.

Finally the the array is tuned to the puddles regime i.e. the top gate voltage remains at 0V and the frame gate voltage is set to $V_f = -1.75V$ i.e. the junction conductance through the junctions are decreased by the electric potential. In this regime, the array barely becomes superconducting. This scenario is very similar to the measurement of the critical current in the puddle regime (figure 8). We suggest it is the same mechanism that is responsible for the suppression of superconductivity: Increasing the electron density in the puddles might cause an inverse proximity effect where the **amplitude** of the superconducting order parameter is suppressed. This effect seems to reduce the critical magnetic field of the superconducting gap. The peaks at f = 1/3 are still visible near the f = 0 peak, but are significantly suppressed near frustration f = 2.

The three measurement in figure 10 support the idea of separating the physics of the array into different regimes in gate-space. The same trends are observed in device C2. A more systematic investigation of the top gate dependence was performed on device C2. The frame gate voltage was

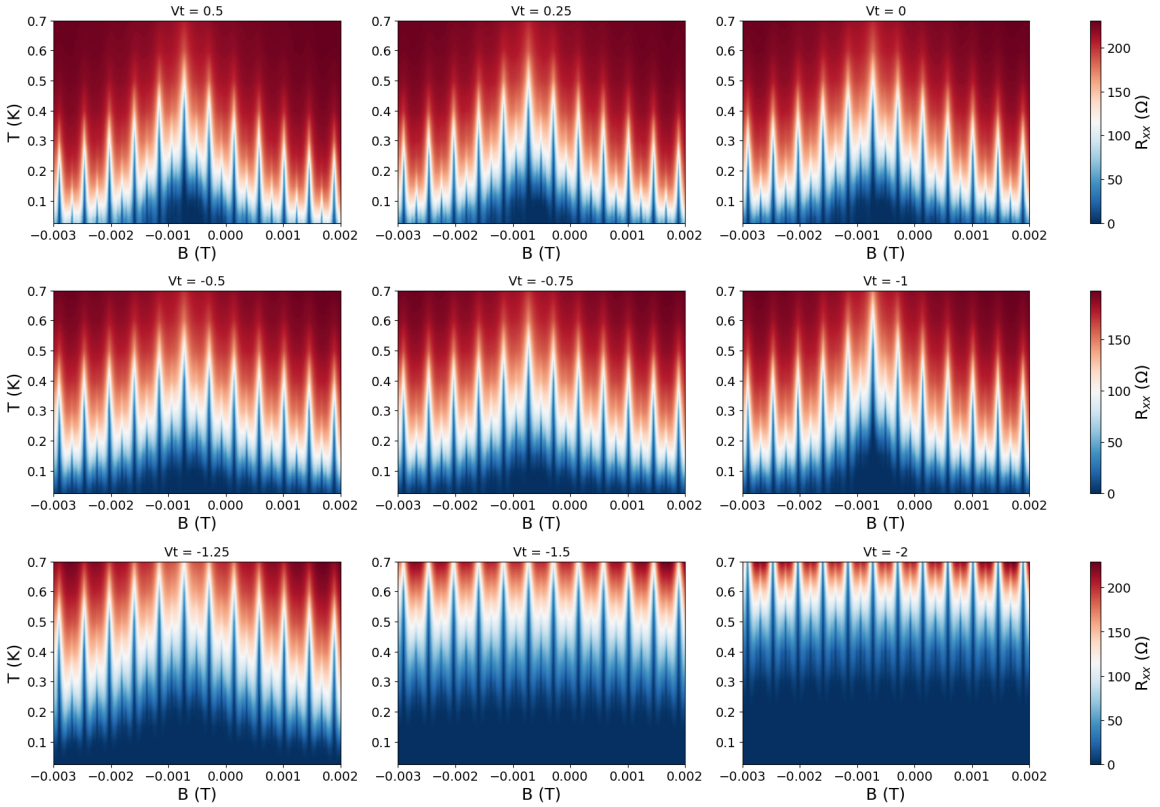

Figure 11: A sequence of magnetic field scans of device C2 from the J+P regime to the junction regime. The top gate voltage was swept from 0.5V to -2.0V.

held constant at $V_f = 0.2$V while the top gate voltage was swept from 0.5V to -2.0V.

The sequence of magnetic field sweeps on device C2 is shown in figure 11. The top gate sweep can be visualized in the gate-gate figure 6 as a horizontal line from the J+P regime to the Junction regime.

The peak at $B = -0.73mT$ is identified as the f = 0. The most visible and widest peaks are the integer frustrations. The periodicity of the integer peaks is $430\mu B$. The integer peaks are always visible and they are the most resilient against the temperature. Between the integers peaks, the f = 1/2 frustration peaks are seen. The superconducting ground state at half frustration is destroyed much earlier in temperature than the integer frustration. The half frustration peaks are flanked by two peaks which corresponds to f = 1/3 peaks. The f = 1/3 peaks are visible for most of the top gate values.

The general effect of the top gate voltage is clearly seen. Increasing the top gate voltage (in this context and in the rest of the thesis, the word "increasing" means changing the voltage to a more negative value), and thereby reducing the fermion density in the plaquettes, causes the envelope function on top of the frustration peaks to become less pronounced. At low top gates voltages, non-integer frustrations becomes suppressed at very low temperatures. Increasing the top gate voltage, the BKT temperature for all peaks are also increasing. The BKT temperature continues to increase until $V_t = -2V$, at which the frustration peaks are perfectly periodic (at least within the a range of six integer frustration peaks). At such high top gate voltages, the fermion density in the puddles is extremely low. Reducing the plaquette fermion density results in isolated superconducting islands and a more well-defined array. Intuitively, one would think that such a system should be well described by the XY model. The model Hamiltonian eq. 7 of the Josephson junction array suggests that all integer frustrations are identical. This certainly seems to be the case for device C2 in the junction regime, but not in the J+P regime. Due to the perfectly periodic frustration peak, the data suggests that the array is indeed well described by the XY model in the junction regime but more complicated physics must be included in puddle and j+P regimes. In order to explain the envelope function, [34] suggests that the coupling constant (The Josephson energy) in the hamiltonian (equation 7) no longer

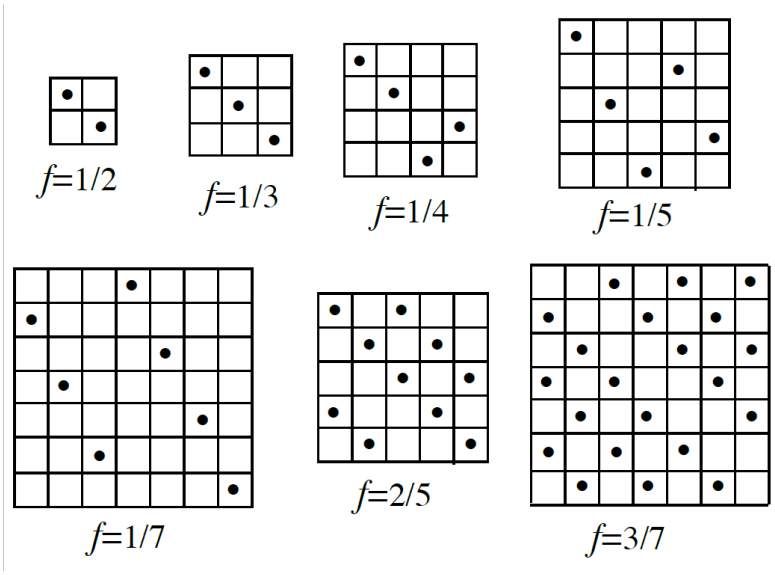

Figure 12: The ground state configuration of vortex lattice at rational frustrations. [34]

is constant, but is dependent on both the temperature and the magnetic field.

The features seen in the magnetic field scans can be explained by considering the dynamics of the vortices in the array. Vortices move in the periodic pinning potential generated by the underlying Josephson lattice [31]. The stability of the vortex lattice is determined by a competition between vortex-vortex interactions (which is determined by the mean distance between vortices) and commensurability with the underlying vortex pinning potential from the Josephson junction array [36]. At rational values of the frustration f = p/q, the vortex lattice induced by the magnetic field is commensurate with the Josephson junction array and the vortex lattice forms a superlattice of size q time q [19].The vortex lattice at rational frustration can be visualized as regular lattice shown in figure 12. The hamiltonian of the XY model can be mapped into a Coulomb gas with "charge" n_i + f where n_i is the vortex vorticity [34].

The relative stability of the vortex lattice at rational frustration depends on the coordination number of the array. For square arrays, the sequence of frustrations beginning with the most stable lattice is f=1/2, f=1/3, f=1/4, f=2/5, which have both been simulated and observed experimentally [20]. It is clear from our data, that we see the same sequence of relative stability in both devices. Experimentally the stability of the peaks are determined by their BKT temperature. The dips in the resistance occurs due to formation a stationary vortex lattice and its stability is inferred by the temperature at which the lattice is broken and the array becomes resistive. Interestingly, the frustration peaks at f = 1/4 and smaller values cannot be seen in any of our measurements.

The general effect of the magnetic field on the array resistance have been introduced. The effects of all the available tuning parameters have been accounted for.

4.6 Precise determination of frustration

The main focus of this project is to study the SIT quantum phase transition the array as a function of frustration. More specifically we have investigated the zero bias resistance as a function of temperature at a handful of precisely selected values of frustration: 0, 1, 1/2 and an irrationals. The first irrational value is approximated as f = 0.22 and the second irrational value is chosen to be $f = (3 - \sqrt{5})/2$.

Therefore it is important that the tuning of the magnetic field is accurate. Theoretically it is possible to determine the precise value of the magnetic field since the area of the plaquettes are known. But this is experimental physics, so everything is always harder than it sounds. We observed that the value would slightly change for each measurement. Both the precise position and the period between

frustration peaks slightly fluctuates between each experiment. Therefore we used the following method to determine the frustration parameter as precisely as possible before each measurement: Firstly the gate space parameters are chosen. Secondly a resistance vs magnetic field scan is started. Such as scan is shown in figure 13. The majority of these magnetic field scans were done at higher temperatures than base 15 mK since the frustration effects often aren't visible in the superconducting state. The array was made slightly resistive either by increasing the temperature (up to 400 mK) or by applying a small DC bias current. The data in figure 13 shows a scan for device C2 in the junction regime at 400mK. The lockin time integration constant was usually set to a low value for the large scan.

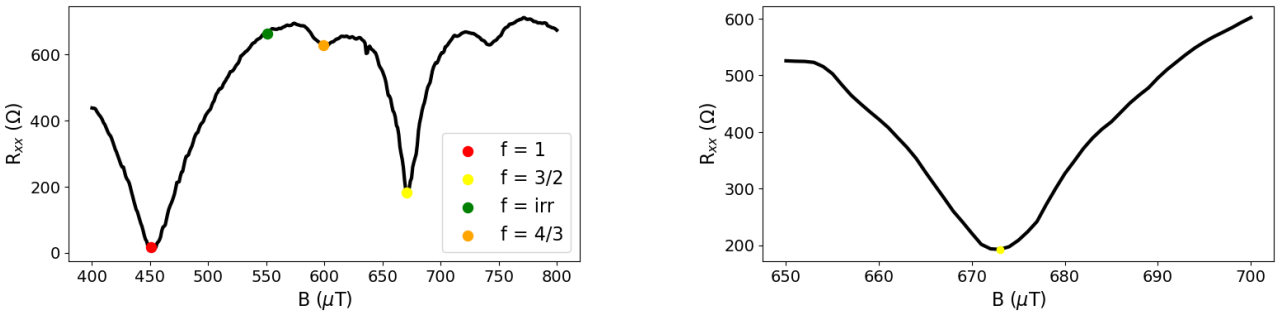

Figure 13: **From left to right. a)** The magnetic field scan is used to determine the precise value of the frustration parameter. We identify f = 1 as the first large dip in resistance. **b)** A small scan with higher lockin integration time was performed in the vicinity of the desired frustration.

In the large scan, the following frustrations are seen: f = 1 at 451μT, f = 3/2 at 671μT, f = 4/3 at 148μT and f = 0.22 at 551 μT. A more refined scan was started after the wide magnetic field scan. The magnetic field value was centered around the desired frustration value and the lockin integration time was increased. Usually it was set to 3 seconds.

4.7 The superconductor to insulator transition

This section introduces the main results of the thesis namely the investigation of the SIT quantum phase transition. During the experiments, we quickly discovered that the SIT significantly depended on the top gate voltage and the frustration. The main features we investigated have been the BKT transition and the low temperature resistance saturation.

In this section, a phenomenological description is presented of the BKT transition in Josephson junction arrays and the appearance of resistance saturation at low temperatures. The first of our main research questions has been under what circumstances the resistance saturation occurs. Specifically we have been investigating how the prevalence of the anomalous metallic phase changes between the junction and puddle regimes. Furthermore, the prevalence of the resistance saturation as a function frustration was investigated in both regimes.

Our second research questions has been in what regimes and at which frustrations the resistance lines deviate from the "perfect" BKT transition. We have been investigating how the resistance lines deviates from the ideal BKT transition line by analyzing the curvature of the resistance lines and by fitting our data to the predicted BKT line. In this section our data of the SIT's are presented.

A typical measurement of device C2 is shown in figure 14. The frame gate was swept from -2.5V to -4.2V while the temperature was kept constant. The frame gate sweep was done for 100 temperatures in the range 0.02 to 1.9 K. The temperature interval is 20mK to 800mK in 10mK increments, and from 850mK to 1.9K in 50mK increment. Similar frame gate sweep measurement was done at top gate voltages 0V, -1.5V, -2.0V and -4.0V and at frustration f=0, 1, 1/2 and irrational. The top picture shows the sheet resistance as a function of the frame gate voltage at multiple temperatures. The lockin phase of the preamplified current was also recorded for each scan and is shown in the bottom picture. It is seen that the lockin phase remains below 20 degrees for the majority of the scan but at $V_f = -4.0V$ the phase drastically increases to approximately 90 degrees. A large shift is caused by

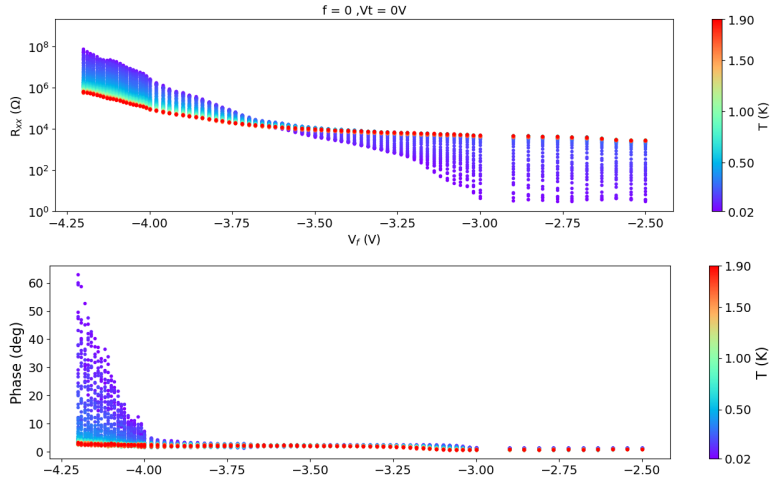

Figure 14: The top figure shows the data of a typical measurement. The resistance is calculated by dividing the voltage drop across the sample device by the current (and divided by the voltage and current preamplifier constants). The bottom figure shows the phase of the preamplified current. When the array becomes insulating, the phase of the current significantly increases.

inductive or capacitive circuit elements. Since no such elements should be present, we exclude data in the analysis if the lockin phase reaches large values. The threshold value for device C2 was set to 20 degrees and for device it is 30 degrees. The large phase shift occurs when the array becomes highly resistive. We suspect this has something to do with the current preamplifier (The Basel). The IV-converter has an internal resistance proportional to the gain. When the array becomes insulating, the sample resistance and the internal resistance of the IV-converter become comparable.

In order to circumvent this problem, the gain on the preamplifier could be further increased. This however would overload the lockin amplifier. The preamplifier gain was 10^8 for all the measurements.

A vertical line cut at a constant frame gate voltage indicates the current phase of the system. At Vf = -2.5V the array resistance is decreasing when the temperature is going towards zero which is characteristic of the superconducting phase. The opposite occurs at Vf = -4.0V where the resistance is increasing when the temperature is going towards zero. This is the main characteristic of the insulating phase. The line at which the temperature dependence of the resistance switches is referred to as a separatrix between the superconductive and insulating phases. Plotting the vertical line cuts in figure 14 generally is how researches present their SIT measurements i.e the resistance lines as a function of temperature.

The entire data set of the SIT experiments are shown in following figures. This may be slightly overwhelming for the reader, but it allows to more easily see the effects of the frustration and top gate voltage. The SIT's of device C2 are shown in figure 15 to 18 and of device D3 in figure 19 to 20. The pink and black lines are used in the analysis in the following section, and will be explained. The data in these figures have been normalized with respect to the aspect ratio of the array aspect ratio (3.77) hence the maximal resistance that can be trusted is approximately 10MΩ. The figures are grouped based on the top gate voltage. The ranges/interval of the frame gate is not the same for measurements at different top gates since the frame gate interval required to push the array out of superconductivity is simply not the same in the different regimes.

4.7.1 Device C2

The top gate and frustration parameters are independently tuned, so ideally each of their effect on the SIT . It turns out to be more complicated since each tuning variable maybe cause the same changes in the SIT data. Furthermore it is difficult to directly compare the measurements of device C2 at

different top gate voltage since the frame gate interval used to drive the SIT is not the same. The frustration dependence on the SIT at fixed top gate voltage is more easily compared. It is seen that frustration causes the SITs to change in multiple ways. When the frustration is set to irrational of half frustration, the BKT temperate decreases. The BKT temperature at f = 1 often is slightly smaller than at f = 0. This trend has already been observed in the magnetic field scan in figure 11.

When the frustration is changed, it causes the curvature of the resistance lines to change. This is very clearly seen in figure 25. Qualitatively the is a difference between the curvature of the superconducting lines at f = 0 and f = 0.22. This feature is very surprising and will be discussed in details in later sections. Finally it is seen that the prevalence of low-temperature

The most direct SIT is observed for the measurement at top gate voltage $V_t = -2.0V$ and -4.0V. When the top gate voltage is increased, the frame gate interval required to drive the transition from the superconducting phase to the insulating phase is extremely small. Hence the density of lines near the superconductor-insulator separatrix is very low. It is also seen in figures 27 and 27 that the data become more noisy. We are not sure what causes this. We investigated if something had happened to our setup by going back to top gate voltage V_t = -1.5V and do the same measurement again. But the obtained data was as good as the previous measurement at V_t = -1.5V.

The high resistance saturation problems due to the Basel are clearly seen in figures 27 and 27. It is seen that the high resistance lines are pointing upwards which suggests that the saturation is due to the Basel on not an intrinsic property of the array in this regime.

Another feature which is seen in all resistance lines occurs at temperature around 1.7K. A gate-independent decrease in resistance is observed. We suggest this drop in resistance occurs due to the formation of superconductivity on the aluminum islands. This feature is observed in all of our data, and it is a common feature in all SIT measurement on Josephson junction array found in the literature.

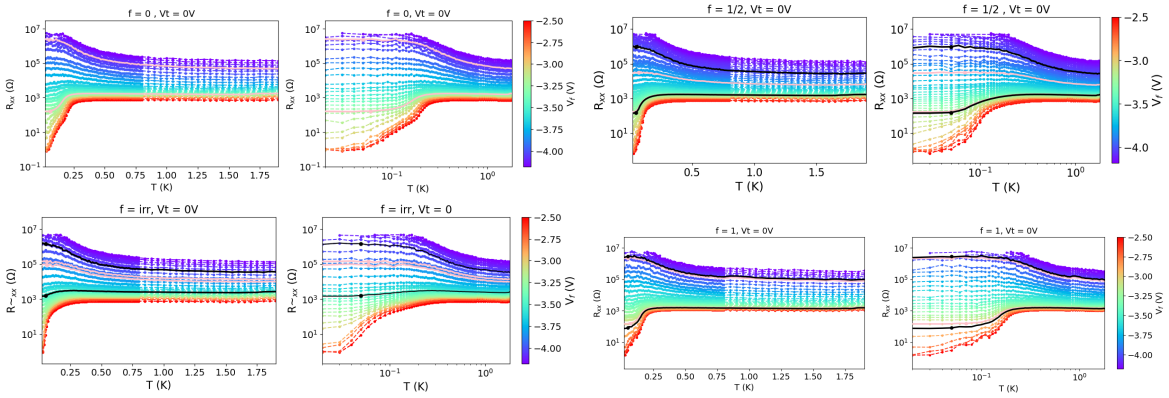

Figure 15: The SIT of device C2 at top gate voltage $V_t = 0$V and at four different values of frustration: f = 0, f = irr, f = 1/2 and f = 1.

4.7.2 Device D3

The top gate dependence is easier to see in the data of device D3 since the frame gate interval used to drive the SIT have similar starting value which is -1.0V at $V_t = 0.0V$ and -0.95V at V_t = -4.0V.

When the top gate voltage is increased to -4.0V, the superconducting phase transition consistently occurs at lower temperatures than for V_t = 0.0V at all frustration. According to the analysis of the critical current and the magnetic field scan, this is not exactly the expected behavior of the top gate. We have shown multiple experiments indicating that the inverse proximity effect is strong when the fermion density in the plaquettes are large. We suspect that the due to the increased thickness of the junction in device D3, the inverse proximity effect might be less prominent in device D3 compared to

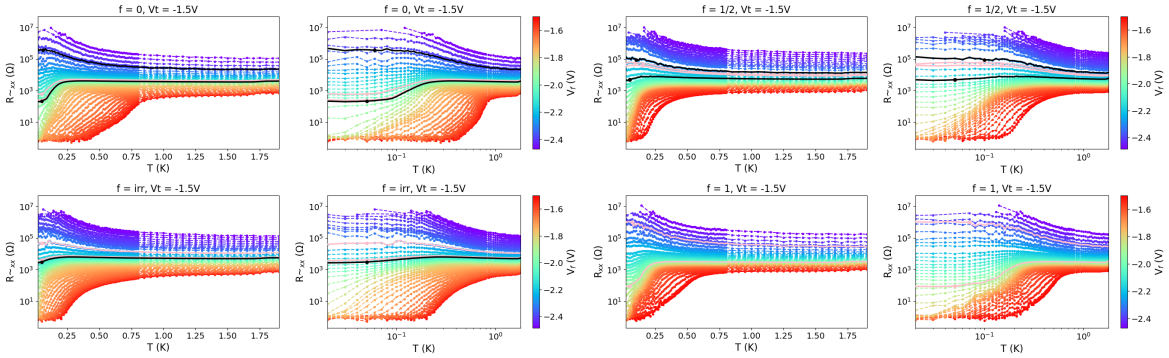

Figure 16: C2 Data at Vt = -1.5V

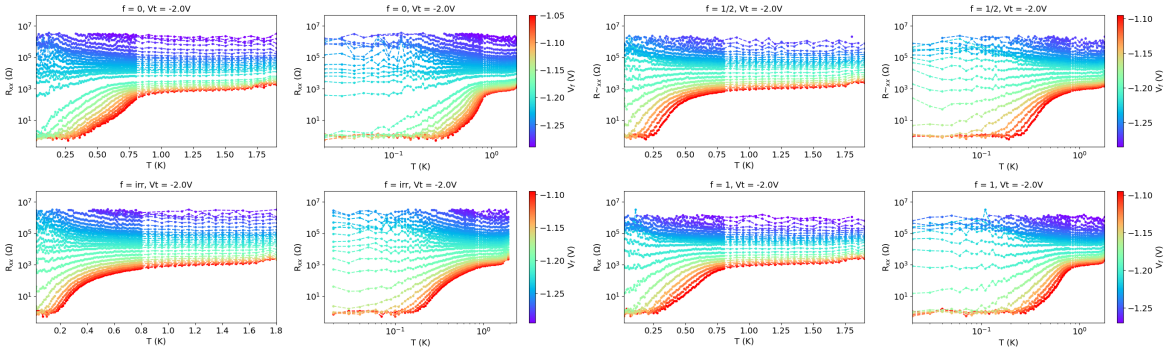

Figure 17: C2 Data at Vt = -2.0V

C2.

When the top gate voltage is large, the the normal state resistance increases much faster. The frame gate interval at which the array becomes highly resistive is approximately 2 volts at $V_t = 0.0$V whereas the interval is less than 70mV at V_t = -4.0V. It is seen in figure 20 that largest reported resistance is $5 \cdot 10^5$. The phase of the current became larger than 30 very quickly in the frame gate scan, and hence these data points are not included.

The frustration dependence on the SIT follow the same trends seen in device C2. Increasing the frustration from zero to an irrational or half frustration value significantly decreases the BKT for both top gate voltages. It also causes significant changes to the line curvature.

5 The anomalous metallic phase

So far only the curvature of BKT phase transition has been accounted for and not for the lines going insulating. The excepted curvature of the insulating lines in a similar system, namely the granular superconductor, is reviewed by V.F. Gantmakher [17]. The tunneling current between two granules consists of two channels: The coherent tunneling of Cooper pairs which constitutes the supercurrent, and a single-particle ohmic dissipative channel which carries a normal current. If the Josephson coupling is suppressed, only the dissipative channel remains. In the case of $E_C >> E_J$, quantum phase fluctuations of the superconducting phase destroy coherent tunneling of Cooper pairs. When the temperatures is going towards zero, the number of single-particle tunneling events decreases exponentially. Hence the resistance of the system increases exponentially as following expression:

$$R \propto R_0 \cdot e^{\frac{E_a}{k_B T}} \tag{20}$$

Where E_a is a fitting parameter and k_B is the Boltzmann constant. Equation 20 is the expected temperature dependence of the sheet resistance in the insulating phase. Such Arrhenius (plotting the

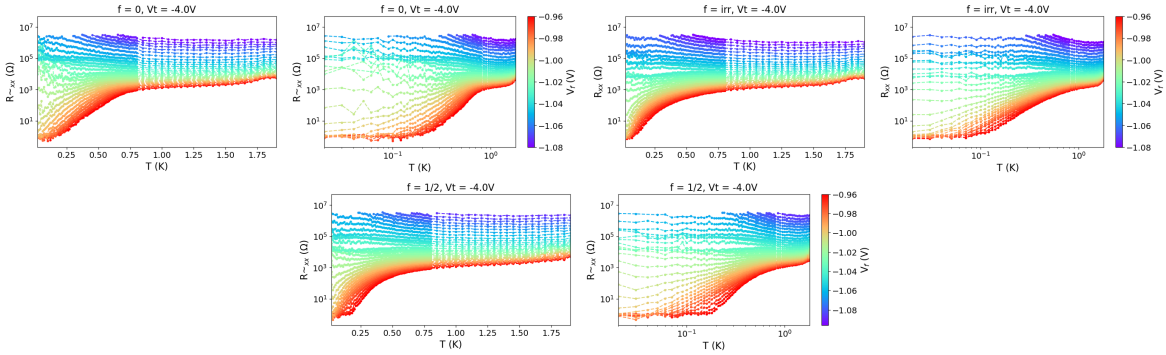

Figure 18: C2 Data at Vt = -4V

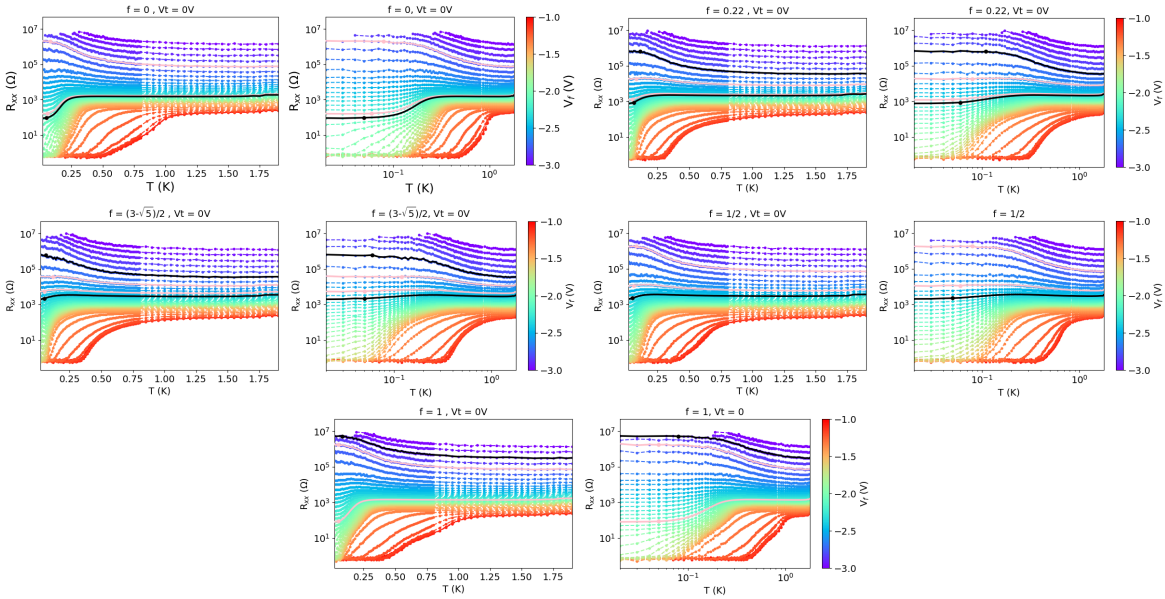

Figure 19: D3 Data Vt = 0V

logarithm of the resistance as a function of 1/T is called an Arrhenius plot) behavior has been seen in experiments on proximitized Josephson junction arrays [2].

It is clearly seen in our SIT measurements that multiple lines do not have the curvature predicted by any of the presented theories. The resistance of multiple lines saturates at low temperatures and become temperature independent. This is main characteristic of the so-called anomalous metallic phase. The key observation of the anomalous phase is the drop in sheet resistance as a function of decreasing temperature as if the system was becoming superconducting, but instead of reaching zero temperature, the resistance saturates at low temperatures. This ground state is referred to as metallic, since the definition of a metal is finite conductance (hence also a finite resistance) as $T \to 0$ [3]. The metallic phase occurring in our data however usually saturates at a resistance multiple orders of magnitude lower than resistance predicted by Drude theory. Furthermore the bosonic description of the SIT suggests that the transition occurs without an intervening metallic phase [29]. If an intermediate metallic phase exists in the in the SIT phase transition, what is its origin? Is it the breaking of phase coherence due to enhanced quantum fluctuations? And if so, what is the difference between the metallic phase and the insulating phase? The appearance of low temperature resistance lines are therefore referred to as the "anomalous metallic phase". The low-temperature saturation of resistance has been observed in numerous experiments on different systems [12].

It is seen in our data that the saturation of the resistance occurs both for lines initially going towards the superconducting phase and also for lines going towards the insulating phase. In order to

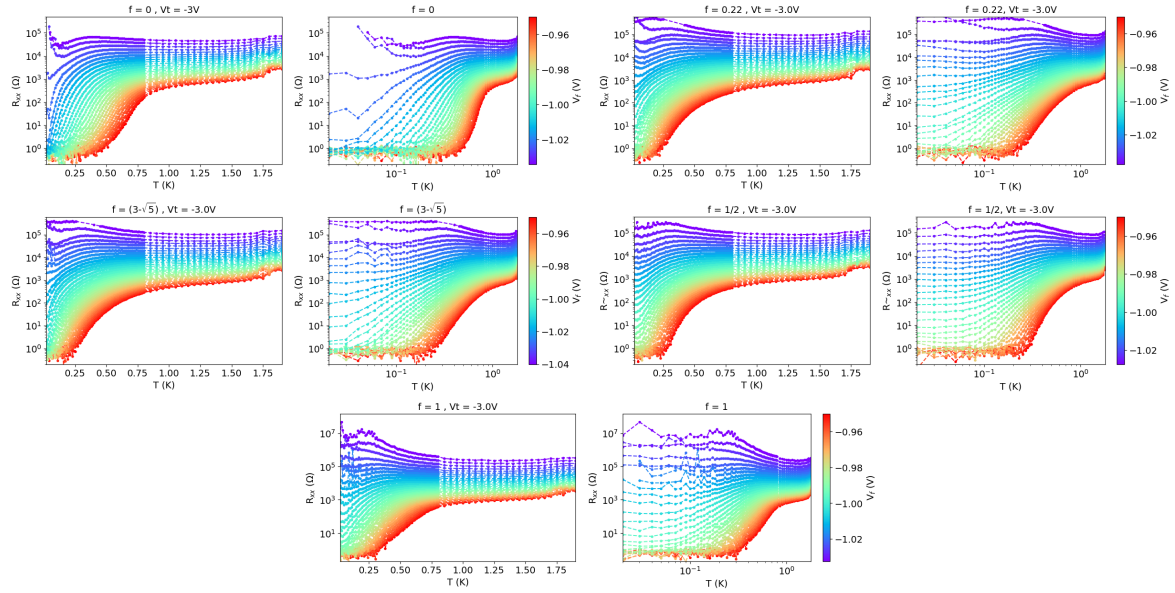

Figure 20: D3 Data Vt = -3.0V

separate the two phenomena, A. Kapitulnik introduces the terms “failed superconductors” and “failed insulators [37]. In this section the prevalence of both failed superconductors and insulators in the SITs are discussed. It is investigated in which regimes and at what frustrations the resistance saturation occur the most.

The “strength/prevalence” of the anomalous phase is based on two parameters. The first is the temperature at which the resistance lines begin to saturate. Higher temperatures suggests that the mechanism which causes lines to saturate are more resilient against thermal fluctuations. The second parameter is the normal state resistance (NSR) interval at which the saturating lines occur. A large normal state resistance interval suggests that the resistance saturation is very prevalent. The normal state resistance intervals are comparable between different top gate voltages whereas the frame gate voltage intervals are not. This is due to the fact that the frame gate interval required to drive the SIT is not the same at different top gate voltages.

In order to categorize the prevalence of the anomalous phase in a systematic way, we have to define a function which determines if the resistance line is saturating or not. Specifically we must define a resistance interval in which data points are allowed to fluctuate. The magnitude of fluctuations in our setup can be determined by measuring the resistance as a function of time without changing any external parameters. We unfortunately didn’t perform this measurement. I therefore define the following criteria to determine if a resistance line is saturating or not: All data point has to be within 6 percent of the data point for the highest temperature in the plateau. This threshold is also increased to 9 percent in order to see, if significant changes occur. Furthermore in order for the function to categorize as resistance line as saturating, the plateau must contain at least three points not including the data point at 20mK. This means the resistance saturation must start at 50mK or at higher temperatures. We have omitted the data point at 20mK because we think the electron temperature might be slightly higher than the mixing chamber temperature in the dilution fridge.

The largest and lowest frame gate voltage at which a saturating resistance line occur are shown in our data as the pink and black lines. The pink lines indicate that the threshold value of the allowed fluctuations is 6 percent, and it is 9 percent for the black lines. If only one color is present, the function finds the same interval for both threshold values. It is important to note, that not all lines in the reported normal state resistance interval are categorized as saturating by the function. Therefore the number of saturating lines is also reported. The number of saturating lines can only be compared for different frustrations at the same top gate value since the number and density of frame gate values is

not the same for different top gate values.

The normal state resistance intervals are summarized in figures 21 and 22. The diagrams show the normal state resistance difference between the first and last resistance line that is saturating The analysis was performed for top gate voltages $V_t = 0$ and -1.5V for device C2 and 0V for device D3. The data for the other top gate voltages are very noisy which makes it difficult to define a proper function that can categorize plateauing lines.

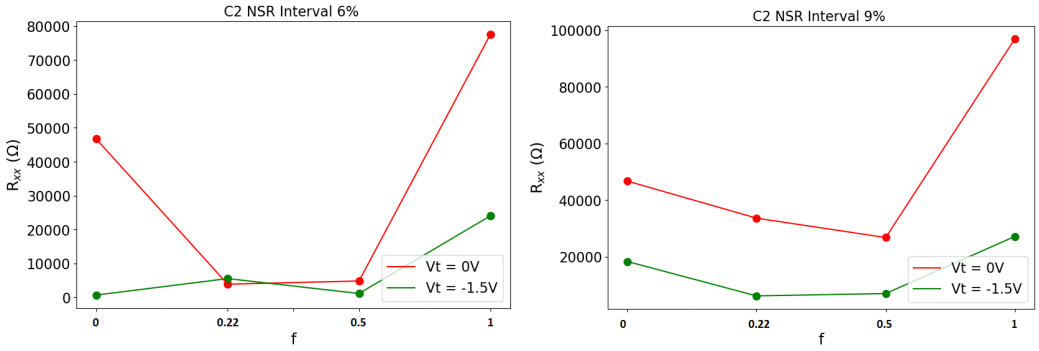

Figure 21: **Left to right: a)** The normal state resistance interval on device C2. The threshold value of the fluctuations is set to 6 percent. The sequence of frustration is, 0, 0.22, 1/2 and 1. **b)** The threshold value is increased to 9 percent.

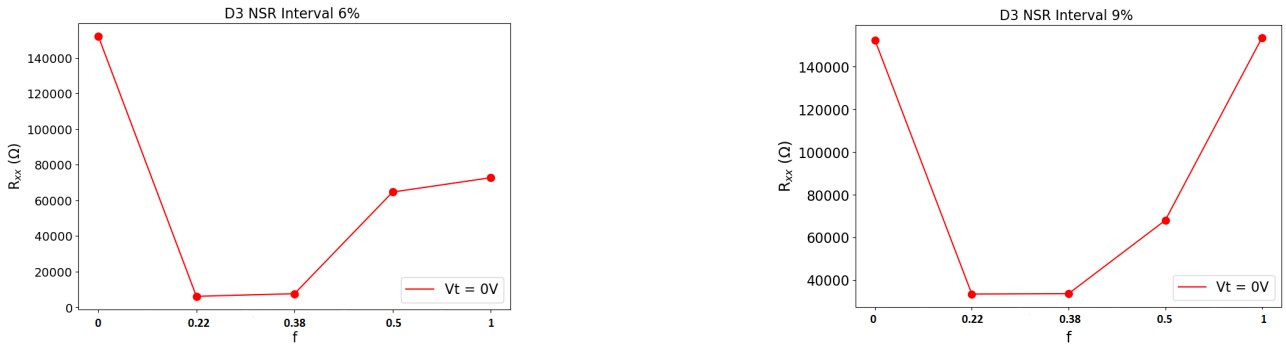

Figure 22: **Left to right: a)** The normal state resistance interval on device D3. The sequence of frustration on the x-axis is, 0, 0.22, (3- $\sqrt{5}$)/2, 1/2 and 1. The threshold value is 6. **b)** The threshold value is increased to 9.

It is clearly seen in figure 21, that the normal state resistance intervals in device C2 depends on both the top gate voltage and frustration. For top gate voltage $V_t = 0.0V$, the NSR interval at integer frustration is much larger compared to the NSR for irrational and half frustration. When the top gate voltage is increased, the NSR at integer frustration are significantly reduced. The same trends are seen in figure 22. The NSR interval is narrow for both irrational values and is wide for integer frustration.

The picture is largely the same for both threshold values with one exception. The NSR interval for f = 0 in device C2 is very narrow when the threshold value is six percent. The number of lines categorized as saturating by the function is only 6 wheres the number of saturation lines at f = 1 is 24 (which increases to 23 and 34 respectively when the threshold value is increased to 9). This is an example of the fact that this method might not be the most precise and reliable, but it can be used to qualitatively describe the prevalence of the anomalous phase as a function of our tuning variables.

The temperatures at which the saturation occurs are generally slightly larger at $V_t = 0.0V$. For instance, for the 9 percent threshold, the range of saturation temperature at f = 0.22 is 50mK to

130mK whereas it is 50mK for every saturating line at $V_t = -1.5V$.

The Hamiltonian of the array introduced in equation 7 is only taking Cooper pair tunneling into account. It does not include dissipation effects. Dissipation effectively means, that a continuum of degrees of freedom couples to the critical modes of the system [11]. The quantum variable of the Josephson junction array is the superconducting phase of each junction. Effects of dissipation in JJa can cause suppression of the quantum fluctuations of the phase [15], [11]. This effect actually stabilizes the superconducting phase of the array. Kapitulnik et al. [11] conjecture, that the dissipation strength continues to stabilize the superconducting phase until a certain critical value of the dissipation strength is reached. At this point, the anomalous metallic phase occurs. The metallic phase is stabilized by a strong coupling to the dissipative environment. In our device, we suspect that the presence of the puddles, which contains a huge reservoir of normal electrons, acts as a dissipative environment (which A. Allain et al. suggests is the case in their proximity coupled JJa of tin islands on top of a graphene sheet [2]).

Extensive research has been conducted on dissipation effects on the prevalence of the anomalous phase. To my knowledge this is not the case for the prevalence of the anomalous phase as a function of frustration. The microscopic mechanism of the frustration dependence on anomalous phase is hence very unclear. It is seen in figure 21 and 22, that frustration is a significant parameter in the stabilization of the anomalous phase. We suggest, that it is more difficult for the dissipative degrees of freedom to stabilize the phase fluctuations due to the incommensurability of the vortex lattice at irrational frustration. At integer frustration, it is easier for vortices to form a stable lattice, and hence the dissipative coupling might be stronger. At irrational frustration, the formation of a stable vortex lattice is harder.

6 The BKT phase transitions

It is clearly seen in the presented data, that the curvature of the resistance lines that go superconducting are not the same for different frustration and top gate voltages. The transition from the resistive phase to the superconducting phase is described by BKT theory. In this section it is investigated if the all features of the superconducting phase transition can be captured the BKT theory presented so far.

Inspired by the work of Bøttcher et al. [13], the curvature of the resistance lines is analyzed by fitting the data to the predicted expression of the BKT transition. In their work, the BKT temperature in a single gated Josephson junction array was obtained by fitting the resistance curves with the BKT form. But the BKT theory presented so far was derived from the XY model which is a simplified model. Neither the magnetic field nor dissipation effects were included. Furthermore the spin coupling energy was assumed to be temperature independent which might be a bad approximation [9]. The natural question that arises is if equation 15 is the best fitting function to use on our data, and if not, what fitting function should be used?. Multiple research groups have suggested improvements to the expression in equation 15 in order to include more detailed physics.

To begin with, the vortex unbinding picture introduced by Kosterlitz-Thouless was originally derived for neutral superfluids [27]. M. R. Beasley et al. argues that the the vortex interaction idea is also valid for charged superfluids (i.e. superconductors) [5]. Due to fabrication limitations, most experimental work on the BKT transition has been on thin homogeneous superconducting films which are considered as continuous superfluids. But can the formulas for the temperature dependence of the resistance in continuous superfluids be used on the discrete Josephson junction lattice? C. J. Lobb et al. [6] have compared the theory of vortices on discrete lattices and continuous superfluids. They argue that significant difference can be found between formulas on discrete lattices and homogeneous superfluids. They introduces the following expression for the temperature dependence of the sheet resistance:

$$R = b_1[I_0(E_J(T)/(10kT)]^{-2} \cdot R_n \cdot e^{-(\frac{b_2}{T'-T_c'})^{1/2}} \tag{21}$$

Where I_0 is the hyperbolic Bessel function or order zero and T' is the reduced temperature shown in equation 16. The reduced temperature is introduced in order to take the temperature dependence of the Josephson energy into account. Near the BKT temperature, the expression 21 becomes very similar to the result of Halperin and Helson: [22]

$$R = b_1 \cdot R_n \cdot e^{-(\frac{b_2(T_{c0}-T_c)}{T-T_c})^{1/2}} \tag{22}$$

Where T_{c0} is the BCS transition temperature of the superconducting film and and T_c is the BKT temperature. Halperin and Nelson derives an expression for the vortex correlation length by interpolating between the two critical temperatures namely the BKT temperature and the BCS temperature. Their result was derived for continuous charged superfluids.

The fitting function for the BKT transitions in equation 15 was initially derived based on the correlation length between vortices in the XY-model. A. M. Kadin et al. [4] suggests, that the expression for the vortex correlation length is wrong and it should be the following:

$$\xi_+(T) = C\xi(T)e^{(\frac{b_2(T_{c0}-T_c)}{T-T_c})^{1/2}} \tag{23}$$

Where $\xi(T)$ is the Ginzburg-Landau coherence length of the superconductor. When deriving the correlation length of vortices in the XY-model, screening effects were not included. Vortices with opposite sign logarithmically interacts. At temperatures close to the BKT transition, the density of thermally induced vortices are low. Hence it is unlikely that the space between a vortex-antivortex pair is occupied by another vortex pair. At larger temperatures this scenario is more likely. Having a closer pair between a large separated vortex pair effectively reduces the strength of the vortex interaction. Kadin et al. go further to suggests that the numerator in expression 23 can be replaced with T_{c0} - T instead.

This is exactly expression which has been used by Bøttcher to analyze the BKT transitions in their Josephson junction array except the temperature dependent Ginzburg-Landau coherence have been absorbed in the fitting parameter. Bøttcher successfully fit their data in the entire temperature interval between the BKT temperature and the BCS temperature of the aluminum. The fitting curves shown in their article matches their data perfectly. We have tried to use the same expressions as the fitting function on our data, but resulted in very bad fits. The function fits reasonably well (square root cusp region) at low temperatures, but does not fit the data at larger temperatures. In fact the fitting function suggested by Bøttcher performs much worse than the function derived by the XY-model.

In summary, the theory is extremely complicated and multiple expression have been proposed to explain BKT transition. The most important feature of the BKT resistive transition is the square-root cusp which is included in all the above expressions. We therefore decided to use the expression in equation 15 since it captures the most essential feature of the BKT transition.
.

6.1 Fits

The BKT fits were obtained by standard least squares fitting methods without any constraints using the SciPy package in python. Performing a least squares fit on data from a SIT measurement introduces an obvious problem: The range of resistance in a single measurement spans multiple orders of magnitude. The best curve is found by minimizing the sum of the squared value of the residuals. Data point in the insulating phase are weighted significantly higher than point in the superconducting phase. Therefore the fitting was performed on the logarithm of the data. The fitted lines was reexponentiated afterwards. The fitting function is the logarithm of the BKT expression 15:

$$R(T) = A - B \cdot \left(\frac{1}{(T - T_{BKT})}\right)^{\frac{1}{2}} \tag{24}$$

Where A, B and T_{BKT} are fitting parameters. The goodness of fit measure is the root mean squared error (RMSE) which represents the average distance between the data data points and the fit. The RMSE value is evaluated before the fits are reexponentiated.

Before the regression is performed, some data manipulation has to be done. The fitting function in equation 24 is not defined in the superconducting phase due to the square root in the denominator hence only the last data point in the superconducting phase should be included in the fit. This data point is chosen by finding the highest temperature at which the resistance is less than the noise in our system which in the superconducting state is around 0.5Ω. In the superconducting state, we measure around 2.5Ω for both device C2 and D3 before dividing with the aspect ratio. The value of the data point must therefore be less than 3.0Ω. When the first data point has been found, all the data used in the regression is subtracted by its resistance value. Furthermore, the aluminum goes normal around 1.9K. These data points are also removed. This procedure is illustrated in figure 23.

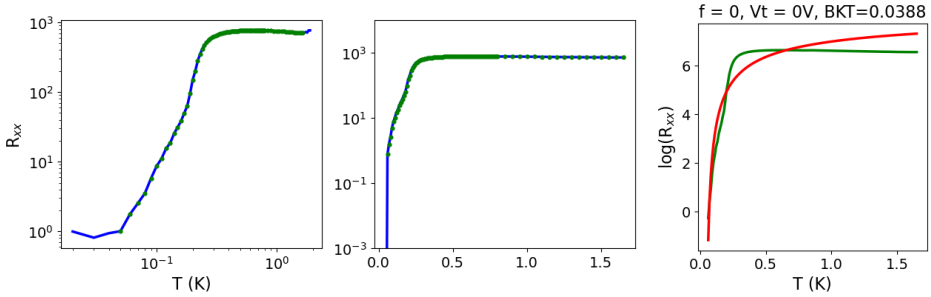

Figure 23: **Left to right: a)** The blue graph shows all the data on in a log-log scale. The green points show the remaining data after points in both ends of the temperature interval have been removed. **b)** The blue graph shows the remaining data points, but the data has been subtracted by the value of the first green point from figure a) and is plotted in a semi-log plot. The green points are the data points included in the fit. **c)** The green data from figure b) is logged. Then the fit is performed and the RMSE is calculated. Both the data and fit in figure c) are exponentiated.

The BKT fit is only performed on resistance lines that goes superconducting. It is investigated if the fits become worse or better when the frame gate voltage is increased and if significant changes of the curvature occurs. Due to the enormous size of the data set, the fit is only performed on two frame gate voltages: The first frame gate voltage in the sweep and the last voltage at which the array becomes superconducting. The fits for device C2 and device D3 are shown in the following subsection. The figures present the fits of the reexponentiated data for the resistance line. Furthermore a summary of the RMSE for all the fits are presented in figure 28 and 31. The figures show the RMSE of the fits as a function of frustration.

6.1.1 Device C2

The fits for device C2 at top gate voltage $V_t = 0.0V$ are shown in figure 24. The first row are fits at V_f =-2.5V. The second value of frame gate voltage is not the same for all the four fits since the frame gate voltage at which the resistance lines does not become superconducting slightly changes.

It is seen in figure 24 that the quality of the fits varies for different frustration. Especially the fits do a poor job of predicting the resistance at temperatures above 600mK. All the fits consistently overpredicts the resistance in this region. The overprediction is worst at integer frustration and is best at irrational frustration. As will be seen in other fits, this is the case for all fit for both devices and for all top gate voltages.

The fits at f = 1/2 and f = irr both do a reasonable job at estimate the square root cusp behavior. The fit at f = 1/2 are slightly worse that the fit at f = irr at describing the curvature of the "corner".

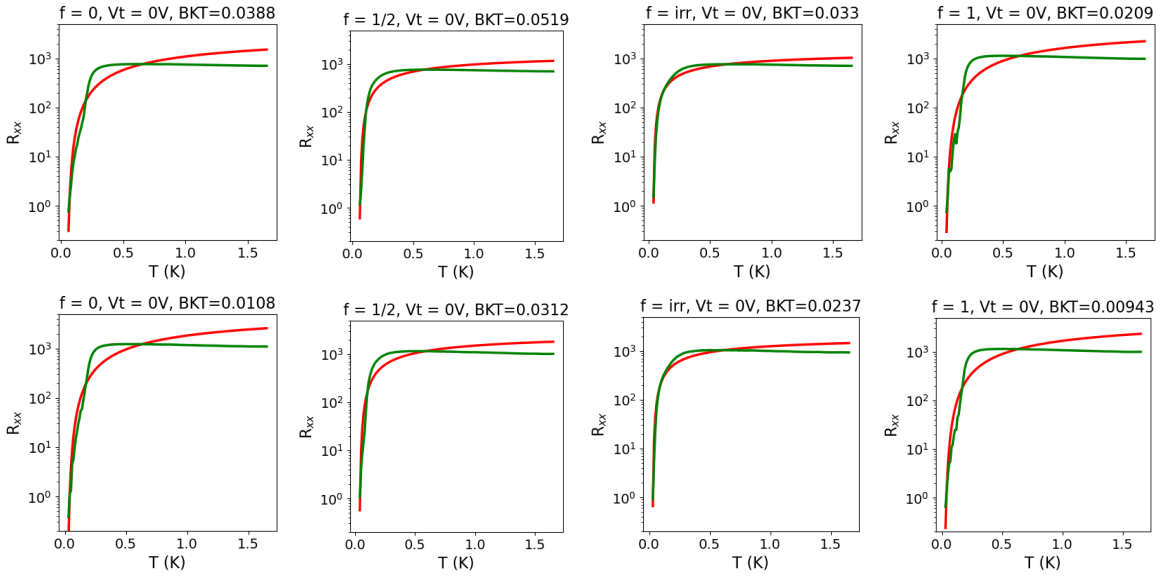

Figure 24: Fits of the data from device C2 at $V_t = 0$V. The first row show the fits at frame gate voltage $V_f = -2.50$V. The second row show fits at V_f = -2.9V.

It generally undershots the corner feature more than the fit at irrational frustration. This is the case for all fits at f = 0.5. It is seen in figure 28 that the best fit is obtained for f = irr. This fit is the best at estimating both the curvature at the corner and the high temperature resistance. This is the case for all the top gate values.

The most notable feature in the curvature of the resistance lines is found at integer frustration where a two-step process occurs. At slightly lower temperatures than the "corner" of the resistance, there is a kink in the line. This kink significantly deviates from the expected square root cusp curvature of the BKT transition. Not surprisingly, the fits are very bad at estimating the array resistance due to this kink. The kink seems to predominantly occur for integer frustrations. As will be seen in later fits, this is generally the case for both devices and for all values of top gate voltage. The kink still appears in the resistance line after the frame gate voltage is increased. The general shape of the resistance lines do not change significantly when the frame gate voltage is increased but the fits become slightly worse (i.e. the RMSE value slightly increases for all the four fits).

It is seen in the second row of fits, that the estimated BKT temperatures are very low. This is consistent with the fact that these lines are the last lines in the SIT measurement to become superconducting.

The top gate voltage is changed to $V_t = -1.5V$. The fits are showed in figure 25. The general curvature of the resistance lines have changed such that the "corner" extends over a larger temperature interval simply because the array becomes superconductive at higher temperatures in the junction regimes. Otherwise the previously mentioned trends seem to continue.

It is seen in 28 that the quality of the fits at f = 1/2 and f = irr have become better. The fit at f = irr perfectly estimates the data at temperatures lower than approximately 1K but slightly overpredicts the resistance at high temperatures. The overestimation of the high temperature region by the fit for f = 1/2 is slightly larger, and the corner is slightly underestimated.

The fits continue to be very poor at predicting the curvature at integer frustration since the kink has not disappeared. It is only present at integer frustrations and cannot be explained by the fit. We think that some thermally activated process is occurring which is not included in the fitting function.

Increasing the top gate voltage has increased the quality of the fits compared to the fits at $V_t = 0.0V$. Based on the RMSE value, the fits at irrational frustration is still the best followed the fit at f = 0.5.

When the frame gate voltage is increased, the shape of the lines become more similar to the resistance lines at $V_t = 0.0V$. Both the top gate and frame gate can decrease the superconductivity in

the array. Although the microscopic mechanisms for the suppression of superconductivity is not the same (inverse proximity vs enhanced quantum phase fluctuations.), effectively both effects reduce the BKT temperature of the resistance lines. This causes the quality of the fits to become worse.

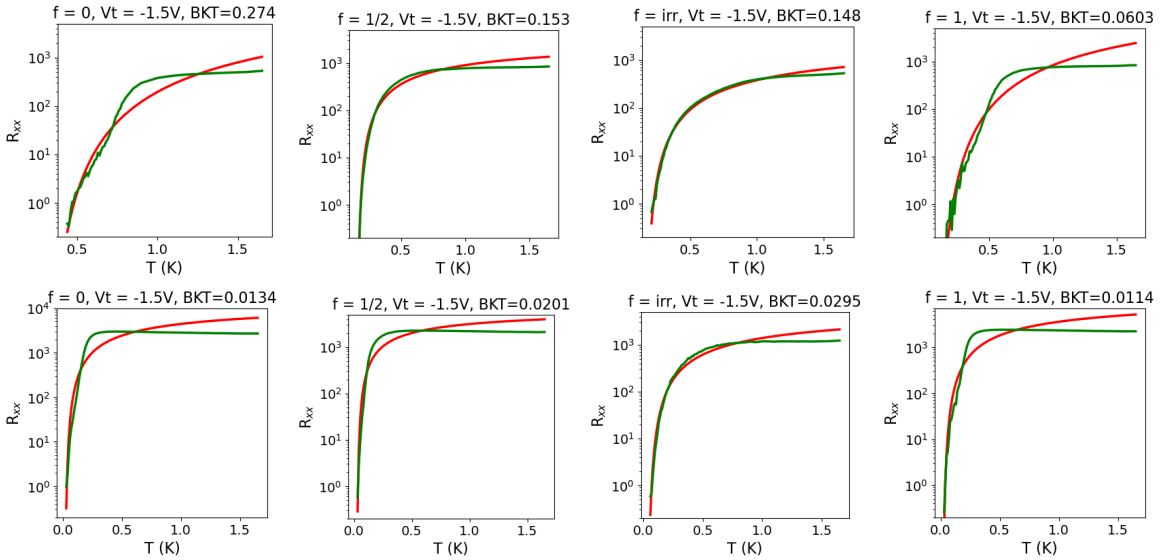

Figure 25: Fits of C2 at V_t = -1.5V. The frame gate voltage in the first row is V_f = -1.5V and V_f = -1.88V in the second row.

The fits on data at top gate voltage $V_t = -2.0V$ are shown in figure 27. It is seen, that the the fit at irrational frustration is remarkably good for the entire temperature interval. The square root cusp is perfectly estimated by the fit, and the error in the high temperature region is small. The fit at half frustration continues to underestimate the corner feature. It can be argued that the kink feature has now appeared at half frustration but it occurs at lower temperatures compared to the kink at integer frustration. When the frame gate voltage is increased, the kink feature seems to become less pronounced.

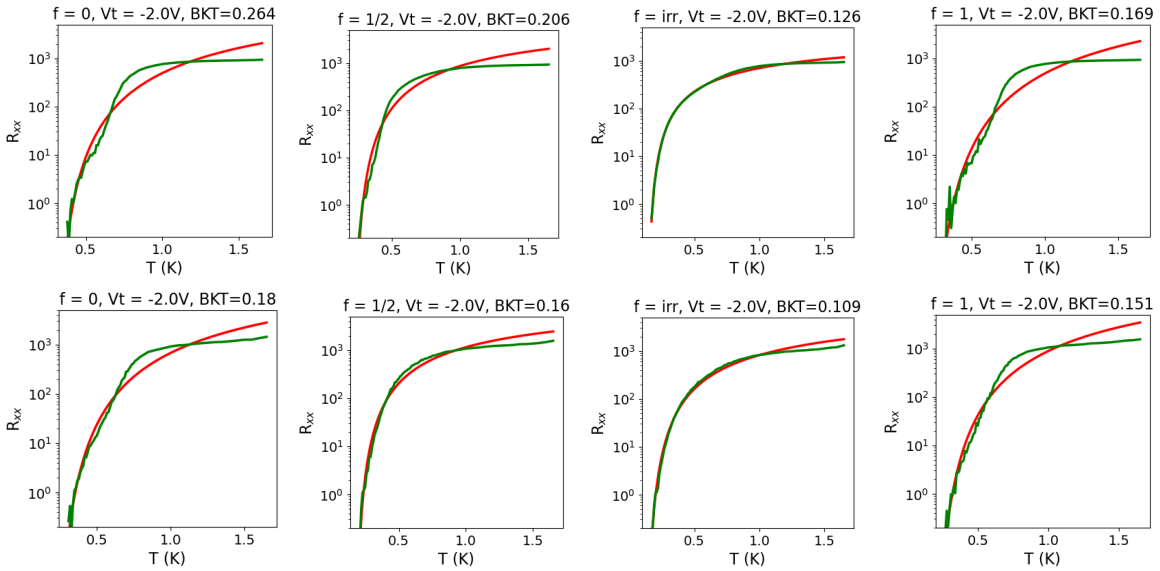

Figure 26: All fits of device C2 at V_t = -2.0V. The first frame gate voltage is V_f =0.0V and the second is V_f =-1.1V.

The fits at top gate voltage $V_t = -4.0V$ are shown in figure 27. No data at frustration f = 1 was measured due to problems with the dilution refrigerator.

The resistance line at half frustration seems to behave similarly to the resistance for the previous top gate voltage. A tiny kink has appeared, and it still occurs at a lower temperature compared to the kink at integer frustration. The kink at half frustration also becomes less pronounced when the frame gate voltage is increased. This is also the case at integer frustration. Closing the junction seems to suppress the mechanism that causes the formation of the kink.

The fits at irrational frustration are extremely good at both frame gate voltages. The fit correctly estimates the resistance in the entire temperature interval. In terms of the RMSE value, the two fits at $V_t = -4.0V$ are the best out of all the shown fits.

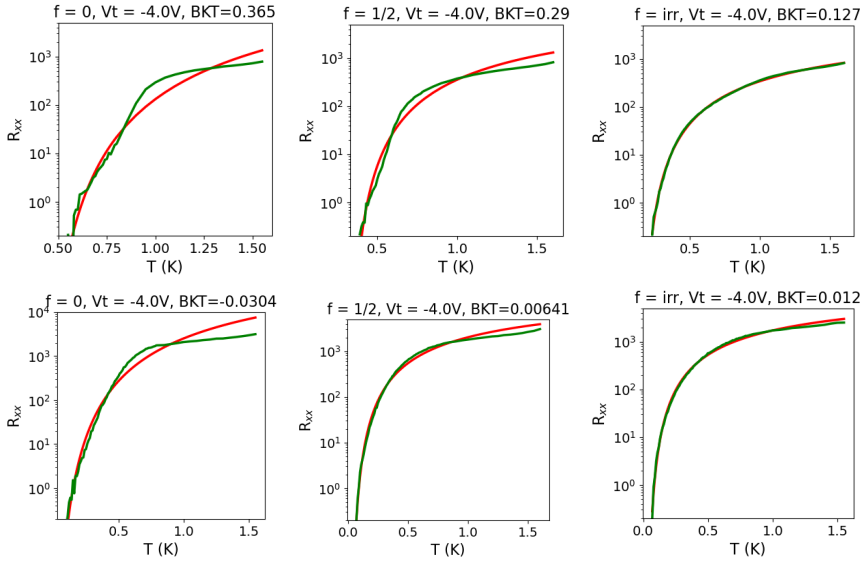

Figure 27: Fits of device C2 at V_t = -4.0V. The first frame gate voltage is V_f =-0.7V and the second is V_f =-0.98V.

The RMSE values for all the fits are shown in figure 28. Are clear trend is seen in both figures: For all top gate voltages and both frame gate voltages, the sequence of worst quality to best quality fits is the same: The fits at integer frustration are the worst followed by half frustration. The best fits are always obtained for irrational frustration.

The top gate dependence on the RMSE value of the fits is not the same for both frame gate values.

At the second frame gate value the quality of the fits at all frustration become better as the top gate voltage is increased. Initially this is the behavior we expected due to the fact that the BKT fitting function was derived for the XY model. Large top gate voltage depletes the plaquette density, which makes the array more similar to the XY model (eq.7). The most surprising result is the fact that the fits at integer frustration are this bad. The quality of the fits for integer frustration is largely independent on the top gate voltage. Increasing the top gate voltage does not change the fact that the function used to fit the lines simply does not capture all the physics. The kink feature significantly decreases the quality of the fits.

The quality of the fit i.e. how well the superconducting phase transition is explained by the simplest BKT theory depends on all three tuning parameters and it is not straight forward to predict which combinations causes the fits to become good.

6.1.2 Device D3

The fits are performed on the data from device D3. The presentation of fits is the same but note that the fits at f = 1 for different frame gate voltage are now placed besides each other.

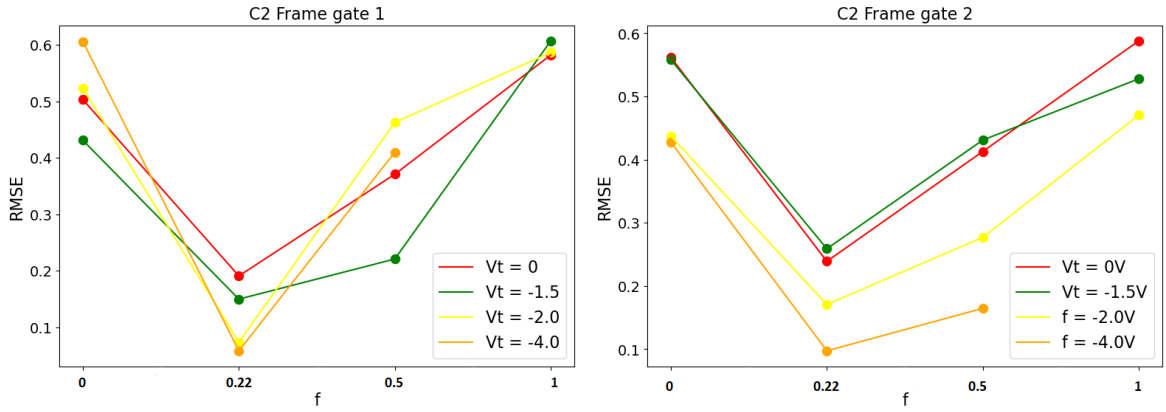

Figure 28: **Left to right: a)** The figure shows the RMSE as a function of the frustration for the first frame gate voltage. The sequence of frustration is, 0, 0.22, 1/2 and 1. **b)** The RMSE of the fits at the second frame gate value.

The fits for device D3 at top gate voltage $V_t = 0.0V$ are shown in figure 29 and in figure 30 at $V_t = -3.0V$. A lot of the same trends are seen in the fits. The kink is clearly seen for both integer frustrations at $V_t = 0.0V$ and it continues to persist when the frame gate voltage is increased, but the temperature at which it occurs gets significantly reduced. The kink is also found at integer frustration at $V_t = -3.0V$ but when the frame gate voltage is increased, it becomes less pronounced and the curvature of the resistance line becomes similar to irrationals.

The summary of the RMSE values are shown in figure 31. The RMSE of the fits at the first frame gate voltage and at both top gate voltages generally follow the same trend seen in device C2. The fits for both the irrationals and half frustrations are much better than the fits at integer frustrations. At $V_t = 0.0V$ the best fit occurs at an irrational frustration. When the frame gate voltage is increased, the fits at $V_t = 0.0$V becomes significantly worse whereas the fits for the both irrationals and half frustration at $V_t = -3.0$V becomes much better.

6.2 Summary of the fits

We are not aware of the origin of the kink in the resistance lines for integer frustration. We have been wondering, if the kink might the onset of the anomalous phase. The previous analysis of the anomalous metallic phase suggests, that the low-temperature saturation of the resistance is most prevalent at integer frustration. At the same time, the kink is also most prevalent at integer frustration. The mechanism responsible for the low temperature resistance saturation might be the same mechanism that causes the kink to appear but cannot fully develop and is destroyed by thermal fluctuations.

The BKT transition at zero magnetic field in square arrays has been measured by other groups. L.J. Geerligs et al. [14] have measured the SIT at zero field, but the kink feature is not seen in their resistance lines. H. Ikegami [24] have been measuring the SIT on an aluminum square array and analyzed the BKT transition by fitting the resistance lines with the function in equation 15 but with the reduced temperature included. The kink is not visible either in their experiment and their fits perfectly estimates the array resistance.

The kink does not seem to be present in the SIT experiments on continuous superconducting films neither, homogeneous or disordered films alike. The SIT has been measured [10], [38] in these systems. In fact, it is difficult to find data of SIT experiments where the kink is visible.

It has been observed that the superconducting transition in arrays at frustrations f = 0 and f = 1 both look as a BKT type phase transition even though the density of vortices at zero frustration is close to zero whereas the vortices of same sign are present at f = 1 but forms a stationary vortex lattice [19]. Our data at integer frustration are also qualitatively the same. Both simulations and

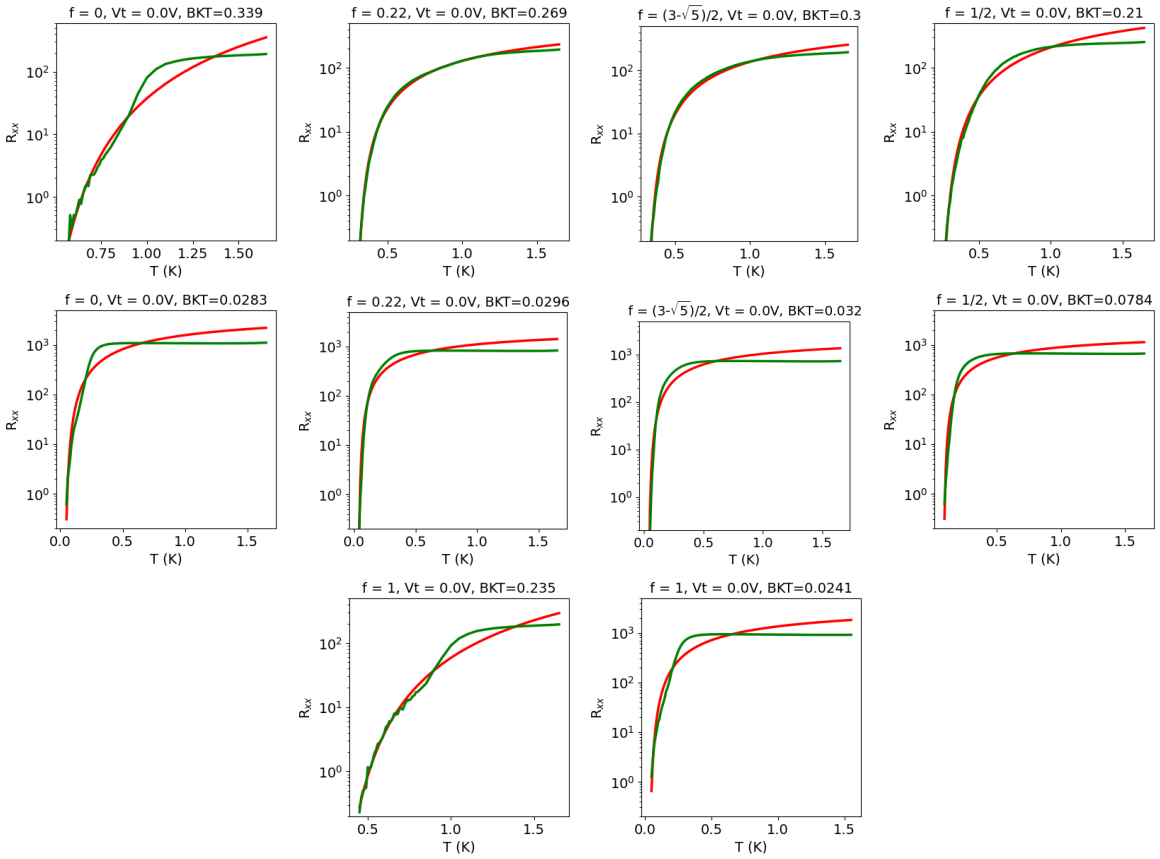

Figure 29: Fits performed on data from device D3 at top gate voltage V_t =0V.

experiments on square arrays have show evidence that the phase transition at f = 1/2 also looks as a BKT transitions but the phase transitions occurs at lower BKT temperature compared to f = 0 [28]. The reduced BKT temperature at f = 1/2 is consistent with our data.

The resistance curves show a two-step feature upon lowering the temperature. Such resistance lines have been observed by Z. Chen et al. [7] They suggest that the first drop in resistance (i.e the kink feature) occurs due to the formation of local phase coherence between superconducting islands. When the temperature is further lowered, global phase coherence is established which leads to superconductivity [7]. The magnetic flux however is not discussed. Based on this idea we suggest that the prevalence of the kink is related to the stability off the vortex lattice. At integer frustration it may be easier for the vortices to find metastable lattice configurations such that local phase coherence between islands can occur. Due to the incommensurability of the vortex lattice at irrational frustration, vortices are more mobile. Hence the possibility to establish local phase coherence is reduced. This also explains the prevalence of the kink as a function of the frame gate voltage. Increasing the voltage also enhances quantum fluctuations which impairs the formation of phase coherence. This idea suggests that the quality of the fits for irrational frustration are better than the fits for integer and half since the fitting function does not include the physics of local .

Of course one has to be careful to compare the RMSE value of fits that clearly are not able to capture all the features of the data. The main results from this analysis is not necessarily that the fitting function used in the regression is the correct one and that it is the correct BKT theory line. The fits are used to qualitatively describe the differences in the curvature and behavior of the resistance lines at different frustration and top gate voltages. But the analysis of the curvature of the resistance have raised some very interesting questions.

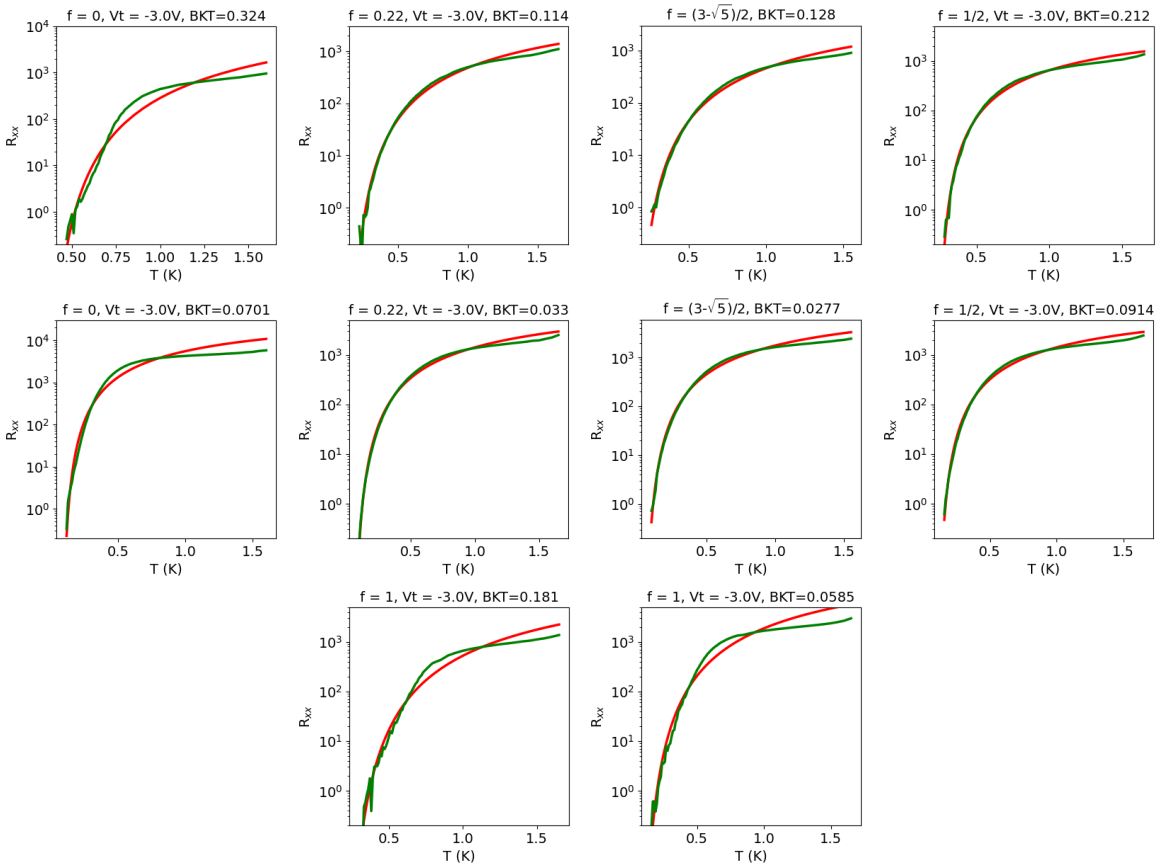

Figure 30: D3 fits Vt = -3.0V

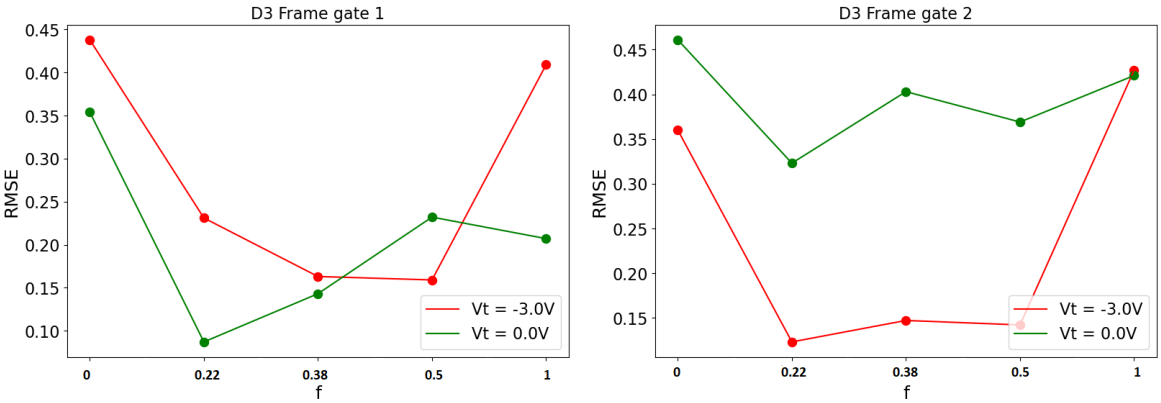

Figure 31: **Left to right: a)** The fits performed on device D3 for the first frame gate voltage. The sequence of frustration is, 0, 0.22, (3-$\sqrt{5}$)/2, 1/2 and 1. **b**) Second frame gate voltage

7 Conclusion

In conclusion we have shown that the dual-gated superconductor-semiconductor Josephson Junction array serves as an excellent platform to study both the SIT and the BKT transitions. We have showed high tuneability in the system. The gate potentials allows us to tune the device to a "puddle" regime, characterized by large fermionic densities in the plaquettes, and to a "junction" regime, and we have seen that these regimes significantly changes the behavior of the array. We have observed that the prevalence of the anomalous phase not only is dependent on the top gate potential but it is also dependent on the frustration. Lots of researches have been investigating how dissipation effects stabilizes the anomalous phase. Much less research has been done on frustration effects on the anomalous phase. Further investigation of dissipation effects as a function of magnetic field strength might also be necessary in order to explain the microscopic origin of the kink in the R-T curves.

Our observations have raised a lot of very interesting questions. It would be very interesting to investigate if our data can be recreated in other square lattice arrays. It would also be interesting if similar trends can be seen in arrays with different geometry for instance in triangular lattices.

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