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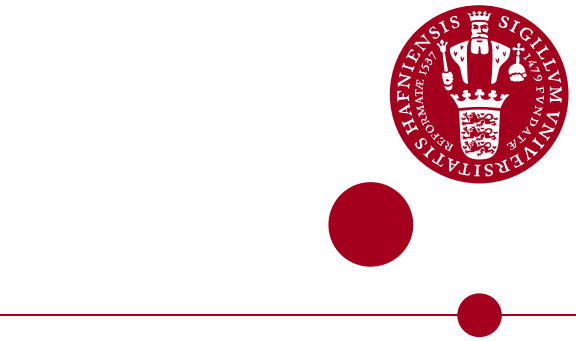

Towards the coherent coupling of multiple three-electron spin-qubits

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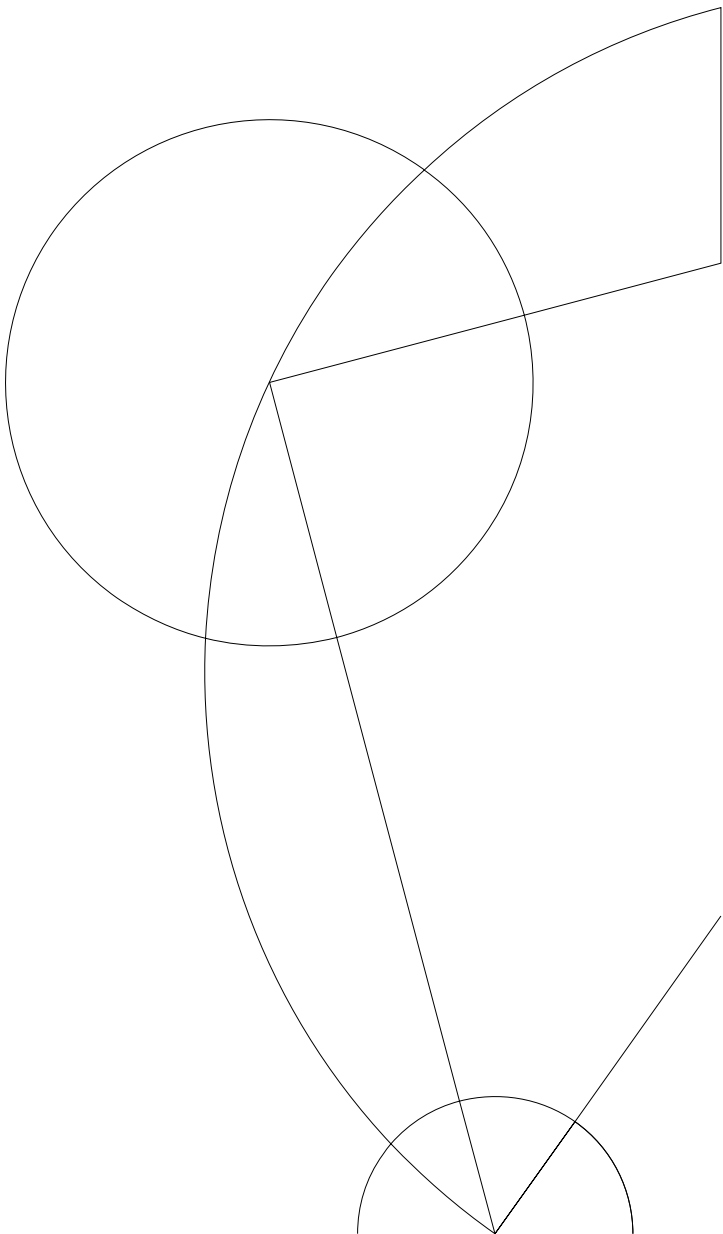

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Abstract

Exploiting the ressouces of entanglement and superposition in quantum two-level systems or "qubits" promises to usher in a new era of information processing. The strength of a quantum computer stems from its ability to coherently operate on large ststems of entangled qubits. The quality of inter-qubit coupling is therefore of paramount importance. The work presented in this thesis aims to build a multi qubit architecture in semiconductor quantum dots. We show a device with 12 working qunatum dots and sucessfully formed a chain of 6 coupled quantum dots. We identify key challenges and possible solutions, some of which are of interest for a wider range of quantum dot based qubits.

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Chapter 1

Introduction

1.1 Computing with quantum objects

The question of what a quantum computer is and what it is supposed to do is most straightforwardly addressed by first looking at a classical computer. On a technical level, a classical computer is a network of switches which can control other switches. The switches can be on or off, corresponding to the basic units of information, classical bits, taking the values 1 or 0. The amount of information that can be processed in a given time, scales in the best case linearly with processing speed and parallelization. Quantum objects are different. If the information is carried by quantum mechanical two level systems, the quantum bits or qubits, with the two states $|1\rangle$ and $|0\rangle$ the state is now described by a wave function $|\Psi\rangle$, which allows for a superposition $|\Psi\rangle = \frac{1}{\sqrt{2}}(\alpha|1\rangle + \beta|0\rangle)$. α and β are in general complex, with $|\alpha|^2 + |\beta|^2 = 1$. This has drastic consequences for information processing. Now, if the computer, the network of switches, preserves the quantum nature of the information during operation, the switches will also be in a superposition and instead of only operating on either 0 or 1 for a single bit, a quantum computer can operate on $|\psi\rangle$. This by itself still has a classical analogue. However, qubits also have the resource of entanglement. This means that the state of one qubit is codependent on the state of its entanglement partner even as both are in a superposition of their internal states. In principle, when entangling all qubits in the input memory, the computer can perform computations on a superposition of all possible input strings at the same time. Consequently, the amount of information that can be processed in a given time doubles with every qubit. This exponential speedup is the fundamental reason why we expect a drastic increase in computational power for certain problems using quantum mechanical objects to store information and a computer which can operate on them without disturbing their quantum mechanical nature. Not all problems, because, since also the result of the operations is going to be in a superposition of all possible states of the memory, one can not access the entire set of solutions. There will not be any speed up for algebraic manipulations, for example. The type of problem for which we expect a drastic speedup are the ones where one is only interested in one particular solution. Examples are : finding the ground-state of complex materials

or molecules [11] [36], factoring prime numbers [9], searching databases [9] or pattern recognition [29] [28]. Maybe with the exception of prime factoring, it is undisputed that being able to perform those computations faster would generate huge technological and scientific leaps in fields such as protein folding, high temperature superconductivity or photo synthesis. This continues to justify the efforts towards building a quantum computer. The challenges however are huge. In classical computation, the information is only stored in 1s and 0s, limiting the errors also to binary events. Additionally, information can be copied to easily create the redundancy necessary to correct for errors. For a quantum computer however, one has to prepare superpositions, not just flips of single bits, which requires full control of all qubits and their interactions. Any interaction with the environment can lead to and unwanted change in the population of $|1\rangle$ and $|0\rangle$, so called decoherence, as well as noise in their relative phase, so called dephasing. The environment can both, measure the qubit as well as cause unwanted evolution. Additionally, just copying qubits to create redundancy in the process is not permitted by quantum mechanics [37]. Concepts on how to deal with this problem and perform "fault tolerant quantum computation" have been developed [31]. Here the information of one "logical" qubit is encoded in many "physical" qubits. The idea is then to interlace detection and correction of errors in the physical qubits with the operations of the logical qubits. The proposed schemes require the physical overhead to be in the hundreds for truly fault tolerant computation. It also increases the number of manipulations one has to perform on the qubits greatly, making the absolute gate time important, since no one will have use for a quantum computer which can perform a computation in a thousand years instead of a billion years. This leads to a "no free lunch theorem" for qubits. On the one hand, the qubits have to be as well isolated as possible to reduce decoherence and dephasing from the enviornment, on the other hand, they have to be strongly coupled to the (classical) control electronics and to each other to enable fast manipulation. It is at this point not clear which physical system provides the best compromise between those requirements. This is why we have seen and continue to see a very wide variety of proposed systems being explored.

1.2 Physical Qubits

Quantum mechanical two level systems which fulfill the requirements outlined above can be found in many different fields of physics. For example, qubits have been explored in atomic physics, with ions in electrostatic traps [2], or atoms in optically defined lattices [3] or in optics with photons as qubits [35]. In solid state physics, advances in cryogenics as well as nanofabrication have made it possible to find qubits in the modes of a superconducting RC circuit [22], the spin states of phosphorus impurities in silicon [27], the spin states of nitrogen impurities in diamond [16] and spin and charge degrees of freedom of electrons confined in semiconductor quantum dots [10] [26], which is the subject of this thesis. Additionally to the requirements above about manipulation speed and coherence, a good qubit also has to be scalable, meaning it must be relatively straight-forward to extend a single qubit architecture to an architecture of many coupled

qubits. Some architectures have already demonstrated quantum information beyond the single qubit level. Quantum algorithms and quantum error correction have been shown in superconducting qubits [1] as well as in ion traps [5]. Also nuclear magnetic resonance on molecules in liquid solution has demonstrated an algorithm with up to seven qubits already before 2000 [6], but the field has moved away from this system, since it is generally believed that it will not scale further. For a demonstration of a quantum computer outperforming classical hardware, hundreds of logical qubits are needed. Since it is obviously useless to have the best single qubit, if it is not scalable, scalability is an issue which has to be addressed early on in the exploration of a given technology.

1.3 Outlines of the thesis

This thesis addresses the question of scalability for the recently developed "resonant exchange" qubit. In this system single qubit operation and high fidelity readout have been demonstrated [21]. In chapter 2 I introducte the physical system hosting the qubit: laterally defined quantum dots. Chapter 3 introduces the resonant exchange qubit and puts it in perspective by briefly covering other qubits in laterally defined quantum dots. The measurement setup built to perform the experiments as well as the devices fabricated are described in Chapter 4. Chapter 5 shows the first measurements on a multi triple dot qubit architecure which has been shown to be in principle able to host three resonant exchage qubits. I identify the challenges for multi qubit coupling and propose possible solutions. The appendices give details on other device attempts, bonding, and the full nanofabrication recipe used for various multi qubit devices.

Chapter 2

Laterally defined quantum dots in GaAs as qubits

This chapter is a brief step by step introduction to multi quantum dots. A thorough introduction to the topic can be found in [15]. All data shown has been measured using the setup described in chapter 4.

2.1 GaAs, AlGaAs heterostructure

One can think of a quantum dot as an artificial atom. As in the atom, the electrons are confined in all 3 spatial dimensions. The nucleus is replaced by the semiconductor crystal and/or surface gates. This confinement can be designed in different ways: entirely by the material in a self assembled quantum dot, to 1D with the material in carbon nanotubes or nanowires, or as in the systems described here to 2D with the material, in a two dimensional electron gas (2DEG) formed at the interface of a semiconductor heterostructure. The heterostructure is grown by molecular beam epitaxy (MBE). MBE is the preferred technique, since it creates the cleanest crystals. In our case, the materials used are GaAl and AlGaAs. Other materials for example SiGe have also been used for spin qubit experiments, and may replace GaAs in the future. However, at this date, growth and fabrication is best developed for GaAs, making it the material of choice for complex devices, as ours. A typical waver used for fabrication is sketched in figure 2.1. In the devices presented in this thesis, the GaAs AlGaAs heterointerface is 91 nm below the surface. 50 - 130 nm materials are commonly used for spin qubit experiments. The conduction band of AlGaAs is higher in energy than that of GaAs. Through doping of the AlGaAs, free electrons are introduced into the structure. The electrons diffuse through the structure and eventually "fall down" the conduction band gap ΔE. Now the electrons are trapped in the GaAs conduction band, by ΔE. Having lost their electrons, the Si donors form a sheet of positive charge, prohibiting the electrons from further diffusing into the material. This creates a triangular well, trapping the electrons in the vertical direction, while they are still free to move horizontally. At cryogenic temperatures, only the lowest mode in this trapping potential is occupied [15], such that

the electrons form a 2D sheet. In a normal semiconductor, the donors are the main source of scattering. Now that the electrons are fare away from the donors, they can achieve very high mobility, where they can travel up to macroscopic distances without hard scattering events [19].

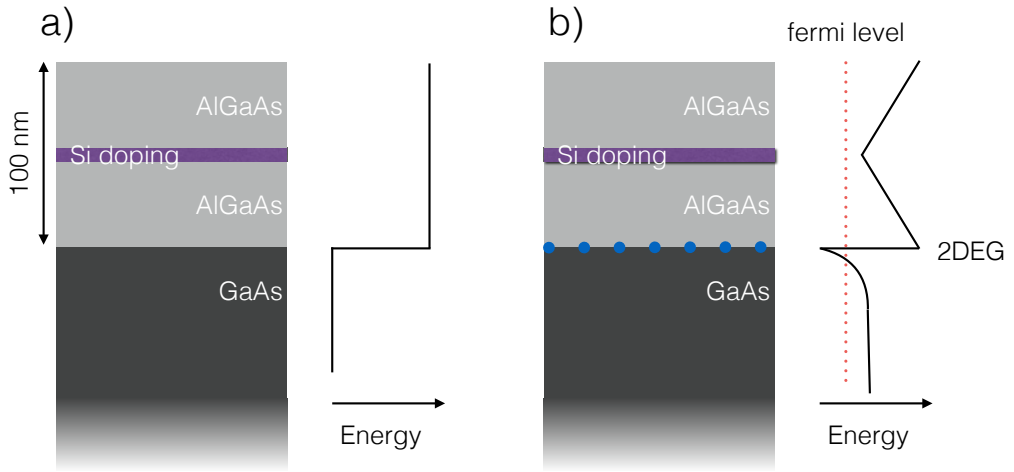


Figure 2.1: a) AlGaAs - GaAs heterostructure before the diffusion of the electrons. The conduction band of GaAs lies lower in energy, thus the discontinuity at the interface. The Si dopant layer is in the middle of the AlGaAs layer. b) Band structure of the heterostructure after the 2DEG (blue dots) has formed. The electrons diffused away from the donors and form the 2DEG at the AlGaAs-GaAs interface, in our case, about 100nm below the surface. At cryogenic temperatures, only the deep well at the interface is populated, as indicated by the fermi level.

To confine the electrons horizontally, depletion gates are evaporated on top of the heterostructure via electron beam lithography. The gates deplete the underlying 2DEG and can be used to form any kind of structure, such as a 1D channel as shown in figure 2.2 or a dot shown in figure 2.4. To contact the 2DEG, Ohmic contacts are also fabricated into the material.

Figure 2.3 shows the effect of a depletion gate on part of a device used in our experiments. A small voltage bias $V_s - V_d = 0.05$ mVis applied across the structure from source to drain through the ohmic contacts while measuring the current (typically at the drain, the instrument forms a virtual ground). As the negative voltage on the gate is increased, the underlying channel gets smaller until the region is completely depleted, so no transport is possible.

2.2 Quantum Dots

Physically, a quantum dot is a small island of 2DEG with discrete energy levels, corresponding to the number of electrons it holds. The levels are discrete if the island size is of the order of the de Broglie wavelength $\lambda = h/2m_e^*E$ of the electrons, carrying a kinetic

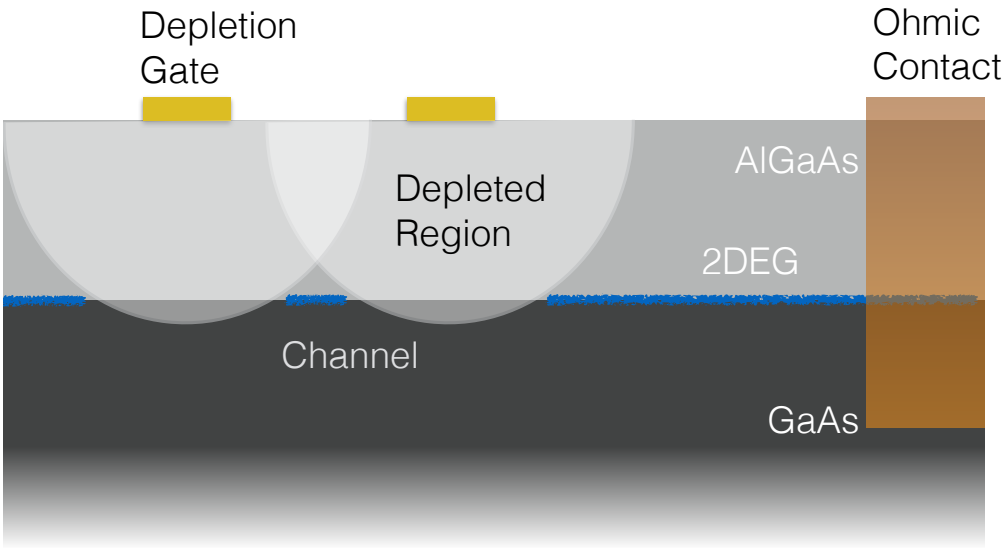


Figure 2.2: Ti/Au gates on top of the material are used to locally deplete the 2DEG. The depletion region is indicated by the circles. Conduction electrons can remain in between the gates and form a channel where conduction is possible. Outside the channel, conduction is suppressed. The size of the channel can be controlled via the voltages applied to the gates. Ohmic contacts (to the right of the gates) are used to contact the 2DEG.

energy E and an effective mass m_e^*. The structure shown in the scanning electron micrograph in figure 2.4 a) can be used to forum quantum dots which can be depleted down to the few electron regime. A single dot is confined by the horizontal bar ("backone") and the three gates below. The shorter gate, so called "middle plunger", controls the chemical potential in the dot. The longer gates on the side control the tunnel rates into and out of the dot and the dot-size. The shape of the gates can also be very different. See [15] for example. There is also significant cross coupling from gate to gate, so tunnel rates, dot size and chemical potential can in practice not be adjusted fully independently without compensation. One way to probe the level structure in the dot is by doing a transport measurement through the dot as shown in figure 2.4 b). A small bias voltage across the dot is applied and the current from source to drain is measured. If there is a discrete level structure in the dot, one can only see conductance if the levels are inside the bias window, as shown schematically in figure 2.4 c). Figure 2.4 b) shows the formation of a dot in a device very similar to the one depicted in a). All four gates are energized and the two outer gates are scanned. As they get more negative, the conduction changes from a continuum to discrete lines. For figure 2.4 d) V_l and V_r are parked on top of one of the lines from figure 2.4 b) and the middle plunger voltage V_m is scanned. Again we see discrete spikes in conductance as expected for a quantum dot.

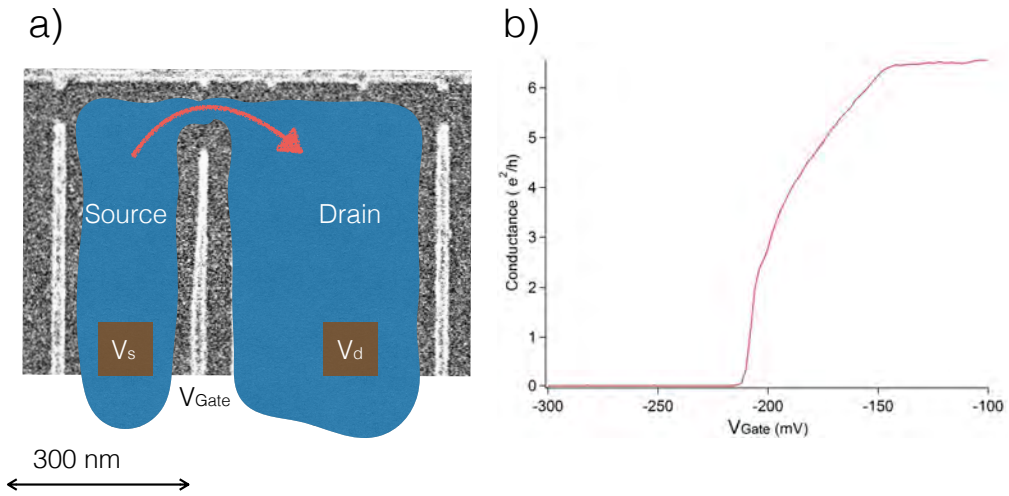


Figure 2.3: (a) False color micro-graph of a part of JB_TTL14 (see table A.1:Table of devices). Negative voltages are applied to all gates visible in white. The remaining regions of the 2DEG are indicated in blue. The ohmic contacts are in the bottom in red. In reality the ohmic contacts are much further away for fabrication reasons. (b) As the voltage V_{gate} gets more negative, the region of the 2DEG connecting source and drain gets smaller until no conduction is possible.

2.3 Multiple Quantum Dots and charge sensing

Similarly to a single quantum dot, as the one shown in figure 2.4 structures of multiple coupled quantum dots in the low electron regime can be created inside a 2DEG via depletion gates on top of a heterostructure. A device for multiple coupled quantum dots is shown in figure 2.5. The nearby quantum dot is used as a charge sensor. The details of the experimental setup used for this measurement can be found in chapter 4. The basic idea behind this "sensing dot" is that the resistance of the quantum around a Coulomb peak is very sensitive to its electrostatic environment. This is also visible in figure 2.4 d). Here the electrostatic environment is mediated by the plunger voltage V_m, but it is also sensitive to other nearby gates and even the charge state of a nearby quantum dot. We can monitor the conductance through the dot, via a transport measurement (or more advanced, reflectometry , see...) and sweep the plunger voltages of the nearby dot, similarly to 2.4 d). Due to linear electrostatic coupling of the gates, we will see a constant background from the gates, but every time an electron tunnels into or out of dot, the resistance of the channel through the sensing dot changes abruptly. After digitally removing the background from the gates it is possible to identify the signal from single electron tunneling event. This allows us to work with arrays of quantum dots in very depleted regime where the tunneling rates through the device would make analysis via transport through the device very difficult. Figure 2.5 a) shows a charge stability diagram of a double quantum dot. The signal is a differentiated conductance

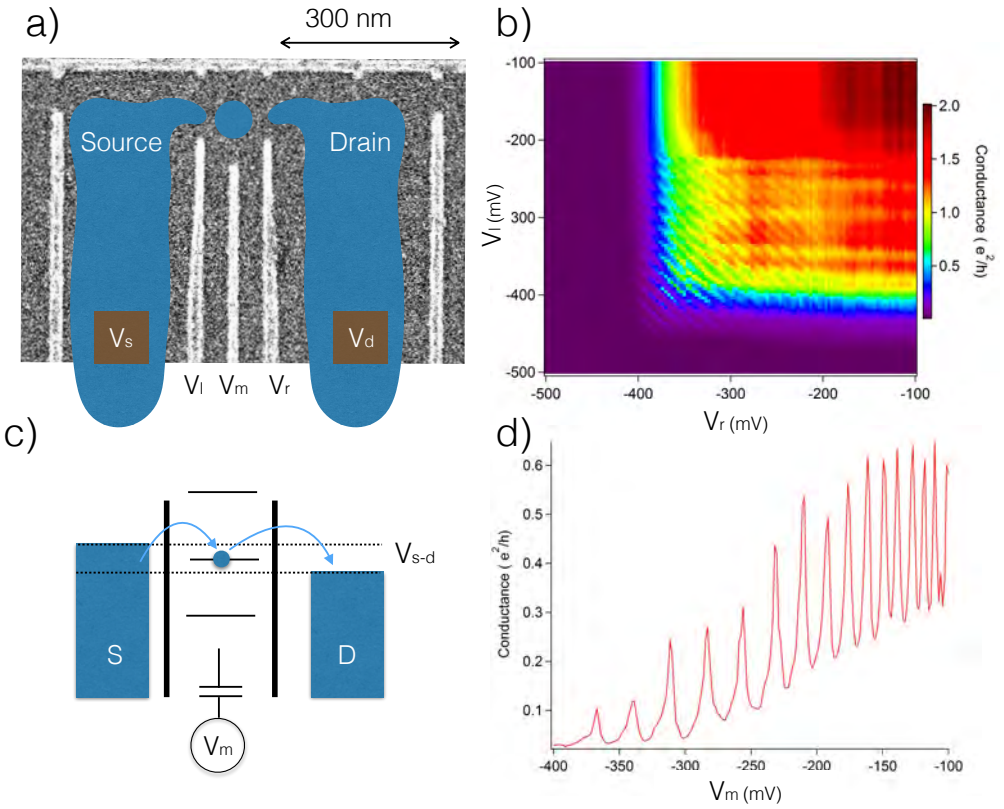


Figure 2.4: (a) False color micro-graph of a part of JB_TTL14 (see table A.1:Table of devices). An island of 2DEG is formed between source and drain. This is the quantum dot. The gate voltages V_l, V_r and are used to control the size of the dot as well as tunnel rates through the dot. V_m controls the chemical potential in the dot. b) Source - Drain conductance measurement while forming a quantum dot with V_l and V_r. As the region around the gates gets depleted we see a discrete structure in conductance emerging from a continuum. c) Schematic of the energy levels of the quantum dot shown at a). V_m controls the chemical potential in the dot, it can bring levels inside the bias window (V_{s-d}). Only if a level is inside the bias window, we see conductance. d) Same measurement as in b) now with V_m scanned. We see sharp peaks in conductance as different levels are brought into the bias window.

through the nearby sensor dot, as described above as a function of the left and the right plunger gates. We see three distinct types of lines (transitions). There are two types of lines with different negative slopes relative to the V_l and V_r axis. We a attribute the lines which are stronger coupled to V_l (V_r) to transitions into and out of the left (right) dot. The line with the positive slope is a charge transition in between the dots.

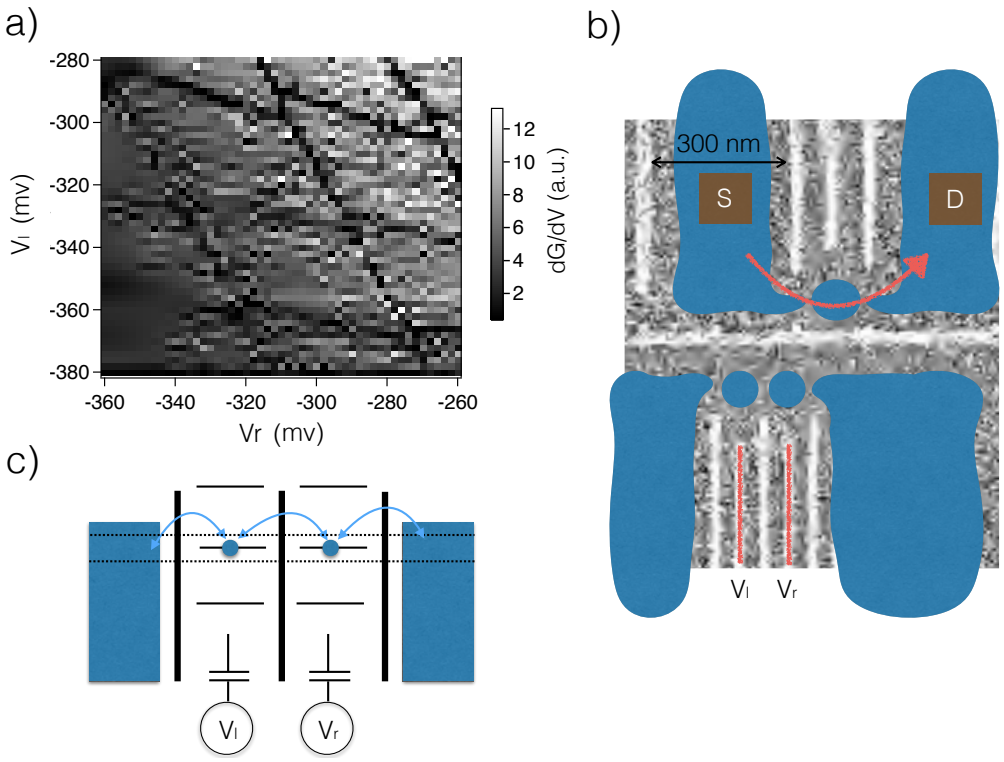


Figure 2.5: A double quantum dot in device JB_TTL14 (see table A.1). (a) Differential conductance signal. The conductance signal through the sensing dot (see micro-graph to the right, dot beyond the backbone) has been differentiated to subtract the linear signal from the depletion gates of the double dot. The dark lines are a change in electron occupation of the dots. We can see two distinct slopes, one stronger coupled to V_l, the other one stronger coupled to V_r, which show transitions in and out of the left and the right dots. (b) False color micro-graph of the part of the device hosting the double dot. The regions of 2DEG are indicated in blue. There are two quantum dots formed in the device and one readout dot. Transport through the readout dot is constantly monitored. The scanned gates are indicated with red lines. (c) Sketch of the energy diagram of a double dot. If two levels are resonant, transport from one dot to the other one can occur. The inter-dot transitions are also visible in a) as the short lines with a positive slope.

Chapter 3

The "Resonant Exchange Qubit"

3.1 Quantum dot qubis

3.1.1 Loss DiVincenzo Qubits

Few electron quantum dots, both in 2DEG as well as in nano wires and carbon nanotubes, have been shown to host many electronic systems which are promising candidates for scalable quantum computing architectures. The field was kicked off by the seminal paper by Daniel Loss and David DiVincenzo [18], where they proposed, what is now known as the Loss-DiVincenzo Qubit (LD Qubit). It uses the spin states $\uparrow$ and $\downarrow$ of a single electron in a quantum dot as the two qubit states $|1\rangle$ and $|0\rangle$. The control is very similar to nuclear magnetic resonance (NMR). A large external magnetic field splits the spin states $\uparrow$ and $\downarrow$ by an energy ΔE. An oscillating small perpendicular magnetic field with a frequency resonant with ΔE can then drive transitions between $|1\rangle$ and $|0\rangle$. The relative phase between $\uparrow$ and $\downarrow$ is constantly oscillating at ΔE, which makes is necessary to define a reference frame rotating with the qubit at that frequency. In this rotating reference frame the driving field is static, as is the phase. The phase between $|1\rangle$ and $|0\rangle$ in the rotating frame can then be easily controlled via the phase of the driving field. Initialization, readout and manipulation of different implementations of LD qubits have been demonstrated within the last 10 years [15]. The techniques differ mainly in their generation of the oscillating magnetic field. The first approach was to fabricate a microwave strip-line on top of the device [10]. This approach will probably be hard to scale up. First, the strip-line is relatively large, so it will be hard to control many closely spaced qubits independently. Secondly, the power consumption is so large that it causes heating of the sample, so it is hard to imagine potentially hundreds or thousands of qubits on a chip with microwave strip-lines. A different approach is to use electric fields to shake the electron and create a magnetic field via spin-orbit interaction [23] [24]. This approach suffers from the realtively weak spin orbit interaction in GaAs, but but is being actively pursued in materials with strong spin-orbit interaction. One can also introduce a field gradient within one quantum dot or across a double dot by fabricating nanometer scale structures out of magnetic materials, such as cobalt onto

the device, or introduce magnetic materials into the gates. [25]. As with spin-orbit LD qubits, electric fields can be used to shake the electron inside the gradient, so it sees an oscillating magnetic field.

3.1.2 Singlet Triplet Qubits

For singlet triplet (ST) qubits, two electrons in two tunnel coupled quantum dots are needed [26]. A ST qubit uses a qubit basis formed via the symmetric $|T_0\rangle = \frac{1}{\sqrt{2}}(\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)$ and anti-symmetric $|S\rangle = \frac{1}{\sqrt{2}}(\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)$ spin states of the two electrons. $|S\rangle$ and $|T_0\rangle$ are energetically split by an exchange interaction J, which thereby can drive rotations around the $|S\rangle$ - $|T_0\rangle$ axes. In order to drive rotations between $|S\rangle$ - $|T_0\rangle$ a magnetic field gradient ΔB_z between the two dots is needed ($|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle$ axis). Several methods have been found to introduce this gradient. One way is to introduce micro-magnets as for the LD qubit. A different way is the active control of the nuclear field in the material, so called Dynamical Nuclear Polarization (DNP). The nuclei of gallium, arsenic and aluminum possess non-zero spins which interact with the electron spin in the quantum dot. For typical dot sizes, the electron overlaps with 10^6 nuclei creating a mean nuclear field $\vec{B}_{nuc}$. The energy structure of the double dot with two electrons contains nuclear mediated, as in, not electron-spin conserving, anti-crossings, such as the $|S\rangle$ - $|T_+\rangle = |\uparrow\uparrow\rangle$ which can be used to manipulate $\vec{B}_{nuc}$. When adiabatically passing a $|S\rangle$ state through the anti-crossing the electron spin gets flipped up, while one nuclear spin gets flipped down ("flopped"). Now one can pass back trough the anti-crossing non adiabatically, fast enough such that the electron state (and the nuclear field) do not change, and re-initialize into the $|S\rangle$. The nuclear spin polarization from doing this many times does not build up evenly in both dots, but creates a nucleaer field gradient, which can then be used as the second control axes of the qubit [12]. The technique has also been used to control random fluctuations in the nuclear fields, a leading cause of dephasing, and thus extend the lifetime of the qubit [4].

3.1.3 Exchange-only

Having to deal with DNP, micro-magnets or even strong oscillating magnetic fields generated near the sample can be seen as a fundamental imperfection of LD and ST qubits, since they add a layer of complexity in control. Since electrons are most easily controlled electrically, pure electrical control via electrostatic gates would be optimal. In 2000 DiVincenzo et al [7] proposed such a spin qubit, formed out of three electrons in three tunnel coupled quantum dots. Assuming a linear design with nearest neighbor tunnel coupling, there are now two exchange interactions J_{12} and J_{23} between the left and the middle, and the middle and the right electron. Maped on a Bloch sphere those two axis are 120° apart and are thus sufficient for all electrical control. Under an external magnetic field, such an electron system has 8 spin states. One can in principle find several different qubit subspaces and different modes of operation in this system [14][13] [20], but here we consider only the regime, where the qubit states are in the $m_s = 1/2$, $S = 1/2$ manifold and both exchange interactions are approximately equal [21].

3.2 Triple dot Qubit

We have chosen the "resonant exchange qubit" as the basis for the multi qubit architecture. A device like figure 3.1 (a) can be brought into the few electron regime and will form a triple dot for appropriate gate voltages. In the proposed scheme the triple dot is operated via the plunger gates V_l and V_r. V_m as well as the tunnel barriers remain unchanged during single qubit operation. Figure 3.1 (b) shows a charge stability diagram for a triple dot. We parameterize the voltage space with ϵ and δ. δ is the common voltage of the two plungers $\delta = (V_l + V_r)/2$ and controls the total electron occupation of the triple dot. $\epsilon = (V_l - V_r)/2$ is the detuning of the left and right side and shuffles electrons around in between the dots. The numbers (111), (201) etc. indicate the charge state of the qubit, where 201 means two electrons in the left dot, zero in the middle and one in the right dot. Qubit operations are done completely in the (111) region along the $\alpha\epsilon$ axis.$\alpha\epsilon$ because it can be better to operate on an axis tilted relative to ϵ. When sitting in the middle of (111) the triple dot becomes a spin chain of three exchange coupled electrons in a potential, as shown in figure 3.2 a). The exact occupation can be found by completely depleting the triple dot. This is the case when sharp charge transitions stop at one point even though the negative gate voltage is further increased. The transitions have to be sharp, because this will also happen if the dot breaks into many dots or the channel is fully closed. In this case, however, the last transitions will show latching, as tunnel rates become slower than the scan speed. From the completely depleted regime, we can count the electrons filling the dot as the voltages become less negative as shown in figure 3.1 (d).

The dynamics of this spin chain are described by a Heisenberg model [34]:

$$H_{Heis} = J_l S_1 \cdot S_2 + J_r S_2 \cdot S_3 \tag{3.1}$$

where $J_{l/r} = \frac{t_{l/r}^2}{U}$ is the exchange on both sides which is given by the tunnel coupling t and the charging energy U. When sitting at the symmetry point, $J_l = J_r$, the four lowest energy eigenstates are :

$$|Q_+\rangle = |\uparrow\uparrow\uparrow\rangle \tag{3.2}$$

$$|0\rangle = \frac{1}{\sqrt{6}}\left(|\uparrow\uparrow\downarrow\rangle + |\downarrow\uparrow\uparrow\rangle - 2\,|\uparrow\downarrow\uparrow\rangle\right) \tag{3.3}$$

$$|1\rangle = \frac{1}{\sqrt{2}}\left(|\uparrow\uparrow\downarrow\rangle - |\downarrow\uparrow\uparrow\rangle\right) \tag{3.4}$$

$$|Q\rangle = \frac{1}{\sqrt{3}}\left(|\uparrow\uparrow\downarrow\rangle + |\uparrow\downarrow\uparrow\rangle + |\uparrow\uparrow\downarrow\rangle\right) \tag{3.5}$$

Qualitatively, exchange lowers the energy of the $|0\rangle$ and $|1\rangle$ states due to hybridization with the (201) and (102) states, which lowers their kinetic energy. The logical qubit basis is $|1\rangle$ and $|0\rangle$. The states $|Q+\rangle$ and $|Q\rangle$ are in the $S = 3/2$ manifold, so magnetic fields

are needed to drive transitions to and from the qubit space. It is possible to populate the $|Q_+\rangle$ state, since it has a contact hyperfine interaction mediated anti-crossing with the $|0\rangle$ state. Unwanted populations of the $|Q_+\rangle$ state can be prohibited by passing fast through the anti-crossing relative to the splitting which is small, so this is in practice not a problem. The $|Q\rangle$ state is split off from $|1\rangle$ by the exchange $(J_l + J_r)/2$ [17]. It can be populated via transverse nuclear field gradients between the dots. Splittings between $|1\rangle$ and $|0\rangle$ are in the range of hundreds of MHz, as for the resonant exchange qubit, so this is also not an issue. A sketch of the energy diagram is given in figure 3.2 c). When leaving the symmetry point, the Hamiltonian changes and so do the eigenstates. For instance, when moving far to the left, exchange between the middle and the left dot dominates. In this regime we have different eigenstates $|S_l\rangle$, $|S_r\rangle$, $|T_l\rangle$, and $|T_r\rangle$. Which adiabatically map onto the $|0\rangle$ and $|1\rangle$ states. The states are :

$$|S_l\rangle = \frac{1}{\sqrt{2}}\left(|\uparrow\downarrow\uparrow\rangle - |\downarrow\uparrow\uparrow\rangle\right) \tag{3.6}$$

$$|S_r\rangle = \frac{1}{\sqrt{2}}\left(|\uparrow\uparrow\downarrow\rangle - |\uparrow\downarrow\uparrow\rangle\right) \tag{3.7}$$

$$|T_l\rangle = \frac{1}{\sqrt{6}}\left(|\downarrow\uparrow\uparrow\rangle + |\uparrow\downarrow\uparrow\rangle - 2\,|\uparrow\uparrow\downarrow\rangle\right) \tag{3.8}$$

$$|T_r\rangle = \frac{1}{\sqrt{6}}\left(|\uparrow\uparrow\downarrow\rangle + |\uparrow\downarrow\uparrow\rangle - 2\,|\downarrow\uparrow\uparrow\rangle\right) \tag{3.9}$$

The way to understand this is, that $|S_l\rangle$ for instance is a singlet between the left and the middle electron while the right electron is just pointing up. $|T_r\rangle$ is a triplet between the middle and the right electron, with the left electron just pointing up. The states given in 3.2 to 3.5 are of course only half of the 8 states, there is also a $S = -1/2$, $S = -3/2$ manifold, which can be neglected here.

Since the qubit is operated in the symmetry point where $J_l = J_r$, one can think of the triple dot as an artificial spin 1/2 particle in an external magnetic field, where the exchange interaction $J_z = J_l + J_r$ takes on the role of the magnetic field, splitting the two states $|1\rangle$ and $|0\rangle$ or $|\uparrow\rangle$ and $|\downarrow\rangle$. We can write the Hamiltonian as:

$$H = J\sigma_z \tag{3.10}$$

$$= \hbar\omega_{01}\sigma_z/2 \tag{3.11}$$

which rewrites the exchange splitting as a rotation around the $\hat{z}$ axis of the Bloch sphere at frequency ω_{01}. Moving away slightly from the symmetry point introduces a small transverse exchange component $J_1 \ll J$, the analog to the transverse magnetic field in NMR. In presence of this transverse field the rotation axis tilts by a small angle $\theta = \tan^{-1}(J_1/J)$. The rotation continues with $\omega'_{01} = \sqrt{J^2 + J_1^2}/\hbar$. Since $J_1 \ll J$, $\omega'_{01} \approx \omega_{01} = J/\hbar$. An especially interesting regime is the one where J_1 oscillates at a frequency $\omega \approx \omega_{01}$. This introduces an additional term to the Hamiltonian

$$H_x = J_1 \cos(\omega t + \phi)\,\sigma_x \tag{3.12}$$

This oscillating field can be rewritten as the sum of J_1^+ and J_1^- which oscillate around the $\hat{z}$ axis in opposite directions.

$$\begin{aligned} H_x &= H^+ + H^- && (3.13)\\ H^+ &= J_1/2\left[\cos\left(\omega t+\phi\right)\sigma_x + \sin\left(\omega t+\phi\right)\sigma_y\right] && (3.14)\\ H^- &= J_1/2\left[\cos\left(\omega t+\phi\right)\sigma_x - \sin\left(\omega t+\phi\right)\sigma_y\right] && (3.15)\end{aligned}$$

We can now look at the qubit in a frame that is rotating with J_1, by transforming the states and the Hamiltonians:

$$\begin{aligned} H_{rot} &= \exp\left(i\omega t\sigma_z\right)\left(H^+ + H^-\right)\exp\left(-i\omega t\sigma_z\right) && (3.16)\\ &\quad +\hbar\left(\omega_{01}-\omega\right)\sigma_z && (3.17)\\ |\psi\rangle_{rot} &= \exp\left(i\omega t\sigma_z/\hbar\right)|\psi\rangle && (3.18)\end{aligned}$$

To see why this makes sense, we compare the $\exp\left(i\omega_z t\sigma_z\right)H^+\exp\left(-i\omega_z t\sigma_z\right)$ and the $\exp\left(i\omega_z t\sigma_z\right)H^-\exp\left(-i\omega_z t\sigma_z\right)$ terms. Using double angle identities, we see that in H^+, the ωt term will cancel out, while H^- will get $2\omega t$ terms. This means that H^+ is static in the rotating frame, while H^- rotates with twice the frequency. If $J_1 \ll J$, as assumed before, we can use the rotating frame approximation, which omits H^- because fast oscillating terms average out. The Hamiltonian in the rotating frame approximation becomes:

$$H_{rf} = = \Omega[\cos\left(\phi\right)\sigma_x + \cos\left(\phi\right)\sigma_y] + \hbar\Delta\sigma_z \quad (3.19)$$

with $\Delta = \omega_{01} - \omega$ and $\Omega = J_1/2$. This shows, that via a phase controlled oscillating field, rotations around any axis on the equator of the Bloch sphere are possible. Experimentally this can be done very efficiently. The oscillating field can be generated simply by putting an oscillation on one of the outer plunger gates. Since there are only very small deviations in voltage space in play, it is not a problem to be not perfectly along ϵ. By using a voltage controlled vector source or a standard signal generator with an IQ mixer to generate the oscillation, one can adjust the phase easily. The typical qubit splittings are in the hundreds of MHz to several GHz, so they are well within the technical capabilities of commercially available hardware. In practice, one tries to be in $\Delta = 0$, on resonance with the qubit splitting to avoid the $\Delta\sigma_z$ drift. It has been shown that the splitting can be controlled via a fast plunger gate on V_m on nanosecond timescales. This additional control nob plays an important role in some proposed multi qubit coupling schemes [34].

3.3 Readout

The qubit states $|1\rangle$ and $|0\rangle$ presented in section 3.2 can in practice not be read out directly, since the magnetic moment of single electrons is weak. Therefore we employ a

technique from ST qubits called "spin to charge conversion". Here we utilize the fact that, if going away form $\epsilon = 0$, say towards negative ϵ such that the middle electron gets pushed towards the left, $|0\rangle$ adiabatically maps onto $|S_l\rangle$, while $|1\rangle$ maps onto $|T_l\rangle$. Now when detuning all the way across the (201) (111) charge transition, two things can happen, as sketched in 3.3). Either, the electron just jumps over, which is the situation we always see when taking a charge stability diagram, since here we are in the ground state $|0\rangle$, where the two electrons in a singlet state can occupy a single quantum dot. If the triple dot was in $|1\rangle$ however, the two electrons on the left are in a spin triplet. In this case, within a certain regime of detuning close to the charge transition, the electron in the middle dot is forbidden to tunnel into the left dot due to Pauli Spin blockade. This gives a clear charge signal of the spin states $|1\rangle$ and $|0\rangle$, as shown in figure 3.3 (a). For good readout, we have to find a region ϵ_r, in this figure near the (102)-(111) charge transition in which the singlet tunnels over rapidly, yet the triplet stays in 111 for long enough time for the charge sensor to pick up a signal. Since everything is symetric, we ideally find such transitions on both sides. 3.3 (b) shows the signal in a charge stability diagram. Here a charge stability diagram of a triple dot (with reflectometry for higher bandwidth, not important now, see section 4.3.3) was taken, but additionally using the arbitraty waveform generator (AWG, high bandwith in real time signal generator, see section 4.3.2) to pulse to ϵ = -15 mV detuning for 100 ns every 4 μs. Pulsing to the negative detuning from (102) mixes in triplet like states $|T_r\rangle$, so sometimes the electron gets stuck in spin blockade. Therefore we see the green color of the (111) state extend in a triangle inside the 102 state. If we start from further in (102), this does not happen anymore. The $|T_r\rangle$ is a metastable state; it will decay into $|S_r\rangle$ on a timescale of 100 μs. By repeating an experiment many times and always pulsing to ϵ_r it is possible to pick up a large enough charge signal in transport through the sensor dot to monitor qubit evolution, through many averages measurements along the σ_z axis. The reflectometry (see section 4.3.3) technique is described in detail in [30]. With this technique, it is possible to distinguish the charge states before $|T_l\rangle$, $|T_r\rangle$ decay, thus enabling us to determine the state for every single experiment. This is called "single shot capability". Single shot, because it determines the state in one shot, not averaging over many experiments or post selection. Single shot readout of qubits is critical for quantum computing. Figure 3.3 (c) demonstrates single shot capability. It shows histogrammed voltage signal from the readout region in figure 3.3 (b) for different measurement integration times. After about 4 μs, two charge signals can be distinguished, corresponding to singlet and triplet like states.

3.4 Initialization

As mentioned in section 3.3 the triplet state decays on a timescale of 100 μs . It is important to reliably initialize into the ground-state when beginning the experiment. Also, we want to repeat experiments faster than hundreds of μs, so we need to initialize into $|0\rangle$ by other means than just waiting for $|1\rangle$ to decay. To do this we pulse close to the (101)-(201) charge transition in which electrons tunnel in and out of the left dot.

Since the electrons preferably tunnel into the ground state, this method creates high fidelity singlets in the left dot.

3.5 Multi qubit coupling

Multi qubit coupling means the physical implementation of two qubit gates, like a controlled phase or a controlled not gate. Controlled not means essentially a rotation of the target qubit around the x-axis depending on its and the control qubit's state. A controlled phase gate is the same but around the z-axis. Two types of multi qubit coupling have been proposed for for the resonant exchange qubit: capacitive coupling and exchange interaction.

3.5.1 Capativite coupling

Capacitive coupling uses the fact that the qubit states have different charge distributions. In $|0\rangle$, there is a larger admixture of (201) and (102) states, so the weight of the wave functions of the middle electron is located farther out on the sides, while in $|1\rangle$ it is Pauli blockaded which is pushing the electrons more towards the middle. This opens two possibilities. One can use the state of the control qubit to modulate the chemical potential of the middle dot of the target qubit, which as shown in [21] modulates the qubit splitting, thus implementing a controlled phase gate. Away from purely $|1\rangle$ and $|0\rangle$ the qubit possesses a dipole moment oscillating at the frequency of the $|0\rangle$ - $|1\rangle$ splitting. Now one can bring control and target qubit into resonance, both with splitting Ω_r. Now the oscillating dipole of the control qubit can act as a driving field on the target qubit when they are oriented in a line. Another possibility is to have the qubit splittings fare detuned and operate the control qubit with a Rabi frequency equal to the splitting of the target qubit. Both approaches conditionally drive oscillations around the σ_x axis on the target qubit, thus implementing a controlled not gate. The two σ_x gates are expected to have the advantage that they are narrow band (they rely on a resonance) and thus less sensitive to noise or cross coupling to other qubit operations going on at the same time.

3.5.2 Exchange coupling

If tunnel coupling between the qubits is allowed, either directly or via an additional quantum dot, the spin state of the control qubit will split the energies of the target qubit, leading to an exchange interaction. In this case controlled-phase and -not gates can also be implemented in middle to middle, and side to side geometries [8]. Leaving experimental difficulties aside, in general exchange coupling is preferred, since it promises much faster gates. There exists data on capacitive coupled ST qubits, which allows us to estimate the gate speeds. For two coupled ST qubits in GaAs 2DEG, the induced field in the target qubit from a full electron in the control qubit relocating into its neighboring dot corresponded to a gate voltage of $10\ \mu$ V [32]. This were two ST qubits right next to each other. For the resonant exchange qubits, the highest sensitivity of the Rabi oscillations to an on resonant external fields was measured to be 5 GHz/mV, which was

already in a regime where the qubit was barely working [21]. In the optimal operating regime, the coupling was 70 MHz/mV. Assuming the best possible coupling, this still only gives a 50Mhz gate, which should be seen as the absolute upper bound, since in a realistic device the qubits will be further apart than in [21] and the qubit will be operated much closer to the 70MHz/mV regime. Now simply assuming a chain of 6 dots, it has been shown in the triple dot experiments, that the exchange interaction between dots can easily be hundreds of MHz. It should be noted though, that capacitive coupling leaves the possibility of coupling to, for instance, a strip-line resonator, opening the possibility for hybrid devices [34]. Coupling to the middle dots has also been abandoned for a first demonstration, since with present fabrication techniques it is hard to imagine how to couple more than two triple dots this way. Figure 3.4 gives an overview over the geometries.

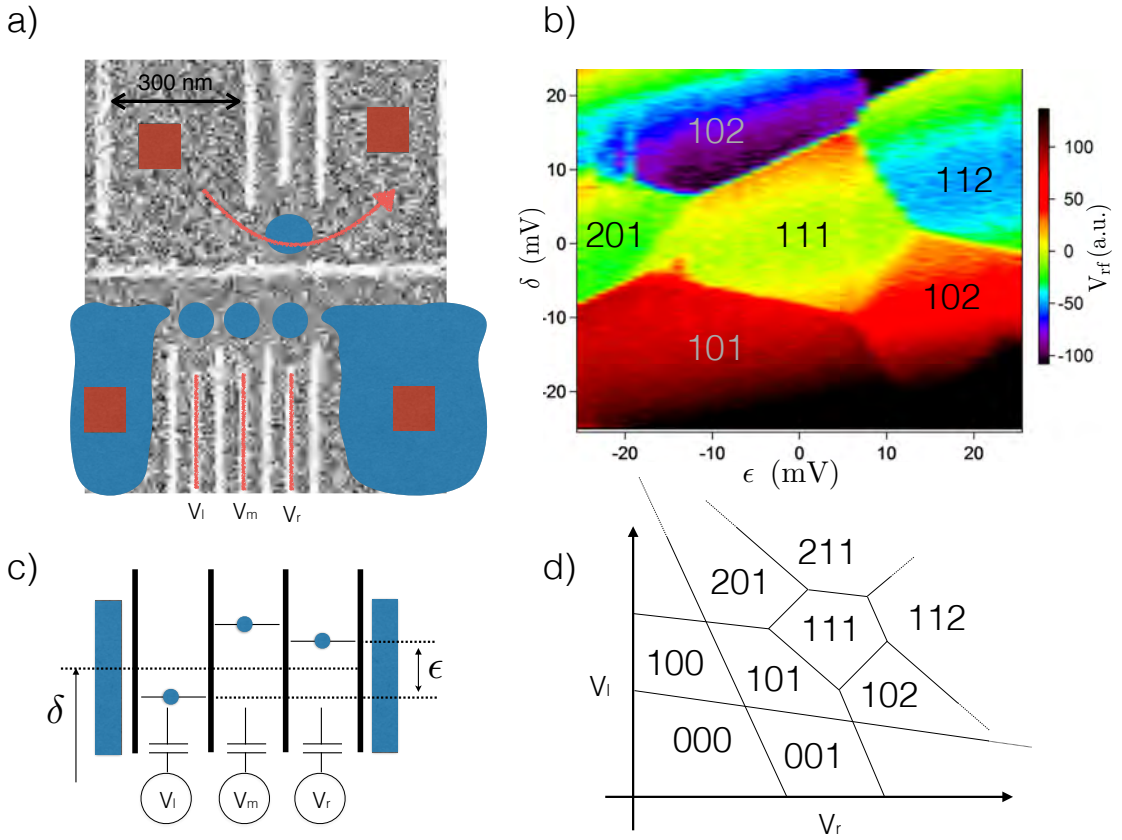


Figure 3.1: Charge physics of a triple dot. (a) Part of the device JB_TTL14. The 2DEG is indicated in blue. Ohmic contacts are red boxes. The electrostatic gates can deplete the 2DEG to form low electron occupancy quantum dots. The voltage space can be parameterized by ϵ and δ, which are the relative voltage detuning of the left and the right plunger gates and their average as shown in c). (b) Charge stability diagram of a triple quantum dot, taken with reflectometry (see section 4.3.3) in the device JM_19_2b (see table A.1), which is very similar to the one shown in (a) using the measurement setup described in chapter 4. This signal is not a differential conductance but the demodulated voltage from the charge sensor after a plane fit, which also subtracts a constant background. In this kind of plot, different charge occupations can still directly be identified. (c) Sketch of the energy levels in the triple dot. d) Sketch of a charge stability diagram of a triple dot. For comparison this is now plotted in the gate voltage space, as for the double dot in figure 2.5 a). The occupation can be determined by counting from the fully depleted region in the bottom left of the plot.

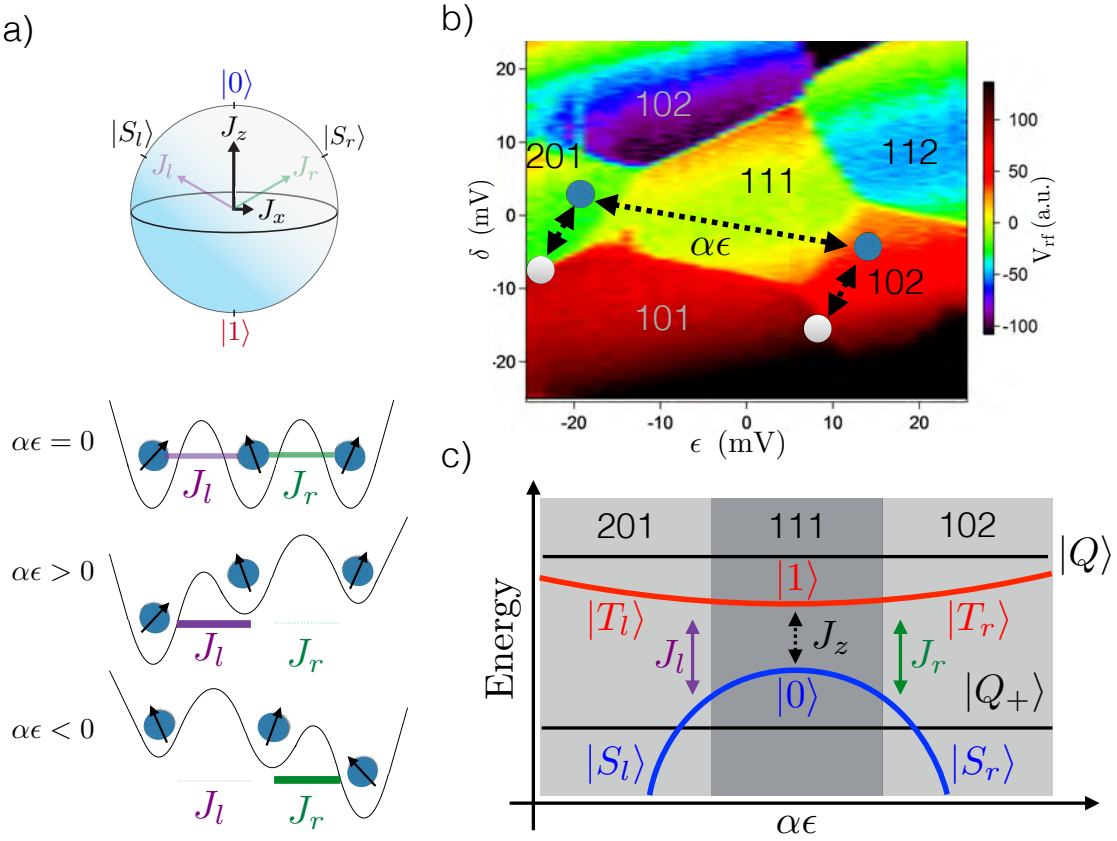


Figure 3.2: The resonant exchange qubit. (a) Mapping of the qubit in the $\epsilon = 0$ regime onto the Bloch sphere. When moving away from $\epsilon = 0$ the potential tilts and the middle dot will move more towards one side increasing the exchange interaction on this side while decreasing the other one. The eigenstates of the two exchange terms are indicated by the two axis J_l and J_r on the bloch sphere. (b) Operation of the qubit superimposed on the charge stability diagram. Blue dots are readout-points, white dot initialization-points. The operation axis can be slightly tilted relative to ϵ by α. (c) Sketch of the energy diagram of the exchange only qubit. Exchange splits the qubit states $|1\rangle$ and $|0\rangle$.

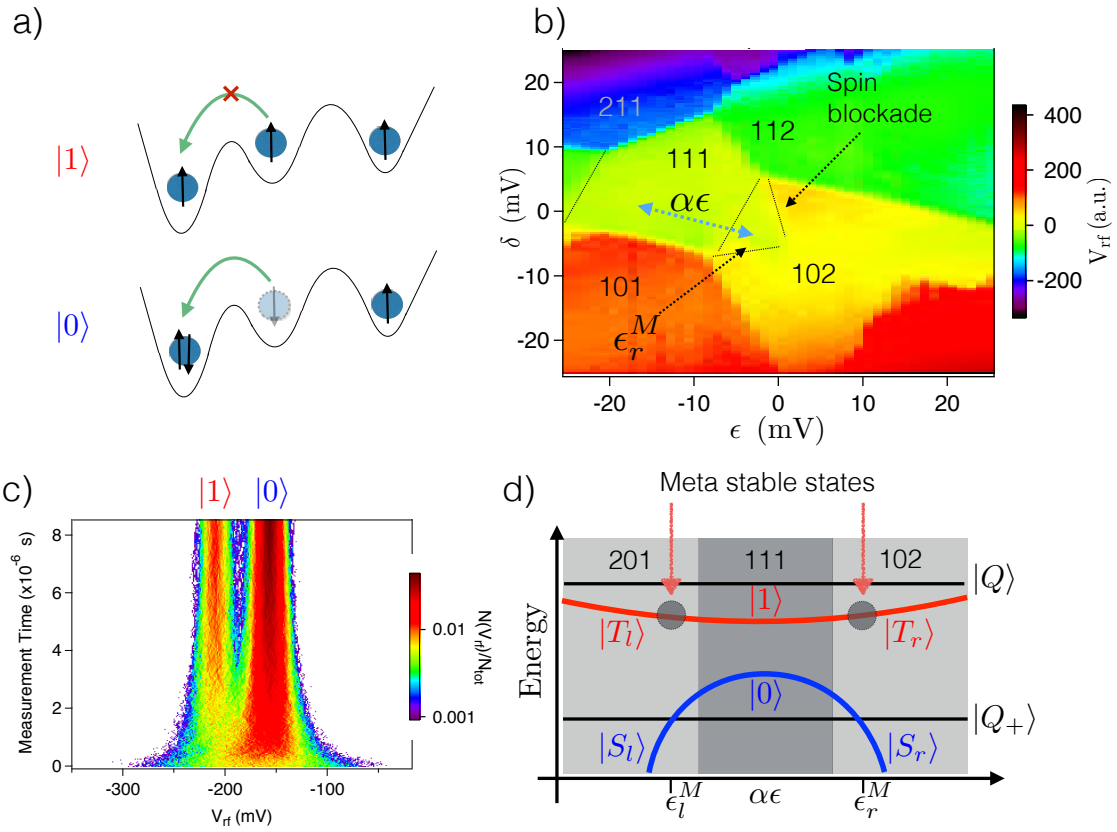


Figure 3.3: Reading out the qubit states. (a) Pauli spin blockade. If the spins are aligned, they can not occupy the left dot. If they are not, they can. This gives a charge signal of spin information. (b) A charge stability diagram of a triple quantum dot (device JM_19_2b measured with the setup described in chapter 4.) By quickly pulsing to negative detuning a region of spin blockade shows up, see main text for details. (c) Histograms of picked up charge signals for an experiment similar to b) for different measurement times. After 4μs the signals become very distinct. (d) Energy diagram of the triple dot illustrating the measurement points $\epsilon_{l/r}^M$.

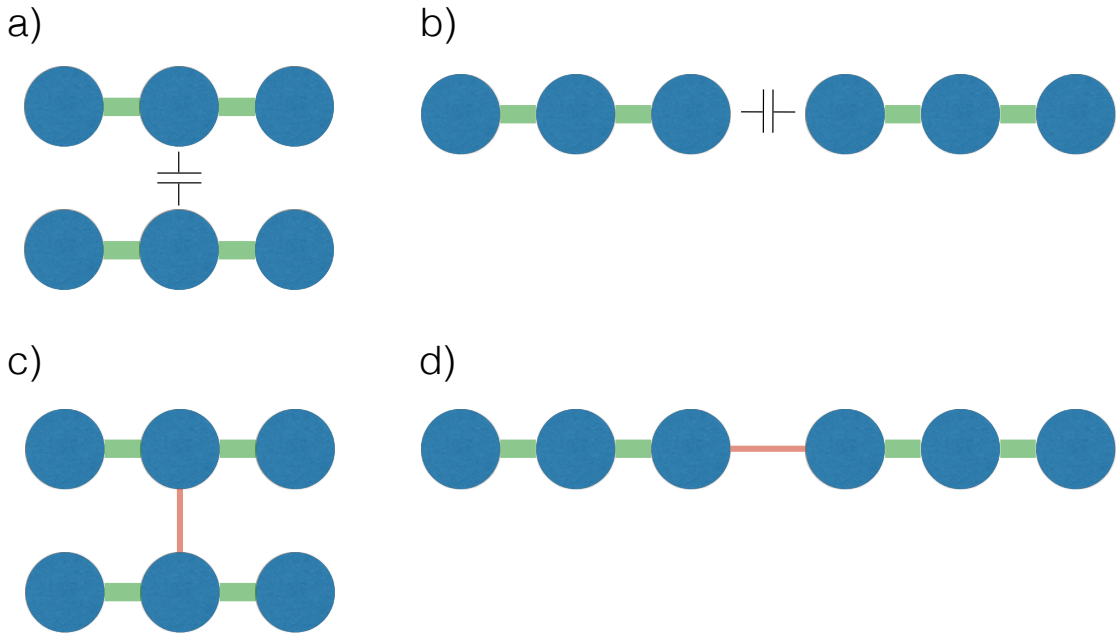


Figure 3.4: Different proposed coupling schemes for the triple dot. (a) Capacitive coupling via the middle dot. (b) Exchange coupling via the middle dot. (c) Capacitive coupling via a side dot. (d) Exchance coupling via a side dot. The coupling via schemes a) and b) is hard to extend beyond two qubits, c) is expected to be relatively slow. Thus we mainly have been working on designs enabling d).

Chapter 4

Device and Measurement setup

In the development of the device, both techniques for two qubit coupling as presented in section3.5 were considered. The starting point for all devices was the linear triple dot design developed by Jim Medford [20] [21], shown in shown in figure 4.1 a). The linear design in which the dots are oriented in a straight line separated from the readout dot by a long horizontal gate ("backbone") has proven to be very efficient, mainly for two reasons: Most importantly the linear design limits the degrees of freedom for the dot, which makes tuning very predictable. The middle dot has no place to go but either to the left or the right making it easy to "squeeze" it in. Other designs which have, for instance oriented the dots in a more triangular shape [14] [17], have suffered from the middle dot escaping towards the top. Limiting the degrees of freedom of course comes with the cost that the design may just not work at all. If, for instance the backbone is too close to the row of plunger gates / tunnel barriers, the voltage needed to pinch off under the backbone is enough to deplete fare into the areas of the intended dots, and it is thus impossible to form them. So it may take several iterations to get the right dimensions, once they are found however, tuning becomes comparatively easy. Secondly, having the sensor dot on the opposite side of the depletion gates forming the triple dot reduces crosstalk between them. The initial generations of devices were designed with capacitive coupling in mind. Figure 4.1 b) and c) show such designs. Figure 4.1 c) shows a so called "dogbone" design. The capacitive coupling in between the two triple dots in enhanced by a floating gate coupler fabricated in the same layer as the depletion gates. The coupler has little circles at the end giving it its name. This design very closely resembles simply two of the original triple dots, of figure 4.1 a). Since the coupling strength is reduced by the self capacitance of the coupler and the distance of the coupler to the dots, one can consider just gate defining a coupler in 2DEG, which is of course much closer to the dots than the surface gates. It also gives the possibility to deplete the 2DEG in the coupler, thus reducing its self capacitance. This also has the advantage that the coupler can easily be switched off with a surface gate, allowing for control of the coupling on ns timescales. Figure 4.1 b) also has the feature that it allows for a change in coupling scheme. Since there are four dots, one can shift the triple dot, such that the coupler primarily couples to the middle or one of the side dots. Eventually,

however, even before cooling one of those devices down, due to the low expected gate speeds, the idea of relying only on capacitive coupling was abandoned in favor of the "15 in a row" design in figure 4.1 d). This is additionally a much larger circuit with 15 quantum dots allowing in principle for up to five qubits. Here one has the option of fully depleting the channel in between two qubits only allowing capacitive coupling, or switching on tunneling for an exchange interaction. A device very similar to this, fabricated by Nastasia Okulova was measured with participation of the author. It was discovered that in such a design the qubits which are isolated from the ohmics in the middle become very hard to tune, since tunneling rates into them are very low. This does in principle not matter once the triple dot is in the low electron regime, where electrons are only shuffled around in between the dots, however in order to get there the occupancy has to be changed over a wide regime. Tuning up say, 9 at the same time also becomes too complicated. Also since the qubits are very close crosstalk as well as the charging energy of nearby dots becomes a huge problem. Those considerations lead to the design shown in figure 4.2, which was the one used in the measurements presented in chapter 5. This is now "only" a three qubits device, however, if shown to work for three qubits, the extension to five or more is straight forward, since one just needs to add more qubits in the chain. Compared to 4.1 d) the tripe dots have been moved apart. In between them we put a large quantum dot, which can mediate exchange or capacitive coupling. The increased distance should reduce crosstalk. Also in the initial phase of the experiment, the plungers defining the coupling dots remain unenergized, leaving a large puddle of electrons in between neighboring triple dots. This object was expected to be metallic and serve instead of the ohmis as a reservoir for the middle qubit, which is isolated from the ohmics once the outer two qubits are tuned into the few electron regime. After all triple dots are tuned up as single resonant exchange qubits, the plungers of the coupling dots can be energized, since no more change in occupation is necessary, and multi qubit operations can be performed. One more challenge would be the initialization of the middle qubit. Normally, this is done by tunneling to the leads. Here the idea was to just use the finding in [21]: If the middle electron is very strongly coupled to the outer two, the lifetime of $|1\rangle$ crashes to 100 ns. The coupling can be controlled via the middle plunger, so with a fast line on the middle plunger this mechanism would reliably initialize the qubit on shot timescales.

4.1 Device Fabrication

All devices measured for this thesis were fabricated with standard GaAs fabrication techniques. It starts with etching the 2DEG away wherever it is not needed, to electrically isolate the devices and reduce parasitic capacitance. The depletion gates on the surface of the device shown in figure 2.2 are made with electron-beam lithography. For electron beam lithography, the chip is first spin coated with a thin layer of electron-beam resist (Polymethyl methacrylate, short PMMA a "plastic"). After that, an electron beam lithography system, writes the specified gate patterns into the PMMA, by exposing it with a focused electron beam. The electron-beam resist is electron sensitive, so the

beam locally breaks up the polymer chains in the PMMA. The exposed area can then be selectively removed via a special developer. The electron-beam lithography system has a piezo controlled stage for rough positioning and can electrically deflect the beam. It constantly measures the stage drifts via a laser interferometer and adjusts the beam. This way, the electron beam can be moved with sub nanometer precision, making nanometer scale patterning possible. The maximal resolution for this technique in our process is limited by the ebeam resist.

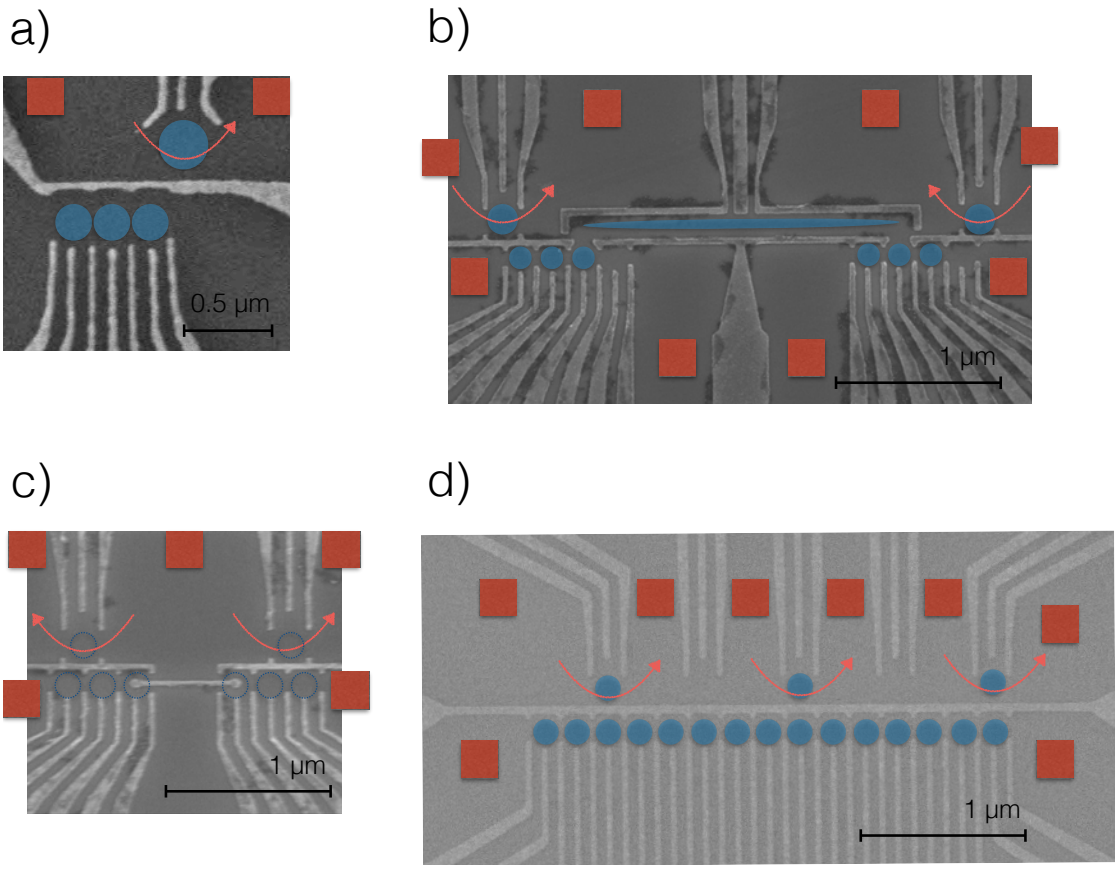


Figure 4.1: Micrographs of other designs fabricated during the development of the resonant exchange multi qubit architectures. The intended dots are indicated in blue. Ohmic contacts are the red squares. The readout channel is the red arrow.(a) The single qubit resonant exchange qubit developed and fabricated by Jim Medford. (b) Two qubit device with a gate defined floating gate coupler. It contains gates for four dots, which makes it possible to couple either to the middle or the left/right dot, as shown in this graph. The left triple dot couples to the right dot. The right triple dot couples to the middle dot.(c) A two qubit design with a floating metal gate over the outer dots to increase capacitive coupling. (d) The five qubit linear design "Pentrium". Every second readout dot has been omitted for visual clarity. Here both exchange and capacitive coupling between neighboring qubits is possible.

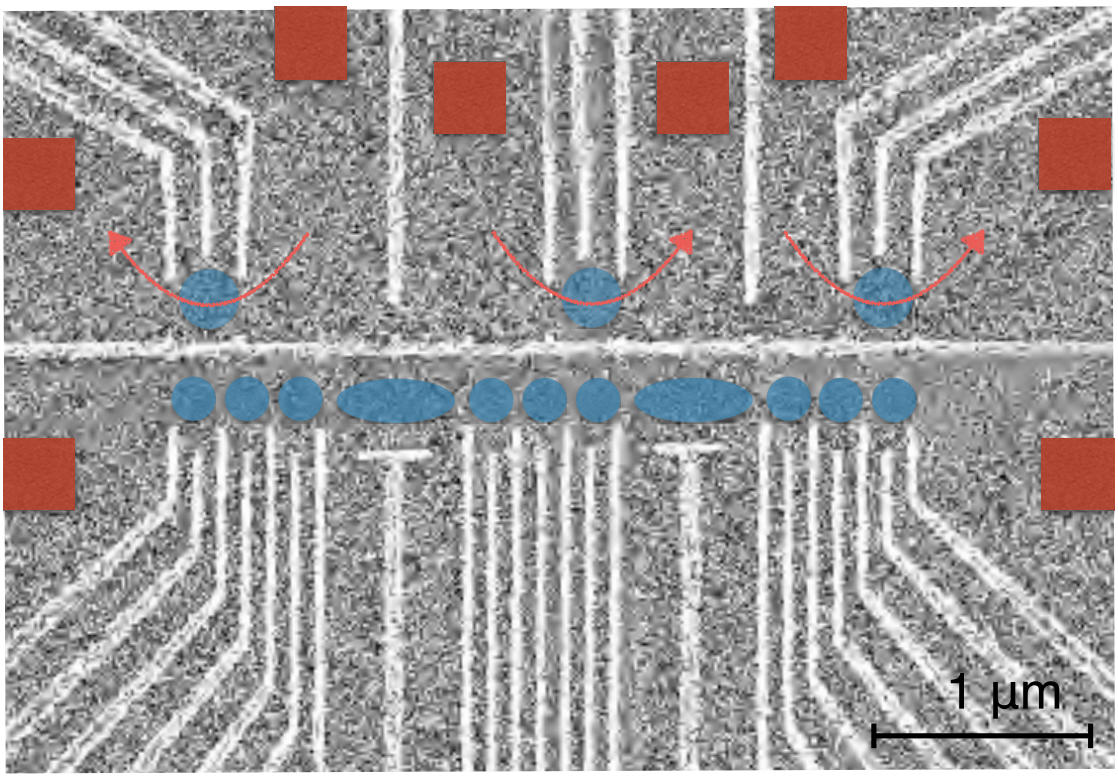


Figure 4.2: SEM image of the device used for the measurement in chapter 5. The intended quantum dots are in blue. The ohmic contacts are indicated by red boxes. The readout channels are marked by red arrows. The idea is that qubits are coupled via a large dot. This moves them apart, thus reducing crosstalk. Not energizing the plunger leaves a large reservoir of electrons, which can be used instead of an ohmic contact to tune up the dot. Once the dot it tuned into the low electron regime, this can be depleted to form the coupling dot.

After development a 5 nm layer of titanium and a 15 nm layer of gold are evaporated onto the chip. Since the unexposed area is still protected by the resist, metal is only deposited on the heterostructure in the predefined gate patter, since this is where it has been exposed. We then put the Ti/Au-PMMA-GaAs sandwich into a bath of Acetone, which dissolves the PMMA, leaving the Ti/Au only on the exposed areas. This technique makes it possible to fabricate depletion gates onto the heterostructure with 10s of nm in width and pitch. Figure 4.3 gives an overview over the entire process. The pattern for the etch step before that is done in a similar way, however, here the resist is locally exposed by UV radiation. The pattern is defined via a shadow mask, which protects the areas which should not get etched away (see figure 4.4). As mentioned in 2.2 the 2DEG is probed through ohmic contacts on the surface of the heterostructure. Ohmic here means that it has a linear current-voltage relation, as opposed to, for example a Schottky barrier. The patterning of the ohmics is also done via electron beam lithography. Here a stack of Ni/Ge/Au/Ni/Au is evaporated and afterwards diffused into the heterostructure via heating it up in an atmosphere of forming gas. This procedure creates contacts with resistance of the order hundreds of Ω at 4K. Low resistance ohmics are critical, since all measurements of the quantum dots are resistance based, so a high resistance of the contact reduces sensitivity. The fabrication details of the devices presented in this thesis are given in appendix C.

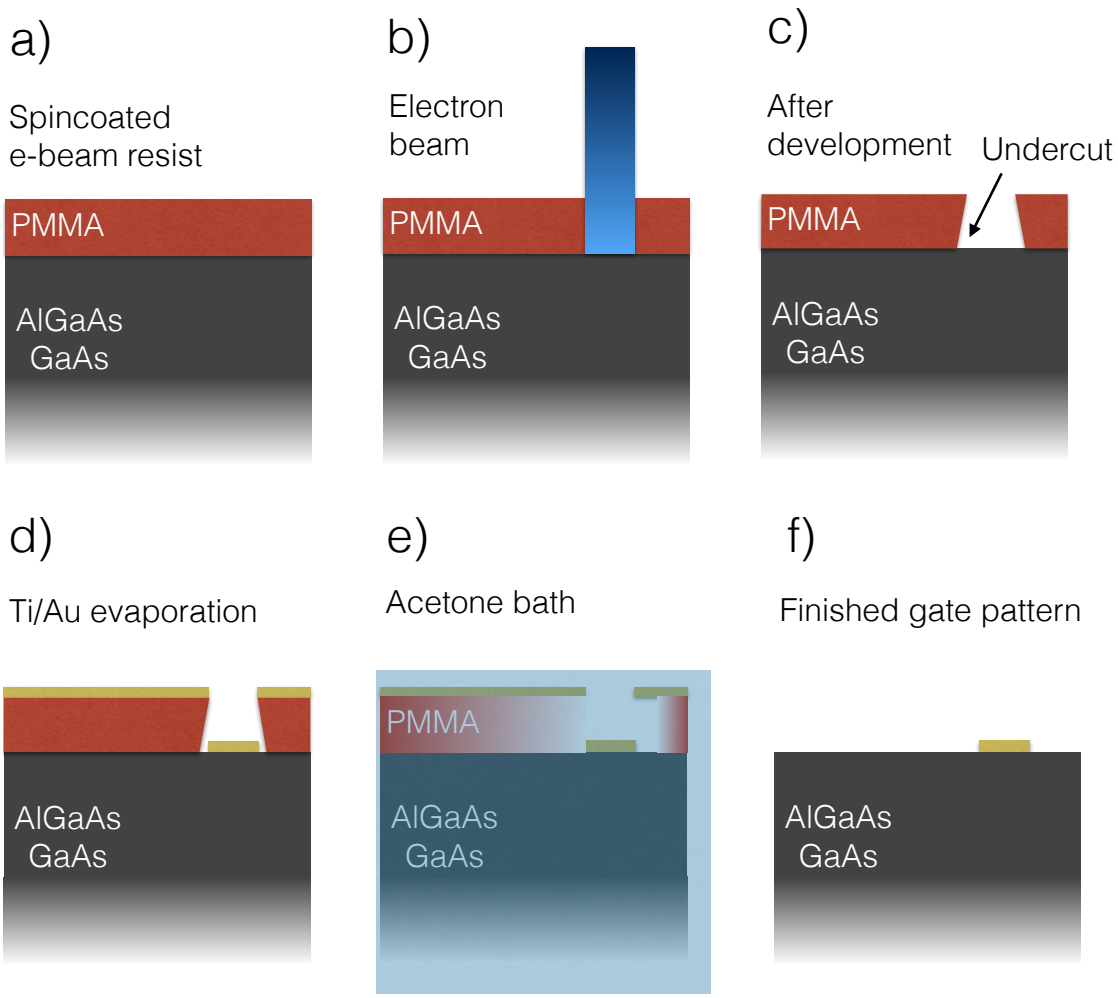


Figure 4.3: Ebeam lithography. (a) The heterostructure is spincoated with the electron-beam resist PMMA. (b) The electron beam writes the pattern into the resist, by locally breaking polymer bonds. (c) A special developer for e-beam resist disolves the areas irradiated by the electron beam. Backscattering electrons form an undercut, which will make liftoff, step e) easier. (d) 5 nm of Ti and 15 nm of Au are evaporated onto the chip. In the exposed areas the metals are deposited directly onto the heterostructure. The 5 nm Ti are a sticking layer; evaporating it in between Au and GaAs improves adhesion of the surface gates. Note how the undercut created a gap between the resist stack and the surface gate. (e) Liftoff: the chip is left in an acetone bath, which dissolves the PMMA. This is where the undercut becomes important, it makes it easier for the solvent to get under the PMMA/Ti/Au layer. (f) A finished surface gate. All PMMA has been removed.

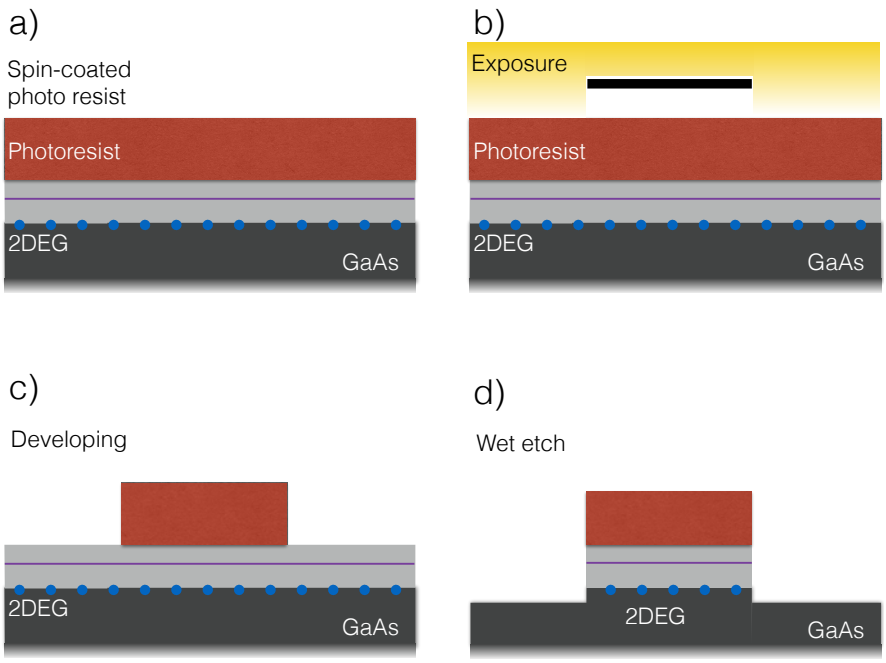


Figure 4.4: Photolighography for mesa etch. (a) The chip is spincoated with photoresist, a UV light sensitive plastic. (b) The chip is exposed with UV light in a mask aligner. The pattern is defined via a shadow mask, shown as the black bar here. (c) A photo resist developer removes all the exposed areas. (d) During a wet etch step, the remaining photo resist protects the chip from the acid. This way the 2DEG is etched away in all of the exposed areas.

4.2 Low temperature measurement setup

4.2.1 Cryostat wiring

The experiments involve setting voltages on the electrostatic surface gates to form dots, applying fast pulses and microwaves to plunger gates, for qubit operations, as well as measuring transport through the device and probing it with microwaves for readout. All this has to be done at cryogenic temperatures, but with measurement electronics at room temperature. The device was cooled to 20-30 mK in a Triton 200 cryogen free dilution refrigerator. Cryogen free means that the cooling power is provided via a pulse tube cooler, and the system's gas/condensate circulation is fully closed. The 20 - 30 mK are the temperature of the mixing chamber (MC) plate (see figures 4.5 and 4.6). On the device this corresponds roughly to the temperature of the semiconductor lattice. The 2DEG is warmer, it does not get cooled very strongly by the crystal lattice due to weak electron-phonon coupling. The electrons get cooled through the DC wires contacting the 2DEG, which are thermally anchored to several stages in the cryostat via copper clamps and a copper pole. The copper clamps are two plates of copper bolted to the plate of the fridge which press against the wires from both sides for good thermal contact. Copper poles are cylinders of copper bolted to the plate of the fridge and the loom wound around and secured with GE varnish (a glue which works at low temperature). To suppress the noise coming through the DC wires two stages of filters were attached to the mixing chamber, denoted RF and RC in figures 4.5 and 4.6. Details of the filters are shown in figure 4.7 [1]. Since the experiments are performed in the 2DEG, the second figure of merit alongside the lattice temperature is the electron temperature. It was determined by Coulomb peak thermometry [33], which gives an upper bound on the electron temperature. For this setup the electron temperature was measured to be $<$ 100 mK. The DC wires which set the voltages on the surface gates, share the same wiring as the ones contacting the 2DEG. Here the requirements are also that they have as low noise as possible. The wires are routed through the cryostat in a nylon loom. The materials of the wires are constantan down to the mixing chamber and copper afterwards. Qubit operation and (reflectometry) readout are done at radio to microwave frequencies, so the wires in the loom can of course not be used for that. Therefore the fridge has been equipped with two sets of coaxial lines. A central bundle of eight coaxial lines is used for control. On the side there are two lines especially set-up for reflectometry readout. More details on the reflectometry wiring are given in 4.3.3. For filtering and thermalization the lines going down to the sample are heavily attenuated on the 4K plate, the still plate and the mixing chamber. The largest attenuation is on the 4K plate since this has the highest cooling power. In order to prevent dissipation heat from a constant current through the attenuator, every signal through the coaxial lines is AC coupled.

[1] This type of PC board filter was developed by Ferdinand Kümmeth at the Marcuslab for Mesoscopic Physics, Harvard University. They are thus commonly referred to as "Ferdie Filters" by everyone except the inventor who prefers the name "PC board filter".

4.2.2 Sample holder

For the experiments in the cryostat, the device is glued onto a sample holder. In this case, this is the "Mayo board", a PC board sample holder developed in the former Marcuslab in collaboration with electrical engineers at Mayo Clinic. The sample holder, connects the chip to the wiring in the cryostat. Figure 4.8 shows the chip glued to the sample holder. The thin aluminum wires connect the surface gates on the chip to the gold bond pads on the sample holder. The board also contains the tank circuits for reflectometry. In order to get good matching on all of the three readout dots, we had to change the inductors. We got good matching with 750, 910 and 1200 nH. In its original version, the board also contains varactor diodes in parallel to the inductors which give the opportunity to increase capacitance to ground to get better matching. We found them not to be very useful at low temperatures and removed them alongside with their coupling capacitors in order to reduce parasitic capacitance on the board. This also frees the varactor bias DC lines, giving four additional lines for qubit control. The board also contains the bias tees for readout and the fast gates (not visible in the picture). The sample board is then bolted down inside the sample puck. Figure 4.9 shows the sample board inside the half opened puck. A DC cable assembly inside the puck connects the DC wires from the sample board to a nano-D connector on the outside of the puck which will then connect to the cold finger of the cryostat. Similarity, semi flexible Cu-Cu coax connect the boards coaxial SMA connectors to the SMA feedthrough on the puck. The puck can be loaded into the fridge via load-lock without the need to warm up and open the fridge. Details on bonding and pinout of the device used in the measurements can be found in figure B.1.

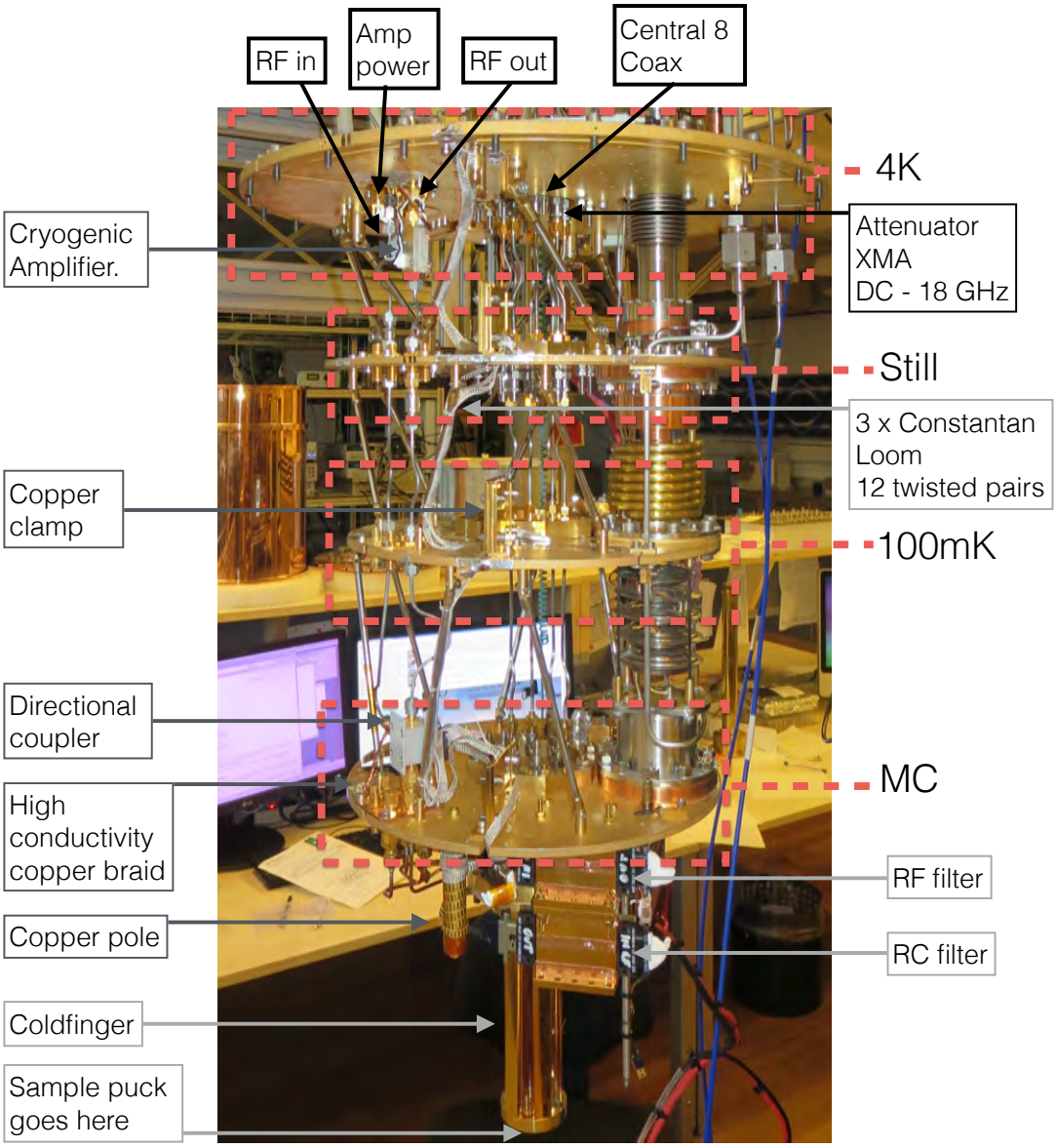


Figure 4.5: The open dilution refrigerator. In the closed state there are two layers of radiation shields and a metal can for vacuum. More details on the wiring are shown in figure 4.6

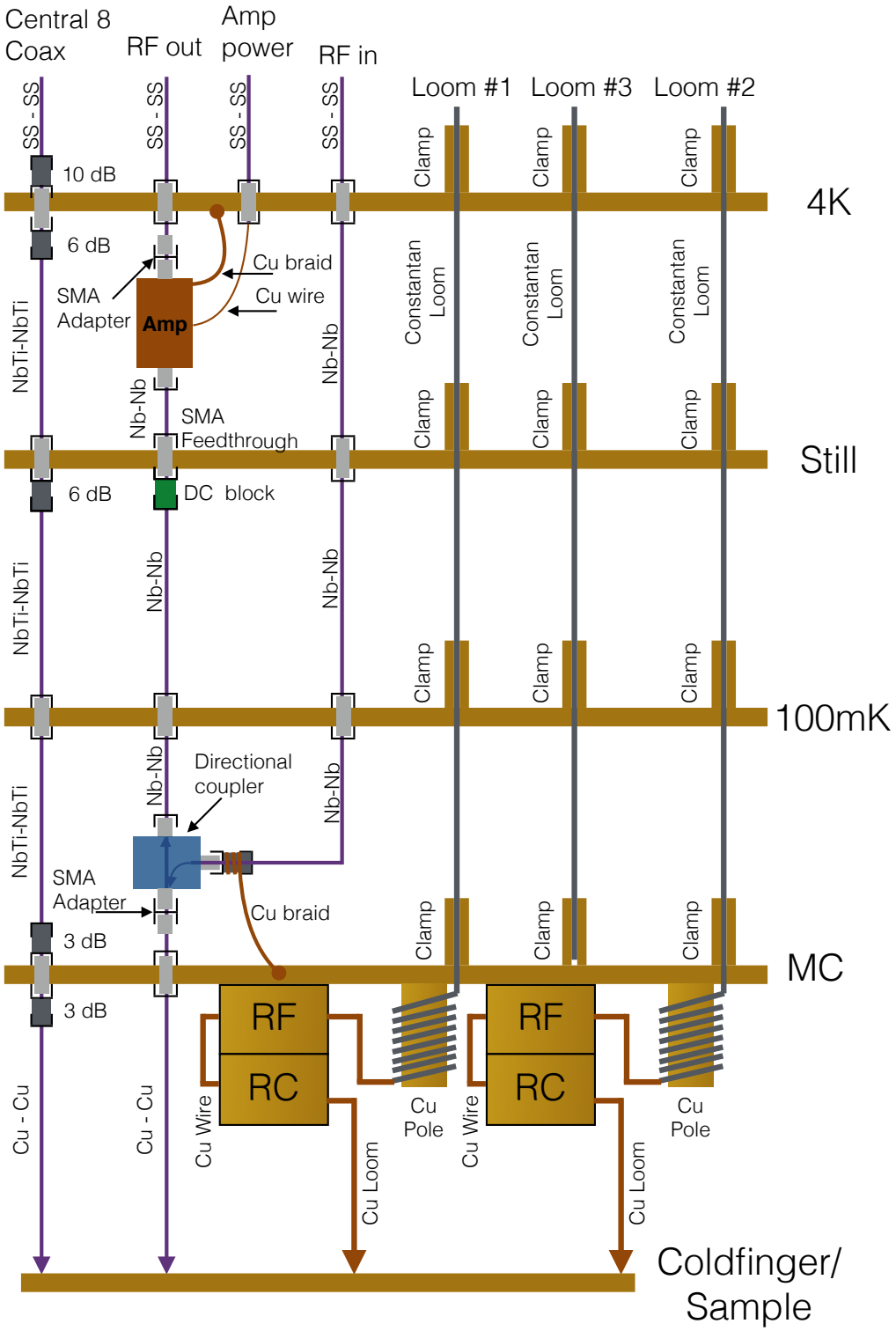


Figure 4.6: Wiring diagram of the fridge. There is a total of 48 DC and 9 coaxial lines going down to the sample. The DC lines are cold anchored to every stage of the cryostat via copper clamps. On the mixing chamber, a RF and a RC pcboard filter, thermally anchored and shielded via a copper enclosure suppress noise in the DC wires. The 8 coaxial lines for control and the input line of the reflectometry signal are attenuated for thermalization and filterning. A DC block between the cryogenic amplifier and the directional coupler protects the sample from noise coming down from the cryogenic amplifier. The cryogenic amplifier is powered through a coaxial line. The arrangement of the RC RF filters and the copper pole is not optimal. It is better to have the copper pole after the filters.

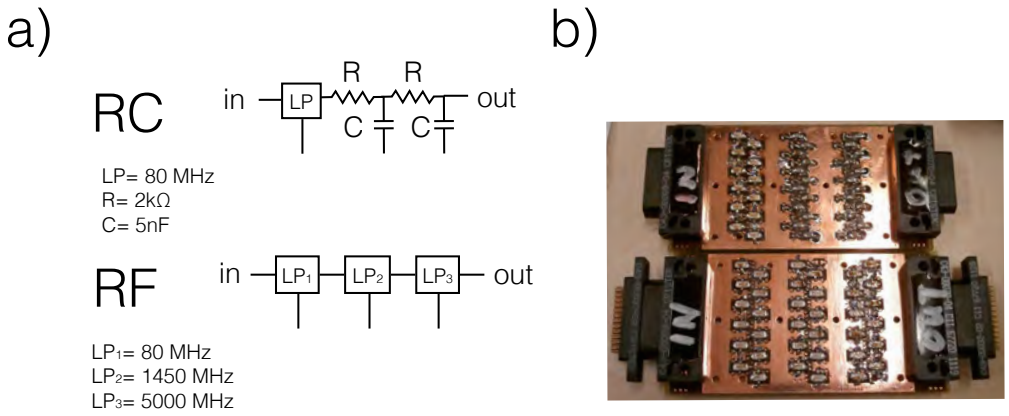


Figure 4.7: (a) Schematics of a single filtered line in the RC and RF filters used inside the cryostat. The low pass filters : MiniCircuits LFCN. Resistors and Capacitors: Digi-key. (b) Picture of the freshly soldered PCboard RC and RF filters. This board is then secured inside the copper enclosure, which is bolted to the mixing chamber as seen in figure 4.5.

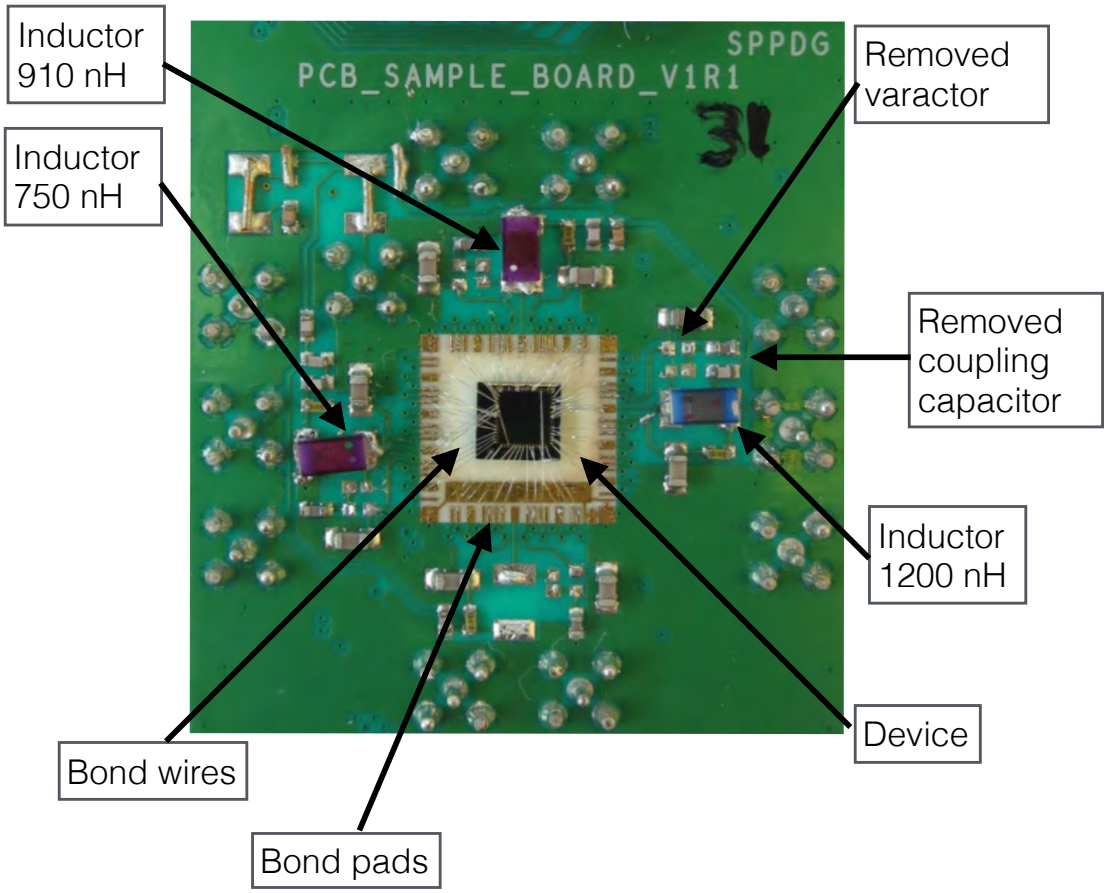


Figure 4.8: The "Mayo board" sample holder with a device bonded to it. The golden stripes around the sample are the gold bond pads. Thin bond wires connect them to the device. Inside the board, they connect either directly to one of 48 DC lines which end in two nano D connectors on either side of the board, or go through a bias tee, where they additionally have contact to one of 10 high frequency lines.

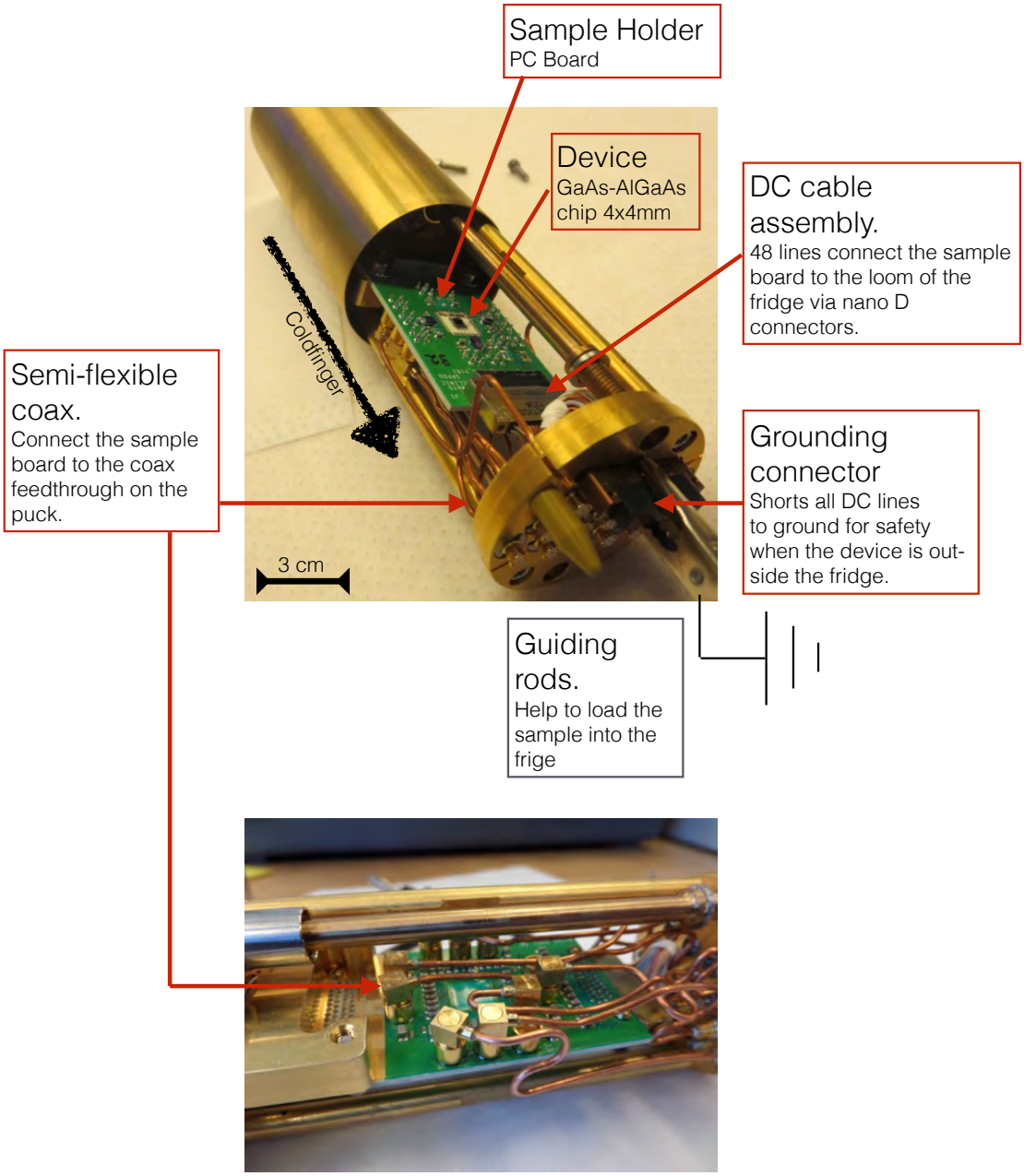


Figure 4.9: (a) The bonded sample on the sample board inside the half opened puck, ready to be loaded into the frige. (b) The backside of the PC board sample holder inside the puck. The high frequency lines are attached via semi-flexible copper-copper coax.

4.3 Measurement electronics

The room temperature part was built very similarly to the setup used at Harvard University for the resonant exchange qubit experiments [21]. The setup was characterized using the exact same device as for the resonant exchange qubit: figure 4.1 a). In terms of noise, the Copenhagen setup in fact performed better, giving an increase of factor 10 in signal to noise for reflectometry.

4.3.1 Slow, DC electronics

The voltages on the depletion gates which form the dots, as well as bias voltages across a sensor dot or a sensing QPC for readout should be very stable over long timescales. Those are provided by the Deca DACs (DAC = Digital to Analog Converter) designed and manufactured by Jim McArthur from the Harvard physics electronics shop. An overview of the measurement electronics is given in figure 4.11. The DAC is in the upper right. The DACs are controlled by the measurement computer via ASCII commands provided by a serial interface. To isolate the DAC from the noisy serial port of the computer, the communication goes through a serial to fiber-optic converter (fiberoptics are orange in figure 4.11). The voltages provided by the Deca DAC then go through voltage dividers/filters with a division factor of 1:5 for surface gates or 1:1000 for bias gates and a low pass constant of 7 Hz. Before connecting to the breakout box they are filtered again by a MiniCircuits BLP-1.9 lowpass (1 Mhz) filter. Details on the breakout box - DAC setup as well as the dividers can be found in figure 4.10. The breakout box combines the single lines in a shielded cable which connects to a fisher connector on top of the cryostat, which feed through to the twisted pair constantan looms going down to the sample. The DC transport measurement are done by connecting the "drain" electrode (through an ohmic, red in figure figure 4.11) via the breakout box to a Itaco current ("Ithaco" in figure 4.11). The current amplifier provides a virtual ground for the drain and converts the current to a voltage which is then measured by a digital multi meter (DMM Agilent 34401 A). For all the measurements presented in this thesis we had up to three current probes simultaneously. Data acquisition from the DMMs is done via their General Purpose Instrument Bus (GPIB). As for the DACs, fiber-optic communication shields the instruments electrically from the data acquisition computer.

4.3.2 High frequency electronics

An overview of the setup is provided in figure 4.11 (High frequency signals are in red). The high frequency electronics are used for fast ramps of the plunger gates and qubit control. The experiment is controlled by a high bandwidth Arbitraty Waveform Generator [1]. For taking fast charge stability diagrams, the output of two slower AWGs [2], "Left Ramp" and "Right Ramp" in figure 4.11, is added to the analog output of Channel 1 and 2 of the AWG, via the "Add input" ports. For driving qubit transitions as described

[1] Tektronix 5014C, 1.2 Giga samples per second, 300Mhz
[2] Agilent 33250

in section 3.2 the output of a Vector source [3] is combined with Channel 1 of the AWG, providing a phase-modulated excitation up to 6GHz to the left gate of the qubit. The signal also passes through a bias tee on the PC board, which provides the DC offset from the DAC as for the slow gates. The electronics setup here is presented only for one qubit. The extension to more is straight forward, one simply needs to multiply the presented setup with additional AWG and synchronize the AWGs via an external clock.

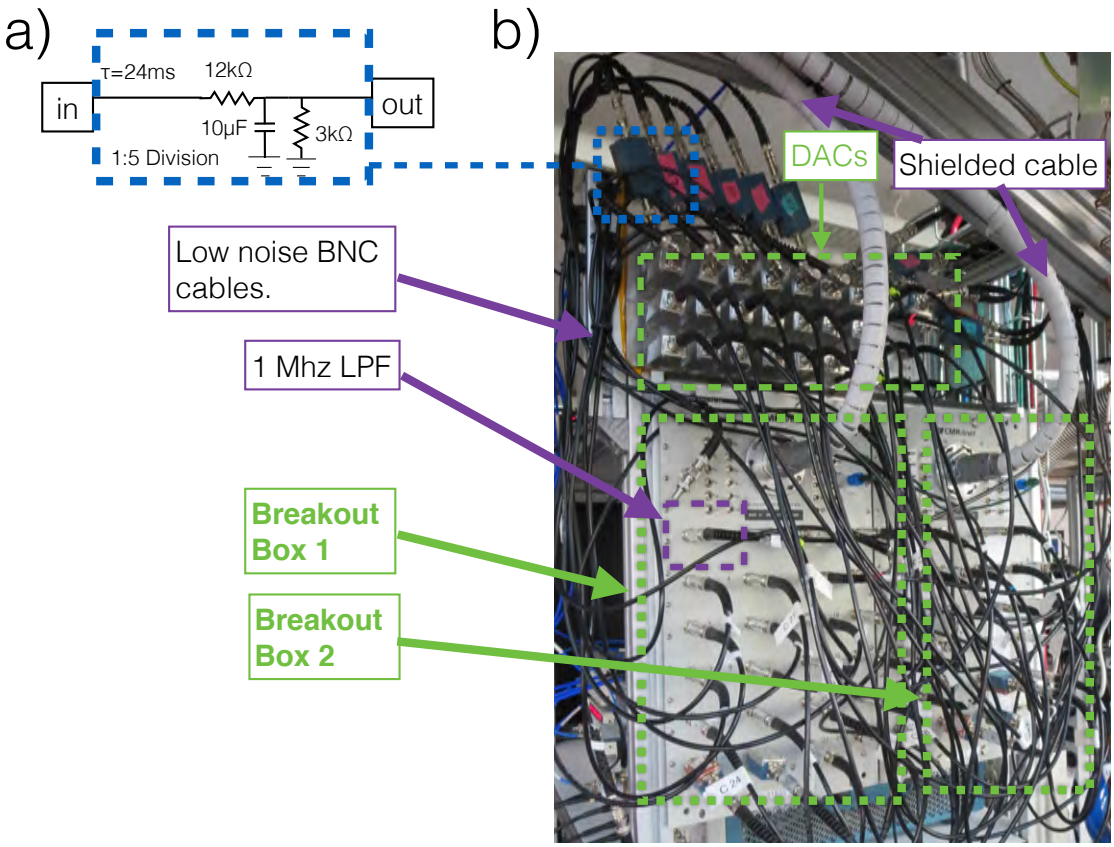


Figure 4.10: The slow electronics setup: DecaDACs and breakout boxes. (a) Schematics of the voltage divider filter boxes attached to all DAC channels. Additionally to this 1:5 divider box, we also have 1:1000 divider boxes for voltage bias lines which are used for transport measurements. (b) The DecaDACs on the top (barely visible behind the dividor boxes and the wires) provide stable precicse voltages. The voltages are divided for higher accuracy and filtered before they go to the breakout box via low noise BNC cables. Before the connector of the breakout box, there is an aditional 1MHz low pass filter (Minicircuits BLP 1.9+) to shield it from high frequency noise. The breakout box connects to the cryostat via a shielded cable (top).

[3] Rohde und Schwarz SMBV100A, 6GHz

4.3.3 Reflectometry

Typical resistances in the charge sensing channels are of the order 100kΩ. The capacitance of the wires in the DC loom is 1nF. The combination gives a low-pass filter of:

$$f_{lp} = \frac{1}{2\pi RC} = 1\text{kHz}. \tag{4.1}$$

This makes it impossible to observe fast charge dynamics (on the order of MHz) with the standard charge sensing through transport technique [30]. Instead of measuring the channel resistance directly, the resistance 100kΩ is matched to the 50Ω impedance of a coaxial line via a tank circuit. In our case, the circuit is right on the sample board, see figure 4.8. The impedance is then probed via a microwave excitation in the coaxial line. In case of perfect matching, the signal sees only an rf ground. In case of a mismatch, part of the signal gets reflected. The reflected power is proportional to the mismatch:

$$P \propto |\Gamma(\omega)|^2 \tag{4.2}$$

$$\Gamma = \frac{z(\omega) - z_0}{z(\omega) + z_0} \tag{4.3}$$

With z_0 as the impedance of the line and $z(\omega)$ the impedance of the RC circuit. From a simple circuit model we get:

$$z(\omega) = i\omega L + \frac{R}{1 + i\omega RC} \tag{4.4}$$

where L is the inductance, R the resistance, dominated by the resistance of the quantum channel and C the sum of the stray capacitance from bond wires, surface mount components, 2DEG etc. The matching resistance is $R_{match} = L/(50\Omega C)$, in which case the matching frequency is $\omega = 1/\sqrt{LC}$. So we see that the reflected power is very sensitive to changes in resistance on the device around the matching condition. It tuns out that typical stray capacitances as well as the resistance of a quantum channel require a matching inductance of 100s to 1000 nH and frequencies of 100 MHz which both can be achieved with "off the shelve" surface mount components and commercially available signal generators. In order to reduce stray capacitance the inductor should be as close to the quantum channel as possible. In our setup the inductors are mounted on the sample holder right next to the device (see figure 4.8) and bond wires were kept as short as possible. It is also possible to remove the bond wire complication by fabricating the inductor right onto the chip. The reflected signal is measured via homo-dyne detection. An overview of the entire setup is shown in figure 4.12. The excitation is provided by a SRS SG 384 signal generator. It is then split up. One part goes through an rf switch and a phase shifter into the cryostat. The rf switch is controlled by the AWG which controls the qubit experiments and makes sure that the excitation is only switched on when we want to read something out. During qubit manipulation, the excitation remains switched off because it would introduce extra noise. For readout the excitation is then lead through a directional coupler towards the sample where it rings the tank circuit up. On the sample

holder, there is also a bias tee which makes it possible to apply a DC bias through the same channel for transport measurements. The ohmic, across the sensing dot, as seen from the excitation is grounded outside the cryostat providing an rf ground. If the circuit is perfectly on resonance, the excitation is just fully dissipated into the rf ground. In case of a mismatch, part of the signal is reflected back. The directional coupler leads the reflected signal into the readout line (blue in figure 4.12), where it gets amplified by a "Weinreb" cryogenic amplifier (46 dB gain, noise temperature T_N 4K) before leaving the fridge. A DC block in between the directional coupler and the amplifier (not depicted in 4.12, see figure 4.6) protects the sample from the noise coming from the amplifier, since the isolation of the directional coupler is not perfect. Besides the DC block there is no filtering on the"rf Out"line since this is the readout signal which we want to maximize. Outside the fridge there is another amplification stage. Thereafter the signal gets mixed down to DC with the second part of the signal coming from the signal generator ("local oscillator"). After adjusting for path mismatch with the phase shifter on the "rf In" side, the reflected signal will constructively (or destructively, depending on the phase one chooses) interfere with the local oscillator and thus show up in the amplitude of the demodulated DC signal. This voltage is then, after a last amplification stage (5 $\times$ gain), read in by the Alazar Card in the data acquisition computer. The alazar card is synchronized with the experiment via the AWG, which provides an external clock and triggers the acquisition at the same time it opens the rf switch (see figure 4.11).

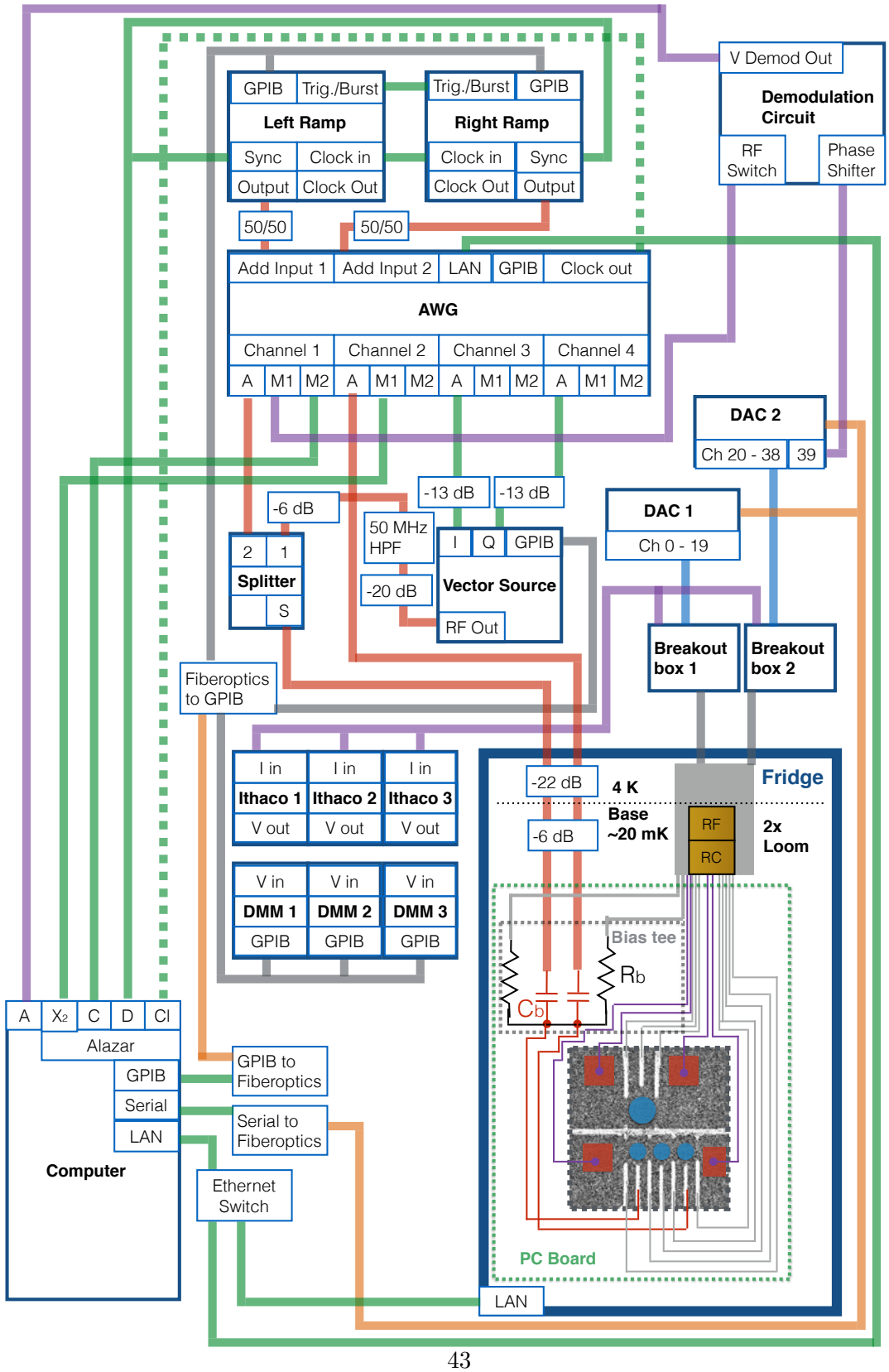


Figure 4.11: Sketch of the control and measurement electronics setup. Instrument coordination, such as triggers, clock synchronization circuits are green, control signals are red when fast, blue when slow. Readout data is purple. Fiber-optics are orange. GPIB is grey. Loom inside the fridge connecting to DC wires is also gray. Bottom right: the cryostat schematically with a device inside.

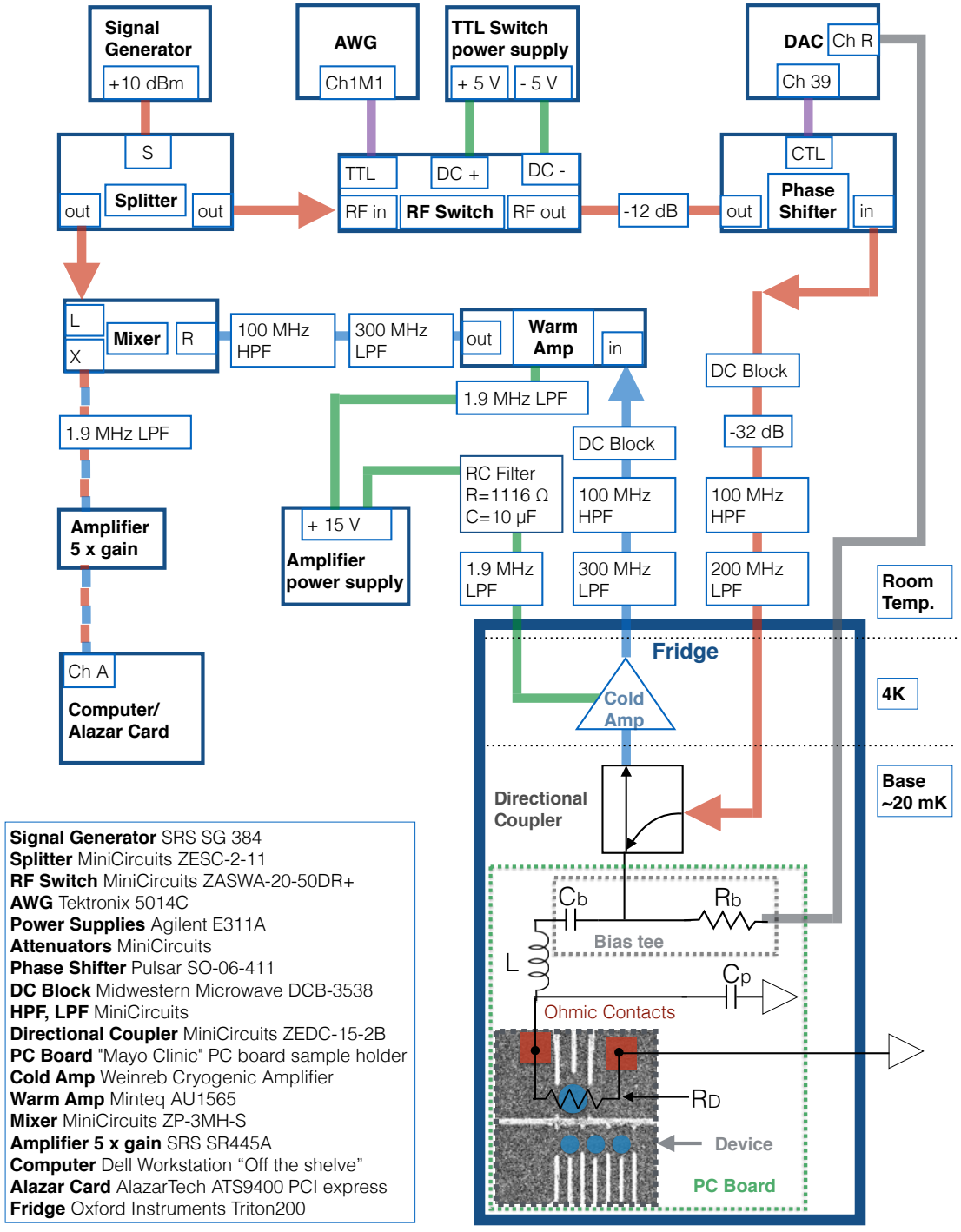


Figure 4.12: Schematics of the reflectometry setup. The signal going into the fridge is in red. The signal coming out is blue. Power supply is green. Control signals such as triggers are purple. See main text for details.

Chapter 5

Experiments towards a multi qubit architecture

5.1 Reduction of gate cross coupling with a screening gate

Cross coupling, from gate to gate, as well as gate to (other) quantum dots is a major challenge for tuning and operation of qubits. Cross coupling can for tuning purposes in part be counteracted via software, but the effects are only linear within a limited range and this does not solve the problem of mutual noise, which causes decoherence. Therefore an "analog" technique to reduce cross coupling is desirable. One possibility is the screening gate. Here, first an isolating layer of HfO_2 is deposited on the entire chip, as shown in figure 5.1. Afterwards the area of the fine gates is covered with a single large Ti/Au gate, connected to a bond pad on the sample holder, which can then be grounded. This way a mirror charge above all of the energized gates is introduced. The electrical field of the dipole falls of faster than the monopole thus reducing cross coupling. In order not to screen the the triple dot from the readout dot, the gate can only cover half of the dots(see figure 5.1 b) bottom). The top of figures 5.1 (a) and (b) show the sections of the devices used to test the effect of the screening gates. (a) is the unscreened version, (b) is the screened version. Besides that, the devices were lithographically identical. The entire device is lithographically similar to the device shown in 4.2, a 3 triple dot device whitch coupling dots. In the experiment we measured the collective pinch-off of two gates, as shown in figure 5.2. The gates were nearest, next nearest and next-next nearest neighbors. For perfect isolation, the conducting region should form a rectangle, so the voltage of any other gate does not influence the pinch off voltage of a gate. If the gates were shorted, it would be triangular. Looking at the first column, the unscreened case, just looking at the green region we see a strong cross coupling in the top graph, for nearest neighbor, less for next nearest and effectively no cross coupling for next-next nearest neighbor. In the screened case, on the second column, the coupling is already weaker in the nearest neighbor case and falls off more rapidly, showing almost no crosstalk already in the next nearest neighbor case. Also note that in both columns, in the inner region where conductance is high (red) coupling

goes down, the angles get closer, indicating screening just from the 2DEG.

5.2 Forming multipe triple dot in one device

After many unsuccessful tries, JB_TTL14 was the first fully functional multi qubit device. It was possible to form all three triple dots separately as well as two at the same time. This can be seen as a proof of principle or rather proof of possibility of this design. It also helped to identify two key challenges of this architecture which will help improve future designs.

5.2.1 Bias cooling

The device was cooled down twice. First without "bias cooling" and then with +200mV. Bias cooling means that a small positive voltage (100s of mV) is applied to the gates during cooldown. It has been observed that this way, gates become stronger and the device over all quieter. The "quieter" depends heavily on the device. It can reduce, both, low amplitude high frequency switching noise (seconds and faster) as well as sudden "jumps" where the potential suddenly shifts by tens of mV (days for a good material). Despite the exact mechanisms not being fully understood, it has become standard technique when forming quantum dots. Practically, in our setup this can be done within the normal loading procedure while using the load-lock. All of the 48 lines on the sample holder break out into two nano-D connectors. One connects to the top of the puck (see figure 4.9) which continues through the cold-finger into the fridge, the other one connects to the bottom of the puck and to the puck loading stick (PLS), where it breaks out into two fisher connectors resembling the top of the fridge. The connection on the PLS can be used to apply a voltage while loading the device. It is important to apply the voltage all the way from room temperature, since much of the effect occurs when cooling the device from room temperature to under 100 K. The device is already cooled significantly before even touching the coldfinger, because the sample puck touches flaps inside the fridge which are at 10 K. We have observed bias cooling having practically no effect when starting it only once the device is loaded. One draw-back of bias cooling is of course that gates can not be "swiched off" anymore. While a non bias cooled grounded gate leaves an unperturbed potential landscape, the bias frozen into the 2DEG can only be removed by warming the device up. Devices of the same material as JB_TTL14 cooled down earlier did not show any switching noise without bias cooling, so we also chose no bias cooling at first. However, as it turned out the devices did show jumping as well as slow (10s of hours) drifts in gate strengths, so tuning was very hard. Therefore, we chose to bias cool it as +200mV. The exact voltage is always an educated guess, it is typicially 100 - 500 mV. We started on the lower end of that spectrum, since collaborators working on the same material reported bias cooling having a relatively strong effect. The bias cooling did make the device more quiet and predictable. However, tuning was still very challenging.

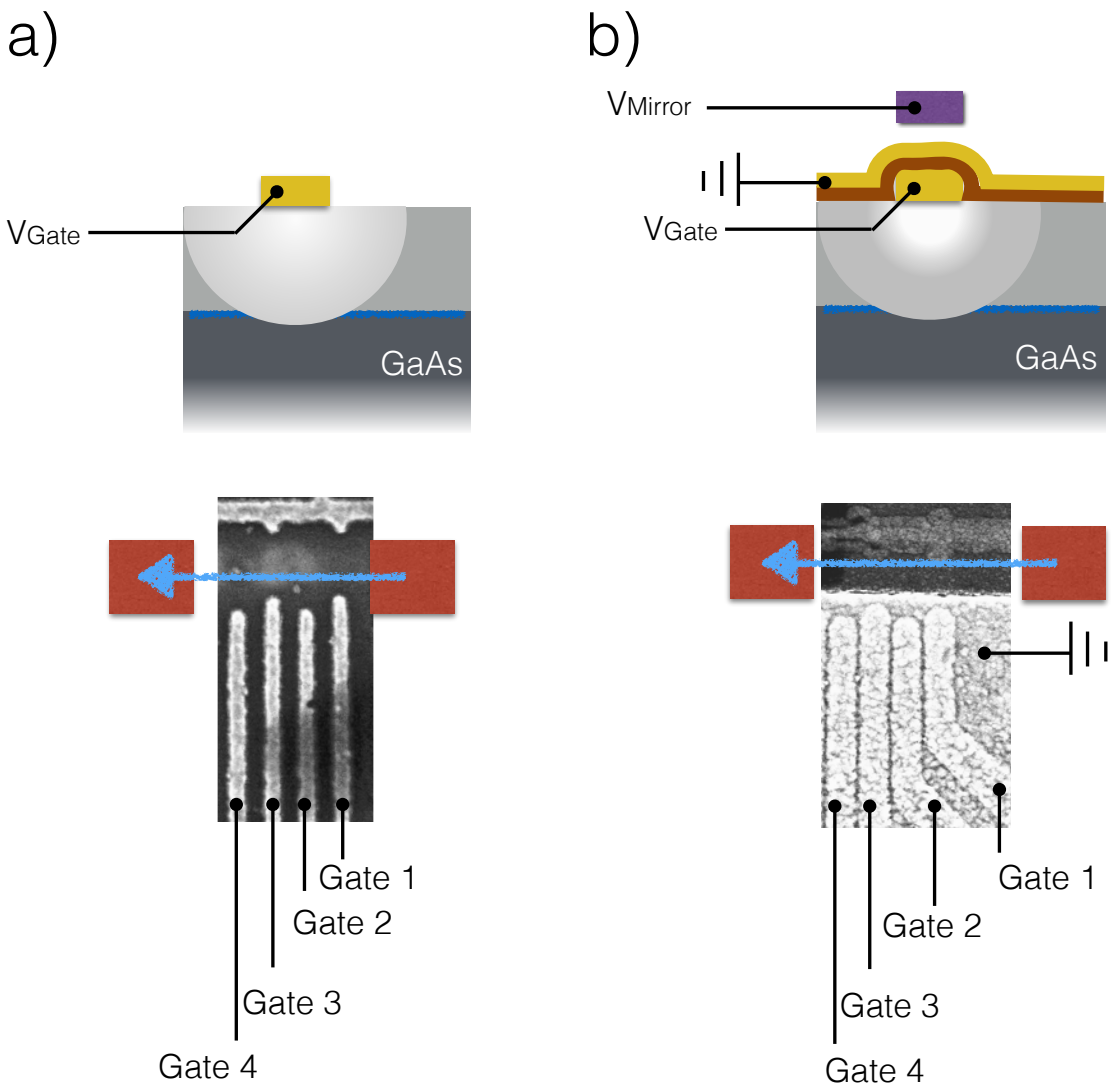


Figure 5.1: Overview of the screening gate experiment. (a) The unscreened case. A sketch of the regular heterostructure with a top gate depleting the 2DEG. Below the part of the device used. We measured transport through the device while pinching the gates off. (b) With a screening layer. On top a sketch of the heterostructure with a screening gate. On top of the gate, there is a layer of insulating HfO_2 and of top of that, one large gate covering all of the depletion gates, which is kept at 0 V. The effective field of this structure can be thought of as the one of a dipole with the mirror charge above the screening gate. The field of this dipole falls of faster with distance than the monopole.

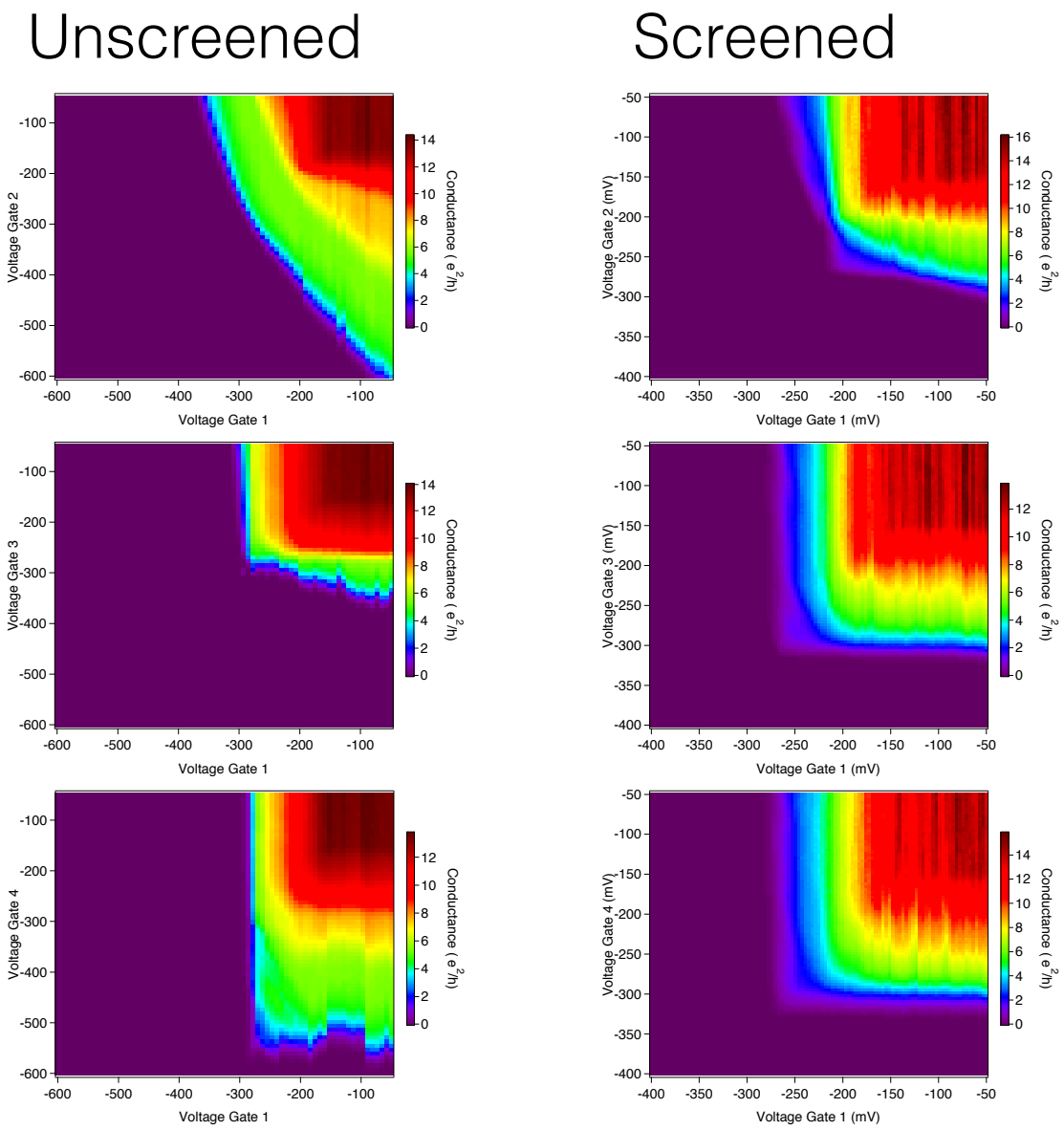


Figure 5.2: The effect of the screening gates on the collective pinch off curves of nearest (top), next-nearest and next-next nearest neighbor (bottom). In the unscreened case, the cross coupling especially in the first two cases is significantly stronger, as seen by the larger angle between the borderlines from higher to lower conductance, for instance green to blue.

5.2.2 Single triple dots

The strategy in general was to try to tune the triple triple system semi simultaneously. The algorithm for tuning up a single triple dot is normally :

1. Put 50 μ V voltage bias across the device to measure transport.
2. Take pinch off curves of all the gates and the sensor dot.
3. Put all of the gates (including the plunger) to about 1/3 of their pinch off value.
4. Form a single large dot with the outer tunnel barriers of the triple dot in transport, typically a wall - wall scan is enough. If that does not work, most likely one of the inner tunnel barriers or a gate is unusually strongly coupled to the wall and pinches off before a dot can form, in this case we just leave the walls at about 0.1 e^2/h and ramp all of the inner gates simultaneously and look for Coulomb oscillations. It may take some offset between the gates until it forms really one dot. Once the right setting for the inner gates is found, we go back to balance the outer tunnel barriers and park on top of a coulomb peak.
5. Once we can see regular Coulomb oscillations through the large single dot, we switch to charge sensing (in transport through the sensor dot). It may take some iterations between sensor dot and triple dot to get them both tuned up to nice dots, since they couple relatively strongly.
6. Now we switch the bias across the triple dot off and deplete it with the plunger gates. Once the transitions start latching, we lower the outer tunnel barriers and deplete more. Eventually multi dot features appear. At one point there should be a line which can clearly be identified as the middle dot transition, as shown in figure 3.1 (c). Using the middle dot transition, the inter-dot tunnel barriers can be balanced.
7. If no clear middle dot transition shows up, the middle dot is normally too depleted, so we make the middle plunger less negative.
8. We continue to deplete while opening the outer and inner tunnel barriers until the dot is completely empty. Using the middle plunger, the middle dot transition can be moved until it forms the "house" like structure, shown in 3.1 which is characteristic of a triple dot. Note that in the strong coupling regime, the "house" may have a "flat roof", which means that there is a direct transition from (111) to (202), not into 211 or 112 (see [20]).

To follow this recipe we need transport through the device. At the same time, it is not a good idea to keep all of the other gates completely off when tuning up a particular triple dot, because eventually we want to turn them on of course and then this may make the found voltages for that dot quite far off. Therefore while tuning up, say, qubit 1 (qubit as in a triple dot, numbered on the device from left to right) we kept the gates

of qubit 2 and qubit 3 at the point where they just start to deplete. This way, it was possible to tune up qubit 1 and qubit 3 following the recipe above, as shown in figures 5.3 and 5.4. Pannel a) on both figures shows a SEM image of the device measured with colors indicating the state of the device. Blue gates are "in qubit mode" so at voltages which allow for low occupation triple dots, purple gates are the "just depleting" regime. The gates in red are scanned, giving the graph on the right in panel b). This is the differentiated conductance measurement through the sensing dot above the triple dot. Both, qubit 1 and qubit 3 show the characteristic house of a triple dot. They are not perfectly balanced qubit 3 is too large for doing actual qubit . However these are fine adjustments are typically done when measuring with reflectometry, since they need many iterations. The higher bandwidth and the better signal to noise of reflectometry allow us to take an image like figure 3.1 b) in about 20s, while figure 5.3 b) took about 15 minutes. The downside of reflectometry is that it itself needs more fine-tuning on the side of the sensor dot, so in our experience it is hard to make it work over triple dot plunger-voltage intervals exceeding 100 mV.
In this configuration, it was however not possible to tune up qubit 2. Surprisingly, it did not even show Coulomb oscillations in transport. When switching the other qubits off, the Coulomb oscillations came back almost instantly and it was possible to tune it into the triple dot regime, as shown in figure 5.4.

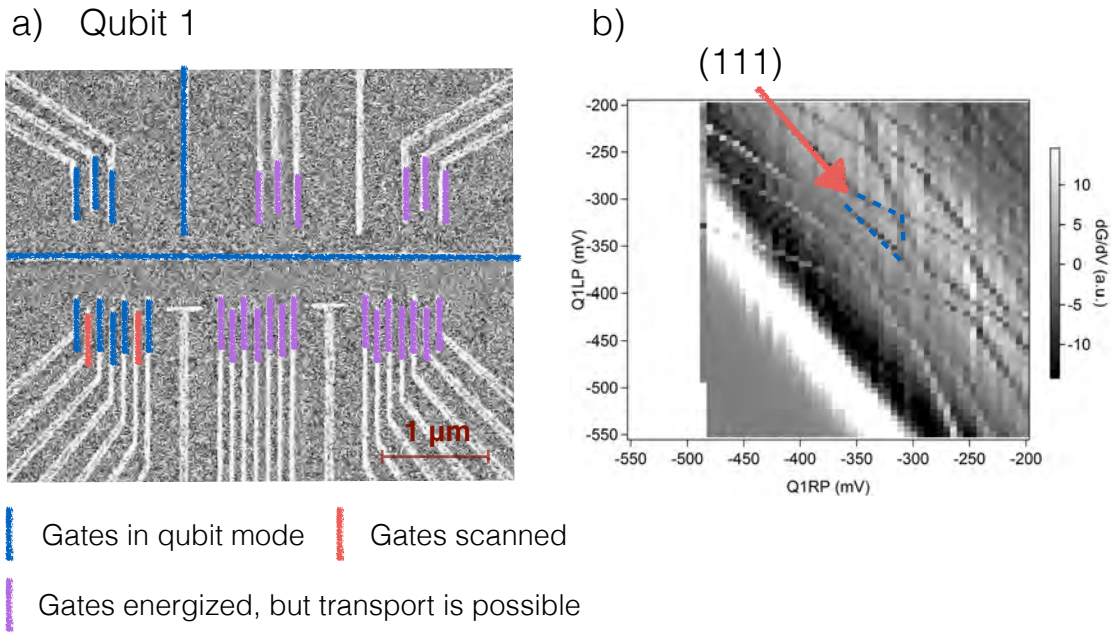


Figure 5.3: Signature of a triple dot in qubit 1. (a): The plungers of qubit 1 are scanned with the gates of the other qubits energized such that they just start to deplete. This way transport is still possible and the gates are not too different from their voltages when forming a triple dot later on. (b): The differential conductance through the sensing dot shows the (111) triple dot region.

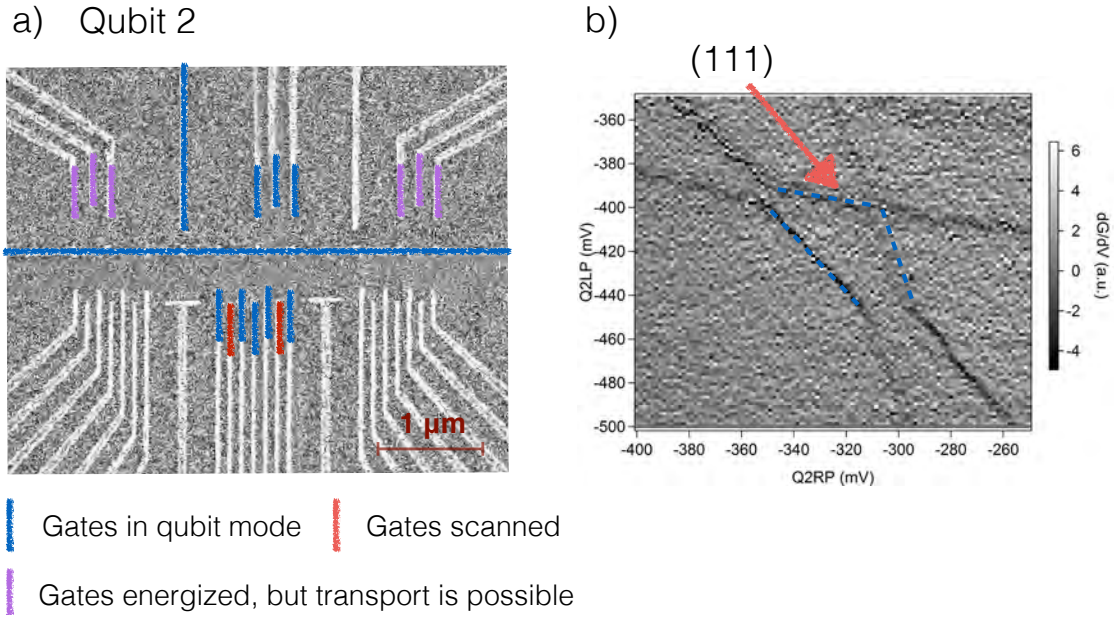


Figure 5.4: Signature of a triple dot in qubit 2. (a): The plungers of qubit 2 are scanned with the gates of the other qubits kept at 0 mV. It was not possible to form a triple dot with the other gates energized. (b): The differential conductance through the sensing dot shows the (111) triple dot region.

5.2.3 Two triple dots

After successfully forming a triple dot in qubit 2, we slowly energized the gates on qubit 1 and qubit 3 while monitoring and readjusting qubit 2. Qubit 1 formed a triple dot with almost the same values found when tuning it up individually, proving our strategy for simultaneous tuning with "just depleting" gates to be effective. This way, we succeeded in forming two simultaneous triple dots in this device, as shown in figure 5.6. It was however not possible to form a sensitive sensing dot or QPC in qubit 3. While tuning qubit 3 we saw drifts on qubit 2 and after about 6 hours there were no more signatures of any kind of quantum dot in qubit 2, regardless of the setting of qubit 3. We experienced those types of drifts in other tuning stages of in this device as well. Gates would become stronger by hundreds of mV over the course of 10s of hours. The effects could always be reversed by fully opening up qubit 1 and 3 and strongly depleting qubit 2. This leads to the suspicion that it has to do with the large electron reservoir between the qubits. Other than on the sides, there are no ohmics, so the 2DEG trapped could effectively form a large metallic object floating up and down.

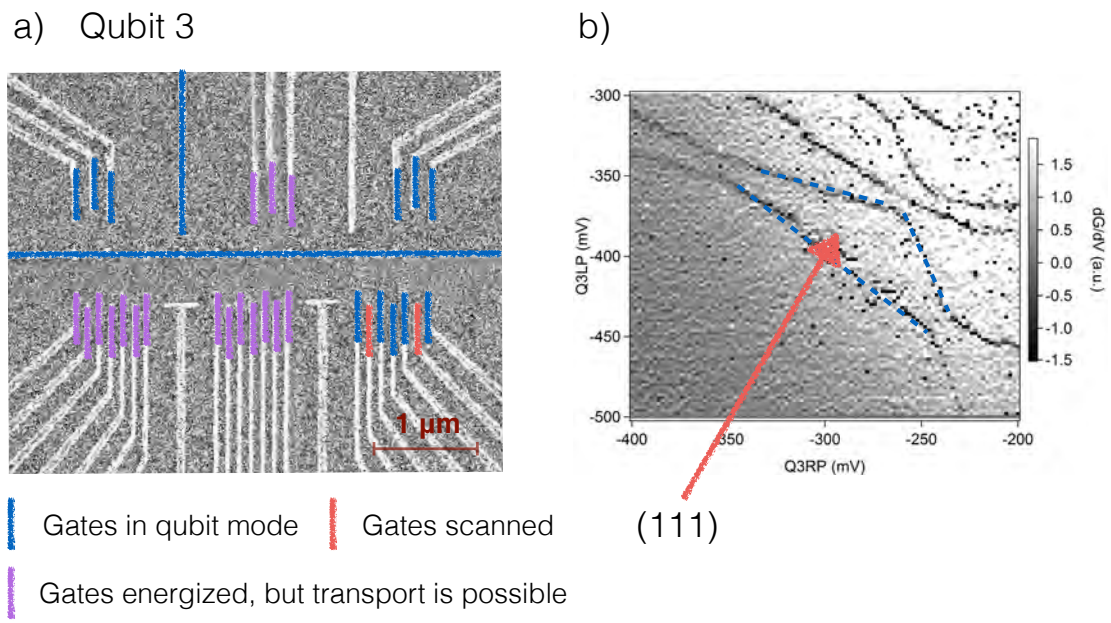


Figure 5.5: Signature of a triple dot in qubit 3. (a): The plungers of qubit 3 are scanned with the gates of the other qubits energized such that they just start to deplete. This way transport is still possible and the gates are not too different from their voltages when forming a triple dot later on (b): The differential conductance through the sensing dot shows the (111) triple dot region.

5.2.4 Challenges and possible solutions

Additionally to the drifts we also saw hysteresis and strong jumping in some gates and (as expected) there was strong cross coupling between gates of adjacent qubits. Figure 6.1 shows for example the cross coupling between the closest dots of qubits 1 and 2. The signal is the differential conductance through the sensor dot of qubit 1. Panel (a) shows the triple dot in qubit 1. When scanning the right plunger of the qubit 1 vs. the left plunger of qubit 2 we can follow the two transitions in qubit 1 (indicated by the red arrows) as we change the plunger on qubit 2. The cross coupling was measured to be $\approx 1/7$. In normal qubit operation the gates would be ramped by up to 20 mV, at the same time we need them to be precise within 0.5 mV, so this cross talk would have to be dealt with.

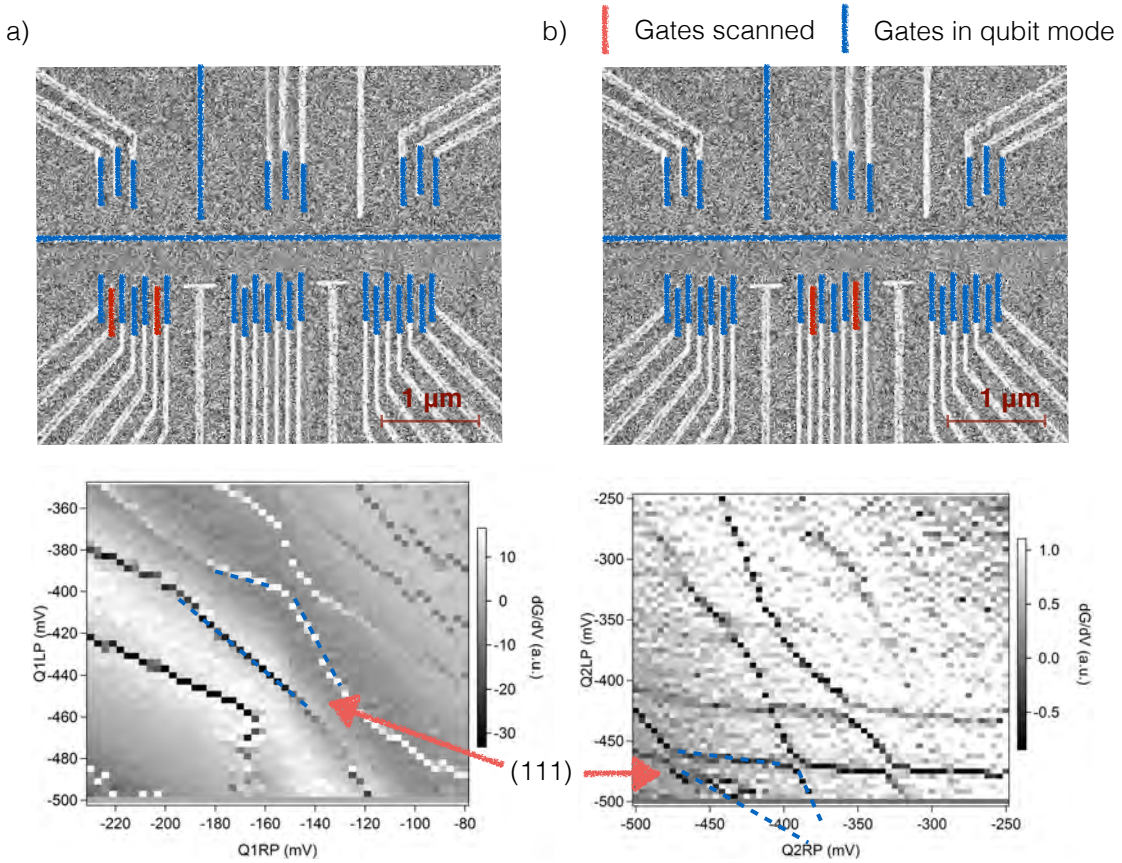


Figure 5.6: Two triple dots tuned up simultaneously. (a) Qubit 1 is scanned while all of the other gate voltages are in regimes forming qubits or sensing dots. The differential conductance through the sensing dot shows a (111) like region. Since there is latching on the bottom left of the plot, it is probably not in the single electron regime. This is in practice not a problem. (a) The same as qubit 1, in qubit 2. Taken right after the scan in a).

Chapter 6

Conclusion: Key challenges and possible solutons

Key challenges for this multi qubit architecture have been identified to be :

1. Hysteresis and jumping in the gates

2. Slow drifts

3. Cross coupling

The hysteresis + jumping issue seems to have appeared with the bias cooling. So there is a good change that this could go away by optimizing the bias cooling voltage, so no changes to the device would have to be made here. Collaborators using the same material did not report such behavior and they used +50 mV bias, which is encouraging. The drifts which most likely come from the electron puddle can be stopped by adding ohmic contacts in between the triple dots. In order to save DC wires, those could in principle be grounded on chip as well. Those first two isses are very specific to this particular design and experiment. The last point is a problem all qubits in semiconductor quantum dots. As shown in section 5.1, the fabrication of a "screening gate" can significantly reduce cross coupling. A summary of the proposed device changes is shown in figure 6.2.

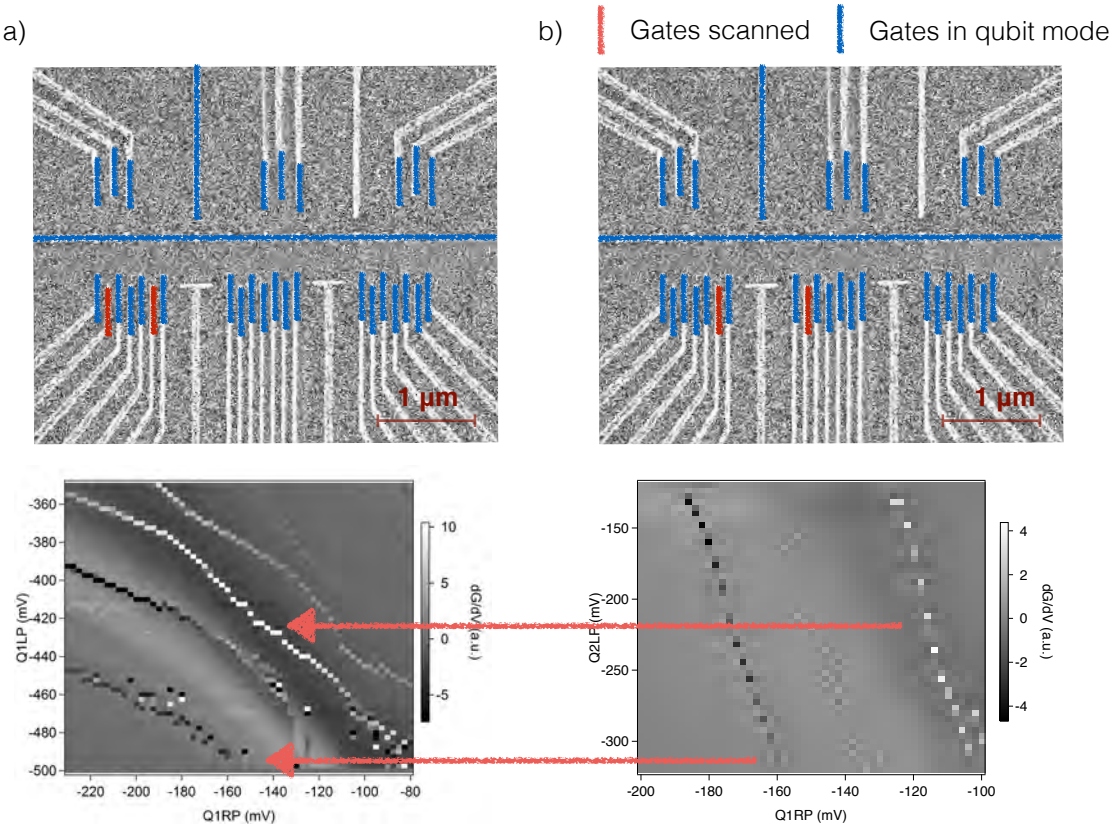


Figure 6.1: Measuring the effective cross coupling on qubit 1 from qubit 2. (a) Triple dot in qubit 1 while the left plunger on qubit 2 is at -320 mV, the bottom of the plot in b) The signal in the plot is the differential conductance through the sensor dot above qubit 1. (b) Differential conductance through the sensor of qubit 1 while scaning the right plunger of qubit 1 vs. the left plunger of qubit 2. The two transitions indicated by the red arrow can be used as a reference to measure the cross coupling: Q2LP/Q1RP $\approx$ 1/7.

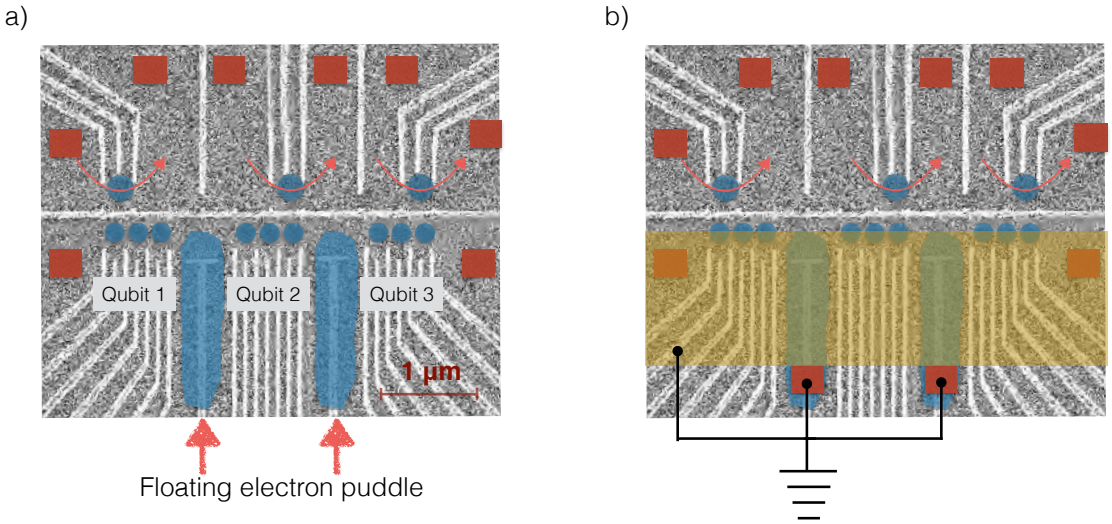


Figure 6.2: An illustration of challenges with the device and possible solutions. (a) When the coupling dot gates are not energized (other than in figure 4.2) a large puddle of 2DEG forms in between the qubits. Since there are no ohmics, it is electrically floating, potentially slowly changing its potential and thus making tuning hard. (b) Proposed changes to the design. Ohmic contacts are added to fix the potential on the electron puddles. A screening gate is added to reduce cross coupling, as shown in section 5.1

.

Appendix A

Cooled down devices

Before the working device JB_TT14 was cooled down there were several failures, their fate shall be remembered in table **??**. A common failure mode were lithographic problems. It used to be a no-go to image devices before measuring, due to concerns about implanted charge traps from the electron beam of the SEM making the material more noise. At the time of the writing of this thesis I have not heard of any evidence for this to happen. As long as there is no evidence, I suggest everyone making such large devices to image before measurement, because a single bad gate can make the entire device unusable.

Device	Type	Material	Bias Cool	Fate
JM_19_2b	single triple dot	Gossard, 110nm	+300mV	triple dot formed
JB_PT1_16	15 in a row	M6-14-13.1	+200mV	all gates not working
JB_PT1_25	15 in a row	M6-14-13.1	no	ohmics not working
JB_PT1_40	15 in a row	M8-30-13.1b	no	some gates broken
JB_TTL_1	triple triple gen 1	M8-30-13.1b	no	some gates broken
JB_TTL_2	triple triple gen 1	M8-30-13.1b	no	some gates broken
JB_TTL_7	triple triple gen 2	M8-30-13.1b	no	backbone broken
JB_TTL_8	triple triple gen 2	M8-30-13.1b	no	backbone broken
JB_TTL_11	triple triple gen 2	M8-30-13.1b	no	bad dimensions
JB_TTL_14	triple triple gen 3	M8-30-13.1b	no	noisy, hysteretic
JB_TTL_14	triple triple gen 3	M8-30-13.1b	+200mV	triple dots formed

Table A.1

Appendix B

Bonding

The deive was bonded to the PC board sample holder using a wedge bonder. Figure B.1 shows the bonding diagramm used to bond JB TTL14. I recmomend everyone bonding large devies to have bonding diagramm and spend some time on thinking exactly how to bond. The graphic representing the device should be drawn to scale. The constraints are:

1. Readout lines as short as possible to reduce stray capacitance. So they should be on the bottom
2. Fast lines as short as possible.
3. A few ninja-bonds [1] as possible.

[1] technical term for more than two bonds crossing

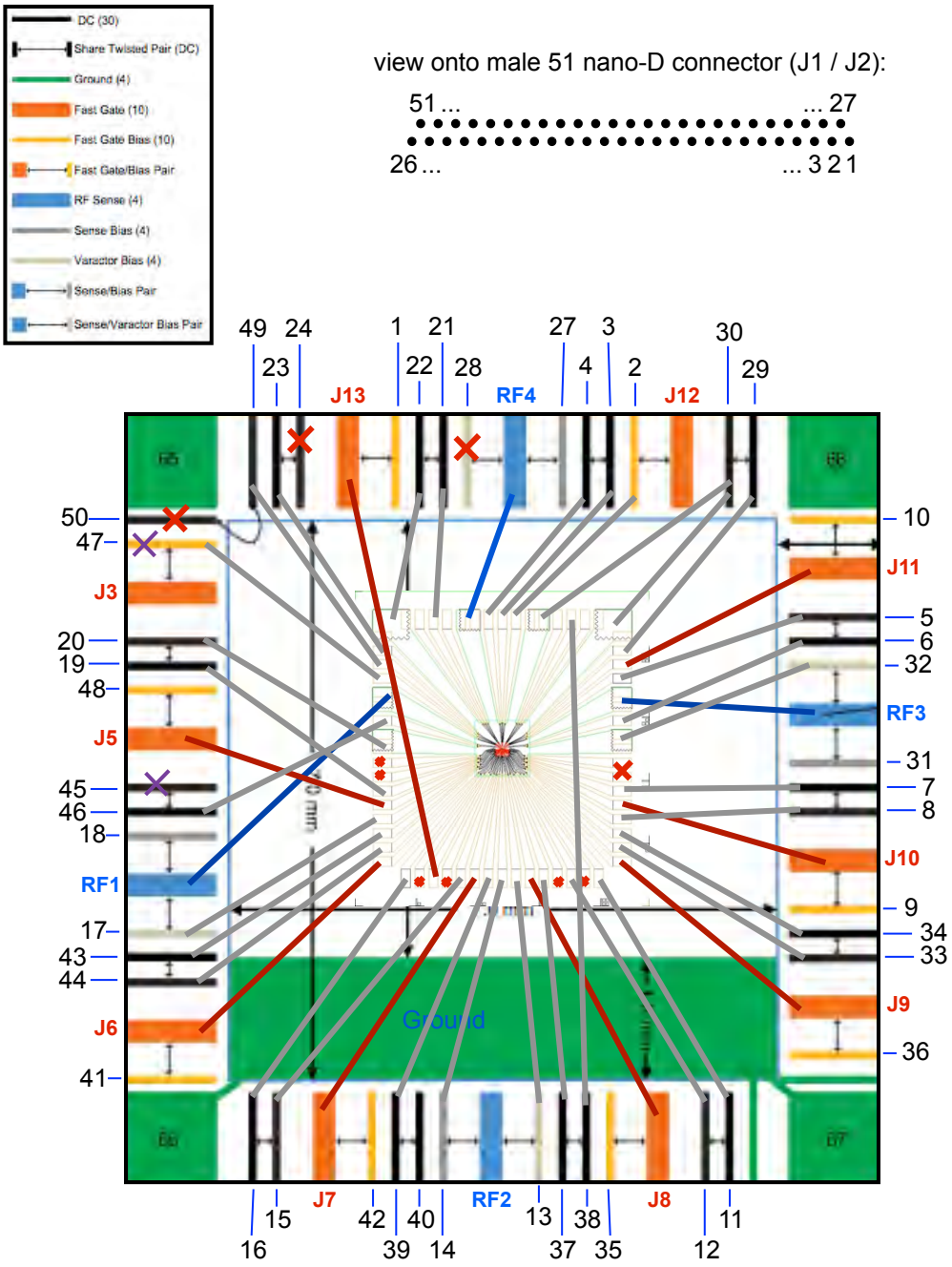


Figure B.1: Bonding diagramm of the device JB_TTL14. Red wires are fast gates. Blue are readout lines. Black are the DC lines.

Appendix C

Nanofabrication

This chapter contains the fabrication recipe developed for the multi triple dot devices with and without a screening gate. It also contains images of all the CAD files. To keep the chapter usable as a recipe, all images are at the end. . In the end of the chapter I give some hints on troubleshooting fabrication failures. The starting point was the recipe of Jim Medford which he used to fabricate JB19-2b (amongst many other decvices) in the Harvard CNS cleanroom. A decice which we also measured on in Copenhagen. However, the change in fabrication environment with different equipment etc. as well as the considerably larger devices we fabricated lead to major changes and improvements to this recipe. The most significant change was to use photo lithography now only for the mesa etch step and replace it with E-beam lithography for the rest. This made the process more flexible, since in photo-lithography, for every alteration of the pattern, one needs to have a new mask manufactured, which can have up to weeks of lead time. A common reason to use photo-lithography (besides the lack of easy access to ebeam lithography) is that it is much faster for large areas. For our patterns, however, this was not the case, since we commonly only expose a maximum of eight patterns at a time, which can be exposed in under one hour using high beam currents on the Elionix. In this case, the faster alignment and the shorter liftoff time of ebeam resist (3 - 4 hours vs. up to 12 hours) shortened the process from about 14 hours to under 8 hours.

Overview

The fabrication consists of the following steps:

1. Cleave chip
2. Mesa pattern
3. Mesa etch
4. Ohmics pattern
5. Ohmics deposition

6. Ohmics anneal
7. Fine gates pattern
8. Fine gates deposit
9. Outer gates pattern
10. Outer gates deposit

In case of the "screening gate" there are additional steps:

11. Atomic layer deposition (ALD) of HfO_2
12. Screening gate pattern
13. Screening gate deposit
14. Screening gate connector pattern
15. Screening gate connector deposit

C.1 Cleave chip

We used chips with 6 or 8 devices (2×3 or 4 array) which meant that we cleaved chips to about 8×13 or 8×15 mm. I recomend not to leave less than 500 μm to the edge of the chip when having that many fabrication steps because it is almost inevitable to damage the side of the chip a little bit. I would not use much larger chips for this kind of fabrication, because it gets hard to hold it in the tweezers and the chance of breaking it in the mask aligner increases. I also do not recomend to fabricate on chips smaller than 5×5 mm if it can be avoided. In general squared chips should be avoided since it may make it hard see the orientation. Also, note that for some materials, front and back side look the same. After cleaving a piece from the waver it may be impossible to tell and the chip can easily be flipped during fabrication, so if this is the case, make sure to mark a side with a little scratch on an edge.

C.2 Mesa pattern

In order to electrically isolate the different devices on a chip and to reduce parasitic capacitance, unnecessary 2DEG around the devices is etched away. A typical pattern is shown in figure C.2. The islands in the middle with the arms extending towards the top are what is going to be left of the 2DEG. The etch rate of the acid bath is quite different every time it is prepared. In order to determine the etch bath, we prepare a second chip on "practice material"(pure GaAs, without a heterostrcuture) which also gets mesa patterned. This is also a good way to practice with the mask aligner again right before using it on the precious real material. The practice chips gets then etched

for 60s and the effect measured via the profilometer to calculate the etch rate. For the real chip we aim for the depth of the 2DEG. In principle it is better to over etch than under etch. Under etch would mean, not even etching the donor layer away, in this case the mesa patterning would not have the desired effect. As fare as the device is concerned it is hard to over etch, however later the outer connection layer has to be high enough to climb over the mesa. Aside from wasting gold, a too high metal stack may not lift off anymore with the resist thickness used in this recipe. This puts the bound for over etching to about 200nm.

1. 3 Solvent clean
   (a) Sonicate in Trichloroethylene (TCE) 5min.
   (b) Sonicate in Acetone 5 min.
   (c) Sonicate in Isopropyl Alchohol (IPA) 5 min.
   (d) Blow dry with N_2.
2. Place chip on a 185 ° C hotplate for however long it takes you to get the resist ready.
3. Place the chip on a glass slide and cover it with a plastic cup for 15 s to let it cool down.
4. Spin Shipley S1813 photoresist :
   (a) 10s, 500 rpm
   (b) 60s 4000 rpm
   (c) Sometimes during spinning, some resist gets on the bottom of the chip. Therefore squirt some acetone on a cleanroom wipe. Carefully move the bottom of the chip across the wetted cleanroom wipe to clean the bottom of the chip.
   (d) Bake 115 ° C, 2 min
5. Expose in the mask aligner. The time has to be determined by dosetest. I used 12 seconds. But do not rely on it, since the lamp may have been changed etc.
6. Develope:
   (a) 60s DC-26
   (b) 20s rinse in micro-pore water
   (c) Blow dry with N_2.
7. O_2 plasma clean. I used the old “microwave oven” plasma cleaner in the QDev cleanroom at the standard setup at 65W for 20s, which means about 17s of plasma etch due to the delay until the plasma ignites.

C.3 Mesa etch

Since this can not be said often enough: **Acids are dangerous! Do not perform this step without begin properly trained.**

1. Prepare etch bath H_2SO_4:H_2O_2:H_2 2:16:480 mL. Stir thoroughly. We typically use a magnetic stirrer for 20 minutes.
2. Etch practice chip for 60 s
3. Sonicate in acetone for 5 min
4. Sonicate in IPA for 2 min
5. Blow dry with N_2.
6. Measure the etch rate with the profilometer.
7. Etch the real chip. Aim for the depth of the 2DEG.
8. Sonicate in acetone for 5 min
9. Sonicate in IPA for 2 min
10. Blow dry with N_2.
11. Clean in warm (55 ° C) acetone or hot (70 ° C) NMP for ¿ 2hours in a closed beaker. Be careful with the warm aceone, since it is very flamable. Use NMP if possible.
12. Measure the etch rate with the profilometer.
13. Rinse with IPA
14. Blow dry with N_2.

C.4 Ohmic pattern

The ohmic patterns for the devices used is shown in figure C.3. The ohmic pattern also includes the alignment marks which will later be used to align the ebeam layer relative to each other.

1. 3 Solvent clean
   (a) Sonicate in Trichloroethylene (TCE) 5min.
   (b) Sonicate in Acetone 5 min.
   (c) Sonicate in Isopropyl Alchohol (IPA) 5 min.
   (d) Blow dry with N_2.

2. Place chip on a 185 deg hotplate for however long it takes you to get the resist ready.

3. Place the chip on a glass slide and cover it with a plastic cup for 15 s to let it cool it down.

4. Spin El-9 Copolymere :

   (a) 10 s, 500 rpm

   (b) 60s 4000 rpm

   (c) Sometimes during spinning, some resist gets on the bottom of the chip. Therefore squirt some acetone on a cleanroom wipe. Carefully move the bottom of the chip across the wetted cleanroom wipe to clean the bottom of the chip.

   (d) Bake at 185 ° C, 3 min

   (e) Spin PMMA4 ebeam resist :

   (f) 10s, 500 rpm

   (g) 60s 4000 rpm

   (h) Clean the bottom of the chip.

   (i) Bake at 185 ° C, 3 min

5. Inspect the chip under an optical microscope. Make sure there are no pieces of dust/hairs/fibres in essential places on the cip. Also measure the distance from the left and the bottom edges to the lower left alignment marks and note them, such that you can find them again easily with the Elionix.

6. Load in the Elionix, condition the beam, align and expose with parameters determined by a dose test. We used 40 nA beam current, 250 μm aperture. I always used two point alignment.

7. Develop:

   (a) 90s MIBK:IPA 1:3

   (b) 20s IPA

   (c) Blow dry with N_2.

8. O_2 plasma clean. I used the old "microwave oven" plasma cleaner in the QDev cleanroom at the standard setup at 65W for 10s, which means about 7s of plasma etch due to the delay until the plasma ignites. This should etch about 5nm of PMMA.

C.5 Ohmic deposition

In our and our collaborators' experience, this special low density "spin qubit" material seemed to be a bit harder to contact than usual GaAs materials. We managed to fabricate low resistance Ohmics (hundreds of Ohms) very reliably using the recipe described below which is based on a recipe found by Xanthe Croot, from University of Sydney. In older fabrication recipes for GaAs, at this step one will find the suggestion to remove the native oxide from the surface of the waver in order to get low resistance ohmic contact to the 2DEG. In the course of the thesis we found out that, at least for all the materials used during that time in the lab, this is in fact not necessary.

For all ohmic deposition I used the "Edwards" thermal evaporator.

1. Load metals in the thermal evaporator using Tungsten boats. The one used had space for four metals, so: Au, Ge, Ni, Ni. The Ni part is a bit tricky in thermal evaporators, because the Ni reacts strongly with the W boat. If too much Ni is put in the boat, it will burn through the boat. Therefore I used only an about 2 mm long piece of Ni wire. Since this is not enough for the two layers of Ni in the recipe, I loaded two of those boats.
2. Clean the vacuum seals of the evaporator carefully.
3. Make sure you know which metal is where and that the sample is correctly oriented.
4. Pump down. Degas metals.
5. Evaporate:
   (a) 5 nm of Ni
   (b) 35 nm of Ge
   (c) 72nm of Au
   (d) 18nm of Ni
   (e) 50nm of Au.
6. Clean in warm (55 ° C) acetone or hot (70 ° C) NMP for ¿ 2hours in a closed beaker. Be careful with the warm aceone, since it is very flamable. Use NMP if possible.

C.6 Ohmics anneal

The anneal recipe is also saved in the rapid thermal annealer (RTA) in the QDev cleanroom as "JB420". We found that, compared to recies developed in the Harvard cleanroom, we needed to use much (80 ° C) lower temperatures to get low resistance Ohmics. Since those lower temperatures are comparable to the ones used successfully by all our collaborators, we suspect that the temperature sensor on the RTA used in the Harvard

CNS cleanroom is off by roughly that amount. So be careful when using recipes from older thesis.

The RTA sample holder should only be opened in the cleanroom, so take it into the cleanroom to open it and load the sample. The anneal process is given in table C.1. :

Step	Function	Time (s)	Temp degC	N_2 (sccm)	Forming gas (sccm)
1	delay	20	0	5000	0
2	delay	20	0	0	5000
3	ramp	20	120	0	2000
4	steady	60	120	0	2000
5	ramp	20	250	0	2000
6	steady	60	250	0	2000
7	ramp	30	420	0	2000
8	steady	120	420	0	2000
9	delay	500	0	0	2000
10	delay	30	0	5000	0

Table C.1: The anneal recipe used in the QDev cleanroom RTA. The actual annealing step is 8. The first parameters to change when optimizing the recipe for a different material are time and temperature of step 8.

C.7 Fine gates pattern

This is the most crucial step in the process since it defines the depletion gates, which will later form the confining potentials for the dots. There are two ebeam sessions writing three patterns. The entire pattern written in this step is shown in figure C.5. In the first session, the finest features are written in a 150 μm write-field with 100 pA. In the second session the connection is made to the edge of the mesa in a 600 μm write-field with 2 nA. This gives a good balance between the needed resolution and writing time. The inner pattern is broken down again into two patterns, an inner and an outer pattern. The idea is that this way, all of the depletion gates defining the device are written within a very short time, making the process less sensitive to stage drifts. In our experience, the result for those fine features does not only depend on the total dose and the aperture. So it does make a difference whether one uses 100pA or 500pA with 1/5 of the dwell time, so make sure you use exactly the same parameters you determined to be optimal with the dose test. For the patterns presented in this thesis it was found to be not necessary to burn spots to optimize focus and stigmatization, using the hight sensor is sufficient. This recipe also uses cold development. It may not be strictly necessary for the resolution needed, but it makes the process definitely more controlled.

1. 3 Solvent clean

(a) Sonicate in Trichloroethylene (TCE) 5min.

(b) Sonicate in Acetone 5 min.

(c) Sonicate in Isopropyl Alchohol (IPA) 5 min.

(d) Blow dry with N_2.

2. Place chip on a 185 deg hotplate for however long it takes you to get the resist ready.

3. Place the chip on a glass slide and cover it with a plastic cup for about 15 s to let it cool it down.

4. Spin PMMA4 ebeam resist :

   (a) 10s, 500 rpm

   (b) 60s 4000 rpm

   (c) Clean the bottom of the chip.

   (d) Bake at 185 ° C, 3 min

5. Inspect the chip under an optical microscope. Make sure there are no pieces of dust/hairs/fibers in essential places on the cip. Also measure the distance from the left and the bottom edges to the lower left alignment marks and note them, such that it is easy to find them again with the Elionix.

6. Load in the Elionix, align and expose with a dwell time determined by a dose test. Use the height sensor. Our parameters; 150 μm write-field, 100 pA beam current, 60k Dots, 1.5 μs /dot, 40μm aperture. 600 μm write-field, 2nA beam current, 60kDots, 0.6 μs / dot, 60 40μm aperture.

7. (Cold)Develop:

   (a) Put a glass beaker with MIBK:IPA 1:3 into the cooling station, put to 0 ° C. Allow for at least 15 minutes to cool down. Also, since the bottom of the cooling block does not make perfect contact with the glass beaker, put some Aceone inside before inserting it.

   (b) Develop 90s in cold MIBK:IPA 1:3

   (c) 20s room temperature IPA

   (d) Blow dry with N_2.

8. Inspect under an optical microscope. The etched out trenches should be clearly visible. Make sure no dust/hairs/fibers are anywhere on the mesa.

C.8 Fine gates deposition

1. Fix the sample onto the AJA sample holder with carbon tape and load the sample into the AJA.
2. Evaporate 5nm Ti, 15 nm Au with a low rate 0.05 nm/s.
3. Lift off in acetone >5 hours. Wet observe it under a optical microscope before taking it fully out of the acetone. It will normally not lift off by itself, so use a pipette to squirt acetone onto the chip while it is still in the acetone. In my experience using a syringe is too violent for the fine gates and can destroy them. Sonication is also definitely too agressive in general. In emergencies try in steps of 5 seconds (sonicate for 5 second, wet observe, if not good sonicate again for 5 seconds) with the sample in a plastic cup and using the net in the sonicator or holding it in your hand, such that the beaker does not touch the walls of the sonicator. This way I have successfully sonicated for 20 seconds without destroying the fine gates. However, only 5 seconds have destroyed fine gates before, so use this only as a last resort.
4. Flush with IPA, blowdry with N_2

C.9 Outer gates pattern

The outer gates are significantly thicker than the fine gates, because they have to climb over the mesa and they are going to connect the device to the bond pads. As mentioned in the mesa etch section, the thickness of the resist stack gives an upper bound for the height of the outer gates and thus how deep one should etch the mesa. Having said that, there is no reason to not just spin another layer of resist on order to be able to evaporate more gold. Just do a dose-test for the triple layer. Our design for the outer layers is shown in figure C.6.

1. 3 Solvent clean **No sonication !**
   (a) TCE bath 5min.
   (b) Acetone bath 5 min.
   (c) IPA bath 5 min.
   (d) Blow dry with N_2.
2. Spin El-9 Copolymere :
   (a) 10s, 500 rpm
   (b) 60s 4000 rpm
   (c) Clean the bottom of the chip.

(d) Bake at 185 ° C, 3 min

(e) Spin PMMA4 ebeam resist :

(f) 10s, 500 rpm

(g) 60s 4000 rpm

(h) Clean the bottom of the chip.

(i) Bake at 185 ° C , 3 min

3. Inspect under the optical microscope for dirt on the resist.

4. Load in the Elionix, condition the beam, align and expose with parameters determined by a dose test. We used 40 nA beam current, 250 μm aperture. I always used two point alignment.

5. Develop:

   (a) 90s MIBK:IPA 1:3

   (b) 20s IPA

   (c) Blow dry with N_2.

C.10 Outer gates deposition

1. Load the sample in the AJA ebeam evaporator.

2. Evaporate 5nm Ti and 1.2 $\times$ mesa hight of Au. Here the rate can be higher, since the features are big and it would take forever otherwise; I typically used 0.2 nm/s.

3. Lift off in warm acetone or hot NMP >3 hours. Wet-observe under a optical microscope before taking it our of the solvent.

4. Flush with IPA, blowdry with N_2.

5. Done! Unless you want screening gates.

C.11 ALD of HfO_2

This ALD recipe is based on the one described by Angela Kou in her PhD thesis. We do not pattern and lift off the ALD for all the designs here but the recipe should also work for that. I used QDev ALD machine from Cambridge Nanotech. It uses a precursor of tetrakis(ethylmethylamino)hafnium and water to deposit HfO_2. Note that the ALD really covers every surface inside the chamber.

1. 3 Solvent clean **No sonication !**

   (a) TCE bath 5min.

(b) Acetone bath 5 min.

(c) IPA bath 5 min.

(d) Blow dry with N_2.

2. Glue chip to a coverslip, bottom of the chip down:

   (a) Spin PMMA8 or some other thick ebeam resist onto a coverslip. Exact rpm etc. not important.

   (b) Place the chip on the cover-slip and bake the sandwich at 185 ° C for a couple of minutes.

   (c) Optically inspect the iterface between chip and coverslip. Make sure that the entire bottom of the chip is well covered by resist.

3. Load the chip into the ALD and run the "HfO2130C"recipe, which deposits 30 nm of ALD in 400 cycles. This takes about 10 hours.

4. Place the coverslip-chip sandwich in warm acetone or hot NMP. Wait until the coverslip falls off. Take out the coverslip and leave the chip in the solvent for 1 hour to get all of the acetone off.

5. The chip should now look light brown-ish.

C.12 Screening gate pattern

Use almost the same recipe as for the fine gates, just no sonication.

1. 3 Solvent clean **No sonication !**

   (a) TCE bath 5min.

   (b) Acetone bath 5 min.

   (c) IPA bath 5 min.

   (d) Blow dry with N_2.

2. Place chip on a 185 ° C hotplate for however long it takes you to get the resist ready.

3. Place the chip on a glass slide and cover it with a plastic cup for 15 s to let it cool it down.

4. Spin PMMA4 ebeam resist :

   (a) 10 s, 500 rpm

   (b) 60s 4000 rpm

   (c) Clean the bottom of the chip.

(d) Bake at 185 ° C, 3 min

5. Inspect the chip under an optical microscope.
6. Load in the Elionix, align and expose. Use similar settings as for the inner fine features, however a higher beam current, for example 500 pA is not a problem here. Make sure to get good alignment.
7. (Cold)Develop:
   (a) 90s in cold MIBK:IPA 1:3
   (b) 20s room temperature IPA
   (c) Blow dry with N_2.
8. Inspect under an optical microscope.

C.13 Screening gates deposition

1. Load the sample in the AJA ebeam evaporator.
2. Evaporate 5nm Ti and 2 × height of the fine gates of Au, so 30 nm, with a low rate.
3. Lift off in room temperatures acetone >5 hours. Wet-observe under an optical microscope before taking it our of the solvent.
4. Flush with IPA, blowdry with N_2.

C.14 Outer gates connector pattern

Same as outer gates pattern.

1. 3 solvent clean, **No sonication !**
2. Spin PMMA4/EL9 bilayer
3. Expose in the Elionix with 40 nA.
4. Develop 90s MIBK:IPA 1:3, 20s IPA
5. Blow dry with N_2.

C.15 Outer gates connector deposition

Same as outer gates deposition.

1. Evaporate 5nm Ti, 1.2 × mesa-height of Au in the AJA.
2. Lift off in warm acetone or hot NMP.

C.16 Notes on fabrication problems and failures

First it should be noted that none of the processes above pushes the boundaries of what is possible with the equipment in the QDev cleanroom. That means, should you try to fabricate devies with similar gate dimensions and encounter failure, it is most likely a simple mistake and not an optimization problem of the recipe. So the first step in troubleshooting should be to just redo it and see if the issue persists. Here a list of problems we encountered and how they got fixed:

1. Fine features do not come out reliably. Symptoms look like overdose and underdose. → Expired PMMA. → Get new PMMA.

2. Bad liftoff → That unfortunately happens randomly sometimes. Just do it again.

3. Thermal evaporator boat blows up while evaporating nickel. → Boat reacts with nickel, increases resistance and heats up too much. → Use less nickel.

4. Bilayer does not lift off. Only after sonication and other rough treatment. → El9 contaminated. → Use new El9.

5. All doses in the Elionix are suddenly off. → Can be because the zero setting of the Faraday-cup has been (hopefully) accidentally changed. → Check the setting together with cleanroom staff.

6. Registration in the Elionix does not converge. → This happened once because the chip was too rotated. → Adjust the chip position in the Elionix sample holder. This is much faster than actually trying to make the registration converge. As a rule of thumb, if you see that your chip is more than 3 mrad tilted, take it out and fix that, since that will save a lot of time in registration.

7. Elionix height sensor goes crazy. → This can happen if the chip is too close to the clamp, in which case the laser may be irritated by it.

8. Chip breaks in the mask aligner. → A major cause of this are edge beats which make the chip uneven and then cause tension as it gets pressed against the mask. One way to reduce the risk for that is to first expose and develop the edges and then go for the actual patterning.

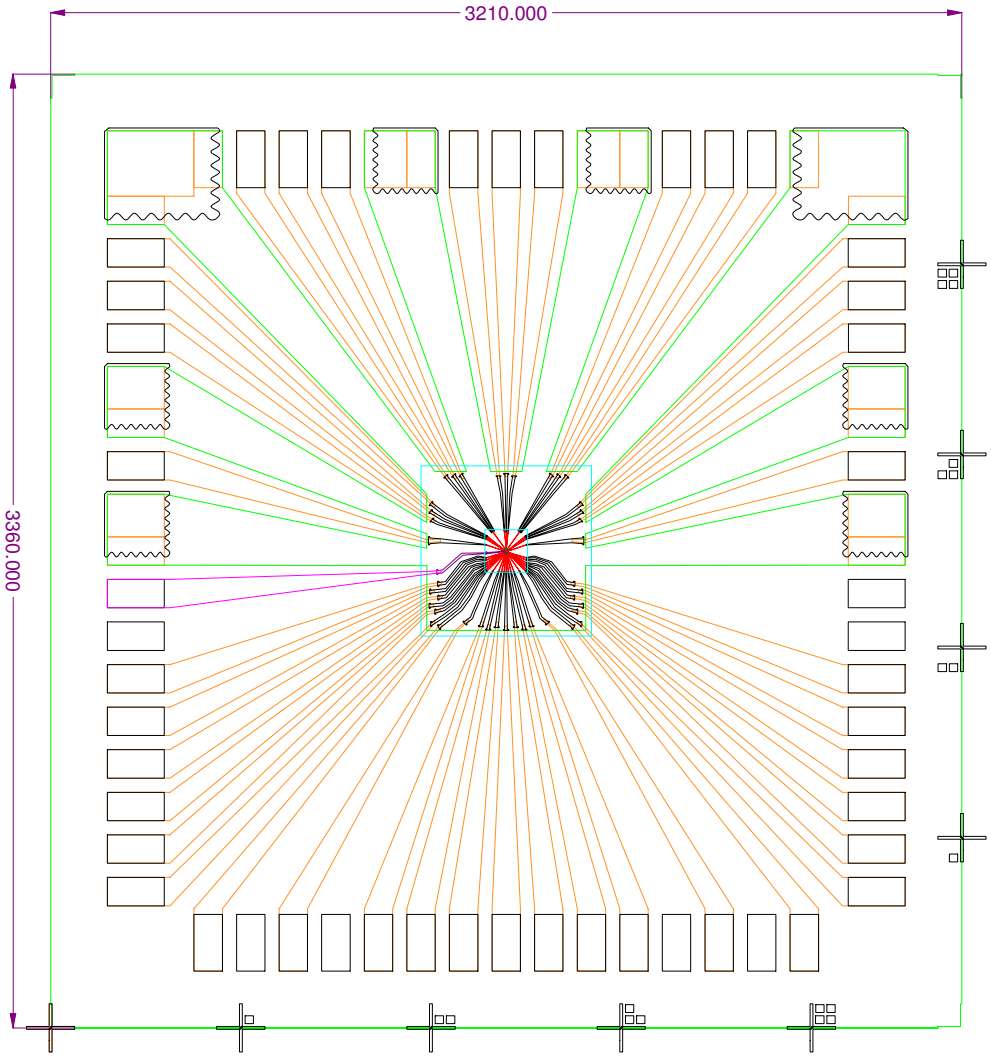


Figure C.1: Patterns for the entire fabrication process of one device including screening gate. Light green: Mesa, black rectangles outside: Ohmics, green/red/back: Fine gates, orange: Outer gates, Purple: Screening gate.

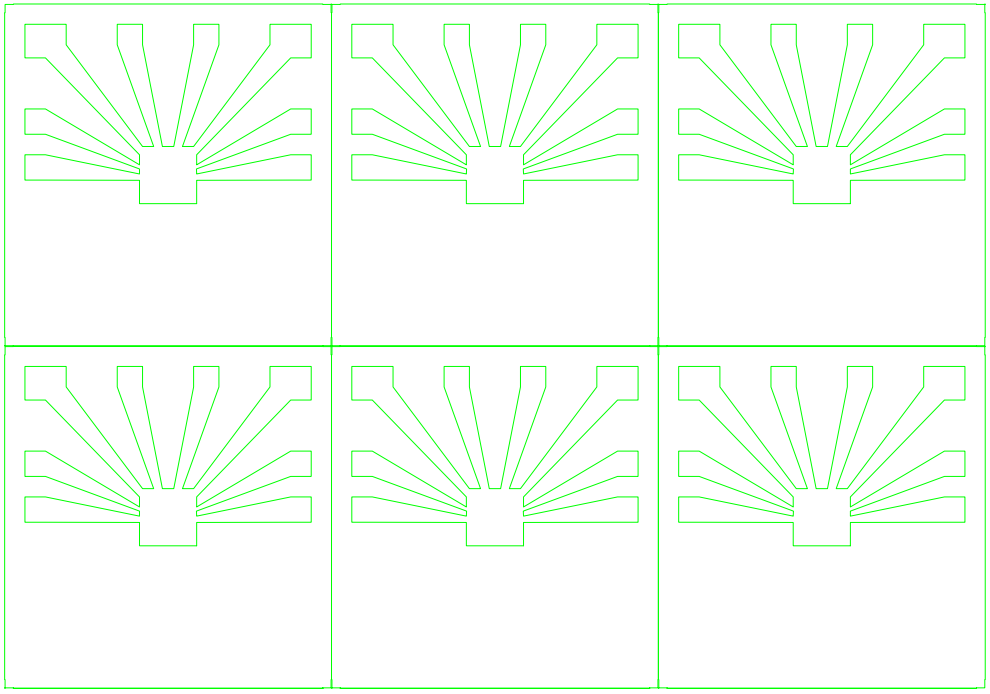


Figure C.2: Mesa etch pattern for a typicial 3 × 2 chip. The lines and crosses on the outside of the patterns are for alignment. The inner structure with the arms towards the top will remain untouched, the heterostructure around will be etched down to the interface to ensure isolation.

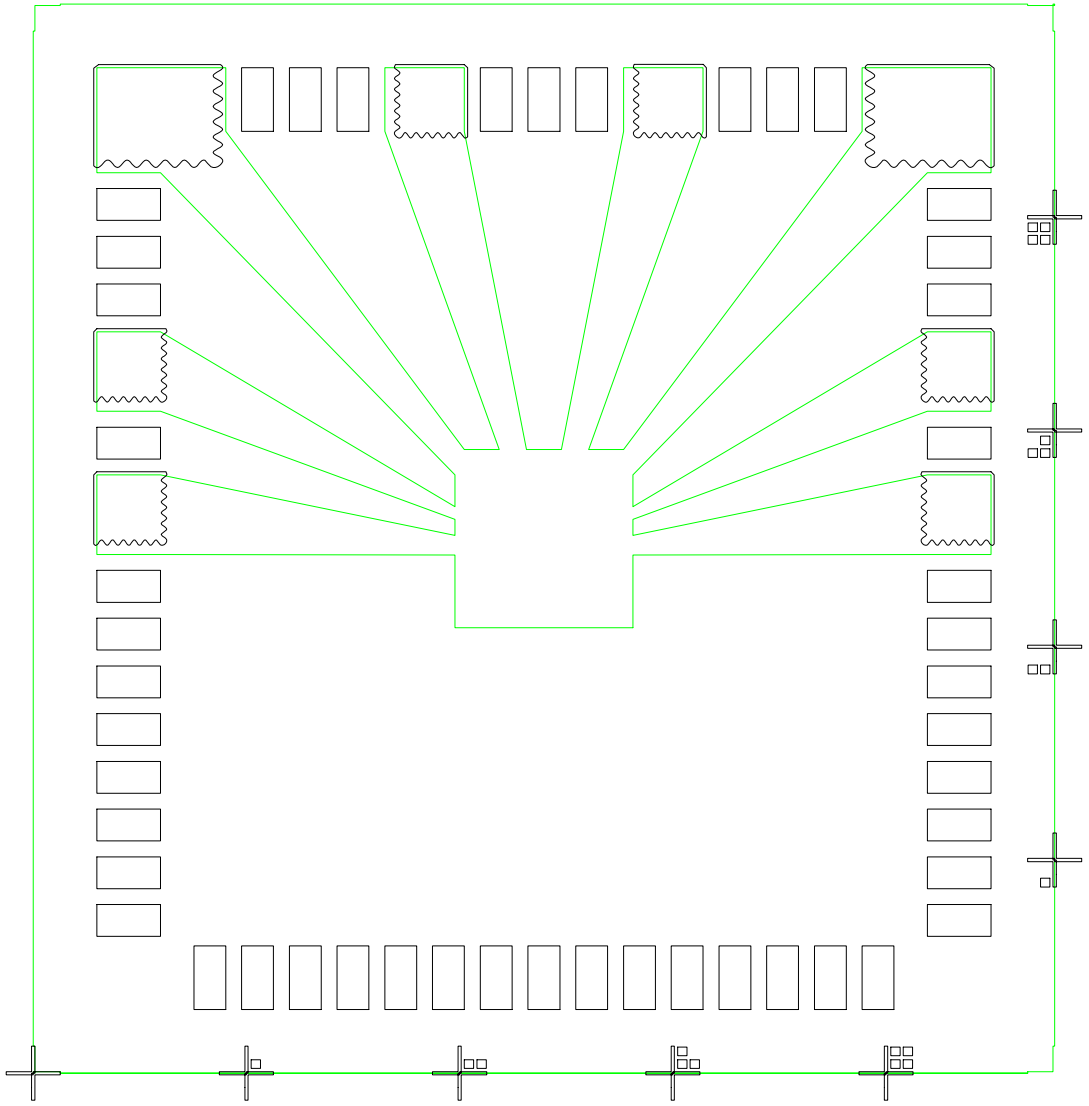
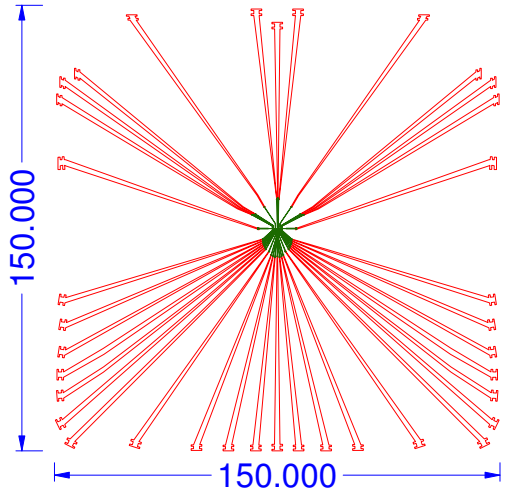
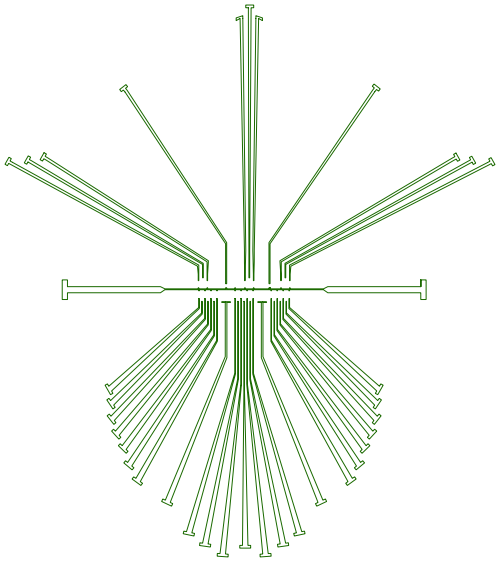


Figure C.3: The Ohmic patterns in back with the mesa underneath in green. The wavy structure on the edge increases conductivity of the ohmic contact. The bond pads for the gates are also included in the ohmic step to make them thicker and thereby easier to bond to. The crosses on the bottom and the side are alignment marks and used to align the several ebeam steps relative to each other. Note that each of the five alignment marks is numbered by squares in the upper right or the lower left quadrant, in order to make it easier to navigate during alignment.



(a) Inner write-field



(b) Quantum dot depletion gates

Figure C.4: 100 pA writing step. It contains two patterns, ensuring that the green part, which are the actual quantum dot depletion gates are writing within as short times as possible, to minimize the effects of stage drifts.

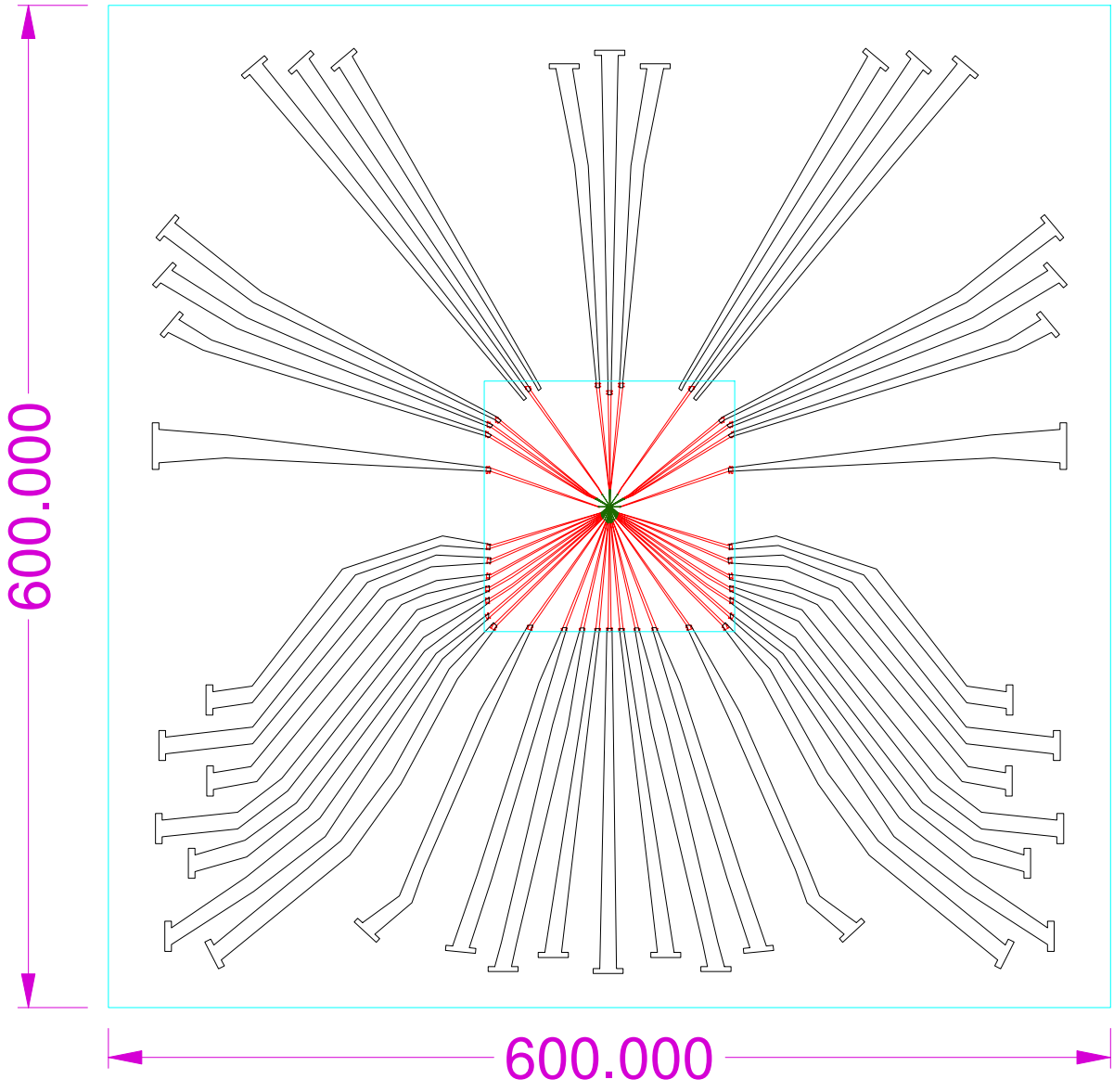


Figure C.5: The fine gates patterns. All the patterns shown are inside the mesa, which is indicated by the blue 600 × 600 μm box. The green and the red pattern are written with 100 pA, the black pattern is written with 2nA.

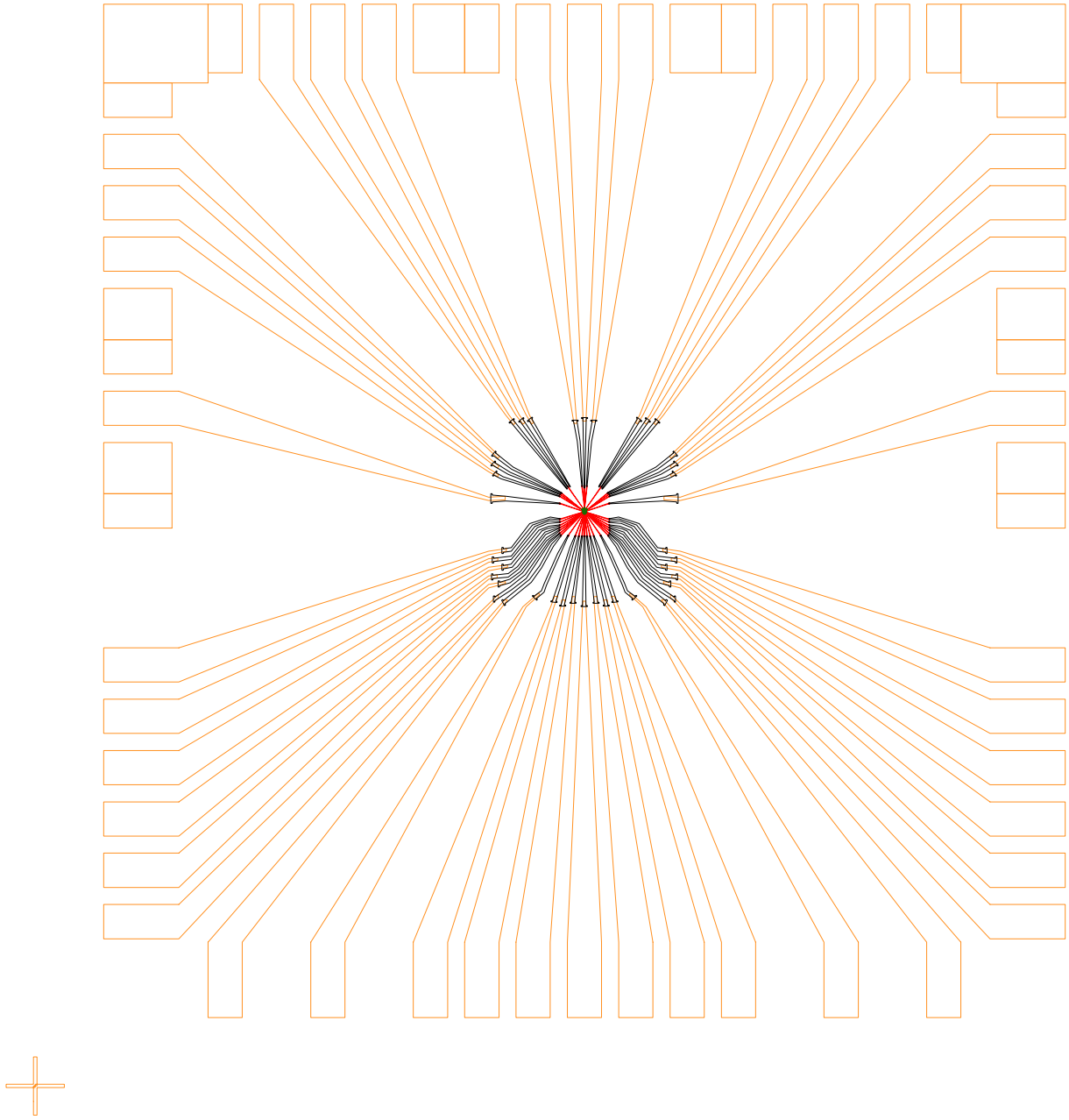


Figure C.6: The outer gates pattern is shown in orange. The fine gates written in the steps before are in black green and red. The pads that do not extend into the center of the design are for ohmic contacts.

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