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Charge sensing of epi-Al InAs nanowire devices:
Towards Majorana Fusion rule experiment

Master thesis
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Abstract

Majorana fermions in condensed matter systems have attracted a lot of attention since first strong signatures came from *Mourik et al.* of Majorana bound states in proximitized nanowires. Other groups quickly followed identifying and reproducing the same results and pushing forward to understand the dynamics of Majorana bound states in 1D systems. The main interest in these quasiparticles that they exhibit non-Abelian exchange statistics and can be encoded as a topologically protected qubits. Device of interest is proposed by *Aasen et. al.*, where two superconducting islands are separated on nanowire that can host pairs of Majorana fermions. Majorana fusion rule protocols can be carried out according to *Aasen et al*. Charge readout, that is crucial for fusion, can be done by charge sensing that was adopted from known spin qubit community, and applied for nanowire system in this thesis.

My main focus of the thesis, was to develop a nanowire based system, where charge readout can be done on Majorana fusion rule experiment devices. With a successful device material and geometry combination, such devices were fabricated and investigated at low temperatures. The devices that were measured are first of their kind, were charge sensing of each and individual nanowire superconducting islands is possible. The devices have the ability to be tuned from single to double quantum dots and vice versa, while taking charge sensing data. Even/odd effect at finite magnetic fields was also observed, indicating that epitaxially grown Al, fully proximitized the semiconductor. Majorana search in these devices was also conducted and presented in this thesis, with a zero bias conductance peak observed at ≈ 275 mT. Conclusions are given according to individual achievement that were done in this thesis.

Although, these devices ar still not the ultimate Majorana fusion rule experiment devices, an outlook for new and modified devices are presented as well.

Acknowledgements

I would like to thank the following people, without whom I think my work would have never been done.

First I would like to thank one of my supervisor P. Krogstrup, for replying to my e-mail and inviting me to start interesting and challenging scientific work at Qdev. Second I would like to thank the head of Center for Quantum Devices - Charles Marcus, for noticing my efforts in creating cutting edge condensed matter devices. Always challenging and pushing me forward to not only work hard but to understand the physics behind. Ferdinand Kuemmeth, for all the discussion in understanding not only complex devices but also experiment it self. Deividas Sabonis for great colleague in experimental physics lab. Erikas Gaidamauskas for the great and clear lectures in condensed matter physics. Hung Nguen for collaboration and discussions on the experimental part. David van Zanten for bring new ideas and pushing forward the T9 and T10 experiments. Filip Krizek for always willing to have a chat and quick learner at anything. Saulius Vaitiėkėnas and Mingtang Deng for all the endless fabrication and measurements discussions. Shivendra Upadhyay for always helping me in the cleanroom with any question I had. For all the Qdev team you are the best environment for experimental physicist. And last but not least I want to thank my family for keeping my dreams alive and giving me the opportunity to follow a path to science.

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Thesis overview

1st chapter gives a brief introduction to why there is an interest in quantum computation and into topological qubits that could be scaled to build first fault tolerant topological quantum computer.

2nd chapter is about relevant theoretical and experimental background on the measurements that were conducted. One important phenomena is the trivial and topological superconductivity. Quantum dot physics is introduced and analyzed. Proposed Majorana fusion rule detection analysis to give a sens of complexity in devices that were under investigation.

3rd chapter is focused on the main device fabrication. It gives complete steps in how the devices with multiple side gates were were fabricated and it should serve as a look up sheet for people who want to make any sort of precise and clean lithography with nanowires. This chapter also consists of the measurement setup that was used to measure and analyze the devices. I will present the main dilution refrigerator. I will give an overview of all the devices that were measured and main differences. I will present what these devices are capable of accomplishing.

4th chapter discussion and presentation of devices that were investigated. Initial measurements that were done, opening and closed regimes. The confirmation of 2e to 1e periodicity transition in magnetic field. Presented zero bias conductance peak. Finally, I will conclude with my thesis by stating the most important findings that were extracted from the measurements.

5th chapter I will give an outlook to what has been done in order to improve the Majorana based qubit experiments and what potential might hold new material growths and proposals that gave new devices to be fabricated and measured.

CHAPTER 1

INTRODUCTION TO QUANTUM COMPUTATION

"Those who are not shocked when they first come across quantum theory cannot possibly have understood it."

- Niels Bohr

Motivation

Alan Turing, father of computing machines, realized during The Second World War that some mathematical problems are impossible to solve by analytical methods. Carefully built machines can solve these tasks very well. By using mechanical motion you could encode information and even perform calculations [1]. These computing devices we now call classical computers. Take for example any computer: laptop, smart-phone or even portable smart-watch. These devices have billions of microscopically small transistors. Information stored and computed in these small things is not by mechanical motion but by electrical signals.

In the middle of 20th century first ever transistor was put forward as a computation machine, where classical bits encode information and gave the ability to calculate and compute. Ever since, the electronic industries were racing to scale the transistor to even smaller systems, to increase its ability to compute even more complicated tasks. Handful amount of hard problems can be solved using supercomputers. To this day, by making transistors smaller we are inevitably approaching the limits of atomic scale and it becomes ever so challenging to push even further. Building smaller computation circuits falls into the end of Moore's law [2]. Therefore, focus has been moved to unconventional materials: *Two-dimension electron gases* [3], *semiconducting nanowires* [4]. Latter are great candidates for *field effect transistor* [5] fabrication, bio-sensing [6] and photovoltaics it is also considered to have a huge potential in non-classical computation.

The purpose of this work is to deepen the understanding in how nature works at a very fundamental level. Hopefully, a system of theoretically predicted quasiparticles that are called Majorana fermions can be realized and manipulated in such devices that are presented here. Exotic quasiparticles in their nature because they are their own anti-particles and posses non-abelian braiding statistics. If one Majorana fermion could be braided with the other in 2 dimensions or in 1 dimensional nanowire networks, over time then the host state is rotated within a degenerate ground-state mainfold. This allows to preform fault tolerant quantum computation, protected from large class of errors because of the topological nature of the ground state degeneracy.

How can we speed up and increase the computational power? Is there a new method to compute complex tasks and will be a complete game changer? Those are the main question of today's condensed matter physics. The answer might be how effectively we can adopt and exploit quantum mechanics, the way nature has done.

1.1 DiVincenzo criteria

Realization of quantum computer has to satisfy certain criteria that have been laid out by DiVincenzo [7]

- ***Scalable system with well defined and characterized qubits.*** In order to have a some kind of a computer, collection of bits or in our case quantum bits (qubits) is necessary. A qubit is a two-level quantum system, e.g. two spin states of an electron. The state notation can be then written: $|0\rangle$ and other state $|1\rangle$. If one wants to flip the states between one and other it can be done in two-dimensional vector space, where the general state is written a$|0\rangle$ + b$|1\rangle$, where a and b are complex numbers and a normalization convection holds as $|a|^2 + |b|^2 = 1$. All qubits are *entangled*, which means that they cannot be written as a product of the states of two separate qubits.

- ***Ability to initialize qubits to any chosen state.*** This is also true for classical computing. Before starting any computation it is necessary to know the initial system before making qubit manipulations.

- ***Decoherence times are much longer then gate manipulation of the qubits.*** The characterization of qubit of its contact with the enviroment in time scales is of great importance. Gate manipulations of the qubits have to be faster the any environment fluctuations can occur.

- ***Make measurements on qubits.*** Main requirement of quantum computer is the ability to readout the specific qubits.

In recent studies, quantum bits have been successfully developed in 2 dimensional electron gas (2DEG) [8] but they all face the same problem which is dephasing errors. This is crucial for fault tolerant and scalable quantum computer. In present research focus has been set to isolate qubits from the environmental fluctuations, which is the main cause of dephasing the system. This led to put efforts in building the so called topologically protected quantum bits, system which is immune to local fluctuations.

CHAPTER 2

THEORETICAL AND EXPERIMENTAL BACKGROUND

"Physicists like to think that all you have to do is say, these are the conditions, now what happens next?"

- Richard P. Feynman

Background in theory behind all the fabrication and most importantly measurement side is a necessity to correctly conduct, interpret and analyze the data. That is why theory part of the most relevant phenomena presented here is discussed in theory chapter.
I will present the most important parts of superconductivity. An explanation of basic quantum dot physics and electron transport. I will briefly introduce key ingredients in making a Majorana based devices and discuss proposed methods in manipulating such a system to show non-Abelian statistics. What challenges one faces in creating such system, like the so called poisoning events of quasi-particles and time scales of operations necessary to perform qubit manipulations.

2.1 Conventional superconductivity

In 1911 H. Kamerlingh Onnes discovered superconductivity phenomena, just few years after he successfully liquefied helium. Being able to reach few degrees of Kelvin allowed Onnes to show superconductivity in materials [9]. This phenomena was not understood at the time of discovery but in 1950s and 1960s theoretical picture of superconductivity was introduced, which followed new discovered superconductors at higher temperatures [10].

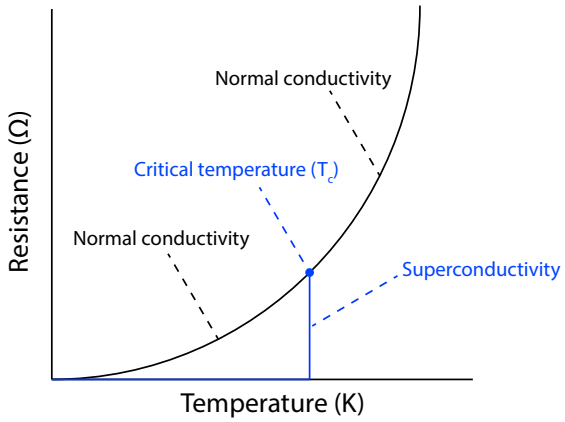

Figure 2.1: ***Type I superconductors***. *For particular metals: Al, Hg, Pb, Sn, Ti and other materials, there is a critical temperature (T_c) at which material undergoes phase transition in conductivity. Reducing materials temperature at a critical point, resistance drops to zero and current can flow through material. As for non-superconducting materials this phenomena is not observed as temperature is reduced.*

One of the main parameters of superconducting metals or materials is their ability to undergo a phase transition at a certain *critical temperature* (T_c) from normal metal to superconductor. Superconductor can also be destroyed by external magnetic field value (B_c) that is different for different for type I superconductors.
Superconductivity can be understood from quantum mechanical point of view but it is not a microscopic effect because it is equally observed at a macroscopic scale. The most interesting and main properties were explained through Bardeen–Cooper–Schrieffer (BCS) theory [11].

After the discovery of superconductivity people thought the material after critical temperature became an ideal conductor at zero external magnetic field. If a superconducting material is placed in a external magnetic field, it does not penetrate the interior of the sample. This can be understood by the following: as soon as the field penetrates the ideal conductor, an induced current is generated in the interior which is an opposite to that of the external magnetic field, therefore the interior magnetic field is zero (type I superconductors).

2.1.1 Cooper pairs and quasiparticles

BCS theory gives an explanation why there is an attractive interaction between electrons, which directly gives rise to ground state such that it contains correlated pairs of electrons [12]. The amount of correlated pairs can be quantified by correlation function *pair amplitude*. By assumption that length scales exceed λ_F, we can write:

$$F_{\sigma\sigma'}(\vec{r}) = \langle \psi_\sigma(\vec{r})\psi_{\sigma'}(\vec{r})\rangle, \tag{2.1}$$

where σ and σ' is electron spin indicies. The pair amplitude is a singlet combination of spin up and spin down for conventional s-wave superconductor.

$$F_{\uparrow\downarrow}(\vec{r}) = -F_{\downarrow\uparrow}(\vec{r}) \equiv F(\vec{r}). \tag{2.2}$$

Superconductivity is present once the pair amplitude is positive ($|F(\vec{r})| > 0$) that means pair of electrons are correlated. We can characterize order parameter by strength pairing potential:

$$\Delta(\vec{r}) = \lambda(\vec{r})F(\vec{r}), \tag{2.3}$$

where $\lambda(\vec{r})$ describes the attractive strength of two electrons. This is more a material parameter but it can also depend on position in heterostructures. This pair potential takes form of a complex function:

$$\Delta(\vec{r}) = \Delta e^{i\psi(\vec{r})}, \tag{2.4}$$

case of a the clean SC, Δ is equal of to the gap of quasiparticle energy gap.

If a superconductor is placed in a small external magnetic field (no vortices) then the pairing amplitude absolute value is constant, but the phase might depend on position, this is what give rise to a supercurrent. The way to understand this attractiveness of electrons in a superconductor is to think of electron-phonon coupling. If an electron moves in a lattice with a negative charge, it exerts a force to positively charge ions of the lattice. Those ions move slightly to the moving electron. This shift effect, results in electrons of those ions that moved toward the initial electron, So they start to move in the same direction. For a specific set of metals (Al, Nb, Ti and etc.),

the average distances between electrons are just right to overcome Coulomb repulsions and superconductivity is observed.

Two types of particles of particles are present in the superconductor: Cooper pairs and excited unpaired electrons called Bogoliubov quasiparticles. Bogoliubov quasiparticles conducts normal current and might be effected by the conventional scattering perturbations. However, in opposite normal state, particle and hole excitations Bogoliubov quasiparticles are quantum superpositions of particles above Fermi level and holes below Fermi level. The usual description of superconductors at the mean field level is based on Bogoliubov-de Gennes Hamiltonian, which allows to describe the physics of superconductors through the properties of quasiparticles. Any quasiparticle states are the solutions of BdG equations and in a case of zero energy solutions, represent equal superposition of particle and hole components, in this specific case are called Majorna fermionic solutions.

2.1.2 Superconducting energy gap

From the BCS theory, density of states in a conventional s-wave superconductor for the quasi-particle excitations from the SC ground state is:

$$N_S(E) = N_F \frac{|E|}{\sqrt{E^2 - (|\Delta|)^2}} \theta(|E| - |\Delta|), \tag{2.5}$$

where energy E is considered in respect to Fermi energy E_F. We can plot the latter function 2.5:

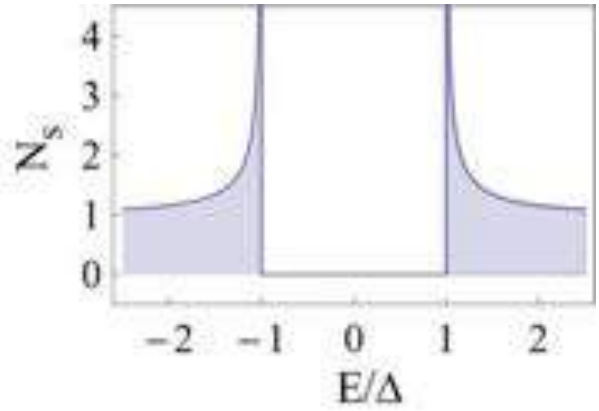

Figure 2.2: ***Supercondcting energy gap***. *Bulk BCS superconducting density of states.*

There are no states for quasi-particles to enter below $|\Delta|$, only Cooper pairs are allowed to be transported. Another important signature of superconductivity is density of states divergence at $E = \Delta$.

Energy gap is both temperature and external magnetic field dependent. The critical temperature is related by the following relation at the weak coupling.

$$\Delta(T=0) = 1.764 k_B T_C, \tag{2.6}$$

Typical Al critical temperature value is $T_C \approx 1.2$ K. Converted that temperature to the energy gap would be ≈ 200 μeV

2.2 Quantum dots

If a resistor is scaled down to very microscopic dimensions, the properties that electrons are moving through can be explained by quantum mechanical framework. This has to do with quantized charge e transport if the devices becoming microscopically small.

Quantum dot is a system where electrons are confined in a very tiny region of a semiconductor, superconductor or normal metal space, dimensions can be order of nm ($10^{-9}m$). Electron de Broglie wavelength is comparable to the size of the dot itself, that is why electrons have discrete quantum levels. If such confined space with electrons are coupled or connected by huge electron sea reservoir (source and drain), then one can study many physical phenomena: quantum systems coupled to quantum dots, quantum Hall effect [13] and many other quantum mechanical behavior of nature.

Characteristic parameter of quantum dots is the charging energy (E_C). How much an energy does one electron have to pay in order to "hop-on" the dot or to "hop-off". If charge e is tunneled on the island, capacitance of the dot changes and the total charging energy is expressed:

$$E_C = e^2/2C \tag{2.7}$$

Charging energy becomes larger that thermal excitations $k_B T$, than this charge quantization becomes relevant. The tunnel barriers have be sufficient high in order to keep electrons separated that are on the dot from the outside contacting leads (source and drain). This means that quantum fluctuations between the source-dot-drain are low compared to the measurement time. This time has be order of the discharge $\Delta t = R_t C$, where R_t is the tunneling resistance of the barriers. If we look at the Heisenbergs uncertainty principle:

$$\Delta E \Delta t = \frac{e^2}{C} R_t C > h \tag{2.8}$$

This implies that tunneling resistance should be above resistance quantum h/e^2=25.8 kΩ, larger that quantum fluctuations.

Quantum dots can be realized in *two-dimensional electron gases* (2DEGs) and in 1D systems as well. With predefined gates one can make constrictions and deplete the 2DEG that is beneath

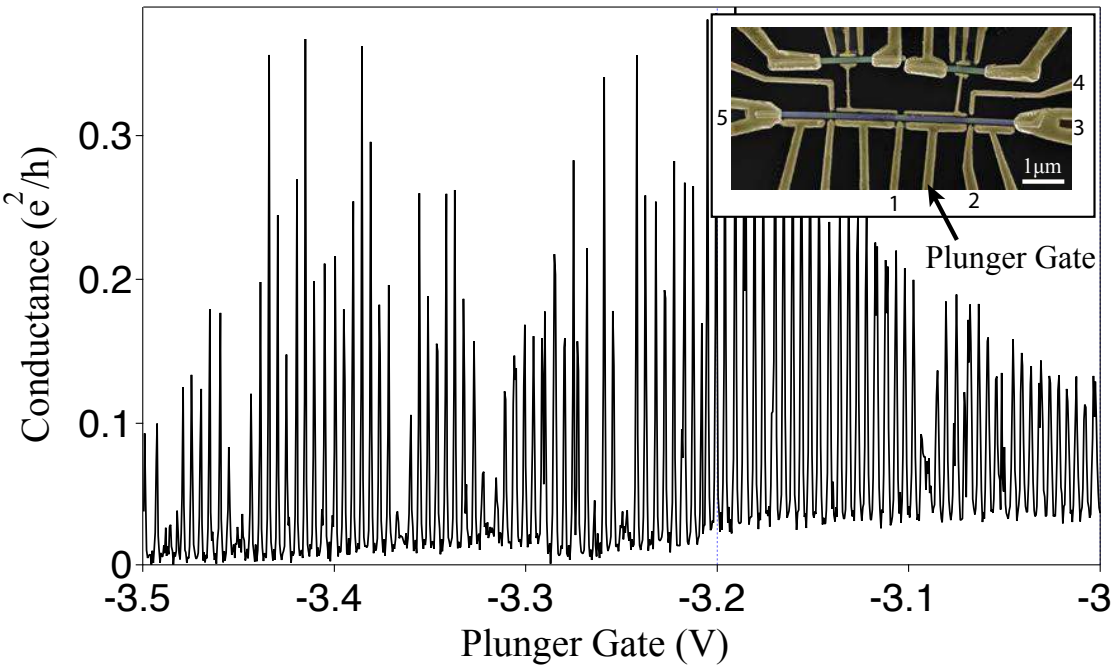

Figure 2.3: ***Quantum dot characterization with electrostatic gate voltage as a function of conductance****. Inset showing a scanning electron micrograph image of the InAs with epitaxial Al device that were investigated. With source-drain (3 and 5) and a plunger gate. Tunnel barriers are formed by cutter gates (1 and 2), making a superconducting quantum dot. As the plunger gate voltage is swept differential conductance is measured in units of e^2/h. Small bias voltage (0.4 mV) is applied between the source and drain contacts. Coloumb resonance are observed.*

the gates. In semiconducting nanowire device that was analyzed in the thesis is shown in Figure 2.3 inset is a *scanning electron micrograph* (SEM) of a gate defined quantum dot that it is possible to tune electron density in quantum dot that is defined with 1 and 2 gates. Gates are patterned on and insulating oxide of the chip. If voltage bias is applied between source and drain (5 and 3 contacts) of 0.4 mV to get linear conductance response. Measurements are conducted at 20 mK base temperature in $He^4 + He^3$ dilution refrigerator. The applied voltage is resulting in current flow through the quantum dot, which can be tuned by plunger gates. If the bias voltage is small then the current is given by $G = I/V_{SD}$. If bias voltage is increased then the current flow is not linear and it is useful to measure differential conductance dI/dV_{SD} as a function of constant V_{SD}.

Figure 2.3 shows the dI/dV in units of e^2/h of applied plunger gate on the quantum dot. From the figure we see the sharp peaks in conductance at different plunger gate values. These peaks represent conductance resonances, which means that reservoir chemical potential is aligned with an empty state within a QD. In between the peaks we have Coulomb blockade, that means electrons ar not allowed to tunnel through, because they have to pay an extra energy to hop on empty state of the QD. These peak oscillations indicate an acceptance of electron on the dot and

out.

2.2.1 Electron transport and Coloumb blockade

Energy potential framework of quantum dot coupled to source and drain can be sketched in Figure 2.4. Chemical potentials of outer electron reservoirs ar noted as μ_S and μ_D, which means electron are filled up to Fermi energy (normal metal lead case) at T = 0. If temperature is not zero, then electrons are filled according to Fermi distribution. If a bias voltage is applied between the two leads then we can write:

$$V_{SD} = (\mu_S - \mu_D)/e \tag{2.9}$$

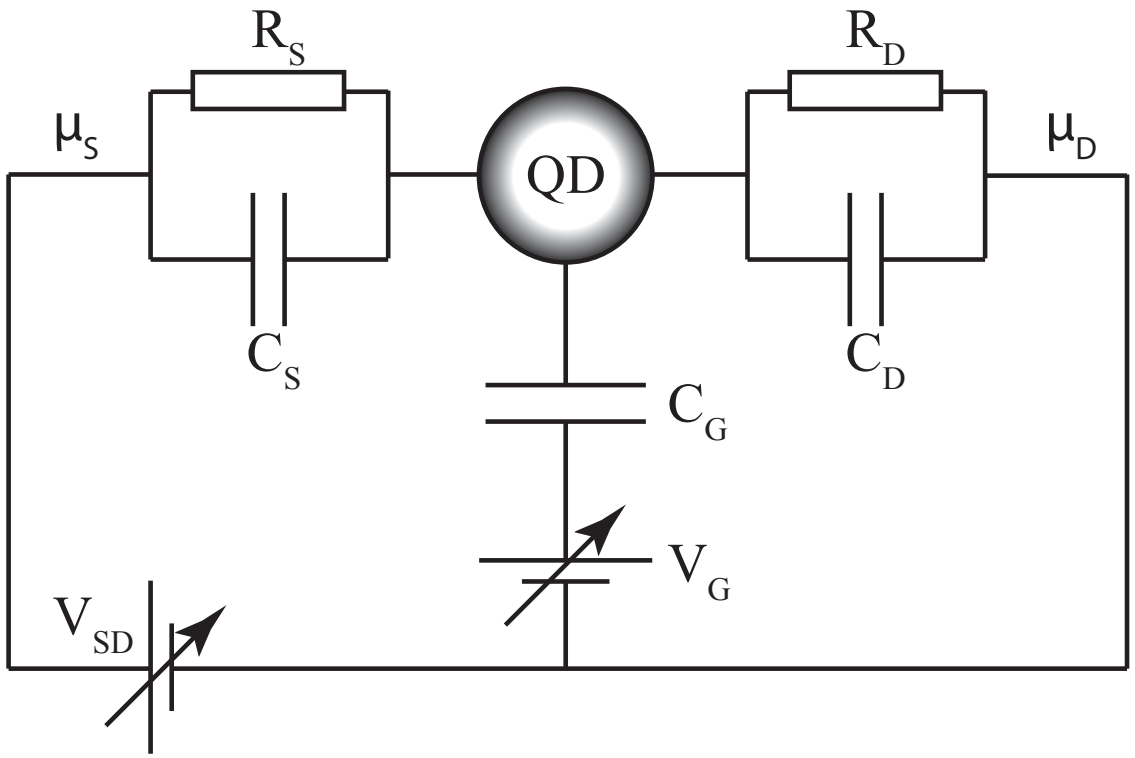

Figure 2.4: ***Quantum dot control with source-drain schematics****. Quantum dot confinement and coupling to the source-drain and capacitive coupling with gate schematics. V_{SD} can be controlled by changing capacitive coupling between the quantum dot and reservoirs μ_S and μ_D. Quantum dot ground state energy can be tuned via capacitive coupling gate by V_G, effectively tuning the electron density within the dot.*

Quantum dot is capacitively coupled by a nearby gate (C_G), that can be controlled by V_G and tunes the electron density in QD. Outside the quantum dot there are tunnel barriers that are tuned with other gates, that tunnel resistance is reached (R_S and R_D), allowing only single

electron transmission.

Electron transport can only occur within the degeneracy points of the quantum dot (at the intersection between n and $n+1$ energy parabolas) Figure 2.5 a). We can write the following equation for energy spectrum [14]:

$$E_n(V_G) = \frac{(ne - Q_G)^2}{2C_\Sigma} - \mu, \tag{2.10}$$

where $Q_G = C_G V_G + C_S V_S + C_D V_D$ is the gate charge, e is electron charge, $C_\Sigma = C_S + C_D + C_G$ is the total quantum dot capacitance that are contributed to the coupling of source, drain leads and gate, n is an integer. For the analysis of transport through a quantum dot it is useful to define chemical potential, as a difference between two adjacent charge states, $\mu_N(V_G) = E_{N+1}(V_G) - E_N(V_G)$. For the finite bias voltage, non zero conducttance willl be measured only if the following energy conservation condictions will be satisfied, $eV_S \geq \mu_N(V_G) \geq eV_D$. Which means that chemical potential should be placed within the bias window.

So far in real systems, source and drain leads might not couple equally ($C_S \neq C_D$) to the quantum dot, meaning the whole picture of Coloumb blockade could be quite different. For a superconducting quantum dots the qualitative picture of Coloumb blockade is different, meaning odd number electron parabola ($n = 1,3,5..$) has a Δ energy gap (is energy is required to break up Cooper pair and have single electron transitions on the dot). If the electron parabola number is even ($n = 2,4,6...$) the there is no energy Δ in order to have Cooper pair transport through the quantum dot. This will be explained in measurements chapter 4.5.

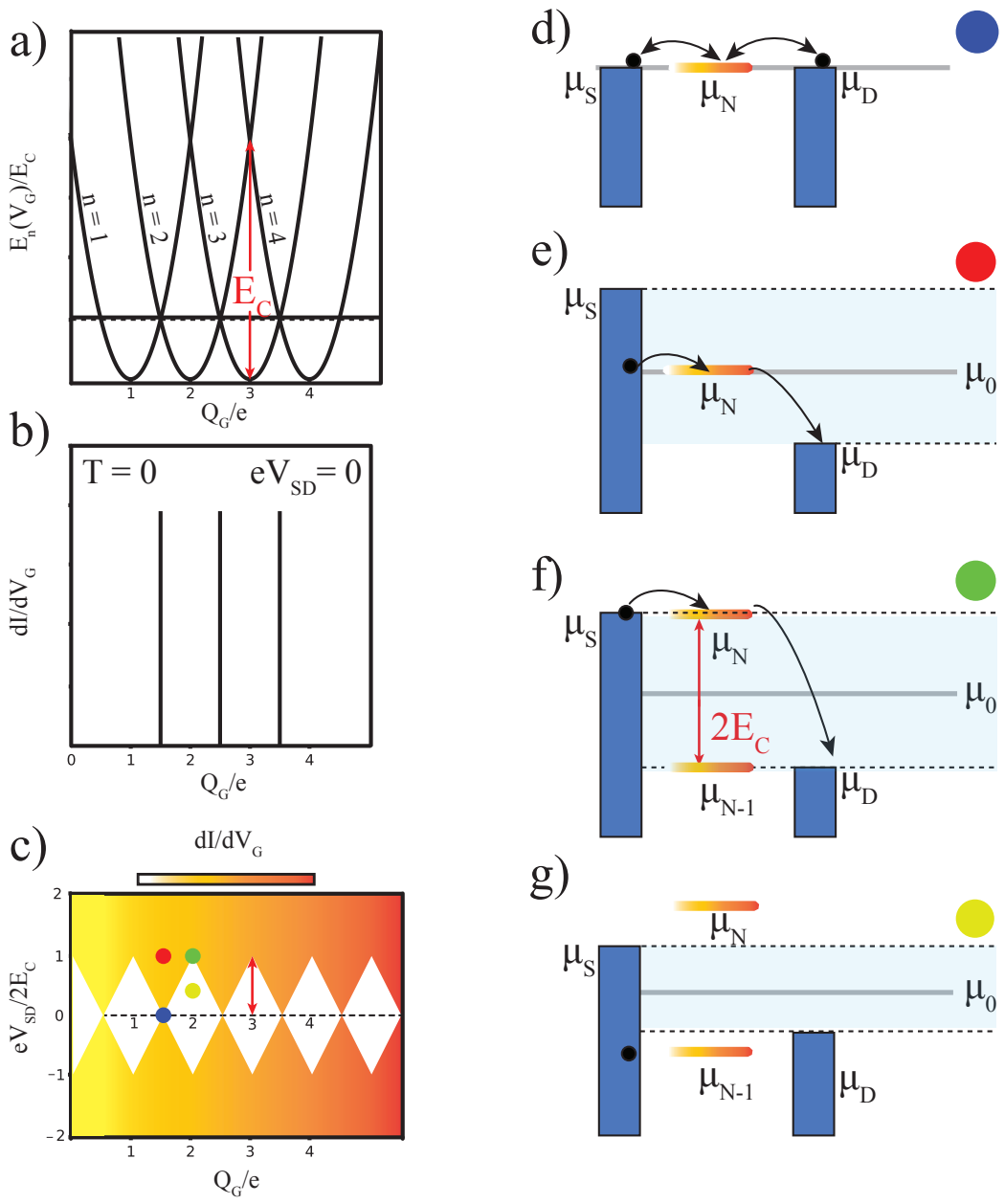

Figure 2.5: ***Quantum dot analysis through energy spectrum and Coloumb diamonds****. a) Energy spectrum of the quantum dot according to 2.10 equation. b) Zero bias differential conductance as a function of gate voltage. Quantum transport can be observed only when gate voltage is at the degeneracy points of the parabolas. c) charge stability diagram of the quantum dot. d) e) f) and g) energy level schemes corresponding to a different points in the charge stability diagram. Quantum transport is allowed in all of these points, except in case g) because of energy conservation condition in a tunneling process.*

2.3 Semiconducting nanowires

Conventional growth techniques allows to grow semiconducting nanowires, in which electrons are confined in two spacial dimensions. The nanowires can range from couple of nanometers to hundreds of nanometers in diameter . And length can vary between $0.5 - 10\ \mu m$. The wire morphology is defined by its crystal structure. $InAs$ nanowires have hexagonal facets which are presented in Figure 2.6. Nanowires (NWs) are grown from their semiconducting wafer in *Molecular Beam Epitaxy* (MBE) system. NWs are grown with Au droplet catalyst epitaxially copying its growth substrate crystal orientation.

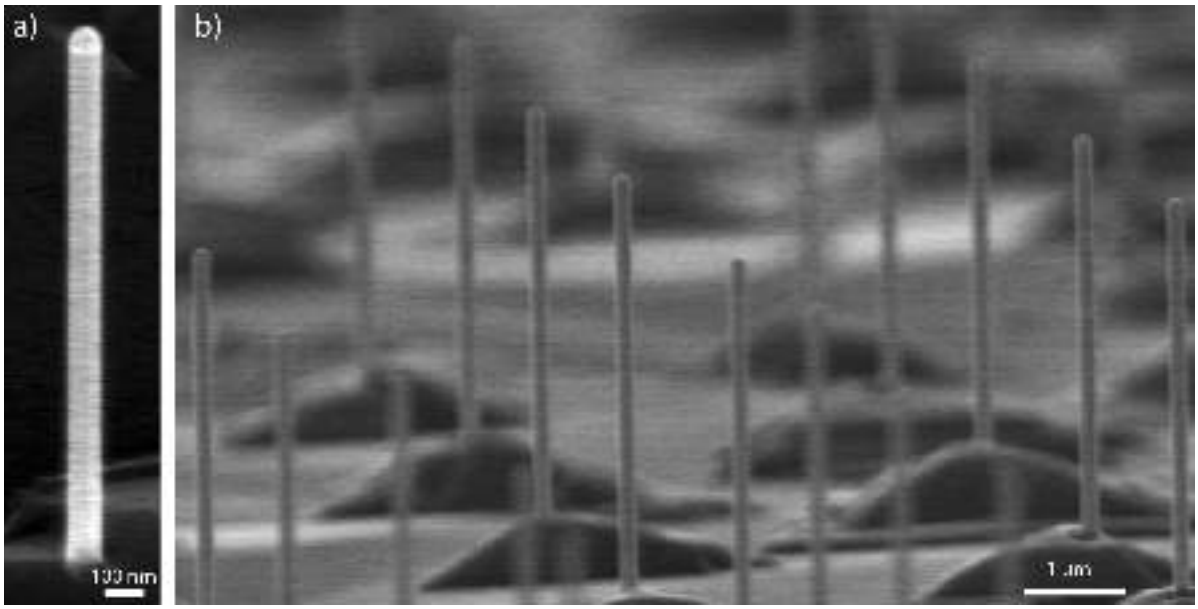

Figure 2.6: ***InAs nanowires on growth substrate (InAs wafer)****. a) Single InAs nanowire grown in Molecular Beam Epitaxy (MBE) system with Au droplet catalist on top of the wire. b) InAs nanowire arrays on the growth substrate. Courtesy of P. Krogstrup.*

Perfect material match

Breakthrough in material science have enabled researchers to fabricated devices that could exhibit exotic theoretically predicted particles that will be introduced later in the thesis. By having epitaxially grown superconductor on semiconductor in MBE system, enables to have perfect interface between two materials. The final result is that Al can induce superconductivity ($\leq T_C$) in the semiconductor and open hard superconducting gap (see Figure 2.7). This would give an advantage to create Majorana devices in hybrid nanowire structures.

As seen from the Figure 2.7 c) V_{SD} bias measurement on the wire has been done as a function of conductance (e^2/h). The device geometry is shown in Figure 2.7 a) where one end of the lead is normal metal (Ti/Au) and the other is a superconductor (Ti/Al). Tunneling barrier is formed by removing the epitaxial Al on one end of the nanowire and pattering side gates that can tune the

electron density in the semiconductor. This allows to conduct spectroscopy measurements. The superconductor has been directly connected to epitaxial Al by milling away the AlO_2 and having an Ohmic contact with epitaxial Al.

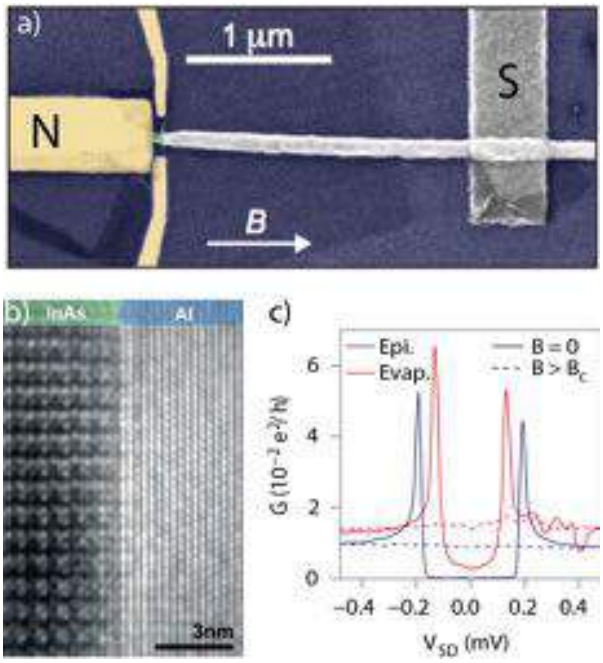

Figure 2.7: ***Hard superconducting gap of epitaxially grown Al on nanowires***. *Conductance measurements as a function of source–drain voltage of an epitaxial full-shell device (blue) and an evaporated control device (red) at B = 0 (solid line) and above the critical field B > Bc (dashed line) [17].*

From the Figure 2.7 c), it is visible that evaporated Al (red) solid (B = 0) curve has soft superconducting gap with multiple subgap states. That means the Al is weakly inducing superconductivity in the semiconductor ($InAs$). This is due to the imperfect interface between the two materials (Al and $InAs$). As for *in-situ* epitaxially grown Al (blue) solid (B = *0*) curve it is seen around V_{SD} = ±0.1 mV bias there is no conduction. This means that the superconducting hard gap has been opened. If the B field is higher than the critical field of Al, then the superconductivity is destroyed (dashed curve) in both cases (epitaxial and evaporated Al) and there is no gap around V_{SD} = ±0.1 mV bias, lead (S) has been driven into the normal metallic state.

There has been a theoretical explanation done by *Takei et. al* [18] to understand the soft gap physics of the imperfect material match. It was found that due to inhomogeneous coupling between the semiconductor and superconductor, could lead to softening of the gap.

2.4 Topological superconductivity

2.4.1 Abelian and Non-abelian anyons

The basic principle that quantum statistics is based on symmetry. This property enables to distinguish between fermions and bosons. If particles are interchanged between one and other they have to satisfy the proper symmetry. If we have a case of 3 and +1 dimensions (three spatial and one time), then under exchange the wavefunction of bosons will be symmetric, while fermionic exchange will be anti-symmetric. These symmetries of particles go back to the roots of Pauli exclusion principle, Bose-Einstein condensation and many other physical laws [19].

Majorana fermions

In 1928, Paul Dirac found a new framework to describe 1/2 spin particles (electrons and protons) which required complex numbers [20]. With Dirac's interpretation of particles, where both real and complex fields were required and it explained why anti-particles and electrons can exist. Paper came out in 1937 by Ettore Majorana [22]. He stated that it is not necessary to have complex fields to describe 1/2 spin particles. Majorana introduced elegant equation to describe these particles which only had real numbers. He gave an idea that 1/2 spin particles could have their anti-particles, which is consistent with general theory and quantum mechanics.

To define these particles we can start by writing the fermionic creation and annihilation operators $c_i^\dagger$ and c_i, they anticommute to each other and have no spin indices:

$$\{c_i, c_j\} = \{c_i^\dagger, c_j^\dagger\} = 0, \qquad \{c_i, c_j^\dagger\} = \delta_{ij} \tag{2.11}$$

We can rewrite our operators in the new form of γ_1 and γ_2, just by separating c_i and $c_i^\dagger$ into their real and imaginary parts:

$$c_i^\dagger = \frac{1}{2}(\gamma_1 + i\gamma_2), \qquad c_i = \frac{1}{2}(\gamma_1 - i\gamma_2) \tag{2.12}$$

By further modification we can rewrite the new operators into:

$$c_i^\dagger + c_i = \gamma_1, \qquad i(c_i^\dagger - c_i) = \gamma_2 \tag{2.13}$$

From the equations, it is visible that $\gamma_1 = \gamma_1^\dagger$ and $\gamma_2 = \gamma_2^\dagger$, creation and annihilation operators are equal to each other, which implies that quasiparticle γ_1 is equal to its own antiparticle, thus a Majorana fermion.
These quasiparticles come in pairs, that is why the operators are split into real and imaginary parts. One Majorana fermion results in single fermionic excitation, so this splitting of operators is sensible to talk when Majoranas are separated in space and their wave functions overlap by

small amount, what is called Majorana bound state (MBS) e.g in 1-dimensional systems. Two pairs of Majoranas are bound to each other at the very edges of p-wave superconductor [23].

2.4.2 1D Kitaev Chain

In 2001 Kitaev proposed and idea that in 1D p-wave superconductor MBS's would arise at each ends of the system [24]. We can write the tight binding chain of a nanowire (1D system) by the following Hamiltonian:

$$H_{chain} = \sum_{i=1}^{N} \Big(-t\Big(c_i^{\dagger} c_{i+1} + c_{i+1} c_i^{\dagger}\Big) - \mu\Big(c_i^{\dagger} c_i - \frac{1}{2}\Big) + \Delta^* c_i^{\dagger} c_{i+1}^{\dagger}\Big), \tag{2.14}$$

where t is the tunneling amplitude between two adjacent sites, μ is the chemical potential of the system, Δ^* is the effective superconducting gap in the chain. The p-wave superconductivity is realized if we pair electrons with the same spin in adjacent sites. That means in the Hamiltonian spin indicies can be excluded and the electrons become spinless.
We remember that Majorana operators can be written for each site: $c_i = \frac{1}{2}\Big(\gamma_{i,1} + i\gamma_{i,2}\Big)$ and $c_i^{\dagger} = \frac{1}{2}\Big(\gamma_{i,1} - i\gamma_{i,2}\Big)$. The subscript 1. 2 are representing different Majorana operators from the same electron site. Inverting the operators to other form: $\gamma_{i,1} = c_i^{\dagger} + c_i$ and $\gamma_{i,2} = i\Big(c_i^{\dagger} + c_i\Big)$. We can now rewrite the 2.14 equation with new Majorana operators:

$$H_{chain} = \frac{i}{2} \sum_{i=1}^{N} \Big(-\mu\gamma_{i,1}\gamma_{i.2} + (t + |\Delta|)\gamma_{i,2}\gamma_{i+1,1} + (-t + |\Delta|\gamma_{i,1}\gamma_{i+1,2})\Big) \tag{2.15}$$

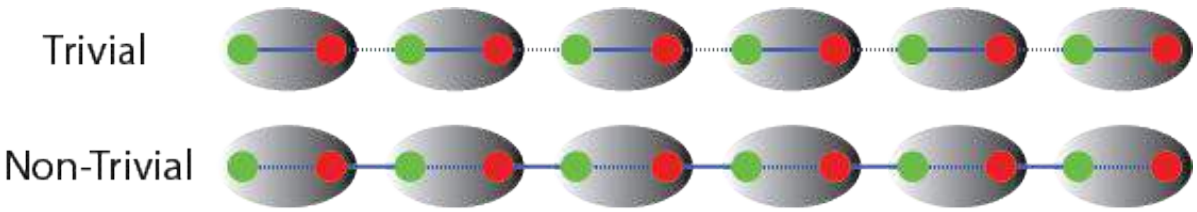

Figure 2.8: ***Kitaev 1D Chain****. Pairing schemes of adjacent sites of electrons in a trivial and a non-trivial superconducting regimes. In Trivial case (top chain) Majorana operators (green and red circles) are tunnel coupled in the same electron site. That leaves with all Majorana operators fully coupled and we are left with a chain of electrons. In the non-trivial case Majorana operators are tunnel coupled by adjacent sites electrons. That leaves us with two unpaired Majorana operators at the very ends of the 1D chain.*

We can distinguish two cases Figure 2.8 (trivial and non-trivial). Lets say that the tunneling amplitude $t = 0$ and that the superconducting gap $|\Delta| = 0$ but $\mu < 0$, then the 2.15 Hamiltonian takes form of:

$$H_{chain} = \frac{i}{2}\mu \sum_{i=1}^{N} \gamma_{i,1}\gamma_{i.2}, \tag{2.16}$$

this form, we can call a trivial case because the Majorana operators are paired in the same electron site and form an ordinary fermion (electron).

P-wave pairing case can be referred to when $|\Delta| = t > 0$ and $\mu = 0$. Then the 2.15 Hamiltonian takes the following form:

$$H_{chain} = it \sum_{i=1}^{N} \gamma_{i,2}\gamma_{i+1,1}, \tag{2.17}$$

In this non-trivial case we have two unpaired Majorana operators at the ends of the chain ($\gamma_{i,2}$ and $\gamma_{i+1,1}$).

Non-Abelian excitation can only be realized in p-wave superconducting materials. But since there are no evidence of such a material except in theoretical models, one can take a s-wave superconductor and with a 1D semiconductor nanowire can form a p-wave character superconductivity with an applied external magnetic field (Figure 2.9). Couple of groups [25] have realized such exotic system, by taking semiconducting nanowire with large spin-orbit interaction [26] and depositing it on a trivial s-wave superconductor. The nanowire is then proximitized having a superconducting properties.

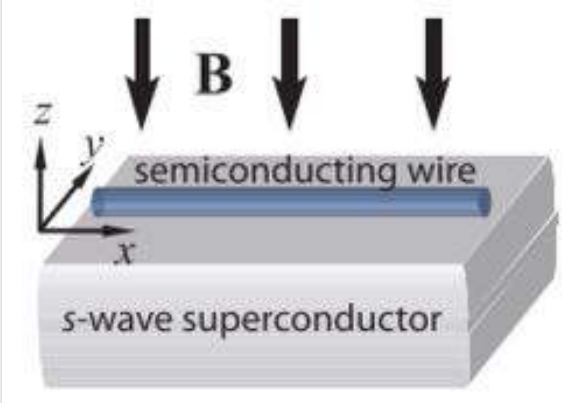

Figure 2.9: ***Theoretical realization of a p-wave superconductivity***. *Combining s-wave superconductor, 1D semiconducting nanowire and external magnetic field [25].*

The Hamiltonian that describes such a wire system can be written:

$$H_{BdG} = \Big(\frac{p^2}{2m} - \mu\Big)\tau_z + \alpha p\sigma_z\tau_z + B\sigma_x + \Delta\sigma_y\tau_y, \tag{2.18}$$

where B external magnetic field, μ - chemical potential. The first term describes the kinetic energy, second term describes the Rashba spin-orbit interaction, third term describes Zeeman magnetic field energy and fourth term describes proximity induced superconducting pairing. Pauli matrices in spin space - $\sigma_{z,y}$ and particle hole space mixing - τ_z. Zero energy solution for the H_{BdG}, if $B > \sqrt{\Delta^2 + \mu^2}$, will give Majorana wavefunction (Ψ_M) [27]. $\Psi_M \propto e^{-L/\xi}$, where L is 1D system length and ξ - superconductor coherence length, meaning that there is an exponential decay on Majorana wavefunction.

2.4.3 Non-Abelian exchange statistics validation

In this part I will introduce Majorana fermion quantum information processing proposed by *D. Aasen et. al.* [30]. For a semiconducting nanowire that is fully proximitized by trivial s-wave superconductor and driven into non-trivial topological state, the finite length of the nanowire has two fermionic modes and possess degenerate parity ground states. Nanowire hosts two pair of Majorana zero modes at the ends. Spatially separated exotic fermion excitations (Majorana fermions).

The Majorana operators satisfy anticommucation relations: $\{\gamma_n, \gamma_m\} = 2\delta_{nm}$. We assume that the Majorana wave functions of two superconducting (SC) islands do not overlap in space. Since the Majorana operators satisfies $\gamma_n = \gamma_n^\dagger$ relation (creation and annihilation operators), we can say that fermionic modes f_{12} and f_{34} is associated with zero "orbital" energy. That means both degenerate parity is only accessible at low energies below the superconducting gap Δ. Of course, the degeneracy of two parity states can be lifted by introducing charging energy (E_C) or by changing coupling of the gate "valve" (Figure 2.10).

Majorana fusion rule

Lets take a half coated 1D semiconductor with epitaxial superconductor and with strong spin-orbit coupling. Middle of the wire superconductor is removed (etched) and only a small semiconductor window is left. Then, one side of the nanowire is connected with a bulk superconductor that is grounded, other side of the wire is left with just epitaxial superconductor. On the side to etched region we have gate that can control the semiconductor electron density by a voltage source. (Figure 2.10)

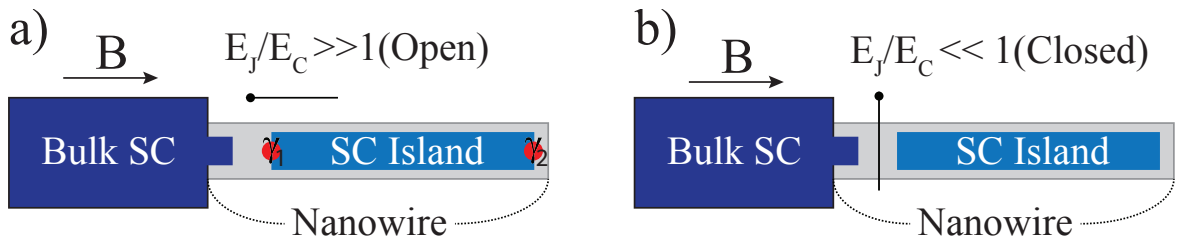

Figure 2.10: ***Schematics of semiconducting nanowire half coated with epitaxial superconductor****. SC is removed and voltage controlled gate is placed near the etched region. One side of the nanowire is connected to the bulk superconductor that is grounded. The device is place in parallel magnetic field (B). a) If the gate is in open regime ($E_J/E_C >> 1$, the SC island hosts pair of Majoranas at each end (γ_1 and γ_2). b) If sufficient negative voltage is applied to the gate, tunnel barrier is lifted and the nanowire is in closed regime ($E_J/E_C << 1$) and MBS degeneracy is lifted by charging effects, no MBS are in the system.*

Ability to tune semiconductor electron density in a junction between bulk SC and SC island, implies that ratio between Josephson E_J and the charging E_C energy of the SC island can be experimentally controlled. Lets place the device into magnetic field that is parallel to the nanowire. Outcome is, superconductor hosts Majorana zero modes, if only the gate is in open

regime[1], γ_1 and γ_2. In open gate configuration, Majorana zero modes (γ_1, γ_2) are degenerate in the ground state and are topologically protected by even and odd fermion parity.
As we start to close the junction, charging energy becomes dominant over Josephson energy. This lifts degeneracy of parity eigenstates into charge states [2]. Then the SC island has no Majorana zero modes anymore.

Non-Abelian Ising anyons follow fundamental and simple fusion rule statistics: pairs can annihilate I or combine into fermion ψ.

$$\sigma \times \sigma = I + \psi, \tag{2.19}$$

where I is denoted as trivial particle (i.e, they can annihilate). These two outcomes correspond to unoccupied and occupied single fermionic state composed by two Majorana fermions. So two possible results can be seen once Majorana modes are fused together [30] proposed an experimental method to fuse these particles. Following rigid step protocols in single-wire geometry with two superconducting islands and three gate-tunable "valves".

Experiment is centered on creating Majorana fermions in the nanowire system by manipulation of the gates, then restoring Coloumb blockade regime ($E_J/E_C << 1$) to fuse fermions together and with a charge sensor readout the probability outcome. Sensing can be accomplished if degenerate parity ground state is converted into charge states, with capacitive coupling the isolated island can be read out by proximal quantum point contact or a quantum dot. The charge sensing techniques are well established, e.g in spin qubits [31]. Based on these experiments it is clear that nanowire based charge sensor is possible and high-quality charge readout can be accomplished, with high fidelity of 99%, this could be achieved with τ_M = 1 μs integration time. If τ_M[3] exceeds poisoning and relaxation event times, than single-shot[4] readout is possible as well.

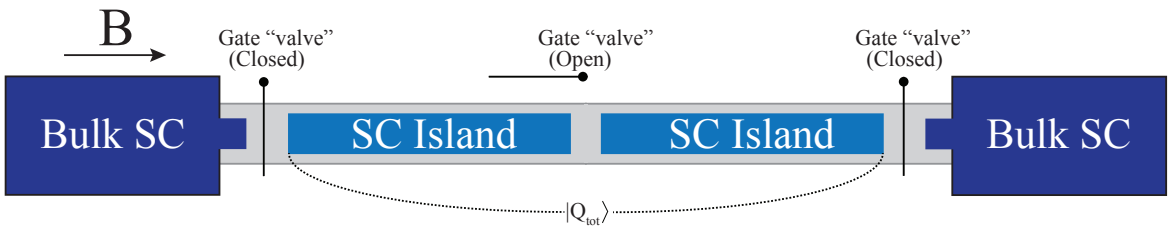

Figure 2.11: ***Initialization protocol for Majorana fusion****. By closing the outer gate "valves" and opening the middle gate "valve" we fix the total charge (assuming that there are no poisoning events).*

[1]Open regime is when the tunneling barrier has more modes and the coupling E_J between two superconductors is dominnat over charging energy.
[2]Even and odd parity states are split into two distinctive states.
[3]Measurement time
[4]Time and single charge state resolved measurement, that counts individual events in real time

Initialization setup has to be as shown in Figure 2.11, Where the outer "valves" are closed and the middle "valve" is fully open. Then two SC island are well coupled by Josephson energy and forming one "big" SC island. The total charge $|Q_{tot}\rangle$ of the "big" topological SC island is fixed at the starting point of the experiment.
Next protocol step is to open outer "valves" and creating γ_1 and γ_4 out of the vacuum leading to parity state of $|0_{14}\rangle$ (Figure 2.12). This state correspond to zero occupancy for the fermion constructed by the Majorana fermions (γ_1, γ_4):

$$f_{14} = \frac{\gamma_1 + i\gamma_4}{2} \tag{2.20}$$

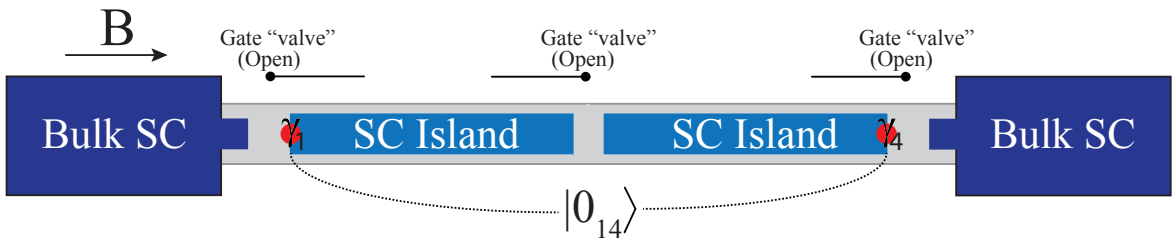

Figure 2.12: ***Topological single island stage***. *If all the gate are in the open regime ($E_J/E_C >> 1$, the SC island hosts pair of Majoranas at each end ($\gamma 1$) and $\gamma 2$).*

Closing the middle "valve" and reducing the coupling between two SC islands, moves the system into double SC dot island. Another pair of states emerge with Majorana zero modes of γ_2 and γ_3. In this case additional fermion operator can be defined:

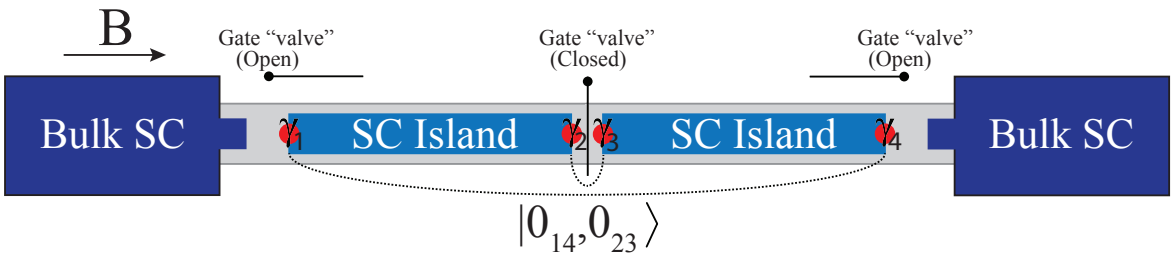

Figure 2.13: ***Topological double island stage***. *If the middle gate is in a closed regime, double island geometry host two pairs of Majorana fermions γ_1, γ_2. γ_3 and γ_4.*

$$f_{23} = \frac{\gamma_2 + i\gamma_3}{2} \tag{2.21}$$

Then the state can now be written as $|0_{14}, 0_{23}\rangle = \frac{1}{\sqrt{2}}\left(|0_{12}, 0_{34}\rangle + |1_{12}, 1_{34}\rangle\right)$ (Figure 2.13).

Closing the outer gate "valves", restores the charging energy and removes the groundstate degeneracy. Then the γ_1 and γ_2 are fused together, as well γ_3 and γ_4. Different parity eigenstates

corresponds to the different charge state outcomes. I.e., state $|0_{12}\rangle$ fuses into charge eigenstate $|Q_L\rangle$ (correspondingly $|0_{34}\rangle$ to $|Q_R\rangle$, $|1_{12}\rangle$ to $|Q_L-1\rangle$ and $|1_{34}$ to $|Q_R+1)$. As a result the initial parity eigenstate $|Q_{14},Q_{23}\rangle$ evolves into the charge superposition state, $1/\sqrt{2}(Q_L,Q_R\rangle+|Q_L-1,Q_R+1\rangle$, which can be measured by charge sensing techniques (Figure 2.14).

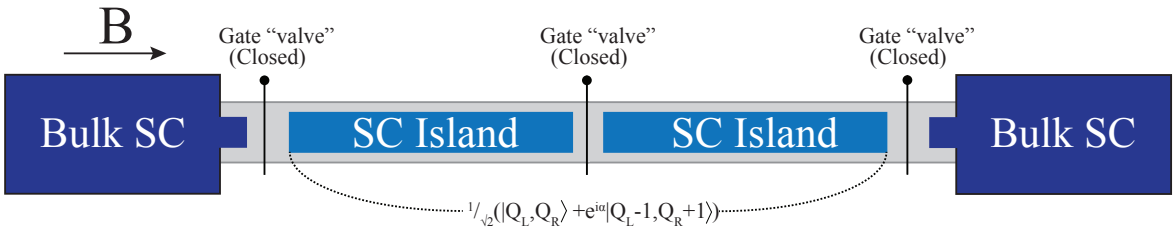

Figure 2.14: ***Coloumb blockaded double island stage****. In a case of closed regime for the all gates, double island device fuses into superposition charge state.*

CHAPTER 3

FABRICATION AND EXPERIMENTAL SETUP

" There's plenty of room at the bottom."

- Richard P. Feynman

In this chapter I will guide you through the entire fabrication process from the Si/SiO_2 blank chip preparation of the wafer to final device that will be placed in dilution refrigerator and low temperature electron transport measurements can take place. I will include brief introduction how semiconducting nanowires are grown and how to prepare such growth substrate with Ti/Au positioned droplets. And finally I will give basics on how the dilution refrigerator works and how it is possible to reach sub-kelvin temperatures for electron transport and readout experiments in nanoscaled 1D hybrid nanowire devices. I will overview the device geometry at the very end of the chapter, pointing out the most important parts that were used to implement charge sensing techniques.

3.1 Blank chips

First step in device fabrication is preparing the Si/SiO_2 substrate where the wires can be deposited and Ohmic contacts, gates can be patterned via electron beam lithography. In order to connect and measure nanoscaled systems, one has to have bonding pads on the substrate from which the device will be connected to the outside world via Al wire bonds. The bonding is accomplished with wire bonder. In order to conduct electron transport experiments in semiconducting nanowires, one must have appropriate insulating substrate so that electrical contacts ar not shorted to each other via the back-gate. In this thesis for efficient tunabilaty of the back-gate, Si/SiO_2 wafers with 500 nm and 200 nm of oxide layer have been chosen and fabricated on. Thickness of the oxide determines your measurements, e.g. leakiness of bonding pads and gates, capacitance to the back-gate.

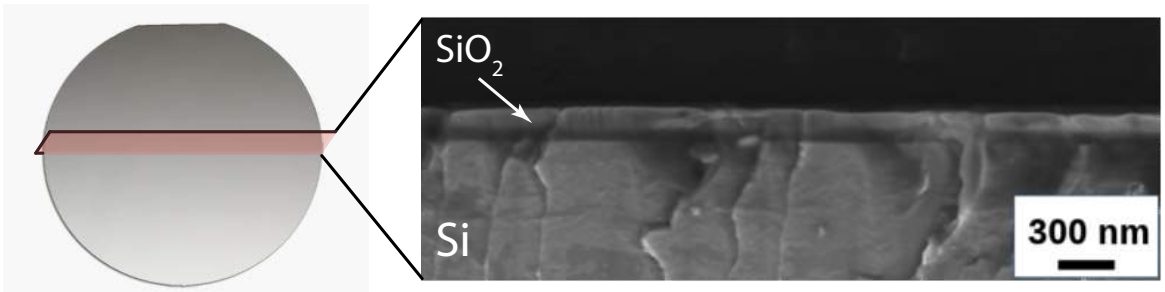

Figure 3.1: ***Cross-section SEM image of Si wafer***. *Left - Si/SiO_2 wafer substrate. Right - cross-section SEM image of Si/SiO_2 wafer showing Si and SiO_2 layers with appropriate thicknesses.*

Electron beam lithography

The 2 inch wafers with 500/200 nm of SiO_2 layer were used. The reason for 500/200 nm oxide thickness is that to gain the ability to control semiconductor charge carrier density with the back-gate by capacitance coupling. Oxide thickness determines how effective and strong the

back-gate will be. It is optional to clean the substrate before proceeding with exposure and deposition steps because usually purchased wafers are clean in the first place.

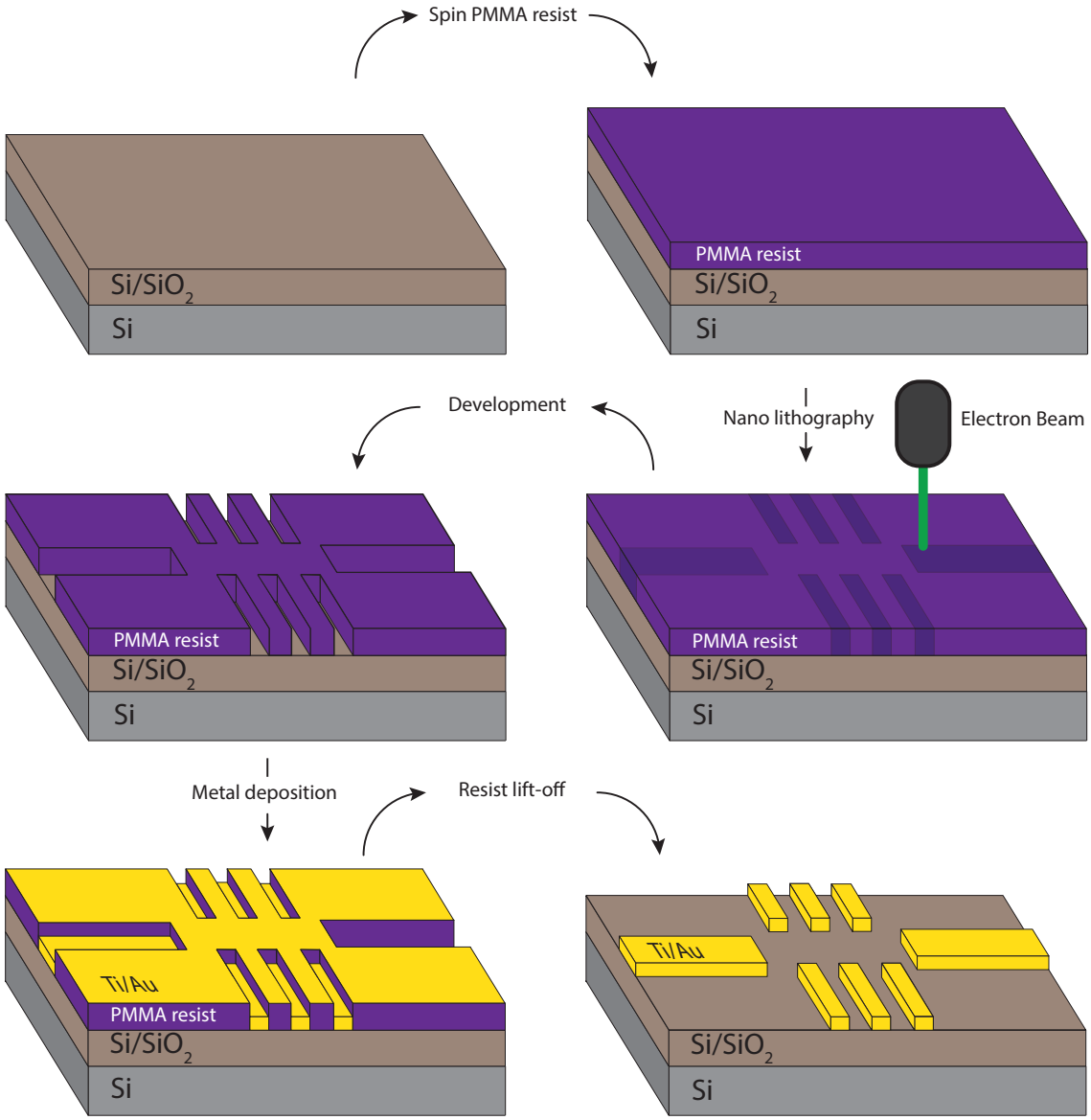

Figure 3.2: ***Electron Beam Lithography (EBL) fabrication steps***. *First step is taking Si/SiO_2 substrate and spinning PMMA resist. The wafer is transfered to electron beam exposure system (ELIONIX) and with drawn design, gates and contacts are defined on the resist. Next, the chip is then developed by immersing in MIBK:IPA 1/3 for 90 s, exposed PMMA resist reacts to developer and is removed in places where it was exposed. The unexposed regions act as a mask and are not removed during development. The chip is then plasma ashed and is placed in metal evaporation chamber (AJA system). Titanium and gold are evaporated on the whole chip. In the final step, wafer is then immersed in hot (55^oC) acetone and left for 60min. The substance reacts with PMMA and peels off the remaining resist, leaving only patterned desired contacts and gates.*

Preparation

1. Take 2 inch Si/SiO_2 wafer (open the box only in cleanroom area!).
2. Immerse the wafer in NMP (N-Methyl-2-pyrrolidone) solution in a plastic cup. Put the cup inside of a sonication bath with applied temperature of 40^oC and type in the frequency and power to 37 kHz and 100 % respectively. Leave it for 5 min.
3. Repeat the 2 step with acetone and IPA (Isopropyl alcohol).
4. Blow dry with nitrogen gun afterwards and insert in plasma asher[1] for 4 min.
5. Spray with acetone and IPA, blow dry with nitrogen.
6. Put the wafer on hot plate of 185^oC for 5 min to bake..

1. Use photoresist AZ1505 as mask for the exposure. By spinning with spinner at 4000 rpm for 60 s
2. Bake Si/SiO_2 wafer at 115^oC for 1 min.
3. Use LED blaster to expose bonding pads and meander contacts.

Development

1. Use AZ Developer for 1 min
2. Rinse the wafer in Milli Q water for 20 s and blow dry with nitrogen gun.

Ti/Au deposition

For this AJA instrument is being used

1. Evaporate 5 nm of Ti at constant 1 Å/s rate. Rotate the sample holder while evaporation at a constant 45% rotation and 10 deg tilt.
2. Evaporate 30 nm of Au at constant 3 Å/s rate. Rotate the sample holder while evaporation at a constant 45% rotation and 10 deg tilt.
3. Evaporate 84 nm of Au at constant 3 Å/s rate. Rotate the sample holder back to initial position (0 deg tilt) but leave the rotation on.

[1] In semiconductor manufacturing plasma ashing is the process of removing the photoresist (light sensitive coating) from an etched wafer

Ti/Au lift-off

1. Immerse into hot NMP 80^{o}C for 30 min
2. Sonication into IPA for 5 min
3. Plasma ash for 2 min.

Finer alignment marks

In order to increase the precision and to find our nanowires on the blank substrate we must write the so-called small alignment marks which dimensions varies from 10 μm to 1 μm. (See Figure 3.3)

1. Spin EL 9 e-beam resist at 4000 rpm for 60 s and bake on hot plate 115^{o}C for 1 min
2. Spin another layer of resist the so-called PMMA A4 type on the same regime and bake as in 1 step.
3. For exposure ELIONIX e-beam lithography instrument was used with 20000 points/ 300 field size/ 5 nA of current/ 120 aperture size.

Development

1. Immerse in MIBK:IPA 1:3 (definition) for 1 min and rinse in IPA for 30 s.
2. Plasma ash for 1 min.

Ti/Au deposition

1. AJA system evaporating with no angle tilt of the substrate and no rotation.
2. Evaporate 5 nm of Ti and 80 nm Au.
3. 55^{o}C Acetone for 60 min.

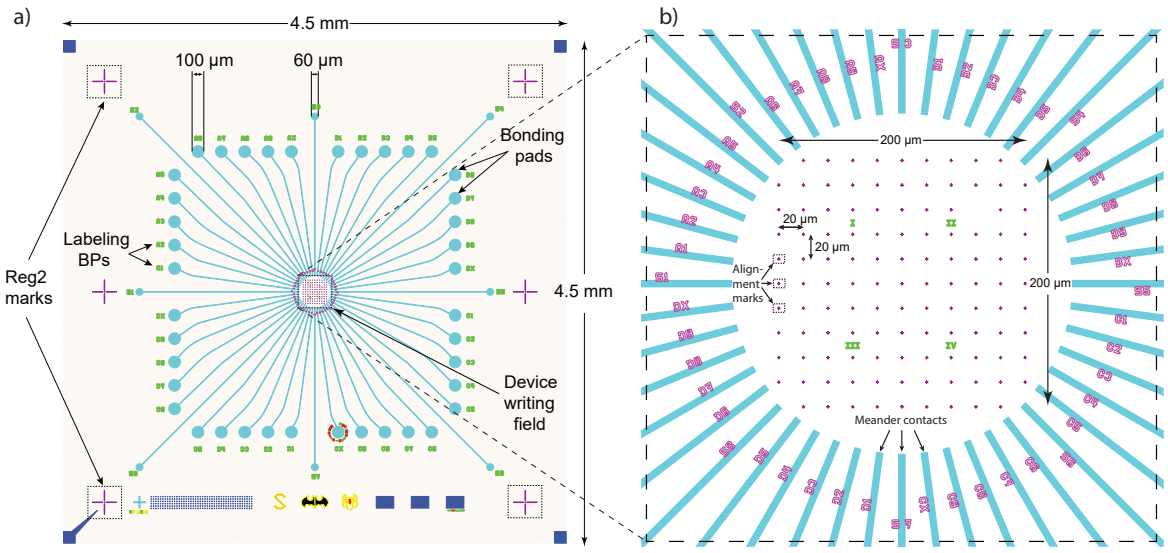

Figure 3.3: ***Fabricated blank chips***. *Completed full fabrication on blank chips with bonding pads, small and big alignment marks, and meander contacts.*

3.2 Molecular Beam Epitaxy of nanowires

In this section I will give brief introduction on basics of $InAs$ nanowire growth in the *Molecular Beam Epitaxy* MBE system.

First nanowires were grown by Wagner and Ellis [32], where they were able to show the vapor-solid-liquid (VLS) mechanism to grown perfect crystal structures without any errors in structure of the entire length of the nanowire. Wires that are presented here in this thesis were grown via VLS mechanism., which has three main thermodynamic phases: vapor phase, liquid phase and solid phase.
All nanowires in this thesis were grown by P. Krogstrup at Niels Bohr Institute in GEN II MBE system. Figure 3.4 shows the schematics of such MBE machine. The system is equipped with effusion cells where pure materials are kept for molecular growth of semiconducting crystals. Materials in the system are: As (group V), In and Ga (group III), Be (group II) and Si (group IV). System also has Au cell as a growth catalist for nanowires. On each effusion cell there is a shutter that can be closed or opened, depending on the usage of the materials. Substrate holder is equipped with thremocouple device in order to control the temperature of the sample. Beam fluxes of different materials is measured with reflection high-energy electron diffraction (RHEED). Cryo-pumps and ion-pump keeps the chamber in ultra high vacuum. In order to have good shielding and cooling of the system in the main chamber, liquid N_2 surrounds the effusion cells and growth chamber. The pressure of the chamber can reach down to 10^{-11} torr.

The growth of nanowires is accomplished by having a metal, say Au that acts as catalyst. If

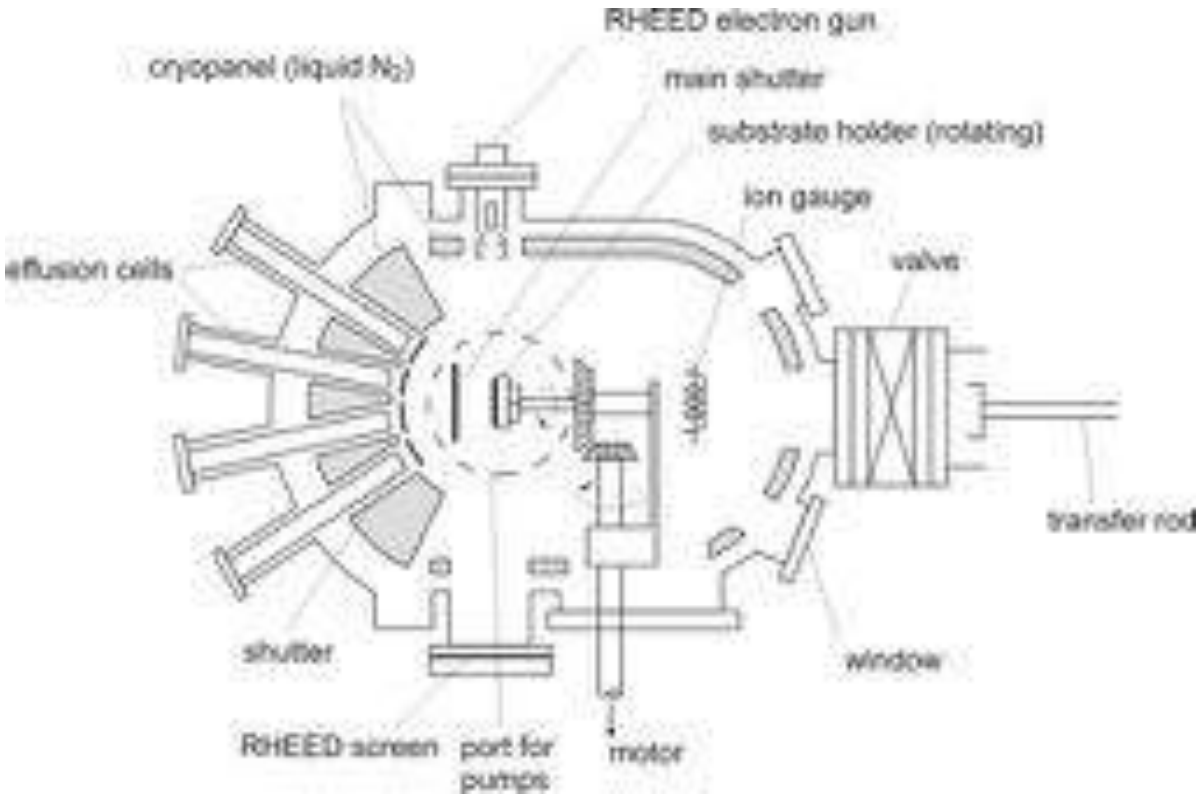

Figure 3.4: ***MBE system schematics***. *Equipped with ultra high vacuum main chamber and outer vaccum transfer chamber. Inside the main chamber there are effusion cells with different materials in hand to use. Rotational substrate holder that can be heated or cooled at anytime [33].*

we pattern holes on the resist with electron beam lithography and deposit the Au metal on the semiconductor, we will have golden particles on the semiconductor surface. The most crucial part is that the two materials have different melting points and once one enters a liquid phase the other stays solid. Then we have a case like in Figure 3.5, where the semiconducting substrate ($InAs$) has Au droplets. At the melting temperature of gold, we introduce a second material in vapor form (Fig 3.5 top right), for that in the MBE system we have As flux source in vapor phase. The liquid Au droplet sinks in the As vapor onto itself and becomes supersaturated. The absorbed material diffuses through the Au droplet and solid $InAs$ substrate, where it tries to minimize the free energy and the growth starts to take place in the crystal orientation of the $InAs$ substrate (Figure 3.5 bottom left). Superconductor (Al) can be introduced from the side with a slight angle, so that the Al can be grown on each nanowire. If the Al would have been deposited without any angle some of the wires would shadow others and the Al would be not on all of them. The Al growth can be half faceted or a full shell superconductor on the wires. But in this thesis the wires ar 3 faceted aluminum in order to have better etch and electron density tunability in the nanowires, as well a better proximity of superconductor to semiconductor.

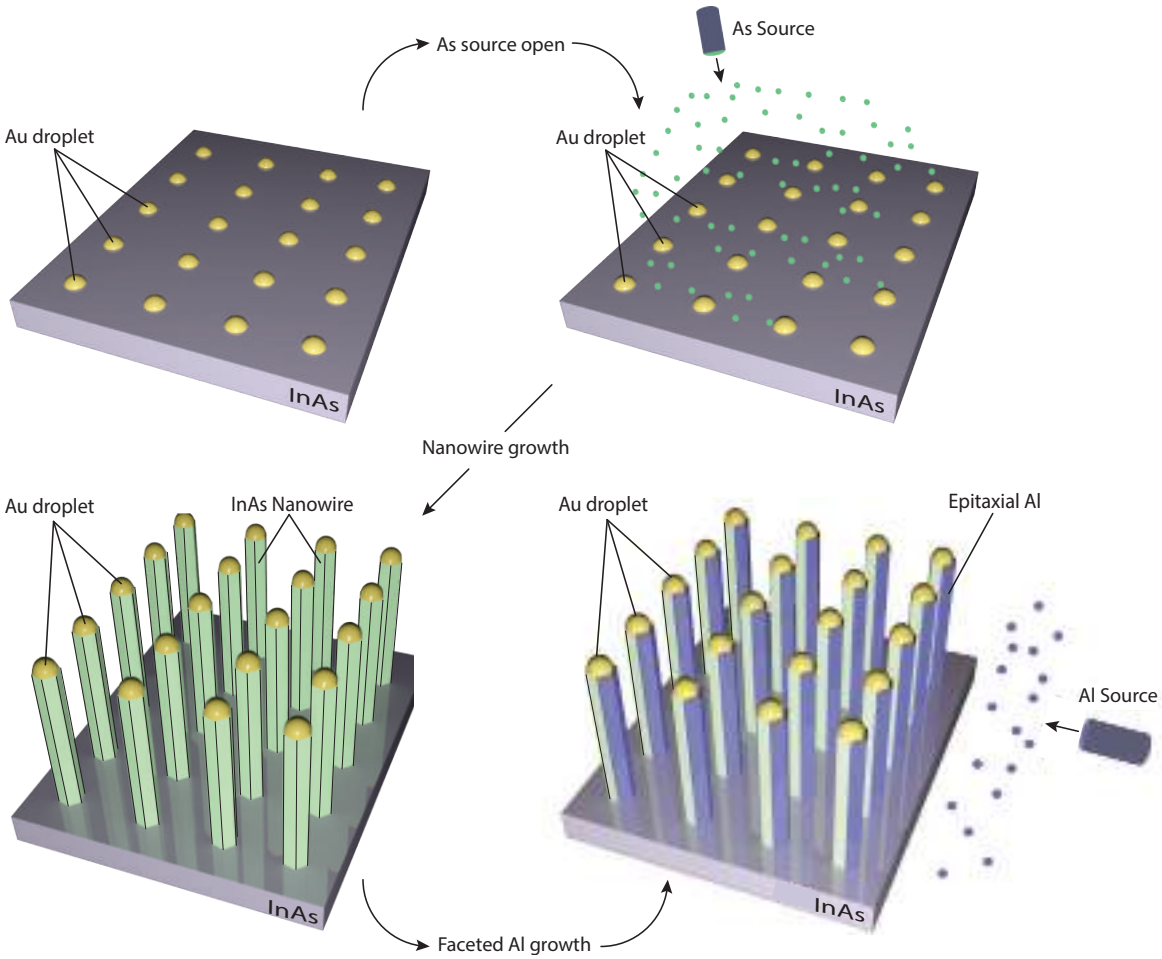

Figure 3.5: ***InAs nanowire growth via MBE system and Al deposition***. *Starting from top figure left - prepared InAs (111) growth substrate with positioned Au droplets in an array. Following arrows to right - the substrate is exposed to As flux and the droplets are supersaturated and As material is diffusing through and reaches the solid (InAs) substrate. Bottom left - crystal growth in (111) direction. Bottom right - Epitaxial superconductor (Al) is deposited from the side with an slight angle in order to cover all the nanowires with Al on three facets.*

3.3 Micromanipulation and device fabrication

The Micromanipulator tool is very useful to have positioned nanowires on any substrates. With devices that will be presented here in this thesis, dry/wet deposition of the wires is almost impossible, because the two different nanowires (with epitaxial Al and bare $InAs$) have to be in close proximity (≈500 nm) and parallel to each other. The chance of having a pair of different wires parallel to each other and distance of 500 nm by dry or wet deposition is very small.

Micromanipulation tool allows to pick up nanowires one by one with 0.2 or 0.1 μm diameter needle from the growth substrate and deposit them on Si/SiO_2 blank chips that have already written alignment marks and bonding pads. The electrostatic forces between the nanowire and

needle is sufficiently strong for picking up and breaking them off from the growth substrate. Insulating substrate (Si/SiO_2) attracts the nanowire once it is close to the surface and the nanowires are stuck.

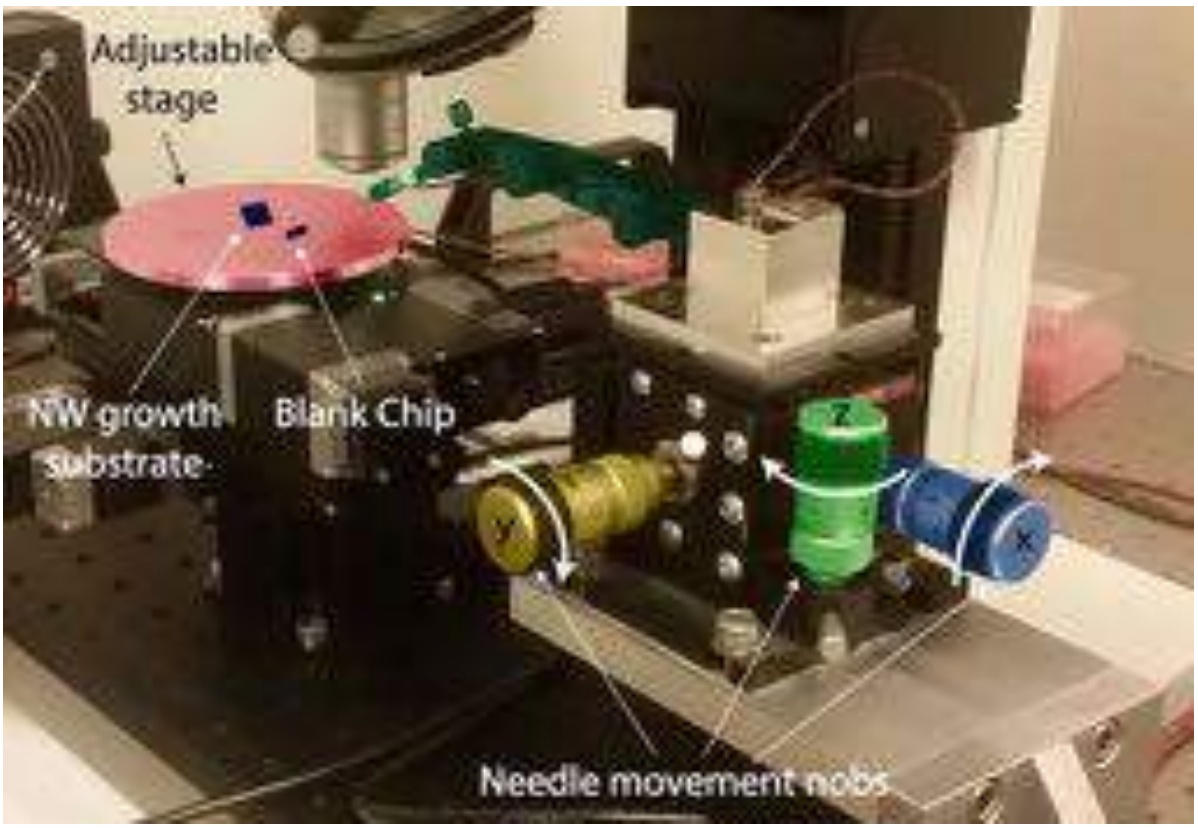

Figure 3.6: ***Micromanipulator tool for positioned nanowire deposition***. *Red - Adjustable stage, blue, yellow, green - needle movement nobs in x, y and z directions,* ***dark green*** *- needle mounting position.*

The wires are then deposited on the blank Si/SiO_2 chip in the area of alignment marks (see Figure 3.8 b).)

Three types of wires have been used for this type of experiment:

1. **Qdev173** growth batch. InAs nanowire of 100 nm in diameter with 2 facet 10 nm epitaxially grown Al.

2. **Qdev418** growth batch. InAs nanowire of 120 nm in diameter with 3 facet 10 nm epitaxially grown Al.

3. **Qdev143** growth batch. Bare InAs nanowire of 140 nm in diameter and 5 μm long.

We place both growth wafers on the micromanipulator adjustable sample holder and in addition we place our blank Si/SiO_2 chip as well. We mount 0.2 μm needle and adjust all the necessary parameters that suits you.

First we pick nanowires with epitaxial Al one by one from the growth substrate and deposit them on the blank chip. Key to have positioned nanowires is to pick them from top and less interaction with the needle in the middle part of the wire. I prefer to search for wires that are already broken off and are on top of the standing nanowires. Then we place Qdev143 (sensor) wires next to the already deposited $InAs/Al$ wire in parallel as close as possible ($\approx$ 500 nm apart). The Qdev143 wires are a bit mobile on the blank chip so it is possible to push with the needle until distance and the angle between two wires is acceptable under the $100x$ magnification microscope.

Roughly 10 separate wire pairs are deposited until it is acceptable for moving forward. I choose to have at least 10 devices on the blank chip. The reason for this is the following. Given the fact that the precision of the e-beam lithography system (Elionix) is roughly 5 nm and the desired gate to wire separation there could be some misalignments and something can be done wrong while exposing or bad lift-off of the contacts and gates, that is why it is better to have more devices to increase the chance of fully working device that can be bonded and loaded in the cryostat.

In order to have the ability to deplete the semiconductor charge carriers with normal metal side gates in specific regions of the wire, one must to remove the metallic part of the wire. Otherwise, the applied voltage to the gate will be screened by the metallic (Al) layer that is on the wire. In that sense, chemical etching of the Al is necessary. Although, the recipe that has been used in this project to remove the Al was quite unstable but nevertheless it works after few trial and errors.

The distance of removed Al has to be in the range of $50-100$ nm. The main reason for this is to create insulating junction (I) from the two superconducting (S) regions. The so called chemically etched region dimensions have to be small in order to have smaller chance of unwanted extra dots in the junction By etching in two regions we are creating a superconducting island in the middle of the wire.

Alumnimun Etching (Transene D etchant)

1. Spin A4 PMMA resist on the chip and bake at 115^oC for 1 min
2. Take 150μm x 150μm optical images of the deposited nanowires on the blank chip that include at least 4 square shaped alignment marks.
3. Align the image with design of the blank chip.
4. Draw 50 - 60 nm etching window boxes and place them on the InAs nanowire that has epitaxial Al.
5. Expose etching window 600 μm writing field and 800 $\mu C/cm^2$ with 500 pA current.
6. Develop the exposed chip in MIBK:IPA 1:3 for 90 s, then rinse in IPA for 30 s and clean with MQ water for 10 s.

7. Plasma ash the chip for 1 min to remove any resist residues in the etching windows. Very important!

8. Prepare one MQ water beaker and Aluminum Etchant type D (aka Transene D) beaker, place them in 55^{o}C bathtub and leave for 15 min.

9. Prepare two extra beakers of MQ water (room temperature) next to the bathtub.

10. Check with a thermometer the temperature of MQ water beaker in the bathtub, if it is ≈ 51^{o}C etching can be proceeded.

11. Use metal tweezer to hold the chip, immerse the chip in Al etchant for 10 s then quickly immerse in warm MQ water (that is next to the etchant, stir for 20 s, and then immerse in other MQ beakers (room temperature) to prevent the etchant in running.)

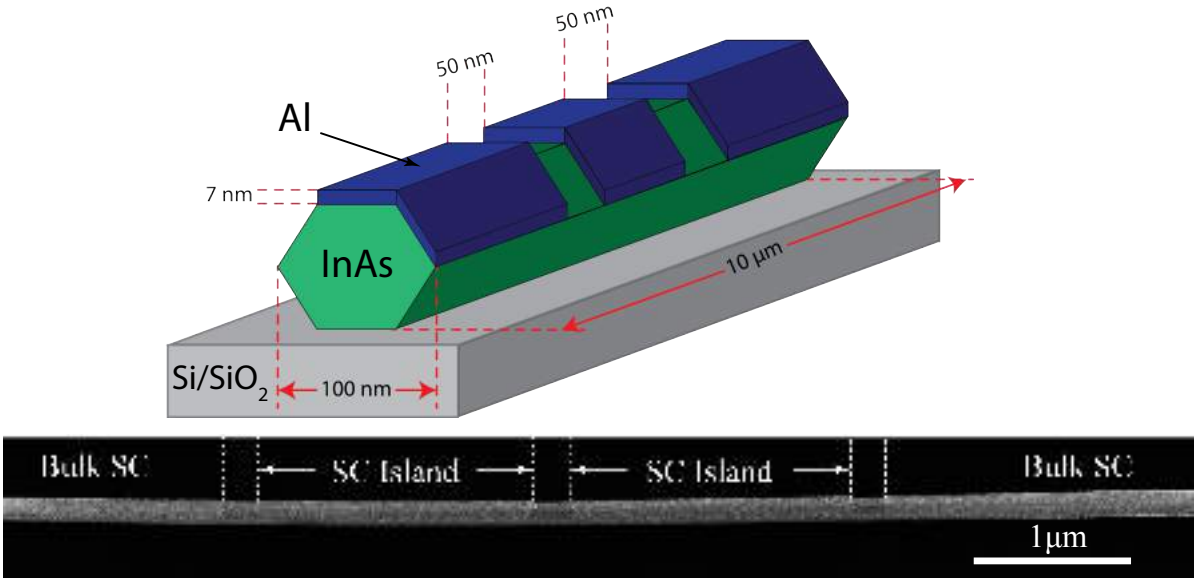

Figure 3.7: ***Aluminum chemical etching on InAs nanowires***. *Top figure - InAs nanowire on Si/SiO_2 substrate with Al etched regions and dimensions. Bottom figure - SEM image of etched InAs nanowire with epitaxial Al in three regions, for making the double dot device with two Al islands.*

For the double dot device (two SC islands) it needs to be etched in three regions separated in above 1 μm apart.

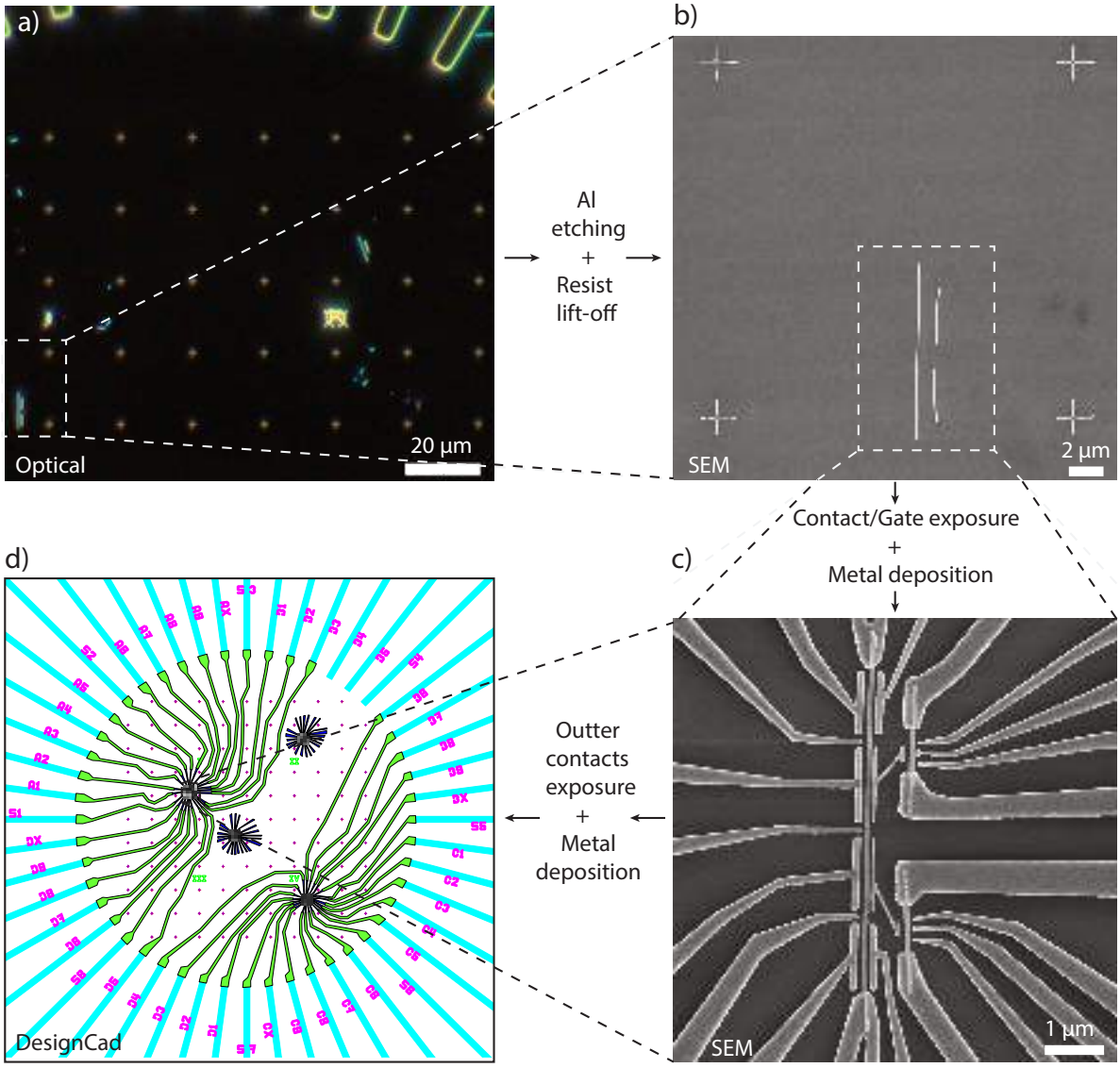

Figure 3.8: ***Device fabrication from Al etching to final product****. a) With micromanipulation tool wires are deposited in such way that there is InAs nanowire with epitaxial Al and two bare InAs nanowires without the superconductor. Spinning PMMA resist and then optical images are taken. Etching windows are drawn in the design and etching recipe is carried out. b) Scanning electron microscope (SEM) images are taken, dimensions of the image have to at least 25µm by 25µm so that the cross alignment marks are visible as well. SEM images are aligned with the design.*

3.4 Dilution refrigerator

In order to perform single electron transport through the double dot devices, one must cool the system down to temperatures where thermal excitations are less than charge excitations ($< k_B T$). By mixing two materials, $^3He/^4He$ is what gives the cooling power that mK temperatures are reached. ^3He atoms are strongly bound to ^4He, then among each other. Atoms of ^3He obey Fermi statistics and with increasing number of density, kinetic energy increases as well. That means

the binding energy is decrease effectively. If ^3He with a concentration of 6.5% is present in ^4He enviroment, the effective binding energy becomes zero as $T \to 0$, and no ^3He atoms can dissolve in ^4He.

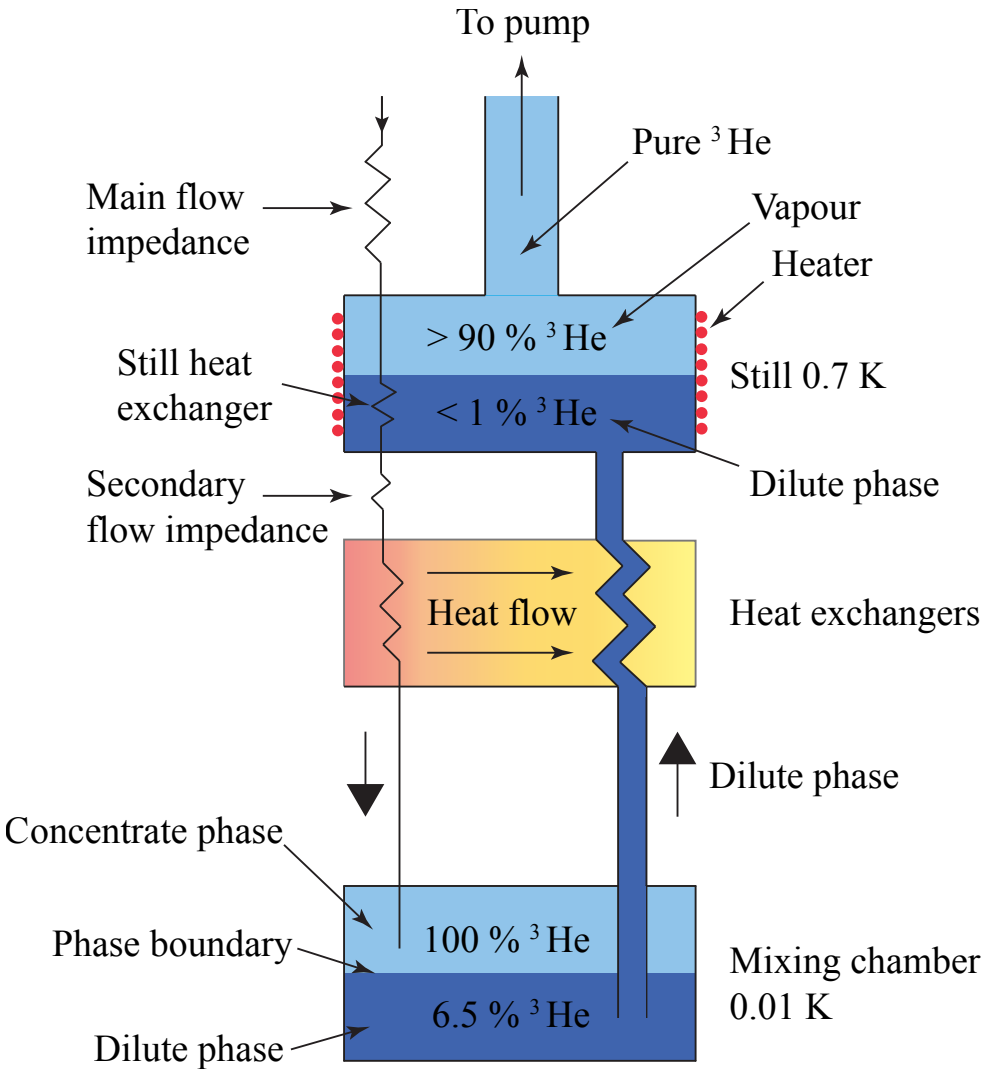

Figure 3.9: $^3He/\ ^4He$ ***based dilution refrigerator schematics***.

We have two phases containing light ^3He-rich and a heavy ^4He atoms. The solubility is highly pressure and temperature dependent. The ^3He atoms in ^3He-rich phase have a lower entropy than ^3He atoms in ^4He phase. This is where the cooling process comes and in the refrigerator this occurs in the mixing chamber and it takes form ^3He atoms are transfered from rich phase to diluted phase (^4He phase).

Devices that were investigated

The fabrication techniques that were introduced have resulted in multiple devices that were investigated and all of the low temperature electron transport and charge sensing measurements were done on them. Here, I will not be directing specific devices to a specific measurements, for the sake of simplicity. All devices were made in a similar fashion, although I will pin point out the main differences that was observed. But in this thesis only side gated devices will be presented.

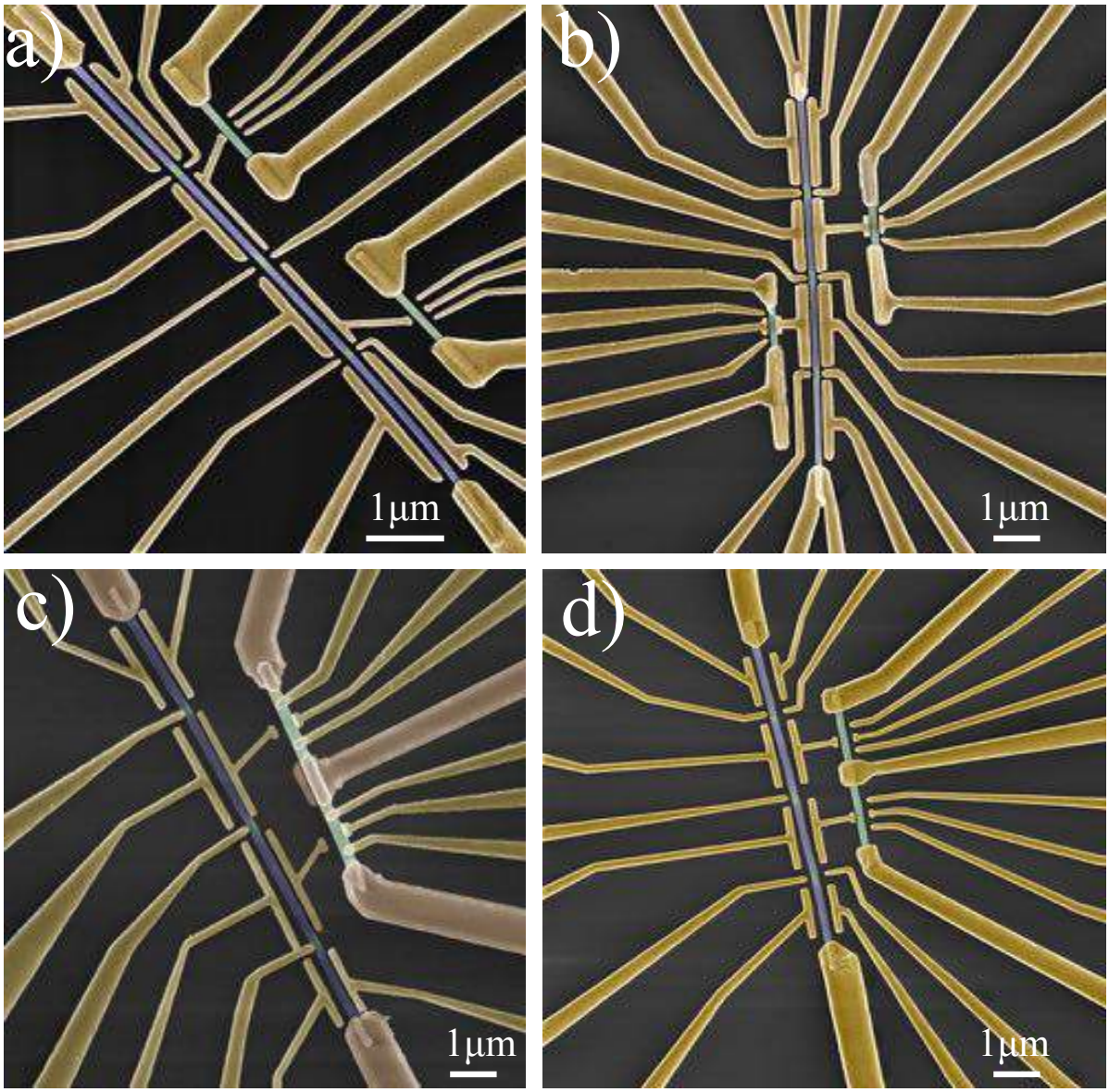

Figure 3.10: ***Devices that were investigated***. *a) Showing side gate device with two sensor wires deposited with micro manipulator on the same side. b) Side gated device with two sensor wires on opposite sides. c) Top gated devices with atomic layer deposition (ALD) and only one sensor wire that can have two quantum dots formed, that could be coupled separately to SC quantum dots of the main nanowire. d) Side gated device with one sensor nanowire.*

3.5 Device overview

Lets look at the device itself for now. The main device consists of etched Al in three regions (Figure 3.11). False coloring gives a distinction between each material. Green - here is denoted as $InAs$ semiconducting nanowire. Blue - epitaxial Al and it was removed in certain regions with etched region of 50 nm in width. The idea here is to have as small etched region, where the tunneling barrier will be created and to have the ability to control charging and Josephson energy ratio. According to [30] the system has to be effectively controlled between $E_J/E_c >> 1$, $E_J/E_c \approx 1$ and $E_J/E_c << 1$. The island length was chosen to be 1.5 μm in length, but due to not perfect etching recipe the etchant runs a bit more to the sides that is why the final length of the Al island is reduced to 1.3 - 1.4 μm in length. One of the reasons to have such long island length is when the device is driven into topological regime and with a parallel magnetic field (B) the islands should host Majorana bound states in each islands. But if the island length is below 1 μm Majorana wavefunctions starts to overlap. Another advantage to have long segments of Al is that charging energy of the island will decrease with increasing length, this gives the opportunity to have better charge sensing data that will be presented latter on.
In order to follow the protocols of [30], one has to have not only double superconducting dot device but also that the system was connected to the outside world by a superconducting leads and the ability to bias the device with source-drain.

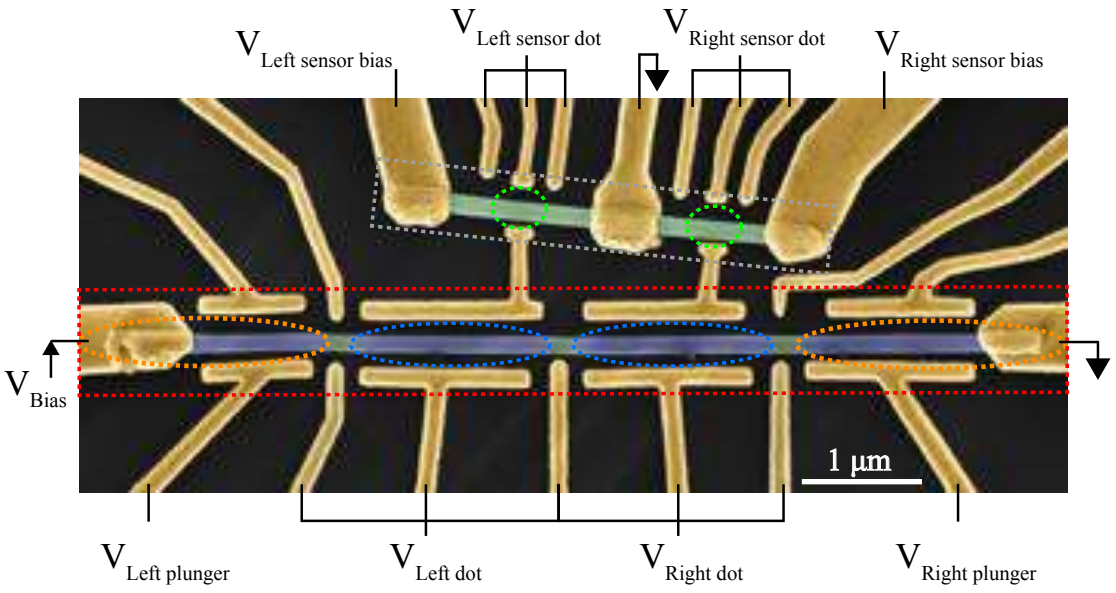

Figure 3.11: ***SEM image of double dot device and explanation***. *Red dashed box - InAs nanowire with epitaxial Al etched in three regions. This region as we call is the main device, where we can tune the system in single and double superconducting island regime. Orange dashed ellipsoid - effectively making two end leads superconducting. Blue dashed ellipsoid - two superconducting aluminum islands. Gray dashed box - nanowire charge sensor device. Green dashed circle - confined quantum dots in the nanowire. Device itself was false-colored, green - InAs nanowire, blue - epitaxial Al, yellow - titanium and gold.*

The device shown in (Figure 3.11) was connected with Ti/Au leads, but the Al on nanowire was not etched at the ends. It was left > 1.5 μm to the etched constriction. Distance is longer than the coherence ξ_0 length of Al and then the system has two superconducting leads (orange dashed ellipsoid), even though it has been connected with a normal (Ti/Au) metal.

Yellow colored contacts that are not touching the nanowires are called plunger and cutters gates. These are our device control nobs to tune the electron density in the semiconductor. "T" shaped yellow gates is what we defined as plunger gates, it uniformly can tune the chemical potential in the nanowire. We know that the nanowires are coated with epitaxial Al only in three facets of the wire, that means other three are bare semiconductor. That is why no screening effects happening if voltages are applied on the plunger gates. Straight line shaped yellow gates is defined as cutter gates, they are more effective in making tunnel barriers once voltage is applied. Charge accumulates at the end of cutter gates and depending on the applied voltage sign, the semiconductor can be depleted (pinched-off) or populated with charge carries. In this system by applying negative voltage on the cutters, semiconductor is being depleted of electrons. As for cutter becomes more negative, the constriction is being populated with electrons and the device becomes more open, so that means electrons are flowing through the device more easily.
By combining one plunger and two cutters ($V_{Left\ dot}$ and $V_{Left\ dot}$), we can isolate individual superconducting islands and create quantum dots that are confined in 2 dimensions. Side plunger gates next to the leads are patterned to tune the superconducting leads from trivial to topological by applying voltage. Epitaxial Al on the nanowire induces superconductivity by proximity effect. So in the final result we have tunable superconducting dots.

Charge sensor [10] in Figure 3.11 top gray dashed box. Bare $InAs$ nanowire has an Ohmic contact with Ti/Au in three regions. Middle contact is grounded and the sensor is biased from two outer contacts ($V_{Left\ sensor\ bias}$ and $V_{Right\ sensor\ bias}$). Three finger gates on each side of the sensor are made in order to confine semiconductor in quantum dot by Coulomb blockade regime. Green dashed circle is the quantum dot position in the nanowire. Below the green dashed circle there is a floating gate, it is not connected to any nanowire, rather it acts as a capacitive coupler between the two quantum dots (Al island and sensor dots). With this floating gate, charge read out on the Al island is accomplished.

[10] Quantum dot that is capacitively coupled to another quantum dot or dots. And can read out the charge occupancy of the other dot or dots.

CHAPTER 4

MEASUREMENTS AND RESULTS

"It doesn't make a difference how beautiful your guess is. It doesn't make a difference how smart you are, who made the guess, or what his name is. If it disagrees with experiment, it's wrong."

- Richard P. Feynman

This chapter is focused on the low temperature (base temperature 20 mK) electron transport measurements of the fabricated double dot devices based on InAs nanowires with epitaxially grown superconductor (Al). These devices were introduced in the fabrication chapter.

For the sake of simplicity, the device geometry in these measurements was the same, so in this chapter the SEM image of the device is the same throughout but actual device for specific measurement was done could be different. Focus here will be side gated devices and how much potential they show in conducting Majorana fusion rule experiment. The most important functions that the device has to show how efficient gates are [1], can the device be tuned into single to double SC quantum dot. Does charge sensing work via capacitively coupled quantum dot that was formed in nearby bare InAs nanowire. Does the SC dots show 2e periodicity in gate voltage and SD Bias space, and how this 2e periodicity changes as magnetic field is applied. Can SC islands host Majorana bound states. These are all primary objectives to test before conducting the full Majorana fusion and qubit experiment.

[1] Fully open tunneling barrier to fully closed barrier range in voltage space. The ratio of interest is E_J/E_C.

4.1 Open/closed regimes

The very first measurements are done by applying constant bias voltage on the device ($V_{Bias\ SD}$ = 3 mV). This is because in order to have electron transport through a device it is necessary to shift the chemical potentials of the source-drain so that SC islands have empty states to accept and transfer single electron. Another reason for conducting high bias pinch-off measurements is that you can neglect charging energy that could dominate the low transport regime. SC islands have BCS density of states, that means island(s) have an energy gap and only transport occurs via excited states. In Figure 4.1 the pinching-off curves presented on a typical side gated device. Three constrictions are investigated separately.

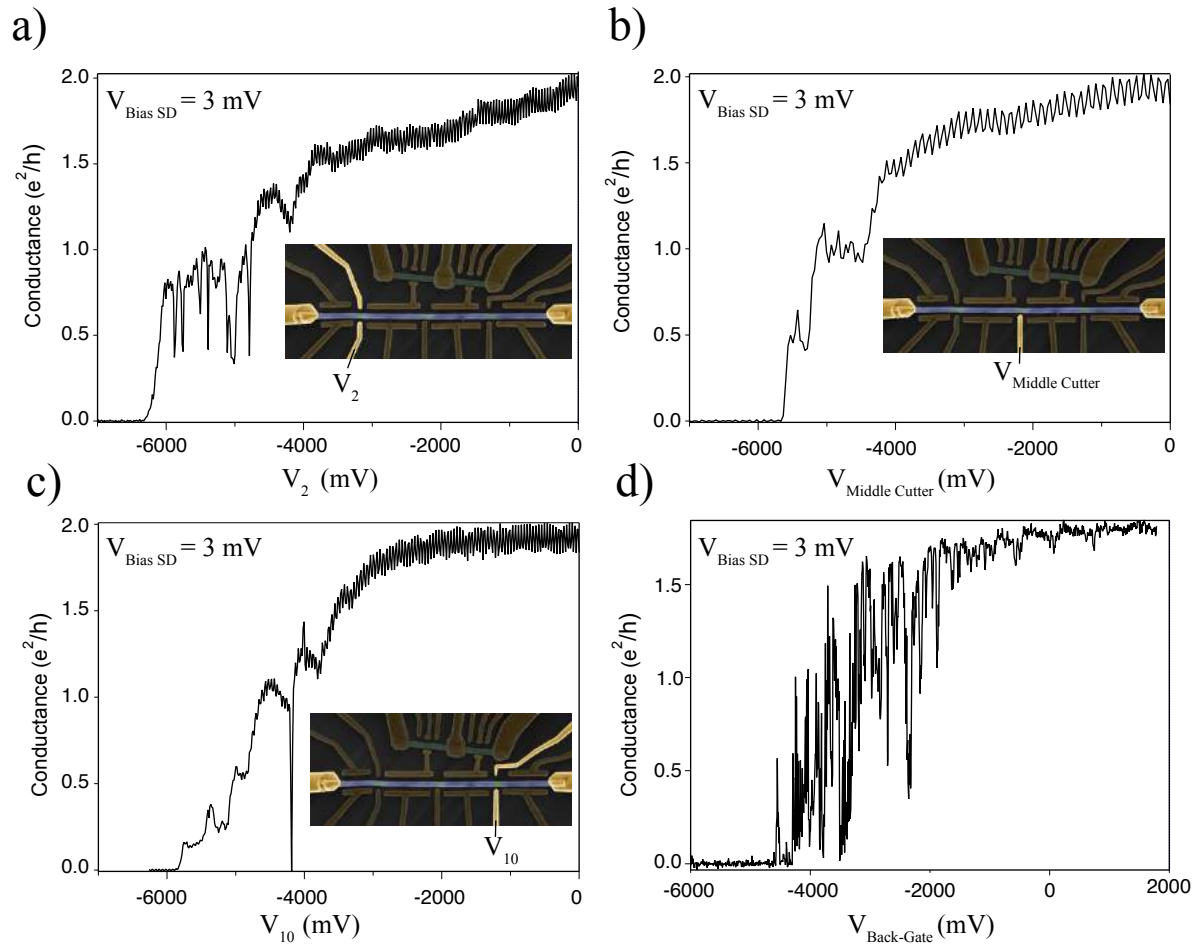

Figure 4.1: ***Open and closed regimes by forming tunnel barriers***. *Applying a constant V_{BiasSD} = 3mV pinching-off curves are acquired. a) pinching-off curve for left cutters of the device. b) pinching-off curve for middle cutter. c) pinching-off curve for right cutters. d) Back-gate sweep to negative voltages, pinch-off region is* ≈ -4 *V.*

Figure 4.1 a) V_2 left cutters are connected in series and voltage has been applied as a function

of conductance in e^2/h units. The pinch off region is above -6 V. In b) Middle cutter is swept and the pinching-off region. As for right cutters in c) pinching-off region was found to be -6 V. The back-gate is also swept and pinching-off curve is shown in d). From three constrictions it is visible that fully open and fully closed range is at least 4 V. In order to conduct Majorana fusion rule experiment the gates have to be manipulated faster then the poisoning rates. Experimental setup can only handle at the moment to apply voltage pulses of range to 2 V. So that means the charging energy will be in our SC quantum dots after from fully closed to half open constriction.

4.2 Quantum dot formation

In order to operate and conduct Majorana Fusion Rule protocols or qubit manipulations one has to tune the device into single SC island and double SC islands with side gate cutters, in a small range of voltages [2] Superconductor is epitaxially grown on the nanowire and in three region the SC was chemically etched in order to tune the electron density in the constrictions, eventually giving the ability to form QD SC island. In Figure 4.2 a) it is shown the devices and highlighted two cutters (V_2 and $V_{Middle\ Cutter}$) that were used to form SC QD island and conductance measured through source-drain. By sweeping those two cutters to negative voltages once can get the 2D scan that shows the stability diagram of the device (4.2 b)). This can also be done with charge sensors that will be presented latter on in the thesis.

In Figure 4.2 b) conductance measurement as a function of two cutter voltages. Coulomb peaks are visible, with a distinctive -45 slope, indicating that two cutters are equally coupled to each other. This gives a strong signature that the devices was tuned into single QD island, while measuring DC transport.

[2] The range has to be around 500 - 2000 mV. The reason for that is voltage pulses on arbitrary waveform generator (AWG) can only handle these ranges, given all the attenuators of cryostat.

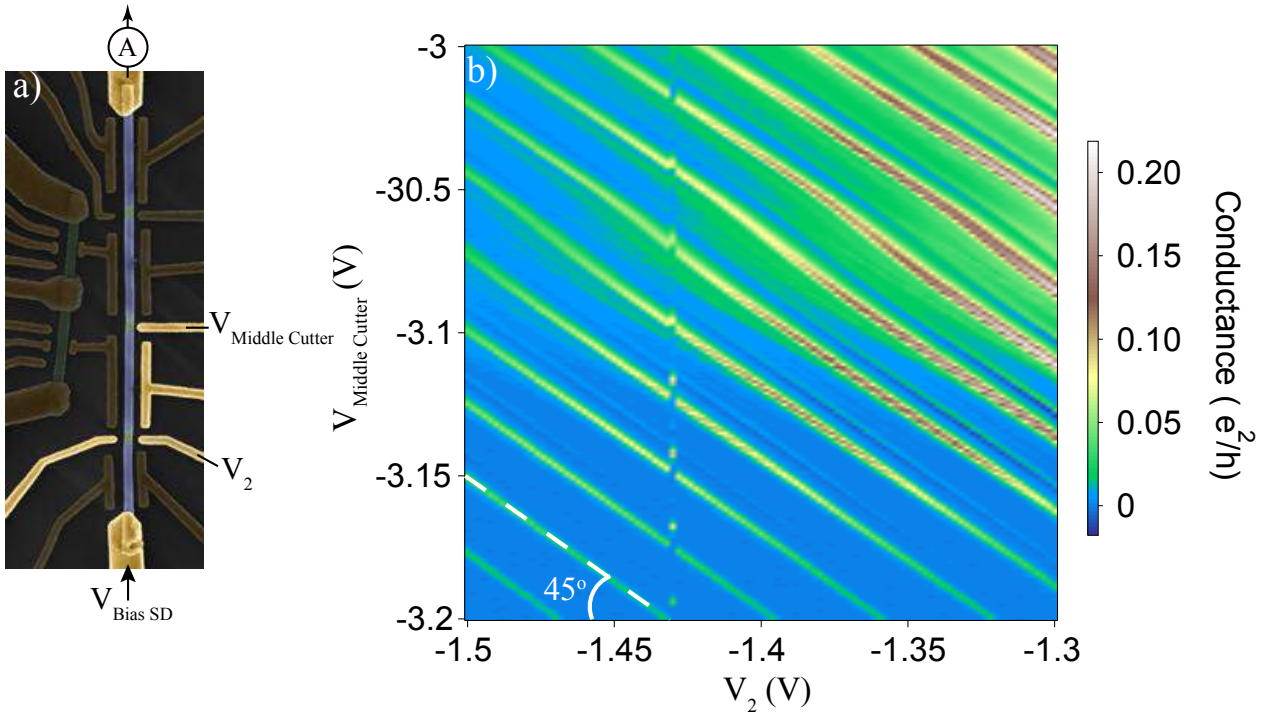

Figure 4.2: ***Quantum SC dot formation by two electrostatic gates****. a) Gates used in order to tune the device into single SC quantum dot. V_2 and $V_{Middle\ Cutter}$ forming tunnel barriers. b) Stability diagram of two tunneling barrier gates, while measuring conductance in units of e^2/h. b) graph indicates that both gates (V_2 and $V_{Middle\ Cutter}$) are equally coupled to each other.*

4.3 Magnetic field dependence

Investigating magnetic field dependence on the SC island device. This is one way to indicate that indeed the islands are superconducting, by reacting to the external magnetic field. In Figure 4.3 a) Showing current measurement while sweeping $V_{Bias\ SD}$. There is no current flowing around zero bias, indicating that indeed there is a superconducting gap $\Delta \approx 0.25$ mV Figure 4.3 b). If one applies perpendicular magnetic field ($B_\perp$) and sweeps the field amplitude, superconducting energy gap starts to get softer and 100 mT it is closed.

Figure 4.3 a) graph shows V_{BiasSD} measurement as a function of Current I, inset to the graph shows and SEM image of the device configuration, where all gates are at zero voltage.

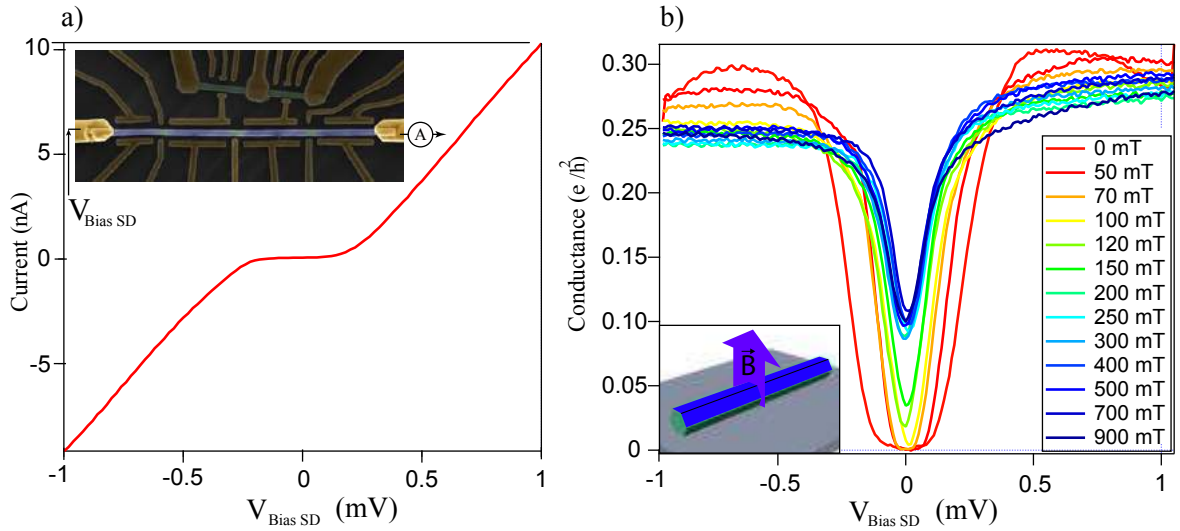

Figure 4.3: ***Bias sweep at different*** $B_\perp$ ***field to the device as a function of conductance****. b) Superconducting gap is seen at 0 mT B field, with increasing magnetic field gap is closing. At* $B_\perp = 100$ *mT the SC gap is closed.*

4.3.1 Quantum dot charging energy

The formed SC QD (single island) Coulomb diamond (stability diagram) sweep is presented in Figure 4.4. In b) it is shown V_3 plunger sweep as a function of $V_{Bias\ SD}$ at perpendicular magnetic field of 1 T. At the same time it is possible to record the current which is presented in c). From the Coloumb diamond sweep it is possible to extract the charging energy E_C of the SC island QD, which is found to be $2E_C = 1.5$ mV.

This specific device was fabricated on a 500 nm SiO_2 insulating layer. The SC island capacitance to ground is smaller compared to 200 SiO_2 insulating layer nm. That means the charging energy is high compared to Al superconducting energy gap Δ, by the following equation:

$$E_C = e^2/2C, \tag{4.1}$$

where $C \sim l$ and l is the distance between back-gate and SC QD. $2E_C$ in this case is $> \Delta$ of Al. This means that observing 2e charge periodicity in these devices is not possible. This will be addressed in Section 4.4.1, when even/odd effect will be presented and discussed. But for now it was decided to switch from 500 nm chip blanks to 200 nm SiO_2 oxide, keeping the same device geometry, since it was not possible to change charging energy of the SC QD by V_3.

At perpendicular magnetic field of 1 T the superconducting gap is no longer observable and there is a normal electron transport at zero bias, Coloumb transport is seen. The SC island E_C is always constant throughout magnetic field sweep and for V_3 plunger sweep.

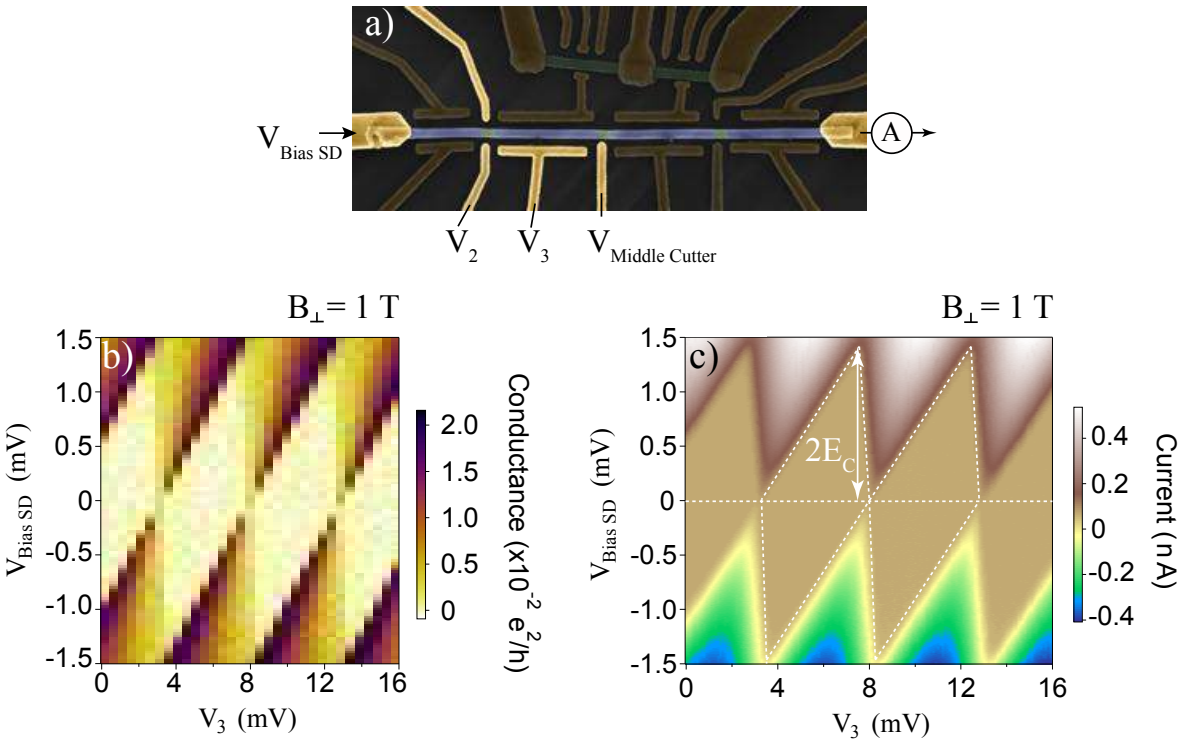

Figure 4.4: ***Coloumb diamonds at finite perpendicular magnetic field.*** *a) Device configuration of the gates used, V_2 and $V_{MiddleCutter}$ forming tunnel barriers while sweeping V_3. Acquired data is the following: b) measuring conductance in units of e^2/h and c) measuring current. The extracted value for the charging energy ($2E_C$) is 1.5 mV.*

4.4 Charge sensing

The principle behind charge readout of quantum dots is to have a nearby another confined quantum dot that is sensitive to its electrostatic environment that can either sens the charge occupancy or give an information of the spin state of the quantum dot.

Charge sensing is known to be a non-invasive measurement technique, that means it is not affecting the quantum dot system of interest. Any small changes in charge of the capacitively coupled quantum dots can lead significant changes in capacitance. Here in this paper *et al L. DiCarlo* [34] investigated double quantum dot in $GaAs/Al_{0.3}/Ga_{0.7}As$ heterostructure 2DEG with patterned electrostatic gates on an insulating ALD grown layer on top. The same techniques were successfully implemented in nanowires in this thesis and are presented.

The device is fabricated in such way that charge occupancy of the SC island(s) can be readout by another InAs nanowire that was placed near by. On the sensor nanowire we can form a quantum dot by three side gates (8, 6 and a plunger gate (V_7) Figure 4.5 a). Once QD is formed in charge sensor nanowire, the plunger gate (V_7) tunes QD states, meaning browsing through Coulomb resonances.

One can choose a single conductance peak that is both sharp and narrow in width (Figure 4.5 c)). After stable[3] resonance peak is found, one can "park" on the edge of the Coulomb peak Figure 4.5 d) green and orange circles. This placement is very important, because it determines how sensitive changes will be in SC dot, peak sidewall has the highest differential change in plunger (V_7) gate space. In contrast, peak point has the lowest dI/dV change.

Charge sensing is accomplished via capacitive coupler (Ti/Au) (Figure 4.5 a)) which was patterned along with other gates and contacts. Any electron that "jumps" on SC island will change the SC QD capacitance, which directly changes coupling to the sensor QD.

Next step, measure the sensor conductance as sensor plunger gate (V_7) is swept and at the same time sweeping the side plunger gate (V_3) that is next to the SC island (Figure 4.5 b)). Note, that SC single island dot was already formed in previous measurements by outer cutter side gates (V_2 and $V_{Middle\ Cutter}$). From the latter graph, it is visible conductance peak that is coupled to both side plunger gates (V_3 and V_7) having 45^o slope. Graph d) shows sensor conductance peak, green and orange circles on the side of the peak indicates different slope cuts in b) graph. Also, from the figure b) it is observed that the peak has frequent "jumps", this is due to V_3 gate tuning the SC QD states and transporting single electrons through the dot. More visible electron "jumps" on the charge sensor are depicted in Figure 4.5 c) and e), where two different slope (n and m) cuts are taken in graph b). In graph c), "sawtooth" electron transitions with a slope k, whereas e) was extracted with a different slope cut l, giving "staircase" electron hoping. This technique shows that charge sensing with two separate nanowires can be accomplished by capacitively coupled floating metal (Ti/Au). The only way these different slope cuts (k,l) can be done is by cross-compensation with other gates, e. g. sweeping sensor plunger (V_7) it is necessary to cross-compensate by SC island plunger ($V_{3\ Compensated}$) to stay on chosen slope (k or l) to have "sawtooth" or "staircase" like electron transitions.

Looking closely in Figure 4.5 c) and e) ("sawtooth" and "staircase") electron transitions. One has the option to count electrons or to see the boundary of charge states, by choosing slope k or l Figure 4.5. e) Right hand side axis counts the charge number. Spacing between $e+n$ and $e+2n$ is the same, where $n=(-2,-1,0,1,2)$. The charge number fits well with the first three plateaus (until $V_{3\ Compensated}$ = -841 mV), but then the plateaus are miss aligned. This indicates that following slope l, charge number spacing is only valid in small gate range of $V_{3\ Compensated}$. As for graph c) of Figure 4.5, it is observed that maintaining on the same charge state (spacing e and $e-1$), electron transition in "sawtooth" are observed in a larger gate ($V_{3\ Compensated}$) range space then of "staircase" cut slope k. It is visible that the spacing between e and $e-1$ is the same on both graphs (c) and e)) in conductance of 0.05 e^2/h.

[3]Sweeping back and forth the plunger gate the peak position stays the same. Peak is well defined and smooth Gaussian distributed function. Peak is separated between other resonance peaks by fully Coulomb blockaded peaks.

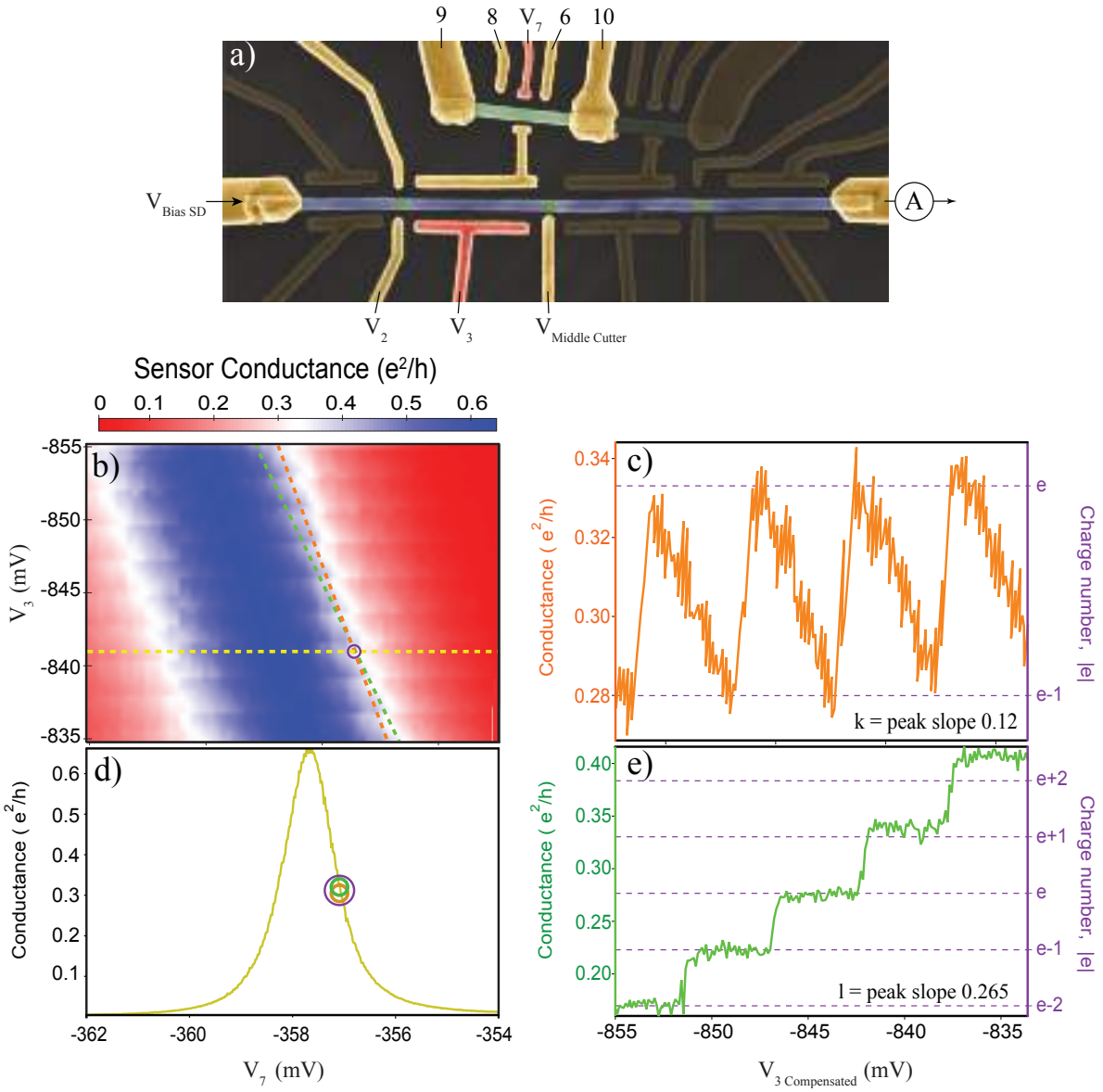

Figure 4.5: ***Charge sensing technique used to readout charge occupancy of SC island(s)***. *a) Device and gates highlighted used in forming QDs on sensor and on SC island device. b) Two plunger gate sweep while measuring conductance on the sensor, three different cuts are shown in c), d) and e). c) cut taken of b) graph, showing sensor Coulomb blockaded peak used for charge sensing. d) cut taken of b) graph showing sawtooth single electron charge sensing. e) cut taken of graph b) indicating staircase single electron charge sensing.*

4.4.1 Stability diagrams

With the charge sensing working, Coloumb diamonds are taken by sweeping V_3 changing the chemical potential of the formed quantum dot (Figure 4.6) and at the same time sweeping V_7, while measuring conductance in units of e^2/h.

Measuring DC transport in Figure 4.6 b) to that shows Coloumb diamond physics with

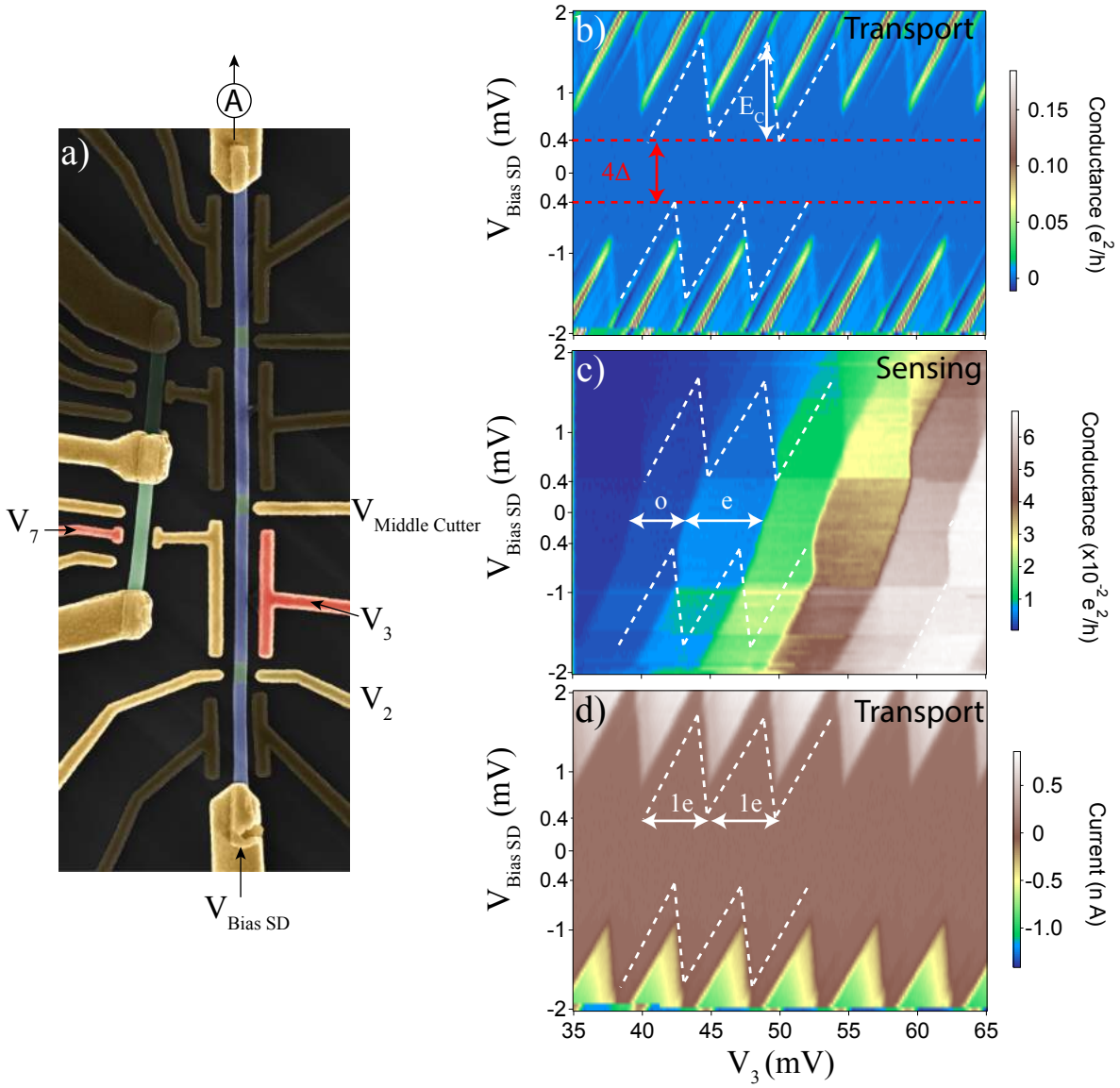

Figure 4.6: ***Charge sensing used for Coloumb diamonds readout***. *Formed QD by side gated cutter (V_2 and $V_{Middle\ Cutter}$) Coloumd diamonds are taken in transport regime b) and charge sensing data c) at the same time. Current measurement was also registered d). Charging energy E_C was extracted from b) and was found to be* 1.5 *mV. The superconducting gap* Δ *was found to be* 0.4 *mV. Charge sensing data indicates even/odd parity structure inside of a superconducting gap (c)). Current measurement data shows 1e periodicity at high SD bias (d)).*

superconducting energy gap of $\approx 4\Delta$. E_C can also be extracted at 0 magnetic field. Figure 4.6 c) charge sensing data take along with transport Coloumb diamond sweep. Here charge sensing gives a distinctive advantage over transport data. It charge sensing it is possible to see charge states inside a superconducting gap. Charge occupancy indicates, at $V_{Bias\ SD}$ = 0 mV bias, an even/odd periodicity. At 0.4 mV $V_{Bias\ SD}$, only 1e periodicity is observed, single electron transition.

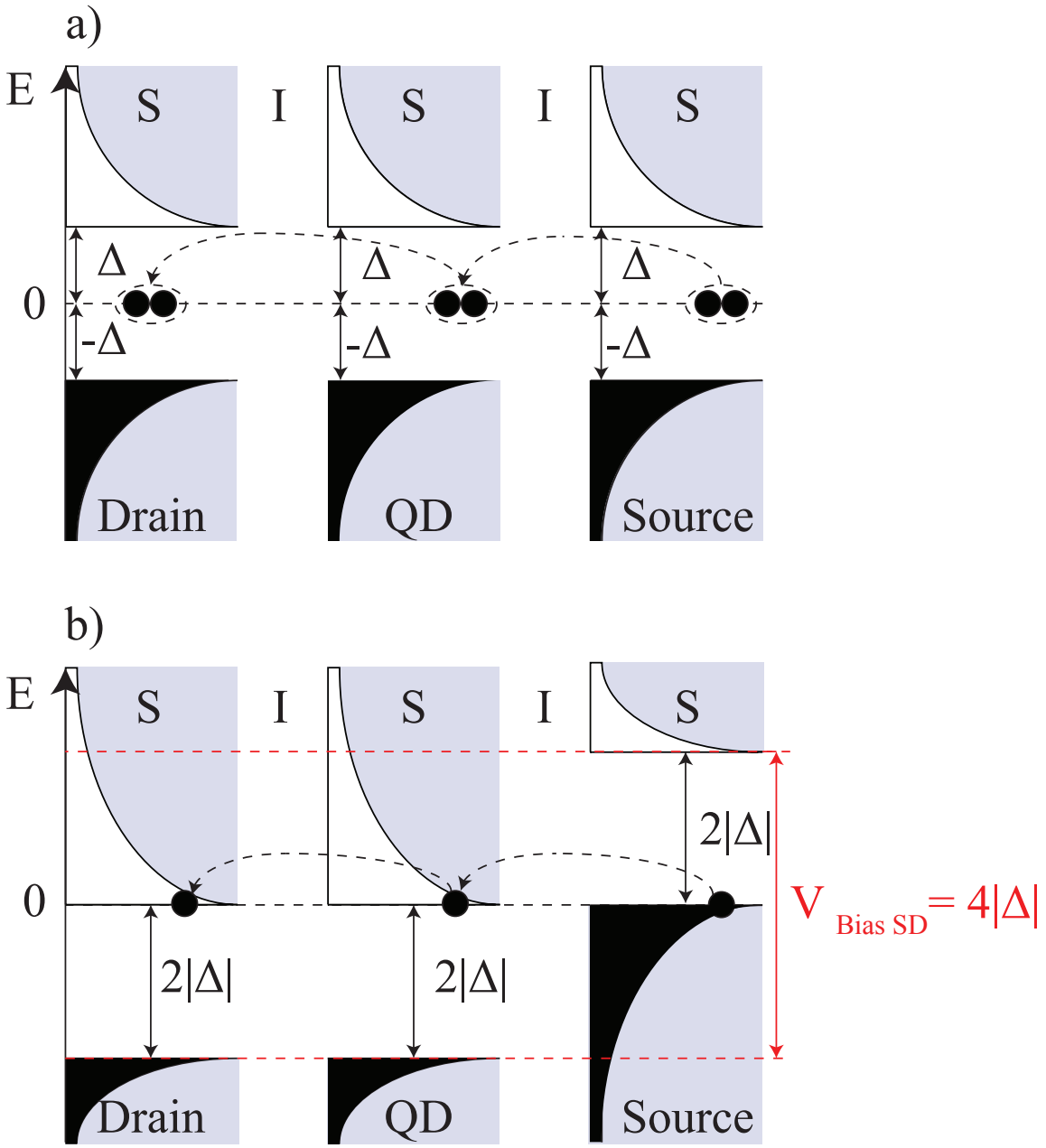

Figure 4.7: ***Schematic representation of energy diagram in SISIS (S - superconductor, I - insulating) geometry device***. *Cooper pair transport a) and single electron transport through b) superconducting QD take place. At $V_{SD} = 0$ only Cooper pairs are allowed to tunnel through the QD a) because other quasiparticles are gapped by superconducting energy gap (Δ). If QD is tuned in the regime as shown in b) then by applying $V_{SD} = 4|\Delta|$ single electron tunneling events take place and we see current flowing. The system then is said to transport only 1e charge at a time in respect to gate voltage on the QD.*

4.4.2 Single to double quantum dot

In the device that were fabricated, one can tune the chemical potential of the InAs to make effective energy barriers via electrostatic gates nearby. In this measurement shown how to tune the device from single to double quantum dot. All measurements here were done by charge sensing, meaning the charge occupancy was readout of each dot by V_7 formed dot on the sensor nanowire (Figure 4.8 a)). The main island nanowire [4]. a) blue colored wire) was grounded and there was no current flowing through the source-drain, this allows to completely reduce the excitation coming from the lock-in, effectively reducing extra noise from SD leads.
Also by forming a tunnel barriers by of the outer gates (V_3 and V_9) and kept constant throughout this measurement. The main gate $V_{Middle\ Cutter}$ was changed, allowing to form two quantum dots on each SC island (Figure 4.8 b), c), d) and e)). Two plunger gates (V_3 and V_9) were swept at the same time and charge sensing technique was used here to record charge occupancy of each SC QD. In Figure 4.8 b) $V_{Middle\ Cutter}$ was fixed at -3.6 V and V_3 plunger gate (left dot) was swept as a function of V_9 plunger gate (right dot). This resulted in fully double dot charge occupancy, where the same charge is transfered from left dot to right dot and vice versa.

The gate configuration was such that outer gates were tuned to have transparent energy barrier between bulk SC (Al) and Al island. We start of in Figure 4.8 a) where the outer gates are in a tunneling regime[5].

[4]The Al covered InAs nanowire with source-drain connected.
[5]Tunneling barrier is formed and charging energy is higher then E_J

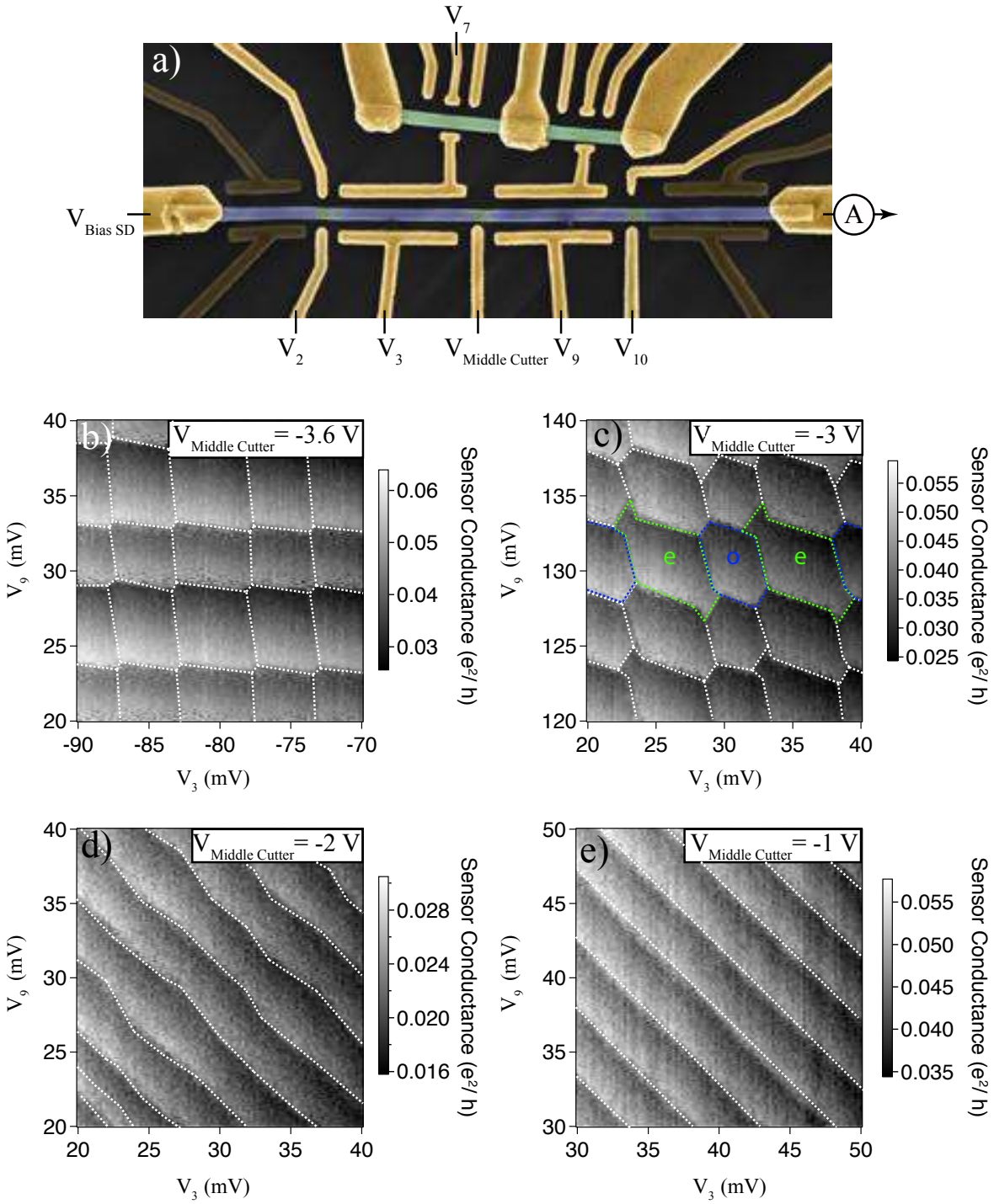

Figure 4.8: ***From single SC QD to double SC QD in charge sensing***. *a) Showing the device gate configuration, V_2 and V_{10} gates used to form tunnel barriers and they are fixed throughout this measurement. $V_{Middle\ Cutter}$ gate was used to change from double QD at negative voltage value to single QD to positive voltage values. b) Shown the double QD charge sensing data, were two axis represent (V_3 and V_9) plunger gates, while tunnel barrier is formed on the $V_{Middle\ Cutter} = -3.6$ V. c) As the $V_{Middle\ Cutter} = -3$ V is more opened, honeycomb pattern is observed and indicating an even/odd behavior in one of the QD. d) Observing transition from double dot to single dot structure, while $V_{Middle\ Cutter} = -2$ V. e) At $V_{Middle\ Cutter} = -1$ V device is fully tuned into single dot regime.*

4.5 2e to 1e transition in B field

In this measurement it is confirmed that SC island is truly 2e periodic, meaning that only Cooper pairs tunneling in and out of the formed SC quantum dot. First, the device is tuned back in single dot regime (tunnel barriers V_2 and $V_{Middle\ Cutter}$, QD states tuned via V_3 side plunger gate) (Figure 4.9 a)). At zero magnetic field ($B_{\perp,||}$), Coloumb diamonds ar acquired Figure 4.9 b). At $V_{Bias\ SD}$ = 0 mV there is a supercurrent signature. Normal current is transformed into suppercurrent at the lead superconductor interface, through Andreev reflection process [35]. During Andreev reflection, electron coming from the normal metal is reflected as a hole at the same time adding one more Cooper pair to the condensate.
From Figure 4.5 a) it's clear that this periodic supercurrent only occurs in 2e steps, because at high $V_{Bias\ SD}$ ($\approx$ 0.1 mV) it is visible that electron transport is 1e periodic.

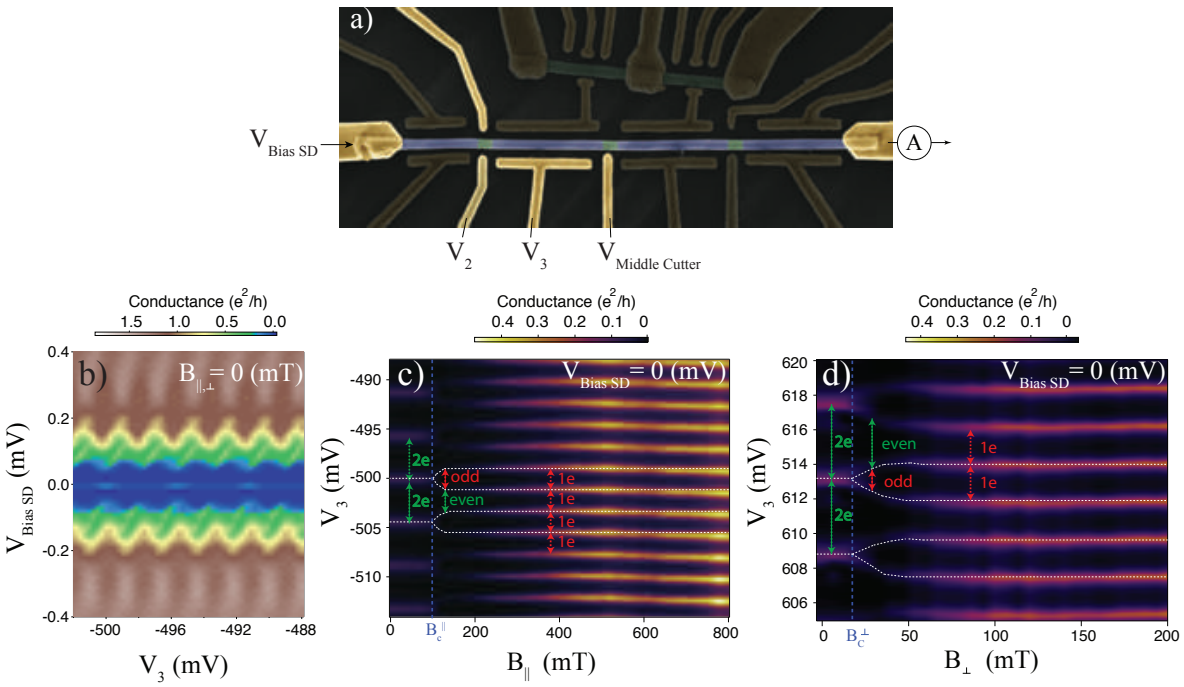

Figure 4.9: ***2e transition to 1e periodicity as a function of B-field****. a) SEM device image and highlighted gates that were used, V_2 and $V_{Middle\ Cutter}$ forming tunnel barriers and at the same time making single SC quantum dot. V_3 plunger gate tuning the quantum dot levels. b) Coloumb diamond data at $B_{\perp||}$ = 0mT, showing superconducting energy gap (smaller then Δ_{Al}). Supercurrent peaks are observed at $V_{Bias\ SD}$ = 0 mV in 2e periodicity. At $V_{Bias\ SD}$ = 0.1 mV 1e peak periodicity is observed. c) $B_{||}$ magnetic field sweep as a function of V_3 plunger gate on the SC QD. Conductance peaks are observed with 2e periodicity spacing. Peaks are then split at critical $B_C^{||}$ field into two conductance peaks. Spacing becomes even/odd periodicity until $B_{||}$ = 200 mT, peak spacing is 1e periodic through multiple V_3 plunger gate values. d) $B_\perp$ magnetic field sweep as a function of V_3 plunger gate. At $B_\perp$ = 0 mT, 2e peak spacing is observed ($V_{Bias\ SD}$ = 0mV). Increasing $B_\perp = B_C^\perp$, 2e peaks start to split and even/odd peaks observer. $B_C^\perp$ was found to be 25 mT. At $B_\perp$ = 50 mT the peak spacing becomes 1e periodic.*

Next step is to show that how these supercurrent peaks behave in different magnetic field

directions, with increasing B field amplitude.

Now staying at zero SD bias and sweeping V_3 plunger gate as a function of parallel magnetic field amplitude (Figure 4.9 c) and d)). First aligning the vector magnet so that it is in parallel with the nanowire and sweeping the magnetic field amplitude (Figure 4.9 c)). As the magnetic field amplitude is increased up to critical value $B_C^{||}$ = 100 mT, the peaks start to split into two. The same phenomena can be seen in a perpendicular magnetic field Figure 4.9 d), where the 2e supercurrent peak splitting occurs at $B_C^{\perp}$ = 25 mT. In both cases after the peaks split, the charge states are driven in even and odd configuration. Meaning, electrons now can tunnel as a Copper pair or single electron. As the magnetic field amplitude is increased up to 200 mT in parallel field, peak spacing becomes perfectly 1e periodic.

As for perpendicular magnetic field sweep 1e periodicity is observed already at 50 mT. This could be indication that the SC QD has been driven into a normal state where there is no Cooper pair tunneling, superconductivity is destroyed. There could be another phenomena happening in such device configuration is that the SC QD has been driven into a topological state when the peak spacing became 1e periodic but only in parallel magnetic fields. Such statement could be true if at the ends of a SC island there are Majorana bound states living at zero energy. This has to be confirmed on either spectroscopic measurements by probing zero energy states of the dot with a normal lead or making entire Fusion rule protocols and see if it agrees with the expected results.

Peak splitting can be understood from energy parabola spectrum in Figure 4.10. The following function that energy parabola spectrum are drawn is:

$$E_n(V_{Gate}) = E_C + E_\Delta, \quad E_C = \frac{(ne - Q_G)^2}{2C}, \tag{4.2}$$

where C - capacitance, V_{Gate} - plunger gate, $Q_G = C_G V_G$ charge on the dot (assuming $C_G = const$). e - electron charge, n - electron number and E_Δ - supercunducting pairing energy. If $E_C = \Delta$, then charge state is odd. In the case of $E_C \to 0$, then charge state is even. Increasing the $E_C >> \Delta$ the charge occupancy becomes 1e periodic in each parabola or in another case if $E_C = const$, reducing $\Delta \to 0$, charge states becomes also 1e periodic.

In Figure 4.10 shown on horizontal axis is V_3 plunger gate voltage. From Figure 4.10 it is visible as the magnetic field amplitude is increased (along the wire direction), the odd parabola is moving down indicating the reduction of superconducting gap Δ. Once Δ = 0 charge state parabolas are evenly spaced with aperiodicity of 1e. Figure 4.10 b) is taken at finite magnetic field ($B_{||} = 120mT$) from the graph of 4.9 c). This indicates that after the critical magnetic field $B_C^{||}$ (after supercurrent peaks are split), there is a new single electron state (odd) in the SC quantum dot. Even/odd effect has been already seen in other systems placed in external magnetic fields [36]

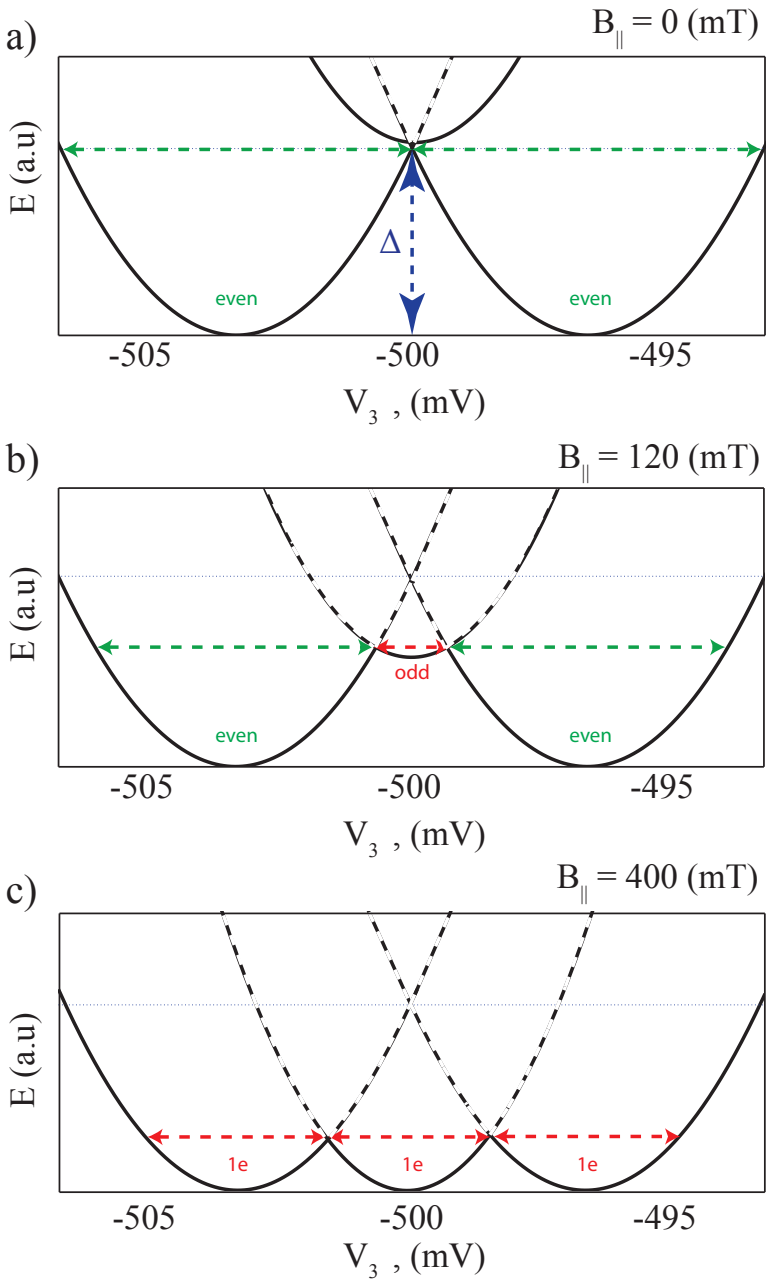

Figure 4.10: ***Charge state parabolas with different magnetic field values***. *Charge state parabolas indicating different electron number on the SC island can be plotted given the equation 4.2. a) illustrating data take in Figure 4.9 at zero parallel magnetic field. There is a two even charge states where only Cooper pair transport is observed. On the x-axis - electron number, which can be read as V_3 plunger gate voltage, y-axis - energy of the charge state given by the equation 4.2. As the magnetic field amplitude is increased b) to $B_{||} = 120\ mT$ odd state parabola is lowered due to superconducting gap Δ reduction. At sufficient high magnetic field ($B_C^{||} = 400\ mT$ the odd parabolas "came" down to zero energy state and now single electron (1e) transport is observed.*

4.6 Search for Majorana

Tuning the device in topological regime and probing zero energy states requires populating the outer superconducting leads with electrons, via V_{11} and V_{12}. This gives the ability to effectively make the superconducting leads switching to normal at sufficiently low magnetic fields. As one has normal leads and a tunneling barrier, it is possible to conduct spectroscopic studies of zero bias features at sufficient high magnetic fields This has already been done *Deng et al* [38]. But since the devices that is investigated in this thesis, the leads are made as superconductor.

The outer lead plungers (V_{11} and V_{12}) were set to +8 V. Magnetic field was aligned to the nanowire direction ($\pm 1^o$) and V_{SDBias} was swept as a function of parallel magnetic field amplitude ($B_{||}$) (Figure 4.11 a)). This 2D scan can be split into six main cuts that are of interest to analyze.

Cut b) at V_{SDBias} = 0 mV along the parallel magnetic field. Small supercurrent signature of 0.02 e^2/h conductance is visible at zero magnetic field. This zero bias conductance peak is dimmed at 150 mT, but at ≈ 275 mT observing significant increase in conductance of 0.15 e^2/h and it is decreasing as the magnetic field amplitude is increase.

Cut c) is at zero parallel magnetic field showing hard superconducting energy gap with two subgap states at ≈ 0.1 and −0.1 mV of $V_{SD\ Bias}$. Also on this graph there is a small supercurrent signature of 0.02 in e^2/h units.

Cut d) is at 100 mT parallel field, where hard superconducting gap is soften and two subgap states are already inside the quasiparticle spectrum.

Cut e) is at 200 mT, softening of the gap is even more significant and no subgap states are observed.

Cut f) is at 275 mT zero bias conductance is observed (black arrow) with 0.15 in e^2/h units.

Cut g) is at 400 mT, zero bias conductance peak is gone and the superconducting gap continues to collapse.

Further investigations need to be done in order to confirm at which gate voltages does the SC island transitions to topological phase and hosts pair of Majoranas. The interperation of zero bias conductance is not conclusive enough, there fore a different kind of devices need to be tested which will be presented in the outlook of this thesis.

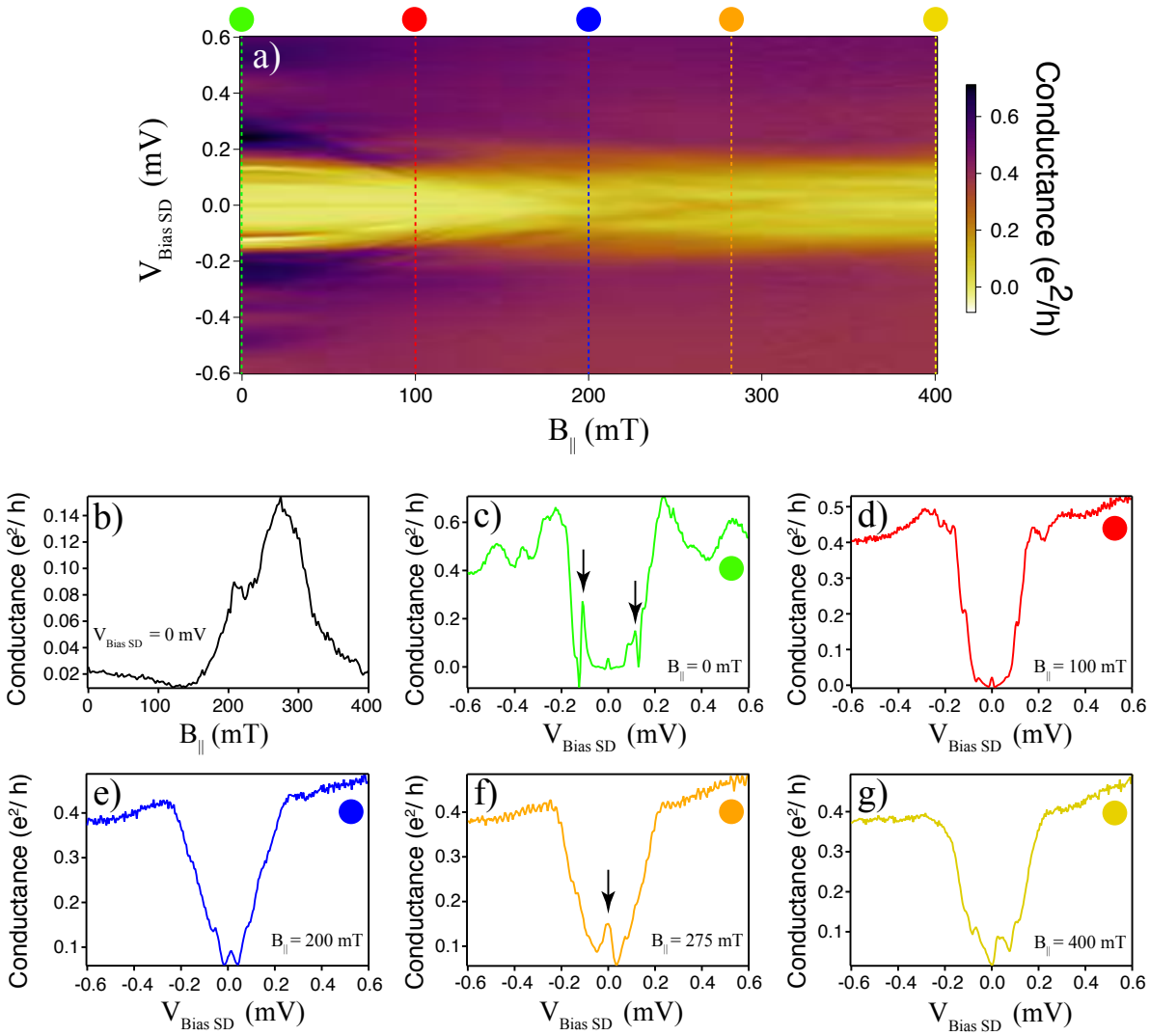

Figure 4.11: ***Zero bias conductance at finite B field****. a) Applying parallel to the nanowire magnetic field ($B_{||}$) and increasing its amplitude as a function of $V_{SD\ Bias}$. There are 6 cuts of the data that are of interest. b) Cut at $V_{SD\ Bias} = 0$, parallel magnetic field. Zero bias conductance of 0.15 e^2/h is observed at $B_{||} = 275\ mT$. c) Cut at $V_{SD\ Bias} = 0\ mV$, observing two subgap states at $-0.1\ mV$ and $0.1\ mV$ of 0.2 e^2/h and 0.15 e^2/h respectively. d) Cut at $B_{||} = 100\ mT$ observing softening of the superconducting gap with no subgap states. e) cut at $B_{||} = 200\ mT$ small zero bias conductance peak of 0.08 e^2/h. f) Cut at $B_{||} = 275\ mT$ zero bias conductance reaches highest point of 0.15 e^2/h. g) Cut at $B_{||} = 275\ mT$ no zero bias peak is observed.*

4.7 Conclusions

To conclude, in this thesis has been shown that micro manipulation of the nanowires can been done without damaging the semiconductor. It was possible to deposit two different nanowires (one with epitaxial Al and the other bare InAs nanowire) in close proximity (500 nm apart) in parallel. This gave the ability to pattern a Ti/Au metallic coupler that can give capacitive coupling between two separate quantum dots that are formed on different nanowires.

By applying known charge sensing techniques in $2DEGs$, successful charge sensing was accomplished in the devices that were presented in this thesis. It was shown that by forming a quantum dot in the "charge detector" nanowire and by cross-compensation it is possible to "stay" on the sidewall of Coloumb peak and be sensitive to charge jumps on main nanowire superconducting quantum dot. This enabled to read out the charge occupancy of formed single and double dot.

In specific three regions were the Al was chemically etched, side cutter gates could pinch-off the constrictions by depleting the electrons in the semiconductor. From fully open (no tunnel barrier) to fully closed (charging energy dominated) range was shown to be ≈ 4 V. This was seen in most side gated devices throughout. This range is too high for arbitrary waveform generator (AWG) to supply such voltage range pulses needed to have fast gating, in order to proceed with Majorana fusion rule experiments. Fast gating is needed in order to not encounter any poisoning events that could occur during the qubit manipulations.

With charge sensing working it was possible to show charge stability diagrams from single to double quantum dot (Figure 4.8) just by changing the $V_{Middle\ Cutter}$. Also in the data it was visible that in the double dot configuration one of the SC islands showed an even/odd parity structure (Figure 4.8 c)), at a $V_9 = const$ and taking a cut along V_3, it is clear that charge states are spaced in even/odd periodicity. This indicates that the single electron transitions occurs only on right dot, because the charging energy of the dots are compared to the superconducting gap Δ. As for the left dot it is always stays SC and transfers only Cooper pairs, charging energy should be lower then Δ.

Nanowire orientation in the cryostat has been found with a help of vector magnet. By rotating the magnetic field amplitude 360^o in θ and Φ angles, and observing the superconducting gap oscillations in $V_{SD\ Bias}$. The distinct values of gap reaching its maximum value was found to be $\theta = 48^o$ in plane, and for out of plane gap oscillations critical value was $\Phi = 40$. This helped to locate the devices orientation inside the cryostat and parallel magnetic field could be applied for further measurements.

Once the nanowire direction has been found and aligning the magnetic field amplitude in parallel to the device. Then with a formed SC quantum dot, sweeping the V_3 plunger value, 2e conductance peaks are observed (Figure 4.9 b) and c)). As the $B_{||}$ is increased 2e peaks are then split at critical $B_C^{||} = 100$ mT field, into two giving even/odd parity switches. This can be explained in Figure 4.10 energy spectrum of the SC quantum dot in B field amplitudes. As the magnetic field is increased the SC energy gap is decreased, which means odd parabola is descending towards zero energy, and electron hoping comes only in 1e. The same can be seen in perpendicular magnetic field sweep, but only this time the critical value at which the 2e conductance peaks split

is lower ($B_C^{\perp}$ = 25 mT). This is consistent with the superconducting model, where perpendicular field to the superconducting material gives lower critical field, in contrast parallel critical field is higher.

Zero bias conductance peak of 0.15 e^2/h was observed at 275 mT parallel field (Figure 4.11). This was accomplished by tuning the outer plunger gates of the superconducting leads so that at some finite magnetic field they would become normal. That way it is possible to probe zero energy states at some critical Majorana bound state parallel magnetic field. The studies on spectroscopic measurements of zero energy states was done are not fully satisfactory that zero bias conductance peak refers to Majorana pairs living at ends of the SC Quantum dot. Further investigations need to be done and more devices have to be measured in order to prove such a statement.

CHAPTER 5

OUTLOOK

5.1 Bottom gated devices

In the thesis it was shown that the open and closed regimes of the device takes $\approx$ |4| V. This pinch-off range becomes problematic in terms of experimental setup, because the AWG cannot handle higher then 4 V voltage pulses. In addition, the cryostat filtering will damp the AWG signal and the final amplitude of pulse will be reduced even more. If the filtering of the cryostat would be removed, additional noise in the system would be present that could only cause more trouble to accomplish any sort of low temperature electron transport measurements.
However, by keeping the same device geometry with all the plunger and cutter gates, and replacing them to bottom gated devices, where no ALD is required. This can be done by having patterned desired gates from Al of 20 nm of thickness. Then oxidizing the small thickness by putting the blank chip on hot plate for 30 min at 270^o C. Al/AlO_2 will be formed on the surface of the bottom gates (Figure 5.1).

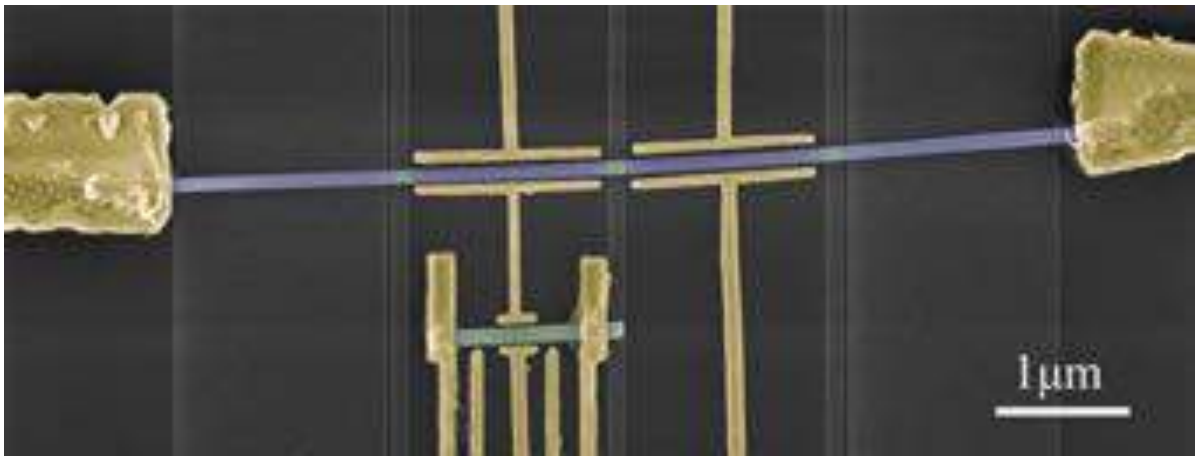

Figure 5.1: ***Bottom gated devices to increase the gating efficiency***. *Double SC QD device with charge sensor. Bottom gates are made out of* Al/AlO_2.

Here in these devices the nanowire is suspended because it was micromanipulated on PMMA resist layer and after the metal lift-off it was fixed in the "air" by the SD leads. The bottom gates have a gap of $\approx$ 10 to 20 nm of distance to the nanowire. This allows to reduce the open and closed regime in the constriction where the Al was etched away to even lower ranges. The outer bottom gated plungers could be even more efficient in gating the effectively made superconducting leads to almost fully depleting the semiconductor and leaving only Al, this could give well defined hard superconducting gap were poisoning events would be suppressed during qubit manipulations or Majorana fusion rule experiment.

5.2 Loop Qubits

Following the proposal from *T. Karzig et al.* [39], theoretically it is possible to accomplish Majorana qubit operations in alsomst the same device geometry as in this thesis, except here the two SC islands are shorted by another superconducting material (NbTiN), keeping the same charging energy of both islands equal. This devices has two leads that are of normal metallic nature where Majorana spectroscopy measurements can be carried out (Figure 5.2)

Figure 5.2: ***Loop Qubit devices****. Double SC QD device with sputtered NbTiN loop that is connected to epitaxial Al of the nanowire. The devices has a charge sensor nearby to read out the charge state of Majorana based qubit.*

Two side gated plunger gates are for to tune each SC QD separately. Charge sensor based on the techniques that were presented in the thesis can be incorporated here as well, reading out the charge occupancy of the total island. By applying parallel magnetic field and tunning the two islands into a topological regime, four Majoranas can be summoned at the ends of the SC islands. With two side gated middle cutters of the main nanowire, the coupling between γ_2 and γ_3 Majoranas can be increased. This leads to $\pi/2$ pulse. After the hybridization of inner Majoranas (γ_2 and γ_3), the outer cutter gates are closed (E_C dominated regime), and then the final charge state can be read out by a charge sensor nearby.

5.3 Nanowire networks

In order to make Majorana braiding operations discussed in [30] paper, nanowire networks are required. By having two wires grown in MBE system with a perfect crystal match is possible. This can be accomplished by having 50% InAs nanowire grown in [111] direction and the other having 50% chance of "kinking" in one of the six facets of the nanowire [37]. This can be accomplished by changing saturated Au droplet that was used as a catalyst, to fall over on the nanowire facets. Then the nanowire is grown from that facet parallel to the InAs substrate. Having a nearby another nanowire that by chance grew straight (without "kinking") and miss aligned by small amount so that the [111] direction wire would be touching with the horizontal grown nanowire (Figure 5.3).

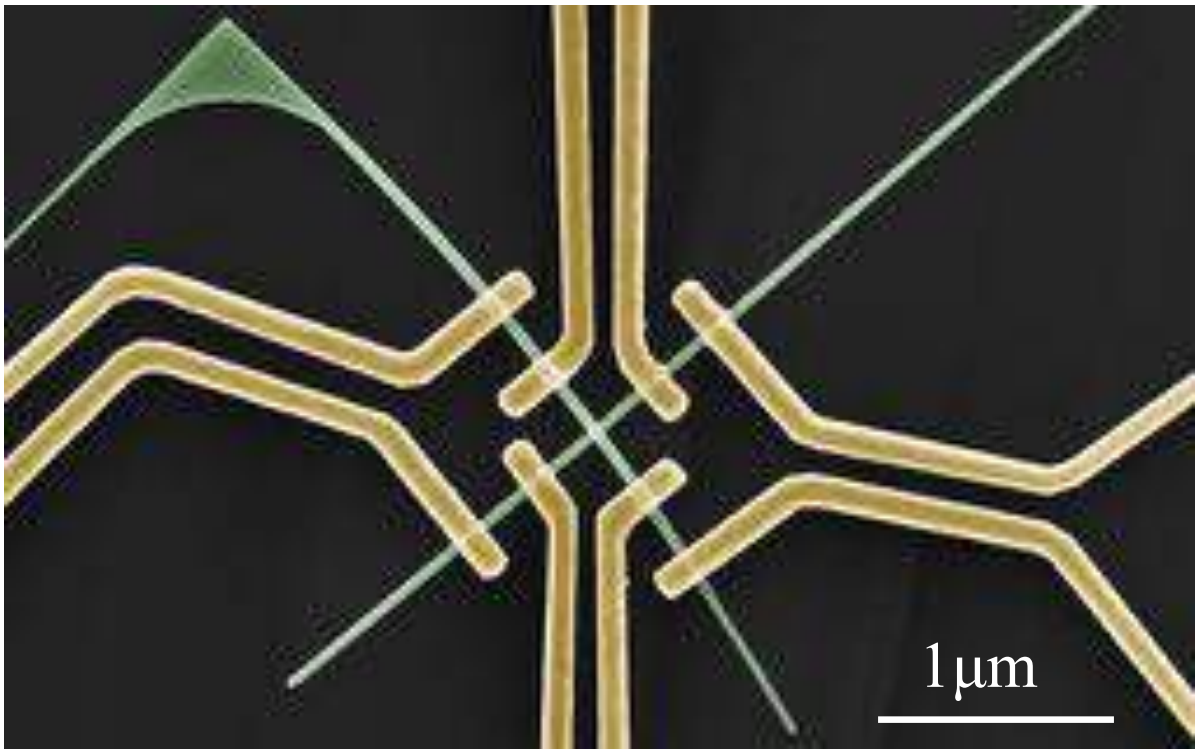

Figure 5.3: ***Nanowire network devices for Majorana braiding experiments****. Two nanwoires were grown to each other with perfect crystal match in MBE system. Four terminal measurements can be accomplished in these devices to show ballistic transport in the nanowire junctions.*

In Figure 5.3 it is a shown such a nanowire network that was micromanipulated onto a conventional blank chip that was used in this thesis and four terminal measurements were accomplished in order to investigate two nanowire junctions. With a global back-gate it was possible to pinch-off the conductance of the junction and the intrinsic resistance can be extracted. For these specific devices it was measured that the nanowire junctions had a intrinsic resistance of $\approx 800\ \Omega$. These devices show potential in making first Majorana braiding manipulations once the epitaxial Al will be grown on the side of these nanowires.

APPENDIX A

APPENDIX

A.1 Experimental setup and techniques

A.1.1 Wire bonding

The fabricated chip is placed and glued with High purity silver paint to the floating cavity of the daughterboard. The back side oxide of the chip has been scratched in order to have tunable back-gate. The daughterboard is then placed on bonding stage and it is grounded via each bonding pads of the daughterboard. The bonding is accomplished with Al wires that connect two points between daughter board bonding pad and the chip bonding pad. With ultrasound the wire is melted and there is electrical connection.

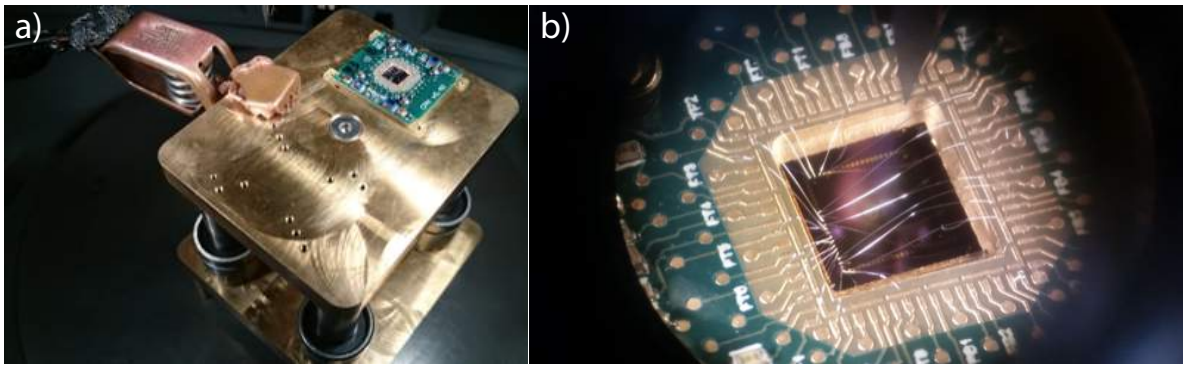

Figure A.1: ***Wire bonding devices to the daughterboard****. a) Bonding stage that the daughterboard is placed via interposer that is in contact with grounded stage. b) Daughterboard with bonded wires to the chip bonding pads.*

After bonding all the numbering is written down and now we know which contact of the device is connected to which break-out-box number of the puck.

The bonded daughterboard is placed in puck motherboard that is grounded via external grounding cap. The motherboard is screwed in firmly and shielding of the puck is mounted and attached to the loading stage. After the attachment of the loading stage to the bottom of the fridge the load-lock valve is open in order to start pumping in order to have comparable pressure to the main fridge chamber. The pumping is left for 12 h and loading is done afterwards.

A.1.2 Daughterboards

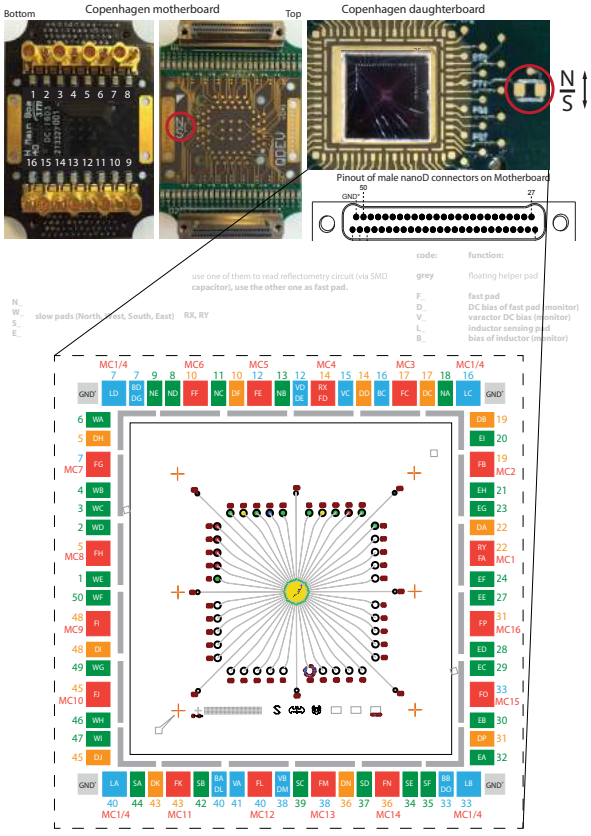

Figure A.2: ***Daughterboard with glued fabricated chip and devices.***

A.1.3 Puck

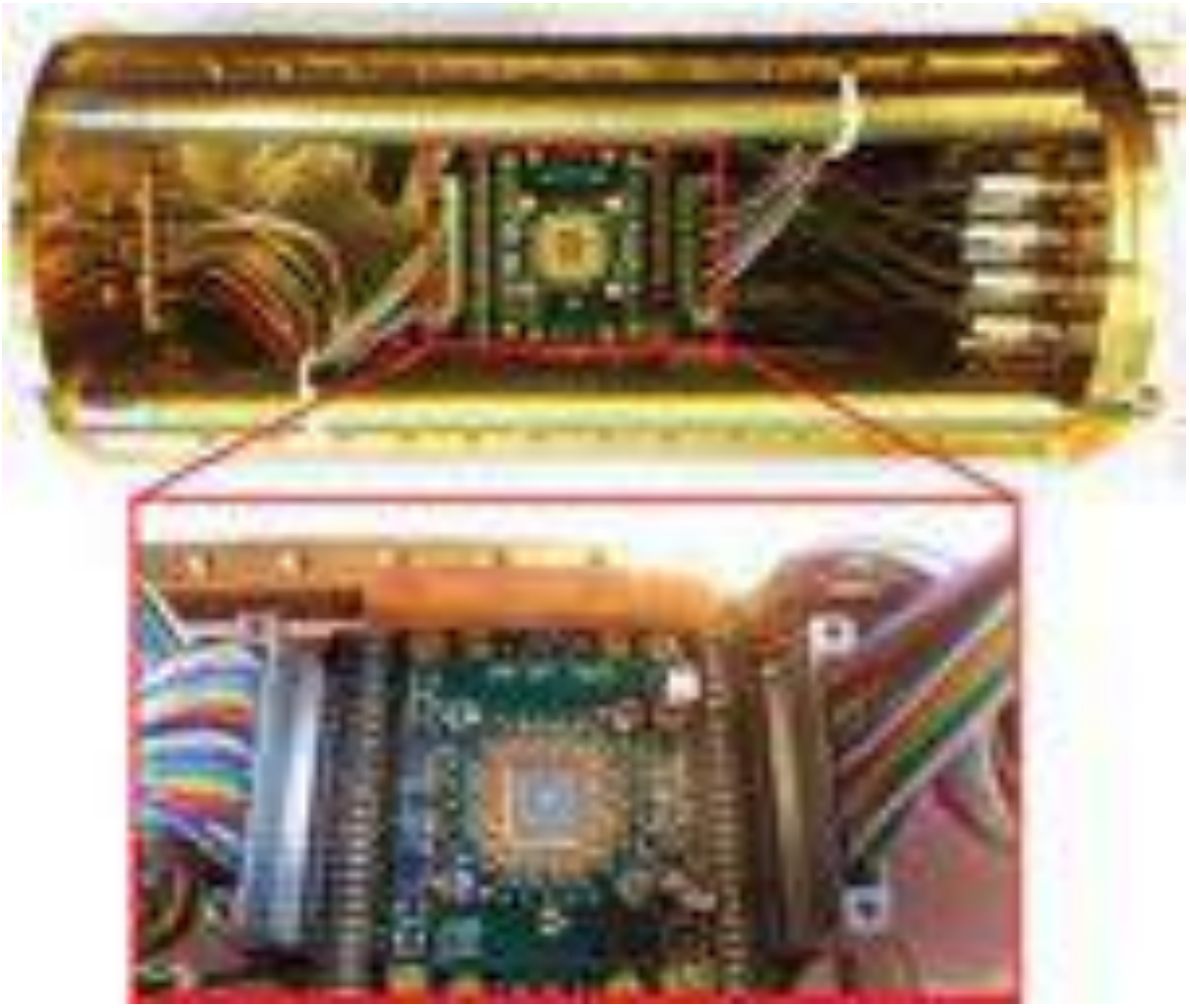

Figure A.3: ***Daughterboard inserted in the puck on to the motherboard***. *The puck of the fridge that is placed in the load lock and pumped for ≈ 10 h. s*

A.1.4 Lock-in amplifier

In order to have low noise in our measurements and to detect even the smallest voltage changes[1], lock-in amplifier technique is used in all measurements. The technique is based on phase-sensitive detection, where specific frequencies of signals are detected and others that are out of phase are rejected and do not contribute to the measurements.

Phase-Sensitive Detection

In all lock-in amplifiers a reference frequency is required. Experiments are carried out by exciting the system at a fixed frequency (by a oscillator or function generator), then the lock-in detects the response from the experiment at specific reference frequency.

[1] As small as few nano volts

A.2 Wiring schematics of the fridge

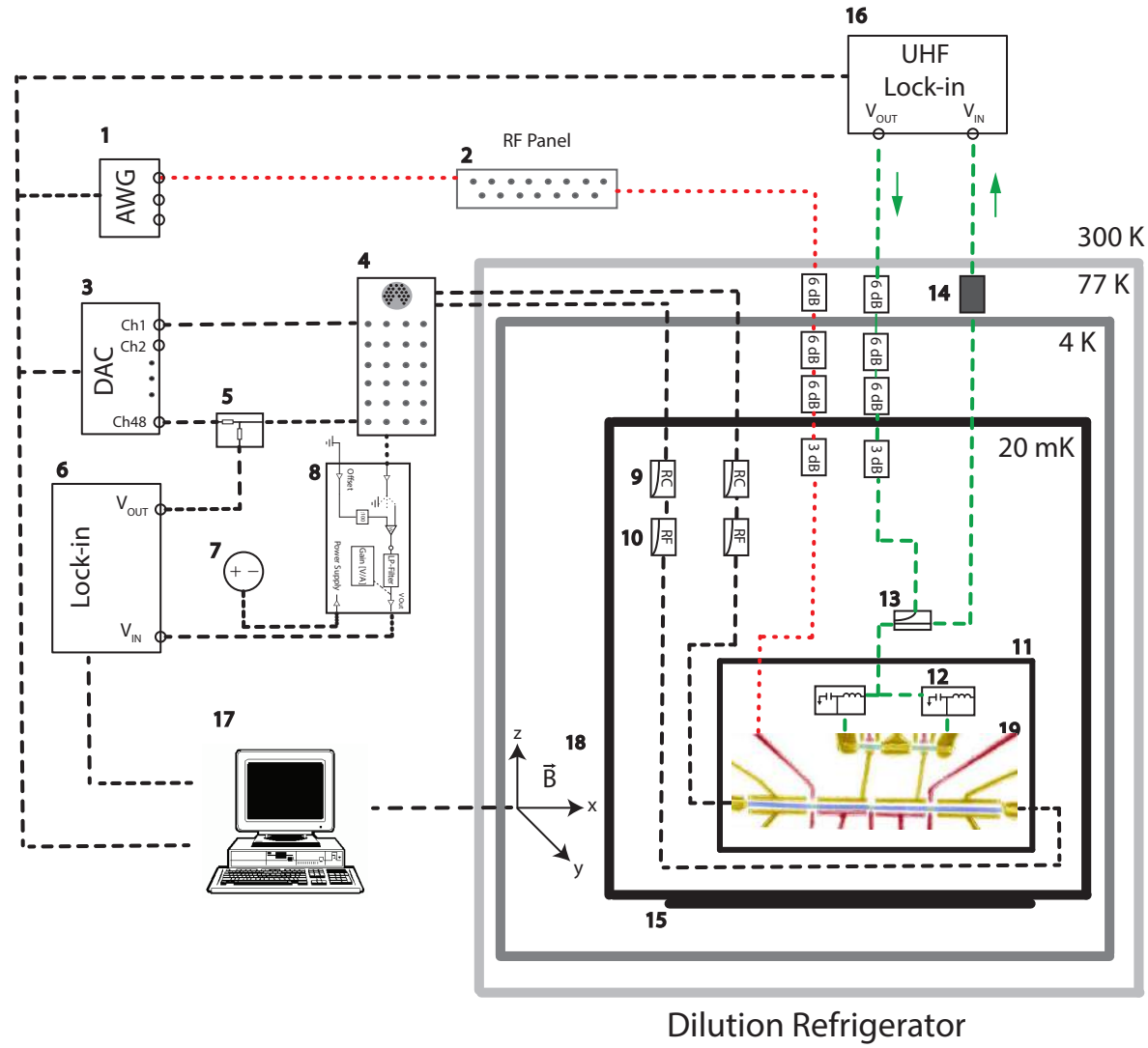

Figure A.4: ***Wiring schematics of the experimental setup****. 1 - Arbitrary Waveform Generator. 2 - Radio Frequency Panel. 3 - Digital to Analog Converter (DAC). 4 - Break-out-box. 5 - Voltage Divider. 6 - Lock-in Amplifier. 7 - Voltage source. 8 - Amplifier (10^3). 9 - RC Filter. 10 - RF Filter. 11 - Puck Shielding. 12 - Tank Circuit. 13 - Direction Coupler. 14 - Cryoamplifier. 15 - "IR-black" Coating. 16 - High Frequency Lock-in (UHF). 17 - Data analysis and instrument control. 18 Vector Magnet. 19 - Device under investigation.*

A.3 Finding nanowire direction

In order to create MZM it is necessary to align external magnetic field along the nanowire. This alignment has to be perpendicular in respect to Zeeman energy splitting component. We form single SC quantum dot as previously. In the cryostat we have vector magnet that we can rotate magnetic field amplitude in three angles θ, Φ and Ψ (Figure A.5 a)). But for identification we only need to rotate at least one axis angle. Full information of the wire alignment can be done by fixing finite magnetic field amplitude and rotating in-plane (θ) angle B-field and at the same time sweeping V_{SD} bias, measuring transport conductance (Figure A.5 c)). Amplitude has been set to $B = 300$ mT.

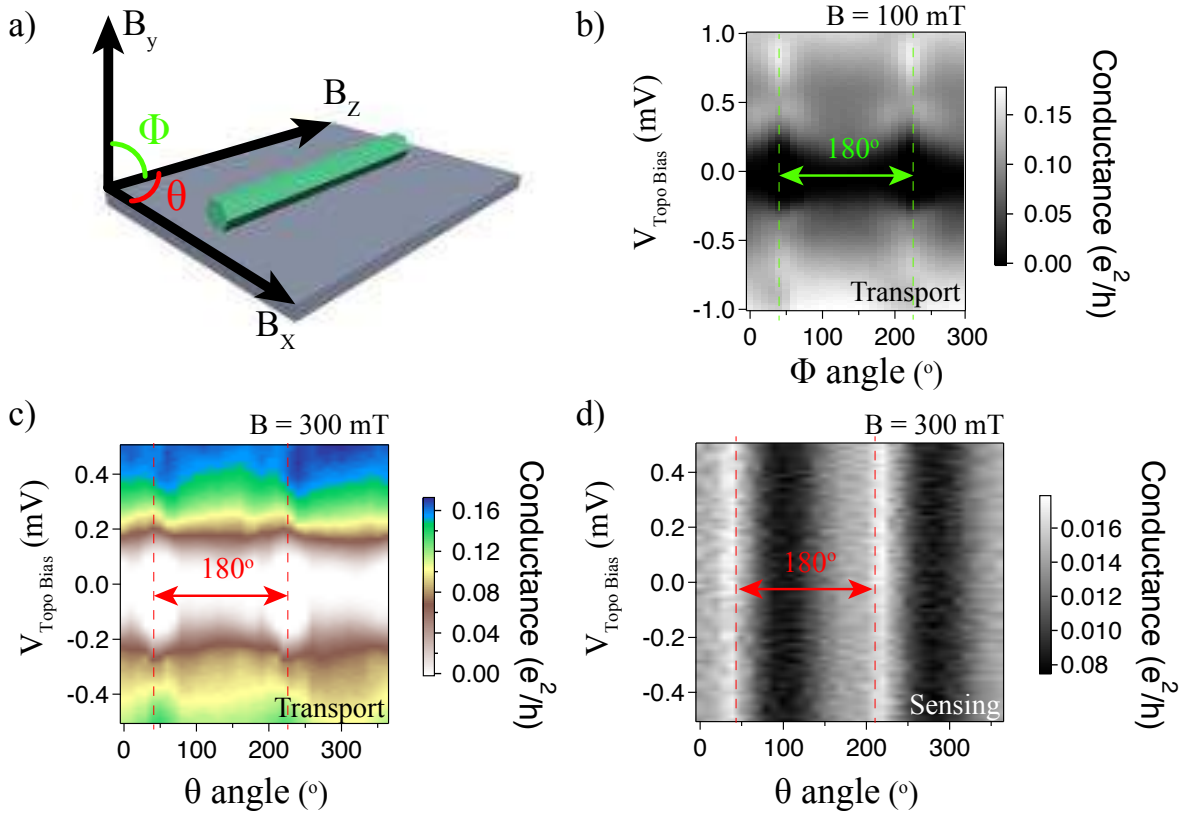

Figure A.5: ***Nanowire direction search with external vector magnet****. a) Vector magnet rotational angle capabilities with a finite magnetic amplitude. b) Rotating* Θ *angle and measuring transport conductance as a function of* $V_{Topo\ SD}$ *bias with a fixed magnetic field amplitude of 100 mT. c) Rotating* ψ *angle and measuring transport conductance as a function of* $V_{Topo\ SD}$ *bias with a fixed magnetic field amplitude of 300 mT. d) Simultaneous measurement with c) except this time with charge sensing techniques applied, taking data conductance of the charge sensor.*

At the same time we can set up the charge sensing with another lock-in and take simultaneously taking charge sensing conductance (Figure A.5 d)) data. From the 2D scan we can see that superconducting gap is changing as we rotate the magnetic field amplitude in θ angle. At a specific ($\theta = 48°$ angle) value the SC gap increases. This indicates that the magnetic field direction

is along the nanowire. We can further see that the SC gap will increase after 180° angle (Figure A.5 c)). The same is visible in charge sensing data Figure A.5 d). We park the magnetic field amplitude in θ = 40° angle and now we rotate angle Φ (Figure A.5 b)). We see that the chip is tilted slightly (40° angle), this could probably be due to silver paste that was used to glue the chip. In ideal case the angle would be 0. As we rotate 180° further we see that the gap increases more. This indicates we have fully found the nanowire direction with $\approx \pm 2°$ accuracy.

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