UNIVERSITY OF COPENHAGEN

Master Thesis

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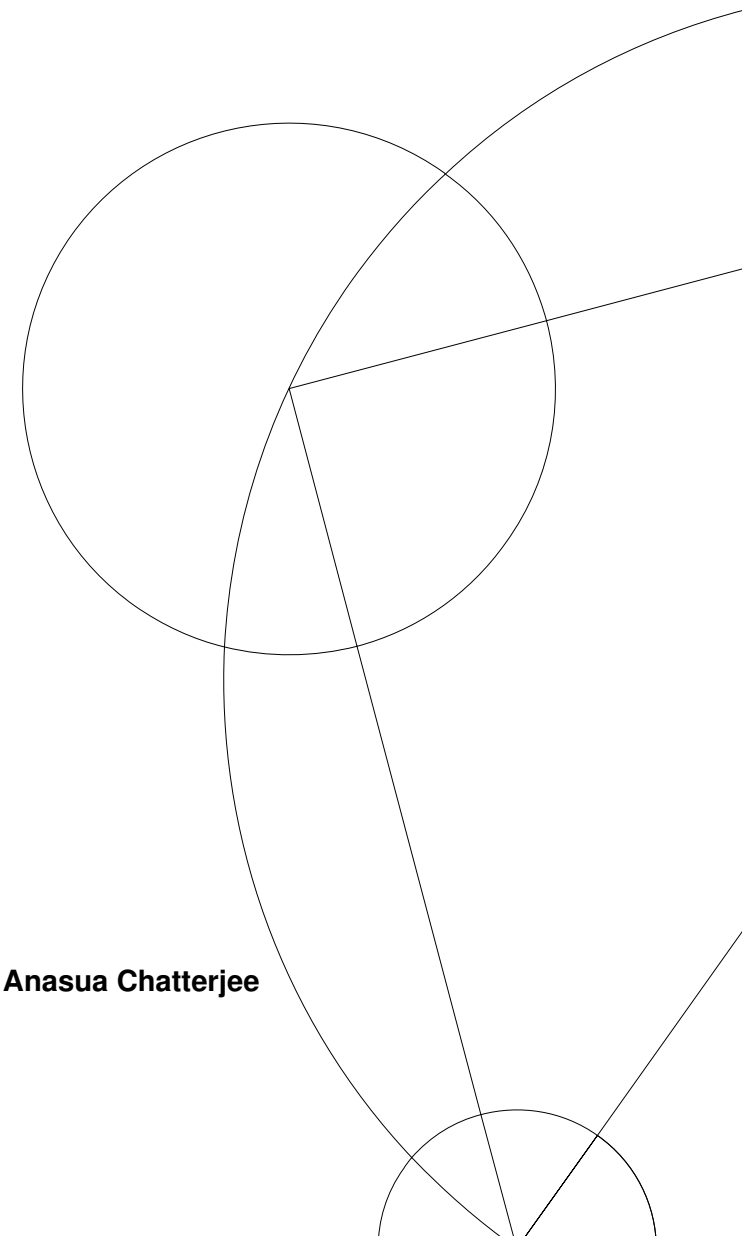
Multi-gate control of quantum-point-contact potentials in GaAs Hall bars



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Abstract

In this thesis I present the fabrication and measurement of a top-gated GaAs/AlGaAs quantum device, designed to investigate algorithm-based tuning of quantised conductance and quantum Hall states. The device consists of a GaAs Hall bar with a high-mobility two-dimensional electron gas (2DEG), on which a pixel-like array of gate electrodes is fabricated in such a fine geometry that a tunable quantum point contact (QPC) can be induced in the 2DEG. Importantly, the presence of up to 17 gate electrodes allows application of up to 17 independent gate voltages, with is far beyond the control capability of prior quantum-point-contact devices. To demonstrate the resulting tunability of the potential landscape experienced by the electron gas, we apply a new tuning algorithm that optimizes for observing a quantized conductance staircase without human intervention. I also present magnetic field measurements in the quantum Hall configuration, with an outlook towards applying multi-gate quantum point contacts in future integer and fractional quantum Hall experiments.

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Acknowledgments

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1 Introduction

1.1 Background and motivation

Quantum devices based on two dimensional electron gases (2DEGs) hosted within heterostructures are becoming increasingly more complex as we try to both scale up qubit devices, the building blocks of quantum computers, and to investigate new quantum phenomena by increasing local control. The number of gates and thereby the number of control parameters make the task of gate tuning increasingly more time-consuming and repetitive. This high-dimensional parameter space makes it difficult for humans to navigate and identify features that indicate the typically small operational area of this large parameter space.

To tackle this tuning challenge in quantum dot systems, machine learning techniques have been used to develop algorithms that can automate the tuning process of quantum dot devices to the single and double dot regime [2, 8, 29, 40, 41], the fine tuning of device parameters [37, 34], such as locating specific charge states [11], and the identification of specific features such as charge state transitions [24] and bias triangles [30].

When it comes to gaining more local control by increasing the number of gates, experiments have been done to investigate the 0.7 anomaly in QPCs [18, 3] and the supercurrent distribution in Jospehson junctions [12]. However, the potential of ML techniques for scientific discovery in systems with high local control is yet to be realised. To test these techniques, the QPC can act as a great platform because of its simplicity and rich physics. This thesis is based on work performed in a GaAs/AlGaAs 2DEG; primarily, a pixelated gate design is developed and fabricated on the heterostructure, following which we allow our algorithm to tune the QPC conductance into the expected staircase pattern.

1.2 Chapter overview

Chapter 2 will cover the concepts lying behind the 2DEG, the physics of the quantum point contact and finally it will present the Quantum Hall effect and some of the physics that describe it. In chapter 3, the fabrication process and considerations will be presented, starting with the considerations that went into designing the device. Then it will present the choices

of wafers that were made, before moving on to how a single lithography step is done. Finally it provides the considerations that went into each of the fabrication steps: Cleaving, Markers, Mesa, Ohmics Contacts, Fine Gates of the QPC and Bond Pads. In chapter 4 an overview of the device is given with a picture of the full chip, a device schematic and the experimental setups that were used. Chapter 5 will present the preliminary measurements we did on a device, that determined the success of the fabrication. In chapter 6 the measurements done using the algorithm will be presented and in chapter 7 I will provide a summary of our measurements and an outlook on possible future experiments. Finally in the appendix the fabrication recipe used to create the device tested in this thesis is provided with further technical details.

2 Theory

In this chapter we present some background for the measurements described in the thesis. The first part gives a description of the two dimensional electron gas, as it is the platform of our experiments. In the second part we present the physics of the quantum point contact, QPC, and finally we will present the quantum Hall effect.

2.1 The two dimensional electron gas

The two dimensional electron gas, or 2DEG, is used extensively in experimental condensed matter physics. It has been as a very fruitful platform to investigate systems such as quantum dots [5] , quantum point contacts [3, 18], the quantum Hall effect, as reviewed in Ref. [36], and many other quantum mechanical phenomena.

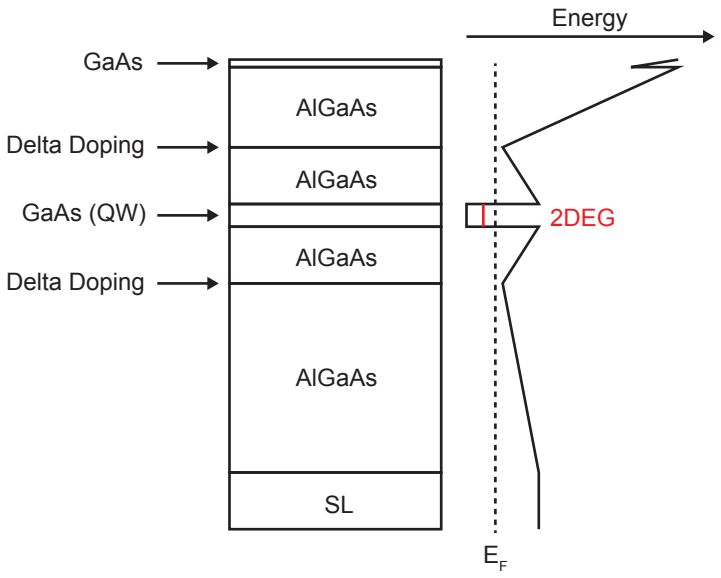

Figure 2.1: **2DEG** Illustration of how the wafer is constructed to realise a 2DEG. This illustration is based on the wafer we used for the third device, the deep well high mobility wafer, where the 2DEG is 190 nm below the surface.

It can also be a very versatile platform because the 2DEG can be manipulated by applying a potential to metallic gates fabricated on top of the heterostructure in which the 2DEG resides.

One of the most famous uses of the 2DEG phenomenon is in the metal-oxide-semiconductor field-effect transistor, or the MOSFET [1], which is used in all everyday electronic devices.

Although 2DEGs do appear in these MOSFETs they are usually not suited to use for the purposes we wish to use them for, because the 2DEG quality is poor [33]. One alternative to silicon based 2DEGs is Gallium Arsenide / Aluminium Gallium Arsenide, GaAs/AlGaAs, based 2DEGs with which some of the highest electron mobilities have been achieved [6].

Because of the difference in energies between the band gaps in GaAs and AlGaAs ,a potential well can be formed at the interface between the two. This confines the electrons to a plane parallel to the interface, and it is in this potential well that the 2DEG resides. The reason why GaAs/AlGaAs works so well, and gives such high mobilities, is because the difference in their lattice constants is very small. This ensures that there is almost no strain between the crystal layers in the heterostructure. If there was strain between the crystal layers, crystal imperfections would appear. This would increase the number of scattering sites, thus resulting in a lower electron mobility [33].

These GaAs/AlGaAs heterostructures are fabricated layer by layer with atomic layer precision using molecular beam epitaxy (MBE) [26]. The heterostructure is grown on top of a separately grown GaAs substrate, which are cut from large GaAs crystals. The heterostructures used for the work showed in this thesis were grown by the Manfra group at Purdue University, USA.

The two main properties of 2DEGs that affected our choice of wafer in this project were the gateablility and the mobility of the 2DEG. We aimed for a high mobility 2DEG which was also easily gateable. Unfortunately, high mobility 2DEGs are typically more difficult to gate than ones with lower mobility. This is caused by the former being highly doped in one or more doping layers in order to achieve these high mobilities. The downside of this process is that the dopants can have a strong screening effect, and can act as charge traps which will lead to hysteresis. A silver lining of highly doped heterostructures is that they are relatively easy to fabricate ohmic contacts on.

2.2 The physics of quantum point contacts

The quantum point contact, QPC, is a simple yet very useful structure, used in many different designs made to investigate physics in 2DEG materials. A QPC can be realised in a 2DEG

by separating the 2DEG into two reservoirs that are connected by a small passage. In this passage the system will be reduced even further in dimensionality, from a 2D system to a 1D system, resulting in interesting physics such as the quantization of conductance.

In practice, the QPC is made by evaporating metal gates on top of the heterostructure, to which potentials can be applied, thereby depleting the 2DEG underneath and in the vicinity of the metal gates. By placing two metal top gates opposite each other with a small gap in between, we can create a QPC, as seen in Figure 2.2.

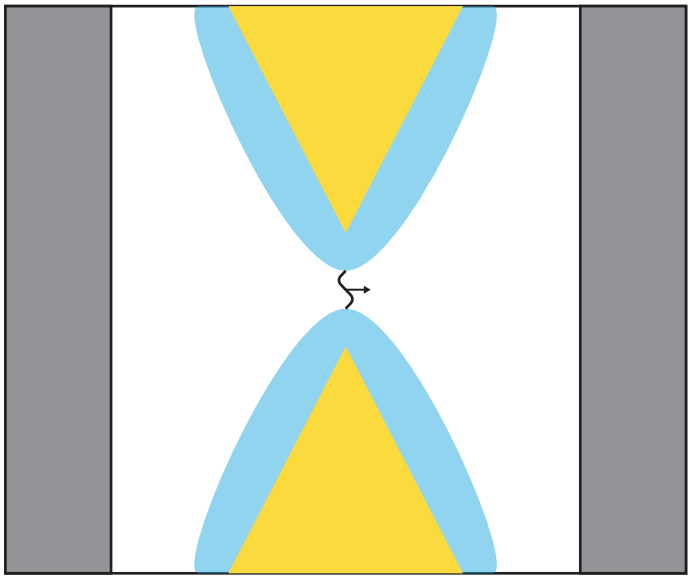

Figure 2.2: **QPC** Illustration of a quantum point contact. The two grey rectangles to the left and right represent reservoirs, the gold triangles are gates, the blue region around them represent the electric field that depletes the 2DEG and the sine wave represents an available mode in the QPC.

The first QPC measurements were done in 1988 by B.J. van Wees et. al[38] and D. A. Wharam et, al[39], both using a 2DEG in GaAs/AlGaAs heterostructures to define the narrow channel. Both groups saw that the conductance showed a step like behaviour as a function of applied gate voltage, and reported quantization of the conductance, which took values of

$$G = \frac{2e^2}{h}N \tag{1}$$

where N refers to the number of modes that are available in the channel, which depends on the voltage applied to the gates.

The quantum point contact is a simple system, well known in the field of condensed matter physics, and the physics of the conductance quantum is well understood. However, for some phenomena observed in the quantum point contact regime, the physics lying behind the origin is still under debate: for example, the 0.7 anomaly. The 0.7 anomaly appears as a step in the quantized conductance staircase at 0.7 of the conductance quantum. It cannot be explained by the 1D quantisation of the system and other factors must be taken into account. Among the proposed explanations of this anomaly are spontaneous spin polarization [10, 35], Kondo effects [19, 7], and Wigner crystallization [27]. Measurements using scanning gate microscopy reveals both Kondo and Wigner physics [4]. Gaining more understanding of the gate potentials [18, 3] required to observe and optimize the 0.7 anomaly, for example, could give us some definitive insight into its origin.

It is exactly because the QPC is so well known, is "simple" to fabricate and contains unknown physics, that it would be interesting to increase the complexity and controllability of the system by increasing the number of gates that realise the QPC. In particular, we aimed to achieve granular and two-dimensional control over the potential of the channel. To try and increase the control of the channel potential by adding pixelated gates, without increasing by a large amount the tuning overhead, we decided to use machine learning (ML) techniques. These ML techniques could help us work with systems that have many control parameters, while at the same time the development of these techniques would let us dare to design devices with more complex arrays of gates.

For the quantization of conductance to appear in a QPC system, the electrons should not be scattered too much in the channel, since this is only observed in the ballistic transport limit, when the mean free path of the electron is much larger than the length and width of the channel. In order to avoid this scattering, a high mobility 2DEG is advantageous when trying to observe the conductance quantum. One of the reasons why the two research teams in 1988 were the first to observe this physics was exactly because they used high mobility GaAs/AlGaAs heterostructures[38, 39].Further, it is required that the level spacing of the transverse modes is much larger than the temperature of the system, which is a reason why we cool the device to around 20 mK using a cryogenic dilution refrigerator. Another reason

is that the 2DEG will not manifest in the heterostructure at high temperatures. Finally the width of the channel has to be comparable to the Fermi wavelength. Since the width of the channel is adjustable with the potential applied to gates this condition will be fulfilled.

We can show that the conductance quantum is equal to equation 1, by looking at the linear response regime when we apply a small voltage difference to the reservoirs. The difference in the electrochemical potential of the two reservoirs is

$$\mu_L - \mu_R = -|e|V_{SD} \tag{2}$$

Expanding this using the definition of a derivative we get

$$f_L(E) - f_R(E) = \frac{\partial f_L(E)}{\partial \mu_L}(\mu_L - \mu_R) = -\frac{\partial f_L(E)}{\partial \mu_L}|e|V_{SD} \tag{3}$$

Because there is a voltage applied between the two electron reservoirs, using an external voltage source, there will be a difference in the distribution functions for the left and right moving electrons which will result in a net current given by

$$I_{tot} = -g_s\frac{|e|}{h}\left(\sum_n \int_{E_n}^{\infty} dE[f_L(E) - f_R(E)]\right) \tag{4}$$

Here f_L and f_R refer to the Fermi-Dirac distributions for the left and right reservoirs. We can insert equation 3 into this equation for the net current and preform the energy integration to get

$$I_{tot} = g_s\frac{e^2}{h}\sum_n f_L(E_n)V_{SD} \tag{5}$$

Further, if we divide by the voltage bias

$$G = \frac{I_{tot}}{V_{SD}} = g_s\frac{e^2}{h}\sum_n f_L(E_n) \tag{6}$$

The sum will reduce to N, the number of modes, if we are at low temperaures and the energy E_n of a particular mode n is below the Fermi energy since then the Fermi-Dirac distribution

is equal to one, and the mode will be occupied contributing $g_s\ e^2/h$ to the conductance[17].

$$G = \frac{2e^2}{h}N \tag{7}$$

2.3 Saddle point potential model

Using the method above we were able to show that the conductance through a QPC is quantized, but we did not consider how the specific potential of the QPC channel looks. A central part of this project is to fabricate a device which is able to form and manipulate the potential of the QPC and so the potential of the QPC plays a major role in the design of the device. One way of modelling the quantum point contact is to assume that the potential takes the form of a saddle point potential[17].

$$V(x,y,z) = -\frac{1}{2}m^*\omega_x^2x^2 + \frac{1}{2}m^*\omega_y^2y^2 + V(z) \tag{8}$$

Using this potential, the Hamiltonian describing the electron motion is separable. Since the system is a 2DEG, where motion in the z-direction is highly confined, we can assume that the states with energies E_z will have an energy spacing much larger than any other energy scale in the system. In the y-direction we have a parabolic potential with the well known harmonic oscillator solutions, with energies $E_y = \hbar\omega_y(m + \frac{1}{2})$. The total energy is $E = E_x + E_y + E_z$. We can write the equation of motion for the x-direction as

$$\left(-\frac{\hbar^2}{2m^*}\partial_x^2 - \frac{1}{2}m^*\omega_x^2x^2\right)\xi(x) = E_x\xi(x) \tag{9}$$

and we can rewrite this as

$$\left(l_x^2\partial_x^2 + \frac{x^2}{l_x^2} + \epsilon\right)\xi(x) = 0 \tag{10}$$

where $\epsilon = \frac{2E_x}{\hbar\omega_x}$ is the normalized energy scale and $l_x^2 = \frac{\hbar}{m\omega_x}$ is the length scale. The solutions to this equation can be written as a linear combination of parabolic cylinder functions $D_\nu(x)$

$$\xi(x) = c_1D_{-\frac{1}{2}i(\epsilon-i)}\left[\frac{(1+i)x}{l_x}\right] + c_2D_{\frac{1}{2}i(\epsilon+i)}\left[\frac{(-1+i)x}{l_x}\right] \tag{11}$$

From this it can be shown that the transmission in the x-direction through the parabolic potential barrier of mode m is

$$T_m(E) = \frac{1}{1 + e^{2\pi\epsilon_m}} \tag{12}$$

where

$$\epsilon_m = \frac{E - \hbar\omega_y(m + \frac{1}{2}) - E_z}{\hbar\omega_x} \tag{13}$$

Here we see from equation 12 that the transmission takes the shape of a step like function. Successive transmission modes m also give a step like function, but shifted, such that the sum of transmission modes gives a function with the shape of a staircase, as seen in Figure 2.3b. We also see that $\hbar\omega_x$ determines the width of the transition region between plateaus or how steep the step is and the energy shift between plateaus is set by $\hbar\omega_y$.

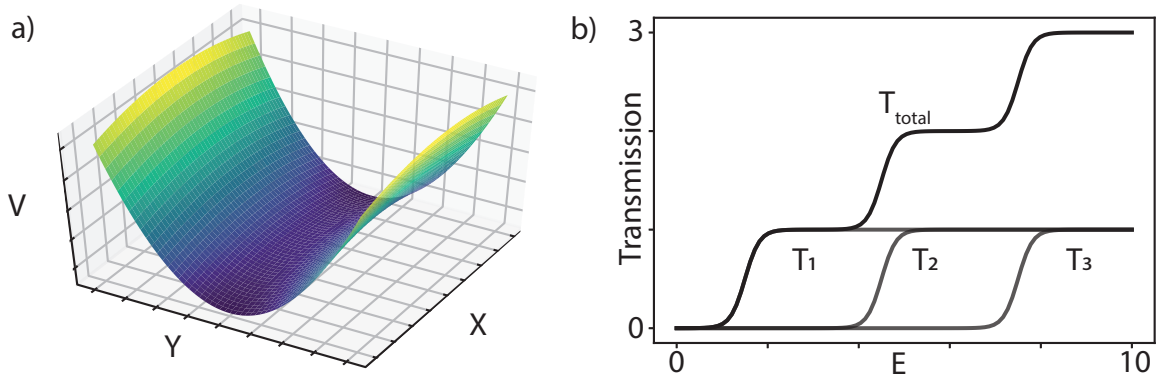

Figure 2.3: **Saddle point potential and Transmission a)** A saddle point potential where $\omega_y/\omega_x = 3$. **b)** Transmission through a saddle point potential.

2.4 The quantum Hall effect

The quantum Hall effect owes its name to the classical Hall effect which was discovered by Edwin Hall in 1879 [14]. Hall found that when he applied a perpendicular magnetic field to a gold leaf, while running a current through it, he saw two characteristic voltages. One voltage, V, was the voltage measured along the current path, which occurs because of the electrical resistance, R, of the sample. The other voltage, V_H, was the voltage measured across the current path, which we now know as the Hall voltage.

Hall found that V_H was proportional to the current, I, and proportional to the perpendicular magnetic field, B, and by denoting V_H/I as the Hall resistance, R_H, we have that

$R_H \propto B$. The reason why we see a voltage difference across the sample can be explained by the Lorentz force, as a perpendicular magnetic field will exert a sideways force on the moving electrons in the sample. This will result in an accumulation of electrons on one side of the sample, and ultimately a voltage difference across the current path. This also explains why a larger perpendicular magnetic field will show a larger Hall resistance because of a larger force on the electrons. We also have that the Hall resistance is dependent on the electron density, n, such that $R_H = B/(ne)$. We see that as the electron density increases, the Hall resistance decreases. In order to maintain the current the electrons move slower and in turn experience a smaller Lorentz force. This results in a smaller voltage drop across the current path or a smaller resistance. When it comes to measuring the electron density of samples, the Hall effect is remarkable because it is independent of size and shape of the sample. It has become a standard for determining the electron density of free electrons in electrical conductors.

2.5 The integer quantum Hall effect

If we then move to measure the Hall effect in a 2DEG at low temperatures and in a high perpendicular magnetic field, we see that the Hall resistance shows a step like dependence on the magnetic field, instead of the linear relationship we see in the classical Hall effect. This was discorvered by K. von Klitzing et al. in 1980 [22], and they found that these steps take on values of R_H at plateaus equal to $R_H = h/ie^2$, where i is an integer and h is Planck's constant. We also see that the longitudinal resistance, or the magnetoresistance, oscillates with increasing magnetic field, and at large magnetic fields the minima of these oscillations will reach almost zero resistance. These oscillations are called Shubnikov–de Haas oscillations. The plateaus of the Hall resistance and the minima of the magnetoresistance also coincide at the same magnetic fields. When the Hall resistance starts a new plateau, the magnetoresistance drops to almost zero resistance.

We can explain this behaviour by looking at how the electrons experience the magnetic field in two dimensions. The electrons are forced into circular orbits, again because of the Lorentz force, where they are only allowed to assume a certain set of discrete energies. The

two-dimensional case differs from the three-dimensional case because in the three-dimensions motion of the electrons can add any amount of energy when the motion is along the magnetic field.

The energies of these circular orbits can be found by looking at the Schrödinger equation for an electron in a magnetic field [17]. We have a Hamiltonian that reads as

$$H = \frac{(\mathbf{p} + |e|\mathbf{A})^2}{2m^*} + V(z) \tag{14}$$

Here $V(z)$ is the potential confining the 2DEG. We chose $\mathbf{A} = (-B_y, 0, 0)$, which results in a magnetic field $\mathbf{B} = (0, 0, B)$. We can separate this Hamiltonian into

$$H_z = -\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2} + V(z) \tag{15}$$

and

$$H_{xy} = \frac{(p_x - |e|B_z y)^2 + p_y^2}{2m^*} \tag{16}$$

The solutions to the Hamiltonian describing the states in the z-direction can be ignored as only the lowest states will be occupied in a 2DEG. To solve the eigenvalue problem for the Hamiltonian describing the states in the plane, we first assume that the wavefunctions take the form

$$\psi(x, y) = e^{ik_x x}\eta(y) \tag{17}$$

which leads to the eigenvalue problem

$$\left(\frac{p_y^2}{2m^*} + \frac{1}{2}m^*\omega_c^2\left(y - \frac{\hbar k_x}{|e|B_z}\right)^2\right)\eta_{k_x}(y) = E\eta_{k_x}(y) \tag{18}$$

Here $\omega_c = \frac{|e|B}{m^*}$ is the cyclotron frequency. We see that this equation resembles that of a one-dimensional quantum mechanical harmonic oscillator, with a k_x-dependent center coordinate.

$$y_0 = \frac{\hbar k_x}{|e|B} \tag{19}$$

The quantized energy states of the harmonic oscillator are

$$E_n = \hbar\omega_c(n + \frac{1}{2}) \tag{20}$$

and if we include the Zeeman splitting of the spin states we have

$$E_n^{\pm} = \hbar\omega_c(n + \frac{1}{2}) \pm \frac{1}{2}g^*\mu_B B_z \tag{21}$$

This quantization of states is called Landau quantization. If we ignore the contribution from the Zeeman splitting of the spins, we see that the energies of these states are proportional to the magnetic field, B, and we also see that there are large energy gaps of $\hbar\omega_c$ in between the different Landau levels. In each of these Landau levels there are a quantized number, $d = eB/h$, of degenerate states which reflects the number of orbits per Landau level that can be packed in to each unit area. This degeneracy is proportional to the magnetic field, which gives rise to an interesting set of magnetic field values where integer values of Landau levels are exactly filled. If we look at the case where we are at a magnetic field, $B_1 = \frac{nh}{e}$, where all the states, n, in the lowest Landau level are exactly filled and we then start lowering the the magnetic field, we would see that the number of available states would decrease, forcing electrons to move to the next Landau level. Since all Landau levels have the same number of degenerate states, at a certain magnetic field, B_2, both the first and the second Landau level will be exactly filled and we can relate B_1 and B_2 as $B_2 = \frac{nh}{2e} = \frac{B_1}{2}$. By lowering the magnetic field even further we can repeat this process of filling up an exact number of Landau levels, and write up the set of fields where this is true as $B_i = \frac{nh}{ie}$, $i = 1, 2, 3, ...$ Inserting this into the expression for the classical Hall resistance, $R_H = \frac{B}{ne}$ we have $R_H = \frac{h}{ie^2}$. Although this explains the values of resistance at which we see the plateaus, it does not explain why there are plateaus [33].

The Landau levels can not explain why we see a constant Hall resistance and an almost zero longitudinal resistance for a range of values in the magnetic field. To explain this we have to look at localized electrons, that appear because of hills and valleys in the potential landscape where the 2DEG resides. These localised electrons act as reservoirs in the sample

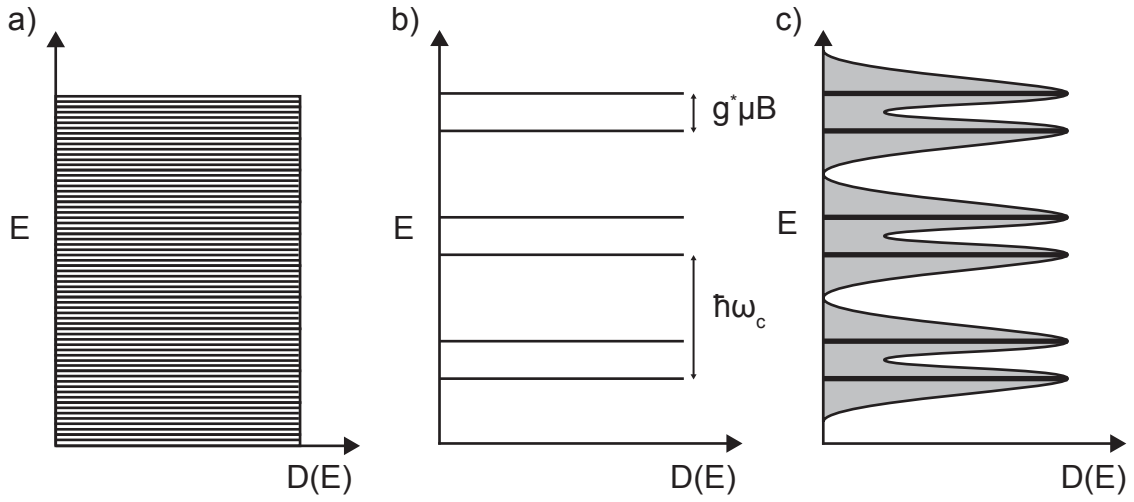

Figure 2.4: **Density Of States, Landau Levels** Density of states for electrons in a 2DEG under different circumstances **a)** DOS in a 2DEG, without a perpendicular magnetic field **b)** Landau levels occur with a perpendicular magnetic field. **c)** The Landau levels are broadened by the presence of scattering sites in the 2DEG, which gives rise to localised states.

and will not contribute to the electrical conduction through it. The consequence of this is that whenever we try to empty or fill the Landau levels of the extended flat regions of the sample, we will instead be emptying and filling the localized states thereby keeping the conducting regions at their full capacity. Because of these localized electrons we see that the Landau levels are kept exactly filled for a range of magnetic field values which shows as quantized plateaus in the Hall resistance and an almost zero longitudinal resistance in the same magnetic field range.

To fully understand why the longitudinal resistance drops to zero we also have to consider the formation of edge states [15]. Along the edge of the sample the electrons experience a steep potential, which keeps them inside. Because of this the Landau levels are pushed up in energy at the edge, such that even when the Fermi energy, E_F, is in between Landau levels in the bulk of the sample, the Fermi energy will cross the energy levels of electrons at the edge of the sample. These edge states allows for dissipationless transport along the edge, such that two voltage probes on the same edge will experience the same voltage, and thus near zero resistance. Edge states on opposite sides of the sample are still separated thereby allowing the Hall voltage to build up [17].

In Figure 5.6b we show a quantum Hall measurement preformed on one of our samples. The Hall resistance plateaus have been marked with their corresponding filling factor. To calculate the location of these filling factors we look at the magnetic field values of two neighbouring peaks in the longitudinal resistance, and calculate the electron density, n_s [9].

$$n_s = \frac{2e}{h} \frac{1}{(1/B_1) - (1/B_2)} \tag{22}$$

Using this electron density we can calculate the magnetic field value, B_i where we should observe integer filling factors, ν_i.

$$B_i = \frac{n_s}{2e\nu_i/h} \tag{23}$$

The electron densities we calculated using this method did not match the electron densities the wafer manufacturer supplied us. We believe the 2DEG was damaged during fabrication and because of this the calculated magnetic field values do no line up exactly with the plateaus in the Hall resistance.

2.6 The fractional quantum Hall effect

Above we looked at how the magnetic field dependence of the degeneracy of the Landau levels, gave us certain magnetic field values where an exact number of Landau levels were filled. For one magnetic field value the lowest Landau level would contain all the states, resulting in a filling factor of one. Intuitively this would mean that we do not expect any more plateaus in the Hall resistance at magnetic field values above the plateau showing a filling factor of one. However, at larger magnetic fields we do see plateaus corresponding to fractional filling factors [33].

To explain fractional plateaus in the Hall resistance, electron-electron interactions have to be taken into account. Some of the fractional states can be explained by the wave function proposed by R. B. Laughlin [21, 25],

$$\psi_{1/m} = \prod_{j<k} (z_j - z_k)^m e^{-\frac{1}{4}\sum_i |z_i|^2} \tag{24}$$

This wave function can explain the fractional states with filling factors $\nu = 1/m$, where m is odd. However, these states do not account for all the fractions that have been observed. Most of the fractional states can be explained with Composite Fermion, CF, Theory [21, 20]. This theory looks at new particles that consists of electrons and flux quanta. Composite Fermion Theory can still not explain all the fractional fillings, and there is still physics to be discovered here.

3 Fabrication

3.1 Designing the device

The design of our device is heavily influenced by the motivation behind the project. It diverges from typical QPC designs by adding local control in two dimensions, and hence we need to design a pixel-like gate pattern. By increasing the number of gates we also increase the dimension of the voltage space we have to navigate, and to help us tune the device we wish to use machine learning techniques. This tuning task is a problem that is becoming more and more clear as the community tries to design new devices with many gates that end up taking many hours to tune. Therefore the device design will also facilitate the goal of seeing if we can use machine learning techniques to develop new tools that could help tune quantum devices.

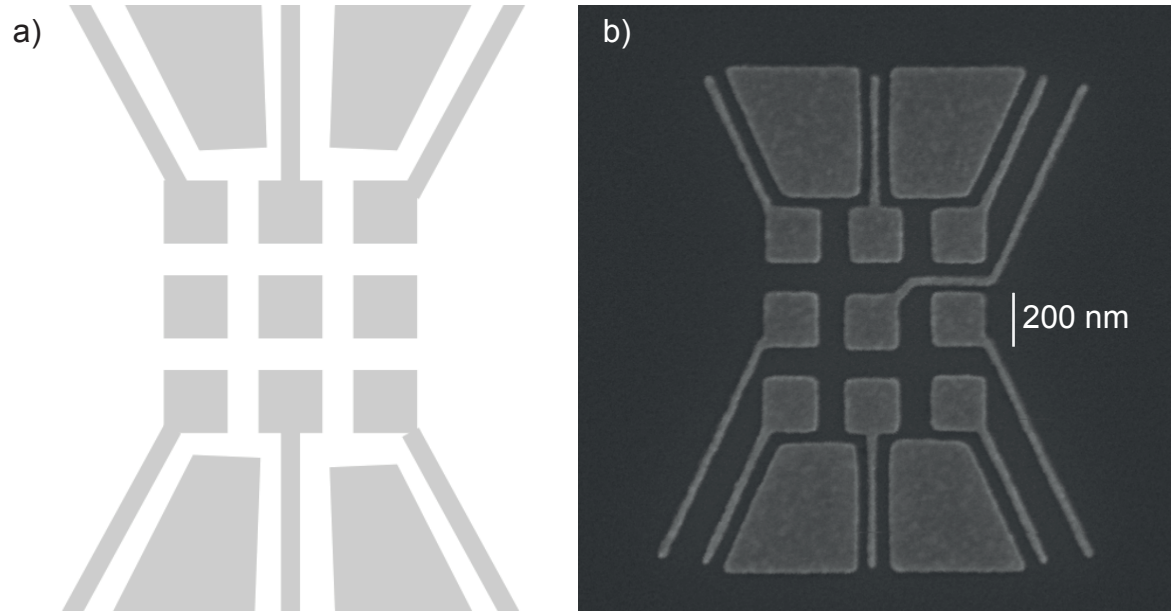

Figure 3.1: **Designing the pixel QPC 1 a)** The concept design of the pixel QPC **b)** First dose test of a pixel QPC deisgn.

Another motivation behind the project is to investigate if the width of integer and fractional quantum Hall effect plateaus could be changed by manipulating either the curvature or the disorder of the QPC saddle point potential.

We would also like the design to be modular, such that we can extend it to even more complex devices, for example to investigate tunneling between edge states by either letting

them pass through the QPC or by separating the 2DEG in two and then have the wave functions of the edge states overlap near the QPC.

A final motivation behind the design is to explore a direction related to recent experiments performed in the groups of F. Bauer[3] and M.J.Iqbal[18], concerning the 0.7 anomaly [35]. The 0.7 anomaly appears as a shoulder at 0.7 $2e^2/h$ in quantized conductance traces. The two papers referenced here explored the origin of the 0.7 anomaly by adding gate complexity; they moved from two facing gates forming a QPC to a double-layer gate structure adding a top gate[3] or to three gates facing each other along the channel[18]. These devices were a step in the right direction, but we would like to take this further, and one way of investigating the 0.7 anomaly could be to make a device in which we had full control of the potential in the QPC channel.

Combing these ideas into a single design makes a lot of sense since large amounts of control and many gates go well together.

The first QPC concept design we discussed can be seen in Figure 3.1a. The design distinctive, with nine pixels that allow us to control the potential landscape in the channel region. This QPC design was designed with the saddle point potential in mind, as the nine pixels allows us to control the curvature of the potential in both the x- and y-direction. The design also poses some challenging fabrication questions. The first question being, how do we apply a voltage to the middle pixel. Since we have chosen to fabricate using a single gate layer, we are limited to fabricating gates that follow the plane of the wafer and we cannot apply a voltage to the middle pixel without also applying it to the connector that needs to be routed out from the middle pixel, passing in between the other pixels. Our first design attempt can be seen in Figure 3.1. In Figure 3.1b we now see the connector that connects to the middle pixel which has to be routed out in between the top right and middle right pixel. In order to justify that the potential of the lead will not have a large impact on the 2DEG below it, the lead has to be much smaller than the pixel. If we can make the lead very thin, then in the far field, the 2DEG will not see the potential of the lead as dominating, but will instead see the potential of the pixels as dominating. This then leads us to the question how small can we make the lead and how large can we make the pixels.

The size of the lead is limited by our equipment and our patience. With our equipment we are able to make the lead around 10-20 nm wide, since beyond this dimension it is just not very reliable. Tests later revealed that we could fabricate the connector reliably if it was 30 nm wide. If we then look to see how large we can make the pixels, we are faced with the question of how wide do we want the QPC channel to be, or rather how large an area do we have to deplete with our gates in order to realise the QPC. This can be seen as the distance between the two large grey gates in the top of the design to the two large gates in the bottom of the design in Figure 3.1. We call the gates that are not pixels the outer gates. Their purpose is to deplete the 2DEG completely so that transport occurs only in between them, so that the pixels can be used to fine tune the channel that connects the two reservoirs.

To answer the question of how large can we make the pixels, we look to other QPCs that have shown good conductance quantisation steps. One QPC we looked at, and also tried to fabricate, was a QPC designed by QDev Master student Christian Olsen in 2015 [31]. His QPCs consisted of three gates, two outer gates and one gate to cover the area in-between the outer gates. The gap between his outer gates varied from 600 nm to 800 nm. In general we would want the distance between the outer gates, and thereby the size of the pixels, to be as small as possible, keeping in mind our other limitations.

Lastly there is the question of the spacing between pixels. Ideally we would want the spacing to be as small as possible to have full control of all the area in the channel. Although if we want a symmetric design, which we do, where the distance between pixels is equal, then the limiting factor is the gap where the connector to the middle pixel passes in-between the top right and middle right pixels. There is the risk of the lead merging with the pixels or the lead not being continuous if the gap between pixels is too small.

Yet again we encounter another limit. This time its the limit of the e-beam resist that we use. We use PMMA A2 resist for this lithography step, which is 50 nm thick. If we were to have a spacing between pixels of 50 nm, then 30 nm would be occupied by the lead and then there would be a gap between the lead and pixel of 10 nm on each side. This means that when we have exposed our pattern onto the resist and developed it, then the space between

the lead and the pixel will be a 50 nm tall resist wall that is 10 nm wide. Structures that are taller than they are wide have a tendency to fall over. Because of this it is recommended to use a spacing between gate features that is larger or at least close to equal to the height of the resist that is being used.

To summarize, we wish to have connectors that are as small as possible, to ensure that they are much smaller than the pixels. We want the pixels to be as small as possible making the distance between the outer gates as small as possible. The limiting factor is the e-beam resist and the width of lead.

The picture shown in Figure 3.1b is a SEM of one of the first test lithography runs, to test if we were able fabricate these thin leads. We ended up redesigning this design because we did not like how the leads of the middle left and right pixels were routed out along another thin lead. In Figure 3.2a we see a SEM of the new design where the bottom and top row of pixel now have their leads routed out in between the outer gates. One consequence of routing the leads out like this is that we split the outer gates thereby increasing the number of gates, which in turn increases the number of bond pads required on the daughter board. Fortunately we were able stay within the 48 bond pads available to us on our daughter boards. If we had exceeded this number one solution could have been to bond several outer gates to the same bond pad on the daughter board. Here, the limit is the number of lines we have available in the fridge.

After doing several test and attempting to fabricate the QPC on a chip with a heterostructure we did one final change to the QPC design to get more reliable results. The change was to increase the size of the entire design by 50% and giving the outer gates an almost bow tie look giving more space to the thin leads when they start to fan out. This design can be seen in Figure 3.2b. The new pixel spacing was chosen since we could relax our design requirements for the high-mobility GaAs/AlGaAs wafer, which had the 2DEG buried around 190 nm below the surface. Hence, gate pitches that were too small, were not required since they would not be resolved to that extent in the far field.

Apart from the design of the pixel QPC there is only the mesa left to be designed. The specific mesa design we used for this project is a design used by many others at Qdev and

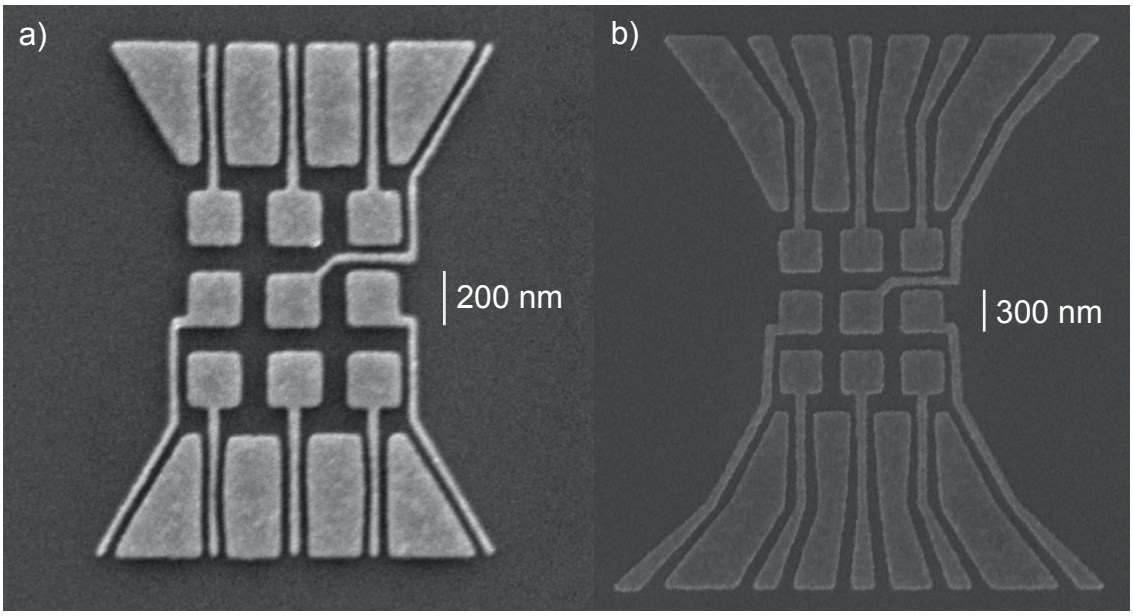

Figure 3.2: **Designing the pixel QPC 2 a)** SEM of the second nine pixel QPC design. **b)** SEM of the final design of the nine pixel QPC.

previously at Harvard University [28, 23]. The mesa can be seen in Figure 3.5 and in Figure 4.1. What stands out in the design of the mesa, are the E shaped ohmics. They are designed in this way to improve the ohmic contact to the edge states that appear at high magnetic fields. The worry is that if the ohmic was in the shape of a square, then an edge state would travel along the edge and thereby not come in contact with the metal we deposit on top.

3.2 Choice of wafer

As mentioned in the description of 2DEGs there are pros and cons to different wafers. Some wafers are grown specifically to have good gate action and low hysteresis, while some are designed to have very high mobility. For our experiment we wished to investigate the physics of the fractional plateaus in the fractional quantum Hall effect, using our pixel-gate QPC. So our ideal wafer would be a wafer which had both good gate action and showed evidence of the fractional quantum Hall effect.

Unfortunately, wafers with very high mobility get their mobility from being very highly doped. This hinders the gating of the 2DEG because the dopants can act as charge traps and screen the gates. Another factor that turned out to have a great influence on the results of our work, was how easily we could make ohmic contact to the 2DEG. Wafers that are highly doped are also much easier to make ohmic contact to, while highly resistive ohmics were exactly the reason why we had to deem our first two devices, attempted on a less-doped wafer, unsuccessful.

The wafers that are available to us are wafers designed and fabricated by Michael J. Manfra and his group at Purdue University. We get the wafers sent together with data sheets that show quantum Hall measurements. From these data sheets we can quickly determine the wafers that have the potential to show signatures of the fractional quantum Hall effect and those that don't, typically by assessing the mobility and density and the magnetic fields available in our dilution refrigerators. When it comes to how well the wafers gate, we have to rely on the experience of others who have worked with the wafers and tried gating them. It was on the basis of these considerations that we decided to use the following two wafers.

The first wafer we tried was a 90 nm deep 2DEG which was designed with the aim to be used for spin qubit devices, meaning it was designed with the aim to have good gate action and because of this it is not highly doped. It had a stated mobility of $4 \times 10^6 \frac{cm^2}{Vs}$, which is not super high compared to the second wafer we used, but could be adequate. It looked like a perfect match, best of both worlds, but we were unfortunately not able to make good ohmic contact to this 2DEG.

The second wafer we used had a 2DEG 190 nm deep and was designed with the aim of having a very high mobility. It has a mobility of $24.6 \times 10^6 \frac{cm^2}{Vs}$, measured at 300mK, and it is highly doped. We were able to make good contact to it and even though gate ramps showed hysteric behaviour we were able to find a measurement method where we could reproduce the behaviour of our pinch off curves described in section 5.3.

3.3 A lithography step

Although the fabrications process is long and each of the fabrication steps has to be fine-tuned to fit the exact needs of that step, there is a common workflow that is repeated several times throughout the process. Each of the main processes has a lithography step, and in total there are five lithography steps to be completed to fabricate one device with the recipe I have used. The five steps are: Markers, Mesa, Ohmics, QPC and Bond Pads.

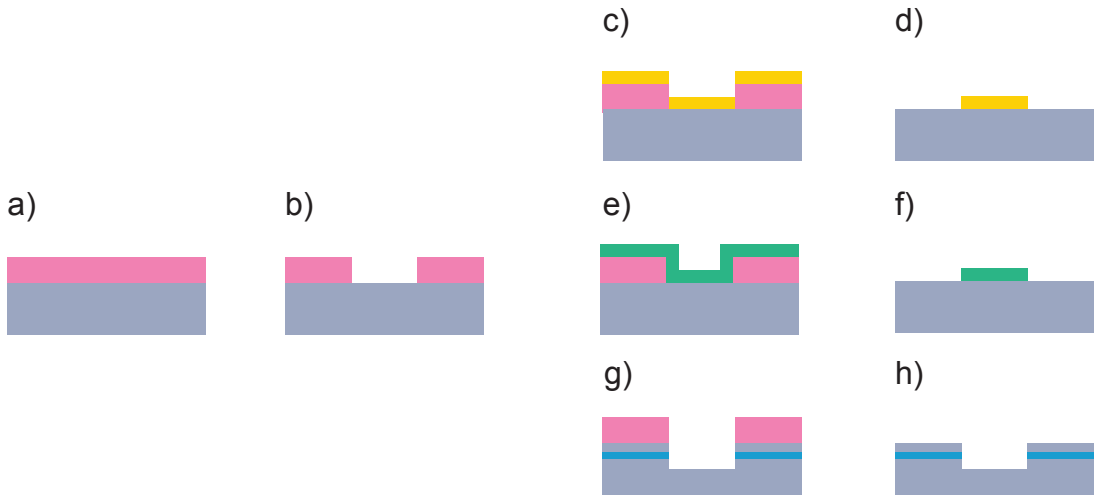

Figure 3.3: **A single lithography step**. **a)** The first step is spinning resist, in pink, on the sample, in grey. **b)** The second step is exposing and developing. After this step one of three things can happen: Metal evaporation, ALD growth and mesa etch **c)** Metal, in yellow, is evaporated onto the sample. This process leaves some of the resist not covered making it easier to do lift off. **d)** Lift off is done in a solvent that removes the resist, leaving behind metal that is stuck to the sample. **e)** ALD, in green, is grown on the sample. This process covers all surfaces of the chip thereby enclosing the resist. **f)** Lift off is done. With ALD it is tricky because the resist is entirely enclosed. **g)** Mesa is etched, the 2DEG is highlighted in blue to indicate that the etch has to pass it. **h)** Resist is removed after the mesa etch.

We start out by cleaning our wafer piece, chip, to ensure a uniform spin coating. If even one speck of dust is on the wafer when we have put on the drop of resist and start the spinner, then this tiny spec of dust will be flung along the surface and leave a rift in the resist.

The resist we use depends on the features we want to make. For the fine gates of the QPC we use PMMA 2%, which has a thickness of 50 nm, because this fits the features size of our gates of around 30 nm. For the ohmics we a use stack of PMMA 8% (500 nm), PMMA 8% (500 nm) and PMMA 4% (200 nm) for a total of 1.2 μm. This is to make sure we can

lift off the metal stack of almost 600 nm metal that will constitute our ohmics.

When spinning the resist there are two parameters that can be chosen for the spinner. There is the rotations per minute of the spin and the duration of the spin, and they will have an impact on the thickness of the resist. In general we use 4000 rpm and 60 sec, which gives reliable outcomes for most of the resists we use. Beyond 4000 rpm the resist will not get much thinner and the same is true for spin time. This can be seen by looking at spin curves from the supplier of the resists.

After spinning the chip we bake it on a hot plate to harden the resist. The baking temperature differs from resist to resist and baking time can also vary significantly. One thing to be aware of is cross linking the resist, by baking it at too high a temperature or baking it for too long.

After the spin is complete, the chip is ready for the exposure. There are many parameters to optimise for the exposure, and these will not be explained in detail. When the resist gets exposed it changes composition and the exposed resist can be removed with a developer. This is true for positive resists. There are also negative resists, where it is only the exposed resist that will not be removed by the developer, but we don't use these.

When the chip has been developed it is ready for the metal deposition, as seen in Figure 3.3c and d, or if we were fabricating the mesa, the mesa etch as seen in Figure 3.3g and h). For the four fabricating steps other than the mesa etch we would now do the metal deposition. This is done using e-beam evaporation, where a crucible with metal is heated using an e-beam and the evaporated metal will cover the entire chip with a uniform layer of metal. A standard metal stack for a generic metal gate, would be of titanium and gold. The titanium acts as a sticking layer to ensure that the gold sticks easier. The amount of metal that needs to be deposited depends on what is being made. For the markers it is important to deposit enough metal to have them be visible under resist during alignment. Around 100 nm Au is sufficient. For the ohmics a special recipe has to be made to fit the wafer. This can vary a lot. For our fine gates in the QPC, we deposit 5 nm Ti and 18 nm Au, to ensure a good lift off. The final fabrication step are the bond pads that have to be connected to the much smaller QPC gates. It is important to be aware of the height of the mesa when

depositing the metal for the bond pads. This is because the bond pads are not on the mesa, so there has to be deposited enough gold to climb the mesa.

The final step is the lift off where the remaining unexposed resist is removed. When the resist is removed, all the metal that was deposited on top of the resist will fall off and only metal that was deposited directly onto the surface of the chip will remain.

In Figure 3.3 the ALD growth is also shown in e and f. Because the lift off of ALD is very tedious, we decided to cover the entire chip with ALD instead. This was done after the ohmics had been made.

3.4 Cleaving

Cleaving a chip with a scribing pen is the first step that needs to be done before any fabrication can begin. Scribing with a pen is done by making a small notch on the edge of the wafer, and then placing the wafer on an edge such that the notch aligns with the edge and then pushing on each side of the notch. The edge can be that of a glass slide, the tip of the scribing pen or ideally a scribing block. Because of the almost perfect crystal structure of the wafers, the wafer is prone to cleave along certain crystal orientations. These are usually the directions which we wish to cleave along and they are marked on the full wafer with the major and minor flat. The major and minor flat indicate some crystal direction which is given by the manufacturer of the wafer.

When cleaving it is important to keep track of the crystal direction of the wafer, if it turns out that the experiments is dependent on crystal orientation. This is one of the reasons it is important to mark the chip with a symmetry break. A symmetry break is also important in general for the fabrication process especially when placing the chip with the proper orientation for exposures.

There are three aspects of cleaving which are important to consider when cleaving. The amount of wafer residue that end up on the surface of the chip, the dimension of the wafer piece and how straight the edges are.

The cleanliness of the surface of the wafer is important because a single dust speck can ruin a spin coating or a part of the design. Because of this we usually spin coat the wafer with a layer of PMMA 4% to protect the surface of the wafer from wafer residue from the scribing. Afterwards the PMMA can be stripped and any residue will be removed with it.

The dimensions of the wafer piece are mostly important with regards to whether or not the design can fit. Other than that the only limiting factor is if the chip can get a good spin coating and if it can fit in the equipment. The smallest wafer piece we tried spinning was 5 mm x 3.5 mm.

The straightness of edges are important, because a chip with sloped edges can be near impossible to pick up with a pair of tweezers. And if it can't easily be picked up with a pair

of tweezers it is not worth fabricating on.

At Qdev there are four ways we can cleave a chip: with a scribe pen , with the manual scribe, with the automatic Loomis scribe and with the wafer saw. During this project we ended up using all of these except the wafer saw. Scribing with the scribing pen is good for quick tests, for example a dose test, on blank wafers that don't have any heterostructure on them. It often happens that the notch is not placed exactly where it was supposed to be and then the cleave can end up giving an uneven edge.

The manual scriber gives more precision and accuracy than a scribing pen, but can leave a lot of residue on the surface on the chip. When using the manual scriber the cleave still has to be done by hand, and this still leaves room for a lot of errors.

The Loomis scriber is an automatic scriber which is controlled with computer commands and it has a cleaving function which cleaves exactly along the scribe. We used the automatic scriber for most of our samples.

3.5 Markers

The first lithography step of the fabrication process are the alignment markers. Their purpose is to ensure that for all of our exposures the lithography equipment exposes the design in the correct place on the chip. It is from the markers that we can make a reference for a coordinate system in which the design is placed.

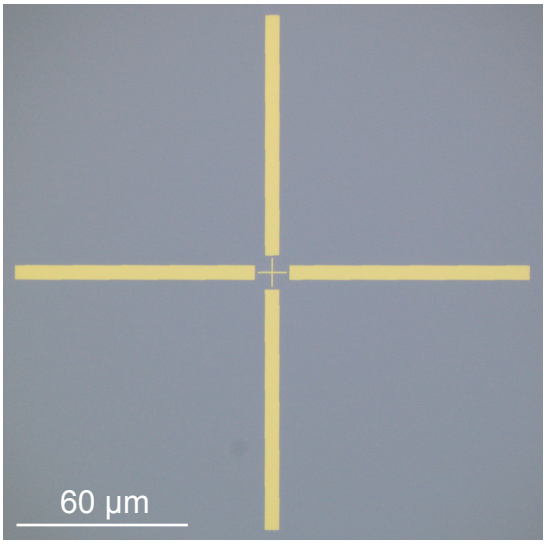

Figure 3.4: **Alignment Marker** Bright-field optical image of a titanium gold alignment marker after lift off. The design of the marker is a standard that works with many different lithography systems.

The markers have the shape of a cross with an even smaller cross in the middle of it, as seen in Figure 3.4. The small cross in the middle has a size that fits the zoom presets on our lithography systems such that when we move to the markers we can easily align to it. Whenever we do alignment with a set of markers, it usually means that we will not be able to use them again. This is because the resist that covers the markers will be exposed during the alignment process and then when we do the mesa etch or a metallisation we will either etch the markers or cover them with metal. To make sure we have enough markers for all the exposures, we expose five sets of four markers.

When we do the annealing of the ohmics, we also anneal the metal of the markers. This results in an uneven surface of the metal on the markers which worsens the alignment. When the Elionix lithography systems locates the markers, it scans a line perpendicular to each of

the four alignment marker arms. It then measures the reflected signal to identify the middle of each arm. If the surface of the marker is not uniform it can worsen this process. We were able to align within 100 nm with annealed alignment markers and this was good enough for what we needed. Using markers that are not annealed we can align to within 10 nm. If we wanted to be able to align with in 10 nm, then we could change the order of the exposures to be: Mesa, ohmics, markers, QPC and bond pads.

3.6 Mesa

The purpose of the mesa is to confine the 2DEG into smaller and more controlled areas on the chip. When we receive the heterostructure wafer piece there is a 2DEG across the whole wafer. In our case we wish to do Hall bar measurements and therefore need to remove some of 2DEG to make Hall bars. One of our Hall bars can be seen in Figure 3.5. An upside to this fabrication step is that we can fit four mesas onto a 5mm by 5mm wafer piece and we can then pick and choose the ones that look best at the end of the fabrication process.

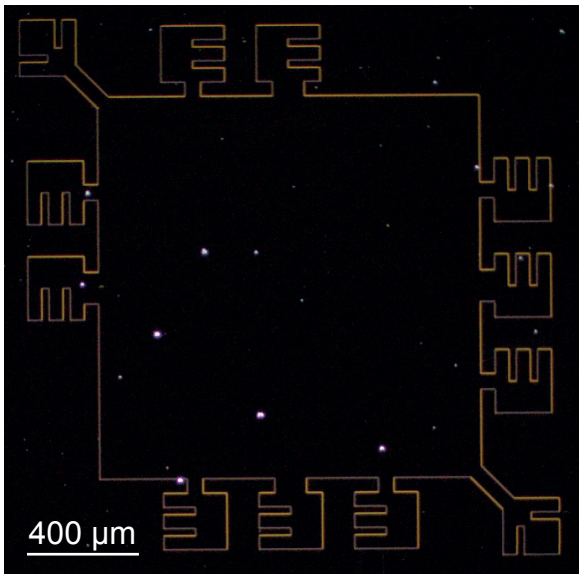

Figure 3.5: **Mesa** Dark-field optical image of the sample after the mesa etch has been done. Dark-field images highlights height differences, so the bright features are edges or dust specs.

When doing the mesa etch it is important to make sure we etch past the 2DEG. To ensure this we do a test etch on a wafer piece without a heterostructure and then measure the height of this piece and estimate an etch rate. We then pick an etch time that would etch at least 20 nm past the 2DEG depth. After the etch we can strip the resist and measure the height of the mesa with a profilometer. Ideally we could measure the height of the resist before the etch and then measure the height of the mesa and the resist at intervals during the etch. Unfortunately we had problems with the profilometer needle sticking to the resist and not being able to measure the height while the resist was on the device.

3.7 Ohmic contacts

In order to do current transport measurements there has to be made an ohmic contact to the 2DEG. We do this by depositing gold, germanium and platinum on the sample, and then annealing it to make an eutectic alloy of the gold and germanium that then spikes into the wafer to make a contact to the 2DEG. An ohmic after annealing can be seen in Figure 3.6.

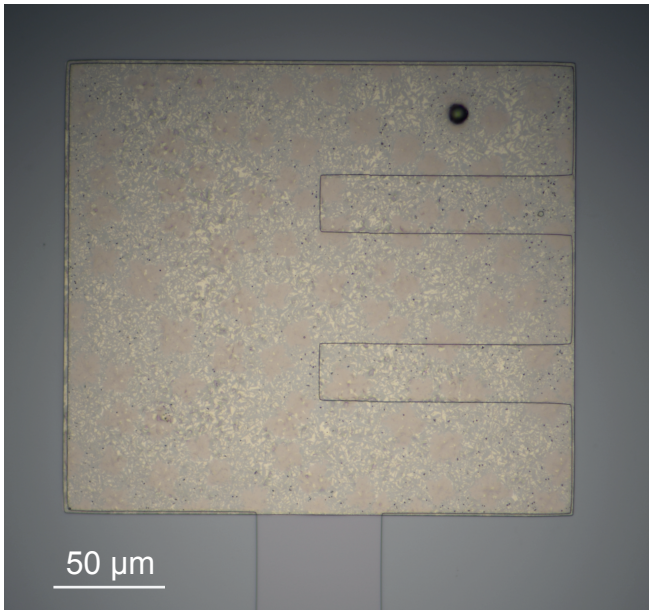

Figure 3.6: **Ohmic**. Bright-field optical image of an ohmic. The mesa, where the 2DEG reside, has the shape of an E, and on top of the E, is a rectangular metal stack that has been annealed.

The process of making ohmic contacts follows the same steps as a normal metal deposition with some alterations. We start by thoroughly cleaning the sample as a clean surface is important for a good ohmic contact. Then we spin it, expose it, develop it and ash it. After doing these steps we load it into the AJA and run a RF milling recipe. RF milling works by filling the chamber with Argon plasma and then applying a small oscillating voltage to the sample holder. This will accelerate the argon plasma into the sample which will clean the surface even more and thereby improve the contact. We then deposit our metal stack, unload and do lift off like normal. After lift off, the chip is loaded into the RTA (rapid thermal annealer), and the ohmics are annealed.

We faced many problems with our ohmics and also spend a lot of time trying to develop a new ohmic recipe for the 90 nm wafer. In total we fabricated three devices, the first two

were deemed not good enough because of their ohmics resistance was too high (of the order of kiloOhms at low temperature). The third device was fabricated using the highly doped deep well wafer, which is easy to make contact to. The tricky part of developing new ohmic recipes is that there is not always an easy method to try many different metal stacks and many different annealing programs, without also using a lot of material and doing many exposures. For our tests we made a chip with four mesas, then spun it with the resist for the ohmics and exposed it. We could then cleave it into the four mesas before development, and then when we developed each of the pieces, the dust from cleaving would fall off. With this method we could try out four different metal stacks and annealing programs with only two exposures.

The metal stack we ended up using for the ohmics is very tall, contains a lot of metal, and takes a long time to metallise. Because of this the AJA chamber can get very hot and end up damaging the resist by hard baking it. To prevent this we would take breaks in between the metal layers to let it cool. We would usually take these breaks after metallising platinum which needs a very large current to melt. Another concern when metallising platinum is that it can ”spit”. These metal chunks that are shot at the sample can damage the resist but is for the most part harmless, and will just leave spots on the ohmics.

3.8 Fine gates of the QPC

The fine gates of the QPC are one of the more challenging exposures because the optical microscope cannot magnify enough to let us see if the development and metallisation went well. If we were to use the e-beam microscope we could end up damaging the device and so we only know if the lift off went well when the device is loaded and we can check for pinch off and leakage between the gates.

One of the main challenges we faced while figuring out the exposure for the QPC gates was a problem concerning the PEC'ing of the design. PEC stands for proximity effect correction and is an algorithm in the design conversion software called Beamer that corrects the exposure dose for back-scattering. We saw that when we did dose tests of the small QPC gates only, where the design covers an area of about 4 μm by 4 μm, we would see one set of doses that gave good results. But then when we expanded the design to include longer gates that fanned out to be about 2 μm wide each for a total exposure area of about 40 μm by 40 μm, the design would end up being overexposed. It turned out that the PEC algorithm ends up assigning a too large dose if the design is too large. To fix this we only PEC the inner part of the QPC exposure and leave the larger features of this exposure unPEC'ed.

3.9 Bond pads

The final step of the fabrication process are the bond pads and larger gates. These gates are done in a lithography step of their own because their feature sizes are much larger than that of the QPC gates and also because they need to be tall enough to climb over the mesa edge. In our case the mesa is 200 nm tall and in order to make sure that the metal on top of the mesa makes contact to the metal not on the mesa, we metallise at least 50 nm more metal than the height of the mesa.

One of most important aspects of bond pads is that they should be easy to bond to. To ensure this we make the bond pads 200 μm by 100 μm to give good space for the bond to stick and in case another bond is in the way we have space to maneuver around it. The metal stack of gold and titanium are also easy to bond to. In general we did not have any troubles with the bonding.

4 Device overview

4.1 Picture of the device

In Figure 4.1, we see an optical picture of the entire device after the final lift off of the bond pads. We see three square mesas, top left, bottom left, and bottom right. For this device we decided to make a mesa with a different design compared to what we had worked with so far. If the other square mesas turned out not to show features of the quantum Hall effect as we wanted, we could unload and re-bond the two mesa seen in the top right.

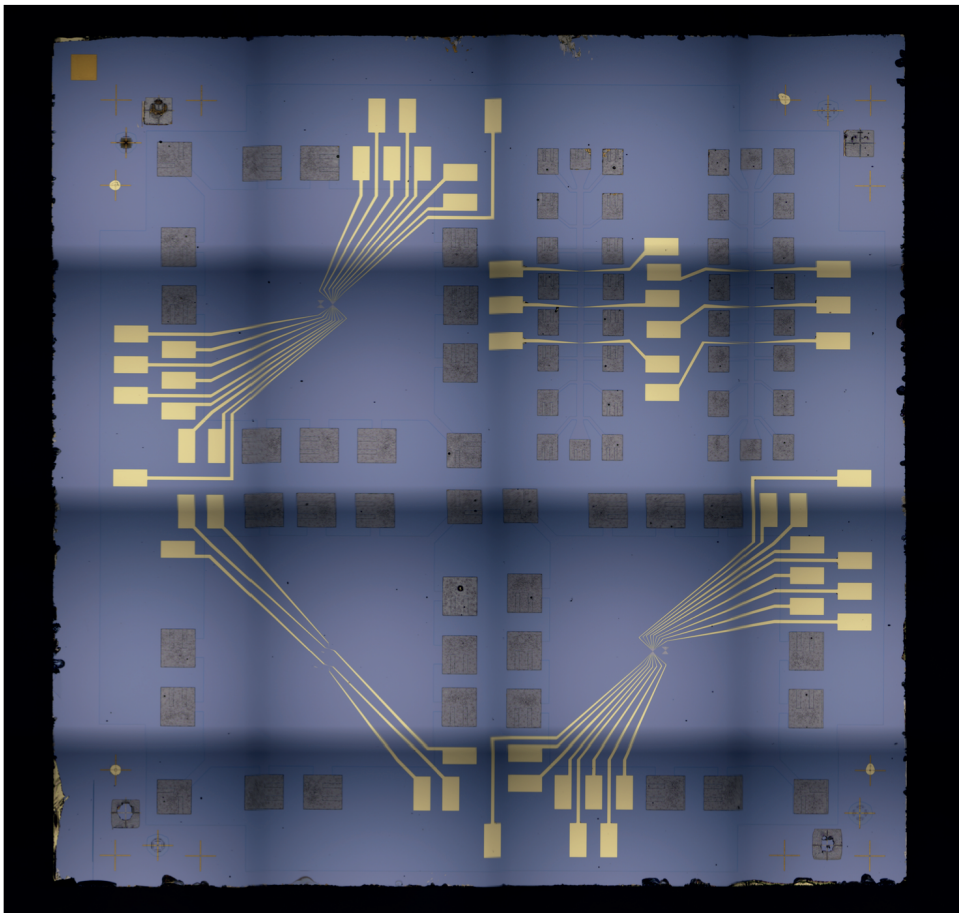

Figure 4.1: **Entire device** Bright-field optical picture of the entire device. The picture consists of 16 individual pictures that the microscope software stitches together to one picture. The wafer piece is 5 mm by 5 mm.

The top left and bottom right mesas each have a pixel QPC, and we decided to bond the top left mesa and QPC. Looking closely at the center of the three square mesas there are also some small spots of gold next to the QPC. These spots of gold are from a QPC exposure where the alignment went bad. So when we had to do the final exposure with the

bond pads, we were not able to align to these QPCs. Because of this we exposed a second design next to it which we were able to align to for the bond pads exposure. The bottom left mesa has two QPCs based of off Christian Olsens QPC design. These two QPCs were not able to pinch off the 2DEG. To bond the top and bottom left mesas and QPCs we need 47 bond pads, leaving us with one left over bond pad on our 48 bond pad daughter board. So we are not able to bond all mesas and QPCs on this device. From the device picture we can also see how all the different features look. In the top left we see a gold square which is the symmetry break. We also see that three of the five marker sets have been damaged from the processes of the other fabrication steps. This leaves us with two sets of markers to spare. We see that the metal of the ohmics and markers are much darker than the metal of the bond pads and gates. This is because of the annealing, and to some extent, the ohmics also containing other metals than gold.

4.2 Device schematic

Figure 4.2 shows a schematic of the top left mesa and QPC as seen in Figure 4.1. Figure 4.2a is of the entire mesa and QPC and Figure 4.2b is a zoom in on the pixel QPC which is located at the center of the mesa. We chose the dimensions of the pixels in this QPC design to be 300 nm x 300 nm, the distance between the center of one pixel to another to be 464 nm and the width of the leads that connect to the pixels to be 30 nm.

For the algorithm run we will show below, we will look at two different QPCs that we call the right QPC and the middle QPC. The right QPC consists of the top right and bottom right pixel(P3,P9) being swept, while the outer gates are at a voltage where the 2DEG is depleted beneath them. Similarly, the middle QPC is realised by sweeping the top middle and bottom middle pixels(P2,P8), while the outer gates are depleting the 2DEG beneath them.

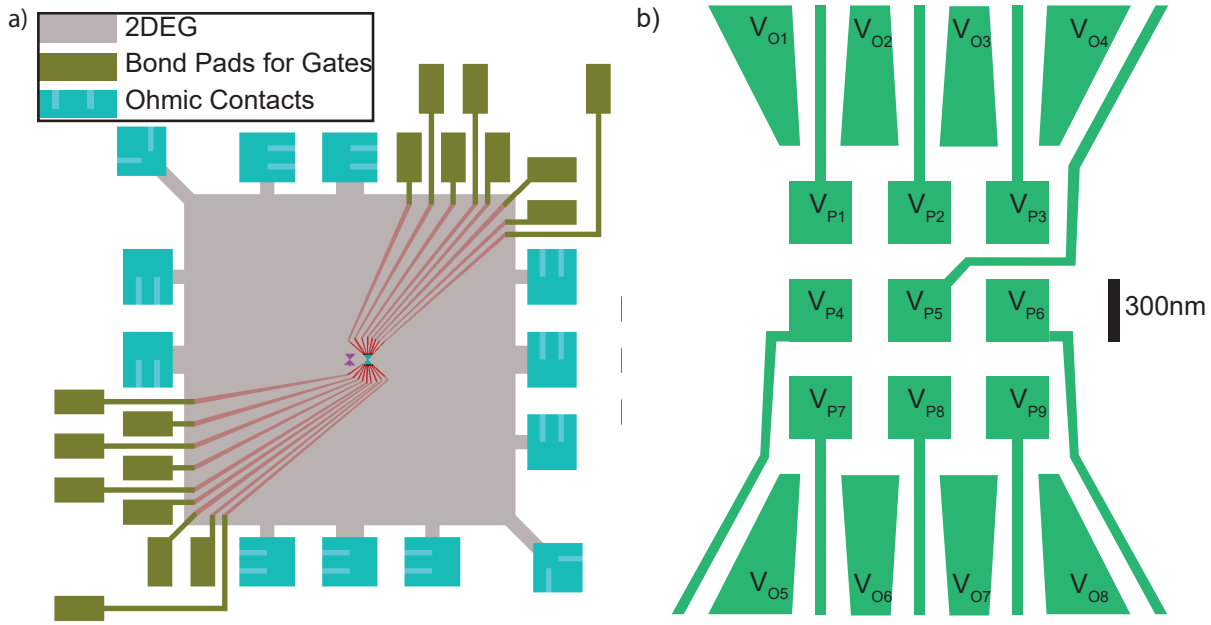

Figure 4.2: **Device Schematic. a)** Mesa and QPC gates overview, showing the mesa, where the 2DEG resides, in grey. Ohmic contacts are shown in blue and bond pads are shown in green-brown. The gate fan-out are shown in red. **b)** Zoom in on the pixel QPC.

4.3 Voltage Bias and Current Bias

The two main measurement setups we have been using have been voltage and current bias measurement setups as seen in Figure 4.3a and b. We used the voltage bias setup when we wanted to measure the resistance of the QPC and we used the current bias set up when we wanted to measure the quantum Hall effect.

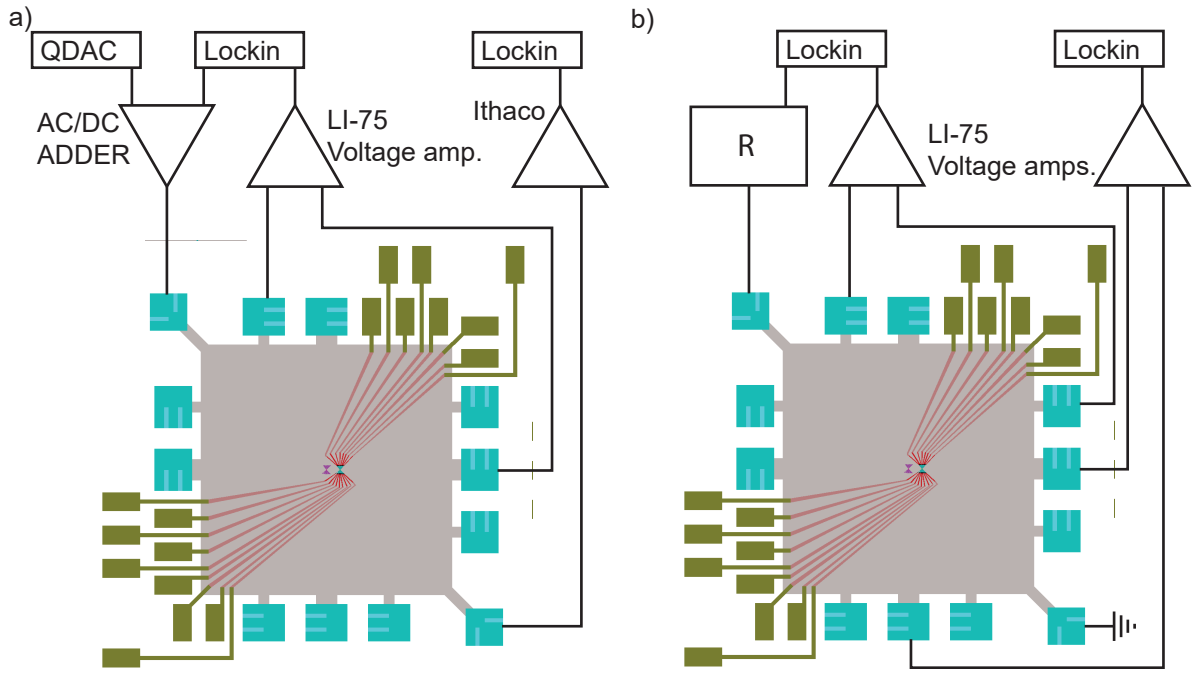

Figure 4.3: **Voltage and Current Bias. a)** Shows the voltage bias setup, which is used for measurements where we wish to pinch off the current. **b)** Shows the current bias setup which is used for quantum Hall measurements.

For the voltage bias setup we use a four-terminal setup where we have one voltage probe on each side of the QPC, an ohmic where we apply a voltage on one side of the QPC and an ohmic where we measure the current on the other side of the QPC. The rest of the ohmics are floating. On the ohmic, where we apply a voltage, we have a AC/DC adder, such that we can set a DC bias offset with our QDAC and on top of that send an oscillating AC excitation from our lock-in amplifier. We then measure the voltage difference across the QPC with the two voltage probes that go to a LI-75 voltage amplifier, from which we get the voltage difference, and this is sent to the lockin amplifier. The current is measured with an Ithaco current preamplifier and a lock-in amplifier.

When we do the quantum Hall effect measurements in magnetic field we use the current

bias setup. This setup differs from the voltage bias setup by having a large resistor of $10M\Omega$ on the ohmic where we apply the excitation voltage. If the resistance of the resistor is much larger than the resistance of the system, then we know the total resistance of the system and since we know the voltage of our excitation we know the current in the system. Because of this we do not have to measure the current, and can let the current run to ground. For the quantum Hall measurements we need two voltage probes for the Hall voltage and two voltage probes for the longitudinal voltage. Again we use a LI-75 voltage amplifier to a lockin amplifier for both of these voltage measurements.

5 Baseline measurements

When the fabrication process is done, and the device has been loaded into the dilution refrigerator we preform a set of baseline measurements to determine whether or not the fabrication was successful. In this section we will go through these measurements and discuss when a device is good enough and when it is needed to go back to the cleanroom and make another device.

5.1 Ohmics

We measure the ohmic contacts by grounding all but one contact to which we connect the Keithley. Using the Keithley we apply a voltage to the bond pad and measure the current leaving the Keithley. The range is chosen such that we sweep through zero bias so we can see if there is a good contact to the 2DEG at the low bias regime which we will use for our actual measurements, typically 1mV and lower.

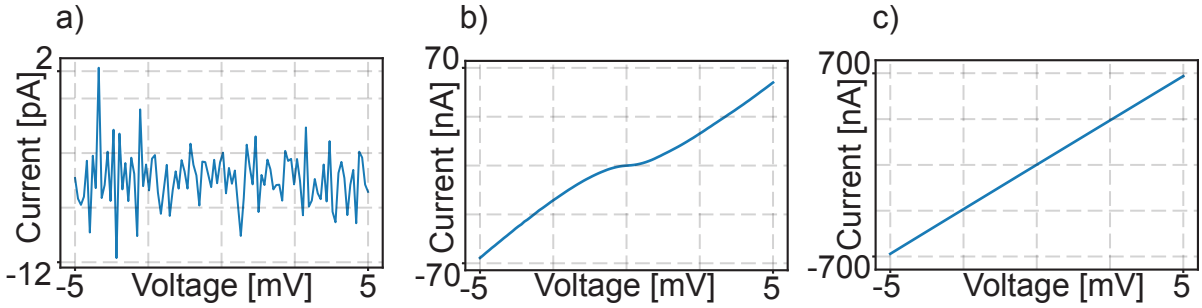

Figure 5.1: **Ohmics** Overview of IV-measurements of different Ohmics **a)** IV-Measurement of an ohmic that does not have contact to the 2DEG **b)** IV-Measurement of an ohmic that does have contact to the 2DEG but with a large Schottky barrier, resulting in a very large resistance at low bias. **c)** IV-Measurement of an ohmic with a good contact to the 2DEG.

The first two devices that were fabricated had ohmics that showed IV measurements resembling those of Figure 5.1a and Figure 5.1b. There were either no contact to the 2DEG or there was almost no current at low bias. The recipe we had been using was developed for a 57 nm deep 2DEG, and after doing a few unsuccessful tests trying to adapt the recipe to our 90 nm 2DEG, we realised that the ohmics might turn out to be a bigger challenge than expected. We had many wafers available to us that we would like to use, but we did not have any ohmic recipes for them.

After unsuccessfully trying to develop a new ohmic recipe for the 90 nm wafer, we moved on to the 190 nm wafer, to which we were able to make good ohmic contact with the first test. All ohmics showed IV-measurements resembling that seen in Figure 5.1c. Because of this we quickly decided not to measure on the 90 nm devices and started fabricating the third device on the 190nm wafer, which also turned out to have good ohmics.

5.2 Pinch Off

When we have determined that the ohmics are satisfactory we move on to measure whether the gates can gate the 2DEG, especially to the point of pinch off, or not. To do this we use a setup similar to the one shown in Figure 4.3a.

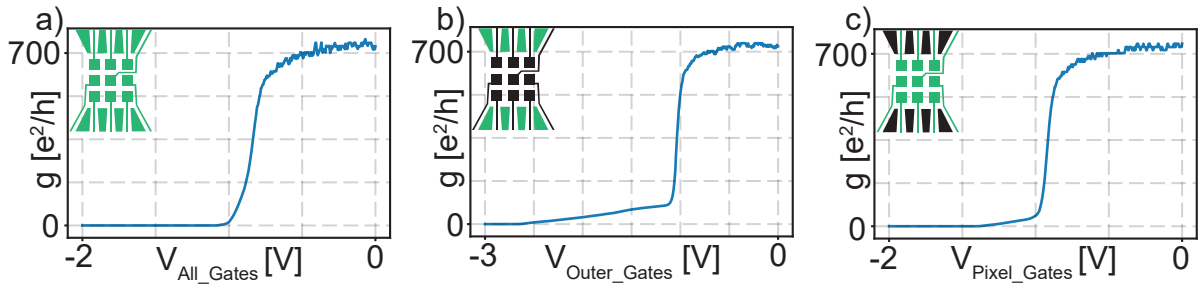

Figure 5.2: **Pinch Off** Overview of the pinch off of different groupings of gates. **a)** Pinching off with all gates **b)** Pinching off with outer gates **c)** Pinching off with pixel gates.

Looking at the three different pinch off curves in Figure 5.2, we see that they all have a sudden drop in conductance at around -1 V. This is when the 2DEG directly beneath the gates is depleted, and is called depletion. In Figure 5.2b and c we see that after depletion there is a gradual decline in the conductance, which we call pinch off. We see that the pinch off region spans a larger voltage range for the outer gates, Figure 5.2b, than it does for the pixel gates Figure 5.2c. The outer gates are more than 1 μm apart and have to deplete the 2DEG in this space. For the pixel gates it is more difficult to exactly pinpoint the path of the current that needs to be pinched, as we are not sure how much the leads influence the 2DEG. It was on the basis of measurements like these that we decided to limit the voltage we could apply to the gates to -2 V, to protect the device.

5.3 Hysteresis

For us to quantify how well each of the pixels gates work, we want to do a set of measurements that show how well each pixel can deplete the 2DEG and how hysteretic each pixel gate is. To do this we would ideally want to deplete the 2DEG such that we create a channel underneath a row of pixel gates. We could then ”close” and ”open” this channel with each of the pixel gates in that row and then compare them. We tried this method of pinching off row by row. For example we would set the top row of pixels to 0 V and then sweep all the other gates with a common voltage to identify a pinch off point. We would then set the gates at a voltage just before the pinch off point and then sweep each of the pixel gates in the top row. Using this method we found that some of the pixel gates did not reduce the current through the device at when sweeping them from 0 V to -2 V. We suspected that the connectors fanning out from the other pixels might have had an influence, and screened off some of the other pixel gates.

Because we were suspecting the connectors to be having an effect on the surrounding pixel gates we thought of an alternative way to characterise the pixel gates, which was to separate the gates into the gates that fan out to the top of the mesa (O1,O2,O3,O4,P1,P2,P3,P4) and the gates that fan out to the bottom of the mesa (P4,P6,P7,P8,P9,O5,O6,O7,O8) into two groups. By doing this we can set the gates fanning out to the bottom of the device (P4,P6,P7,P8,P9,O5,O6,O7,O8) to -2 V to deplete the 2DEG beneath those gates. Then we sweep the top outer gates (O1,O2,O3,O4) to a pinch off point, and set them to a voltage just before that pinch off point. This would leave the top row of pixel gates (P1,P2,P3) and the center pixel (P5) gate at 0 V. We would expect the current path to be beneath these gates. Each of these pixels can then be swept for pinch off and the same procedure can be done for the pixel that fan out to the bottom of the device. The data shown in Figure 5.3 was taken using this method, and the position of the plots matches the position of the pixels. The orange data points are from the down sweep and the blue points are from an up sweep. We see that the up sweep and down sweep have a pinch off point that differs less than 0.1 V for all the pixels which indicates that there is very little hysteresis. We also see that the pinch

off point for each of the pixels is also very similar for each of the pixel gates and lay between -1.3 V and -1.1 V. If the pixel gates had shown to have had large differences in pinch off points, we would be able to account for this by either applying more or less voltage to those gates compared to the others. Knowing that the pixels show almost identical behavior also gives us a good basis for interpreting the data from the algorithm runs. If we see that the algorithm assigns a potential of 0.2 V less to one pixel gate than the others we will know from this data that it is not because that gate is stronger.

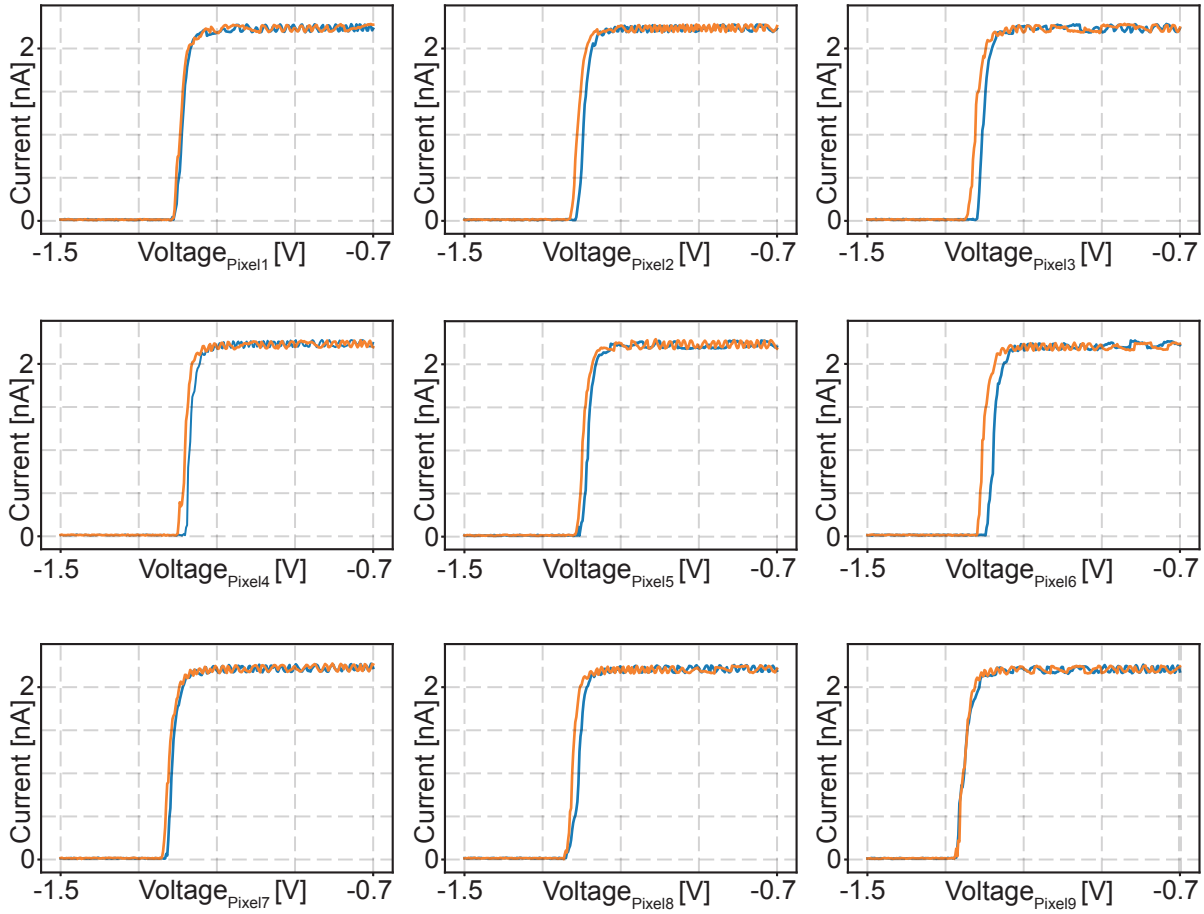

Figure 5.3: **Single Pixel Hysteresis Measurements** Overview of how hysteretic each pixel gate is. The orange data points are from a down sweep and the blue data points are from an up sweep preformed right after the down sweep. Each of the graphs are positioned like each of the pixels, so top left graph is from the top left pixel.

Unfortunately the device did not show this behavior when we started running the algorithm to optimize for conductance steps. The device had changed, as seen in Figure 5.4a, and we were forced to implement a routine where we wait at 0 V before each down sweep to

ensure a consistency in the pinch off curves. Because we are interested in the voltage range just before the pinch off, where the conductance is around 20 conductance quanta, we jump from 0V to the starting value of our sweeps and then also wait at this voltage before every sweep. We found that if we wait at 0 V for 20 s and at our starting voltage for 10 s, we were able to better replicate the pinch off curves as seen in Figure 5.4c. Using this routine we were able to run our algorithm and find configurations of voltages that showed conductance steps. Had we not used this routine then the loss function score landscape would have changed every sweep and the algorithm would be looking for moving minima.

Taking the hysteresis into consideration for the next device fabrication is important since there is a very large time loss when we have to wait 30 s for each data point for the algorithm. We are interested in running this algorithm as quickly as possible such that we can explore as many configurations as possible. Each down sweep takes about 90 s to measure so removing the wait time will reduce our measurement time by 1/3. In future, a careful choice of wafers, to identify one where quantised conductance is not difficult to observe but which is not hysteretic for gating purposes, would be a good direction to try.

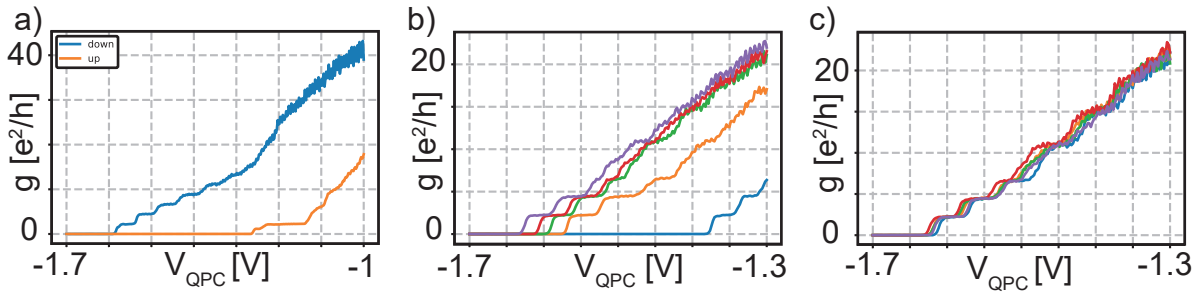

Figure 5.4: **Waiting Times** Because the device showed to be very hysteretic we would set all the gates to 0V and introduce a wait time before every sweep. **a)** A down sweep and an up sweep done in succession without waiting. **b)** Several down sweeps where we wait at 0 V for 10 s then jump to -1.3 V and wait 3 s there before doing the down sweep. **c)** Several down sweeps where we wait at 0 V for 20 s then jump to -1.3 V and wait 10 s there before doing the down sweep.

5.4 Quantum Hall effect

In order to apply an algorithm with the aim to investigate the fractional quantum Hall effect, we have to first be able to measure the fractional states at all in a given wafer. To do this we perform magnetic field measurements and look at the Hall resistance. We use a current bias set up by placing a large resistor of 10 MΩ on the sine out of the lockin such that the total resistance of the system is dominated by the large resistor. We then apply a voltage of 40 mV from the lockin which results in a current bias of 4 nA. To measure R_{xx} we have to measure the voltage along the current path, so the ohmics have to be "on the same side" of the current path. To measure R_{xy}, the Hall resistance, we have to measure the voltage across the current path, so there has to be an ohmic "on either side" of the current path. The setup we used can be seen in Figure 5.5a. This setup was picked based on symmetry of the ohmics, as we thought that was important for the measurement. A perpendicular magnetic field is needed to do the measurement, so we also had to mount the device in the sample puck such that it was perpendicular to the z-direction of our vector magnet, because it is in this direction it can produce the largest magnetic field (6T, while the x- and y-directions are limited to 1T). When we set the magnet to increase its field, we do it using a continuous sweep at 30 mT/s. We then record V_{xx} and V_{xy} twice a second throughout the magnetic sweep. The measurement can be seen in Figure 5.5b.

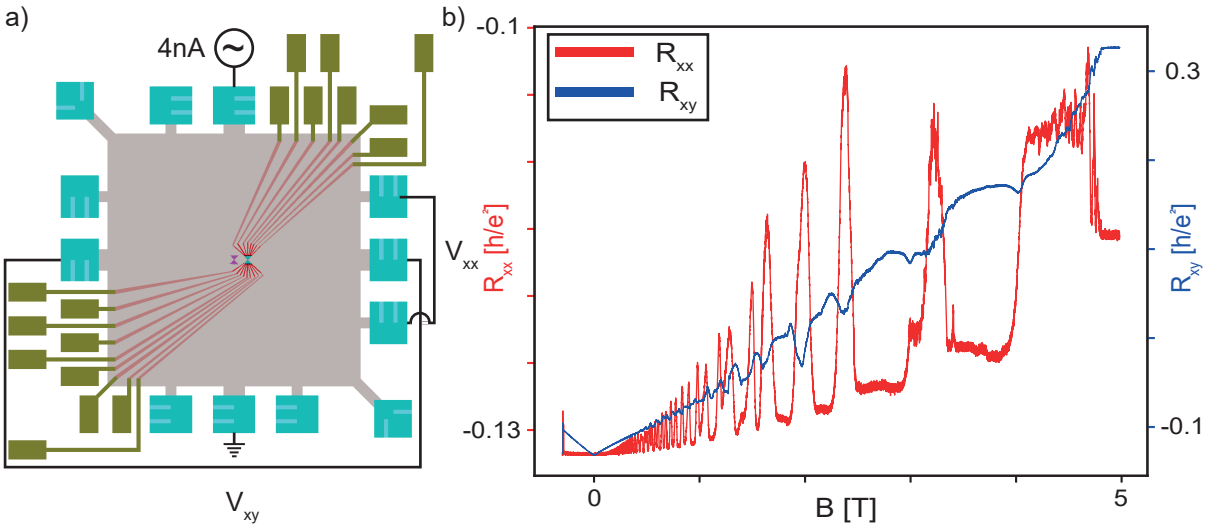

Figure 5.5: **First Magnetic Field Sweep. a)** Device overview with experimental setup used for the measurement **b)** Quantum Hall measurement with the Hall resistance shown in blue and the longitudinal measurement shown in red.

The data points shown in blue are the Hall resistance, which should ideally look like a staircase with flat steps, that indicate the filling factor of the system. We do see some resemblance to a staircase, but it is far from ideal. The red data points show the longitudinal resistance, R_{xx}, which should show zero resistance when R_{xy} is at a plateau, indicating perfect conduction, because of the edge states, and then show a peak in between plateaus in R_{xy}. We do see the peaks in R_{xx} but we do not see the resistance drop to zero in between peaks, which is again not ideal.

Some of the possible reasons to why we see this behaviour could be: (1) the mesa etch had damaged the 2DEG, (2) the ohmic anneal temperature had been too high and damaged the 2DEG, (3) the ohmic metal stack, (4) the wafer being too old or (5) the mesa design.

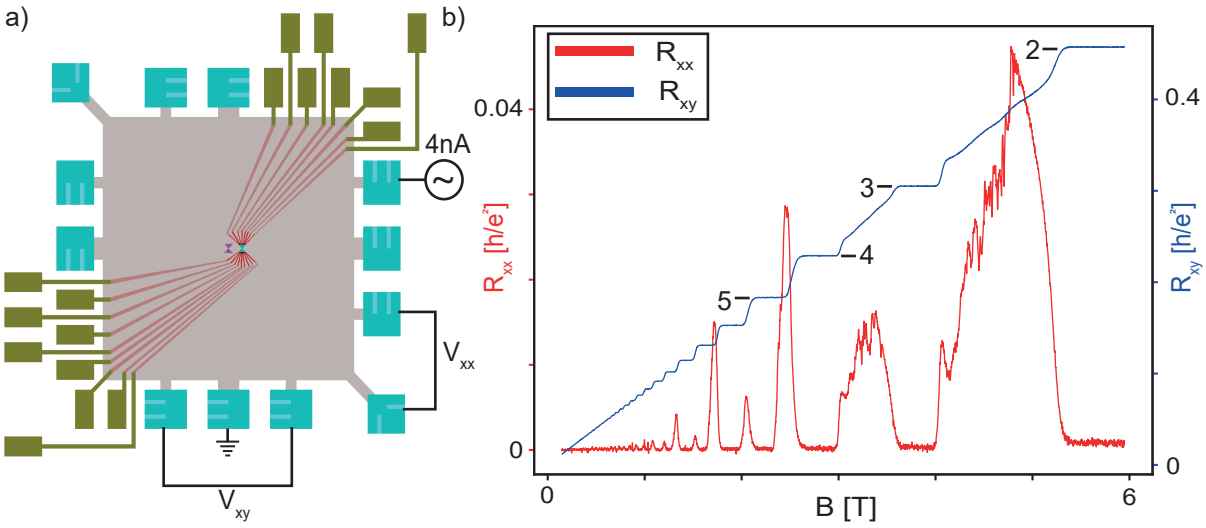

Figure 5.6: **Second Magnetic Field Sweep a)** Device overview with experimental setup used for the measurement **b)** Quantum Hall measurement with the Hall resistance shown in blue and the longitudinal measurement shown in red.

After this measurement we started trying out different ohmics, and found in the notebook of Christian Olsen, who has also done similar measurements on an almost identical mesa, that doing the measurement using only ohmics on one side of the QPC gave good results for him. It was on this basis that we tried out the setup seen in Figure 5.6a where we chose to have both the current and ground ohmics and the voltage probe ohmics on one side of the QPC. Using this setup we obtained the data seen in Figure 5.6b, where the steps in R_{xy} are much more defined and R_{xx} reaches zero resistance in between peaks. We however do not see any fractions and after discussions with the Manfra group who developed the wafer, we

concluded that it was likely that the 2DEG had been damaged during fabrication.

6 Algorithm measurements

In this section we describe the main result of the thesis, apart from the development of the pixel gate array, where we use an autonomous algorithm to tune the pixel qpc to show quantized conductance. This master project was performed in collaboration with Torbjørn Rasmussen who developed the algorithm, using CMA-ES [16], that could preform an optimisation of the voltages on the gates of the QPC devices that were fabricated, to find the best looking quantized conductance staircase. The algorithm was developed in collaboration with Assistant Professors Oswin Krause of DIKU and Evert van Nieuwenburg of the NBI. Measurements in this section were performed by both of us working together. Details of the algorithm developed are presented in Torbjørn Rasmussen's Master thesis [32], but I will describe briefly below how it works in principle. The algorithm works by assigning voltages to the gates that have to be optimised from a distribution that is changed according to the score of former runs. We start by assigning voltages to the gates we wish to optimise. Then we sweep another set of gates to produce a pinchoff curve. This pinchoff curve is then scored by a loss function based on its resemblance to a staircase such as expected from a quantised conductance measurement. Based on this score we can then change the distribution to favour voltages that showed good scores. This is then repeated until the pixels are assigned the voltage value that gives the best staircase, according to the loss function.

In this section we will look at two algorithm runs, one performed on the right QPC and one done on the middle QPC. Both algorithm runs are prepared similarly, as we first apply a voltage of -2 V to the outer gates to deplete the 2DEG underneath them, such that we are confident that the current path is constricted to be beneath the pixel gate array. The parameters that the algorithm has to optimize, are the pixel gates that are not being swept, so in the case of the right QPC, this would be the left and middle column of pixels and the middle right pixel (P1,P2,P4,P5,P6,P7,P8). These pixel gates would be set at a constant voltage and then the top and bottom right pixels (P3,P9) would be swept. This would result in a pinchoff curve which a loss function will score and according to this score, the distribution from which the voltages are chosen will be altered.

The two runs differ slightly as the algorithm run done on the middle QPC was done using a newer version of the algorithm which includes a feature we call dynamic window mode. In the dynamic window mode, we let the algorithm move the voltage "window", i.e. search a larger voltage range with the sweeping gates (however, each sweep is still constrained to a smaller and fixed voltage range than the total available voltage range).

It is important to point out that the algorithm's performance is limited by our ability to define a loss function that can differentiate between curves that look like staircases and curves that don't. Also, the absolute value of the loss score should not be given much importance, only that lower scores are better.

6.1 Right QPC

To manually look for QPC-like conductance staircases, we found it useful to sweep one pair of gate electrodes within the 3x3 array with one voltage, V_{QPC}, and plot the resulting conductance curve $g(V_{\mathrm{QPC}})$, while keeping all other gate voltages constant. When sweeping the pair P_3 and P_9, we refer this configuration as the "right QPC". (The "middle QPC" is formed by the pair P_2 and P_8.)

The right QPC is the QPC configuration we have had most success with when tuning by hand and when using the algorithm when it comes to reproducible quantized conductance staircases. To prepare it for an algorithm run, we apply -2 V to the outer gates and the algorithm is then able to tune the other seven pixels to a voltage such that we see several conductance steps. The exact setup can be seen in Figure 6.1a where we see the outer gates in black at -2 V, the seven orange pixels that are being controlled by the algorithm, and the two green pixels that are being swept in a fixed voltage range. These measurements were done using a voltage bias setup as shown in Figure 4.3a.

When setting up an algorithm run there are several different limits for the different gates that we can set. We set the voltage range in which the QPC gates are being swept and we set the voltage limits within which the other seven pixels can be set. In Figure 6.1d we see that the voltage sweep range is from -1.1 V to -1.5 V and in Figure 6.1b we see the voltage range of the seven pixels is 0.2 V to -1 V. When choosing the voltage range to sweep, we try

to pick it such that we don't have too many measurement points that have zero conductance as these do not add much information to the algorithm.

As we saw in Figure 5.3 we had to introduce a waiting time in between each measurement to get reproducible pinch off curves. For the algorithm run shown in Figure 6.1 and Figure 6.2, for every measurement we waited at 0 V for 20 s then we jumped to the start value of the gates and waited 10 s before measuring the pinch off curve.

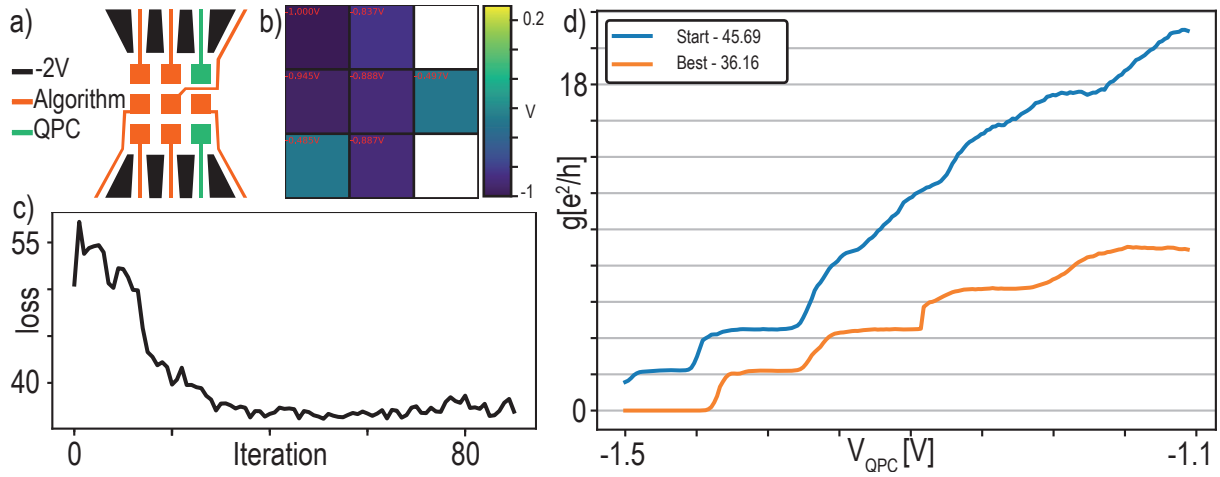

Figure 6.1: **Right QPC algorithm run** Overview of the algorithm run preformed on the right QPC. **a)** Illustration showing the setup of the algorithm run. The outer gates in black are set to -2 V. The seven orange pixels are being optimised and the two green pixels are being swept. **b)** Voltages of the seven optimised pixels that produced the best staircase shown in d. **c)** Best loss score from each iteration. **d)** First pinch off curve where all seven pixels are at 0V and the pinch off curve with the best score.

Figure 6.1 shows an overview of the algorithm run, where Figure 6.1a shows what is being optimised, Figure 6.1c shows how the best loss score from each iteration develops for following iterations, Figure 6.1d shows the first pinch off curve and the pinch off curve with the best loss score and Figure 6.1b shows the optimised voltages of the pixel gates from the best pinch off curve shown in Figure 6.1d.

Looking at Figure 6.1c we see that the loss score drops and reaches a saturation point at around iteration 40. After this point the average change of voltages within an iteration is less than 100 mV, and the small changes in score after this point can be attributed to the device being hysteretic even with the waiting. Seeing the loss score fall and reach a steady value shows that the algorithm is able to optimise the pixel gates to improve what we informally

call the "staircasiness" of the pinchoff curve. We can look into how the pinchoff curves evolve at different iterations in Figure 6.2.

In Figure 6.2a, b, c and d, we see pinchoff curves for the different iterations, 0, 10, 25 and 50. In each of the plots, three of the curves are highlighted in green, blue and red. The pixel voltages for these pinchoff curves are shown above where the frame has the color corresponding to the curve. The other pinchoff curves for these iterations are shown in grey. Just by looking by eye we can clearly see that the pinchoff curves transition from curves that show very little resemblance to a staircase, to curves that most definitely look like staircases. We also see that the voltage values of the seven pixels become more equal at the later iterations and that the curves are more bunched up or more alike, at later iterations. This indicates that the algorithm has found a minimum in the loss score landscape, and that these voltage values give reproducible results.

We also see that the conductance value ranges from $40\frac{e^2}{h}$ to $0\frac{e^2}{h}$ in iteration 0 and in iteration 50 it ranges from $10\frac{e^2}{h}$ to $0\frac{e^2}{h}$. One concern we have had, that would be important to examine in future work, is that the loss function does not reward the number of steps, so a perfect four step staircase is better than an okay ten step staircase. Another concern we had was the fixed voltage range in which the sweep was preformed. We saw that the pinchoff point was almost always close to the lowest voltage, pushed all the way to the right. And finally we were also concerned that we were optimising for noise. At high conductance values there was more noise than at low conductance values. Because the loss function rewards flat plateaus, staircases with noise will get a worse score than staircases without. These were some of the considerations we had while developing the algorithm and the loss function.

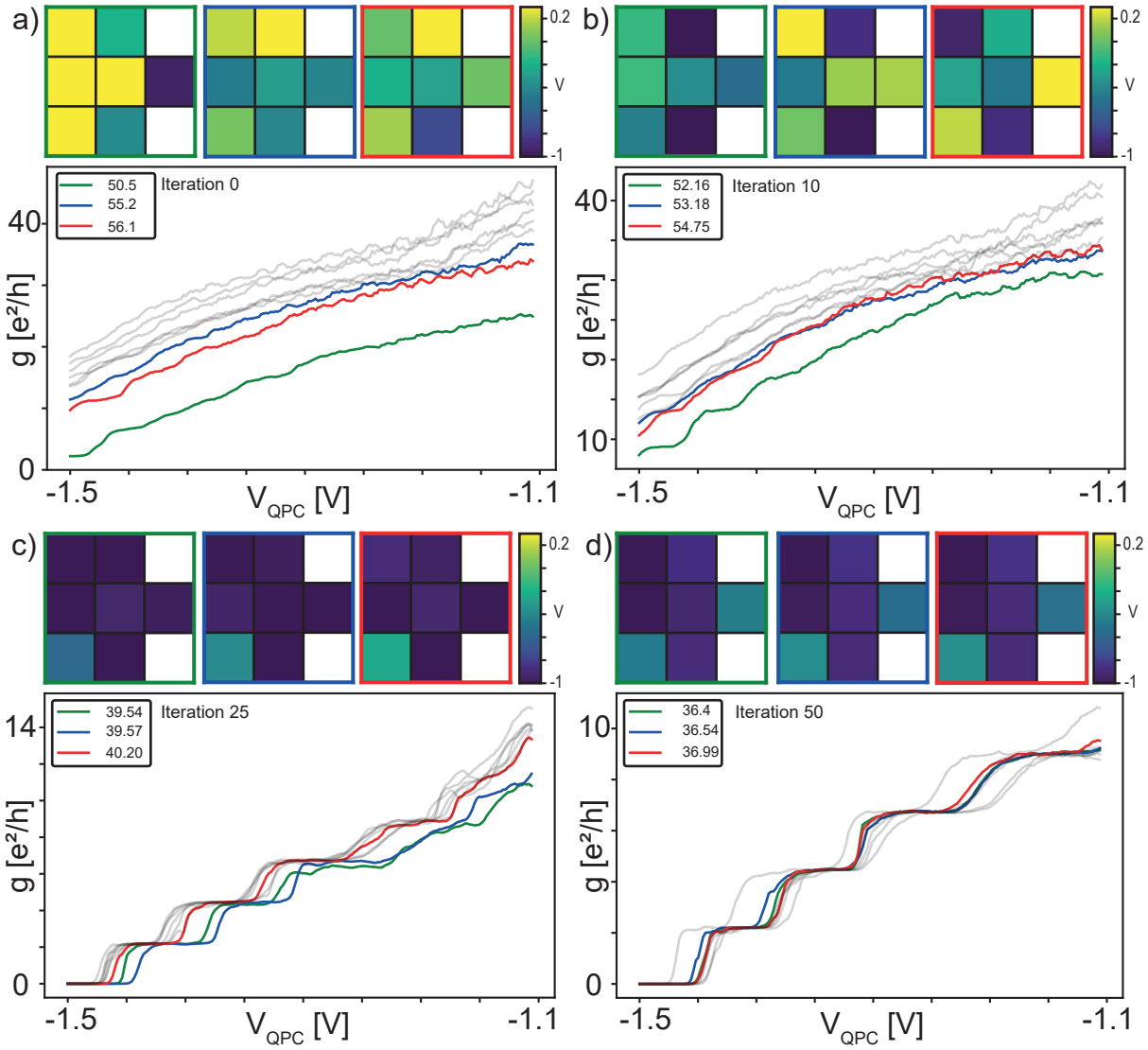

Figure 6.2: **Iteration Overview of Right QPC** Overview of the pinch off curves for four different iterations in the algorithm run. Three pinch off curves are highlighted for each iteration with red, green and blue. The voltage values of the seven pixels for each of these curves are shown above. **a)** Iteration 0. **b)** Iteration 10. **c)** Iteration 25. **d)** Iteration 50.

6.2 Middle QPC

By applying V_{QPC} to P_2 and P_8, we now turn towards the "middle QPC". As stated above the algorithm run done on the middle QPC differs from the algorithm run shown above done on the right QPC. Based on some of the considerations mentioned above the algorithm was altered such that it was able to choose the sweeping window in a larger range and it was also altered to make the loss function only evaluate the curves between $0.01\frac{e^2}{h}$ and $11\frac{e^2}{h}$. The sweeping window is 800 mV and the algorithm can choose to do this 800 mV sweep in the range 0 V to -2 V. If a measurement does not have data that spans the entire $0.01\frac{e^2}{h}$ to $11\frac{e^2}{h}$ range the curve is assigned a score of 1. This can be seen in Figure 6.3d where the starting pinch off curve has been assigned a score of 1.

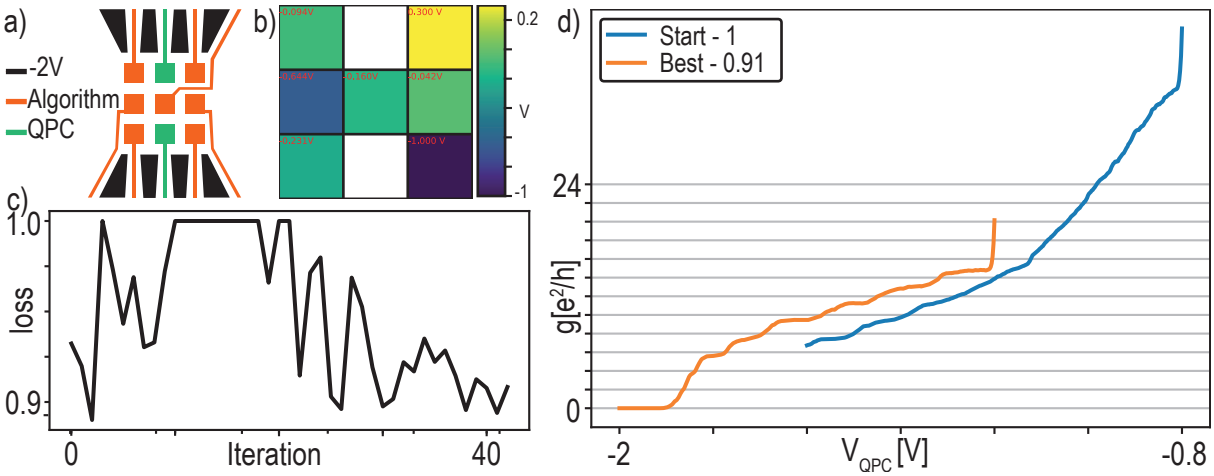

Figure 6.3: **Middle QPC algorithm run** Overview of the algorithm run preformed on the Middle QPC. **a)** Illustration showing the setup of the algorithm run. The outer gates in black are set to -2 V. The seven orange pixels are being optimised and the two green pixels are being swept. **b)** Voltages of the seven optimised pixels that produced the best staircase shown in d. **c)** Best loss score from each iteration. **d)** First pinch off curve where all seven pixels are at 0V and the pinch off curve with the best score.

In Figure 6.3 we see an overview of the algorithm run done on the middle pixel, similar to Figure 6.1 for the right QPC. For this algorithm run we see from Figure 6.3c that the loss score does not converge as clearly as it did for the right QPC. This also aligns with our experience of tuning the middle QPC by hand. It was more difficult to produce pinch off curves with clear conductance quantization on the middle QPC than the right QPC. We also see that we see a minima at the very beginning of the optimisation run, which turns out to

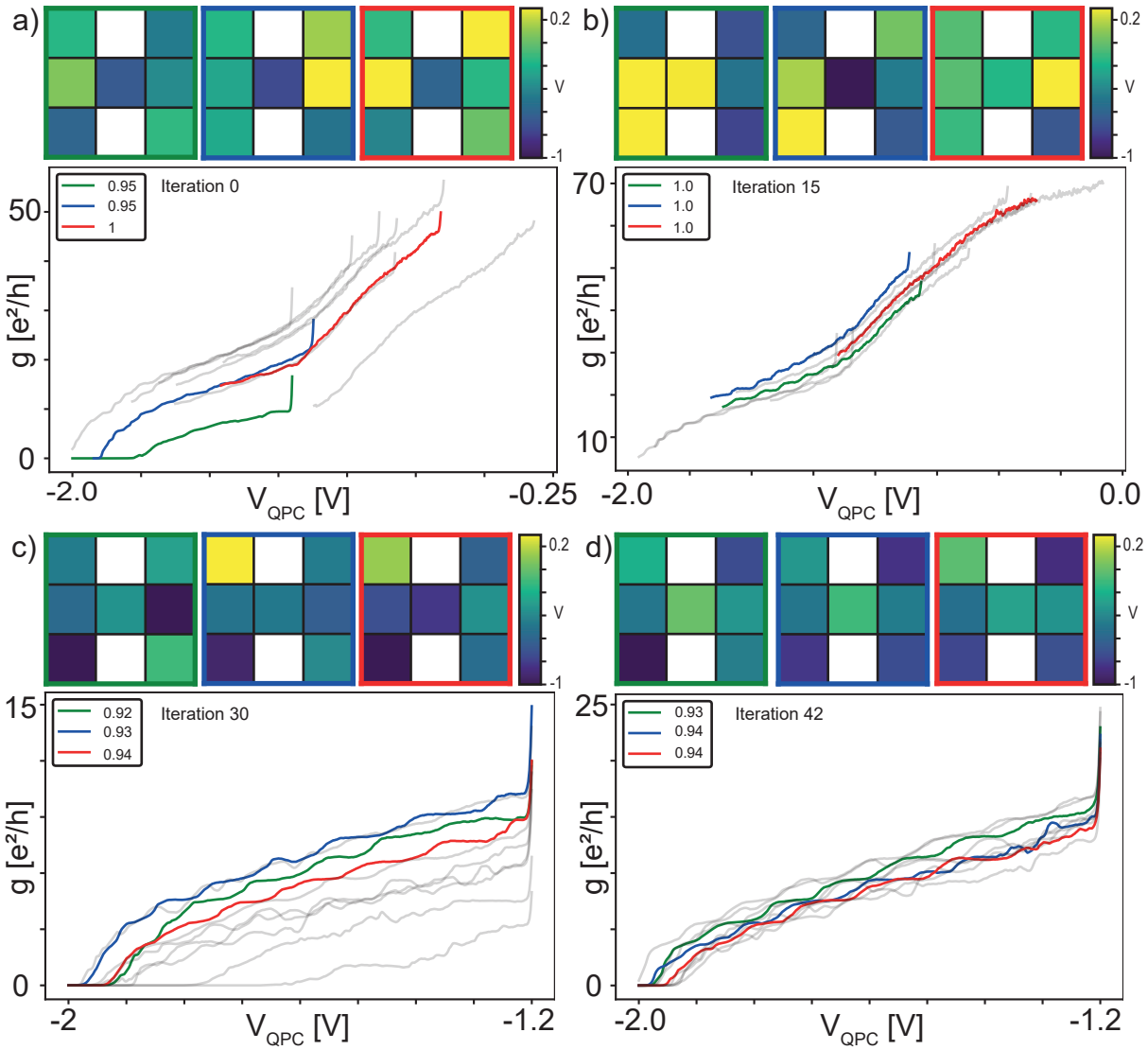

Figure 6.4: **Iteration Overview of Middle QPC** Overview of the pinch off curves for four different iterations in the optimisation run. Three pinch off curves are highlighted for each iteration with red, green and blue. The voltage values of the seven pixels for each of these curves are shown above. **a)** Iteration 0. **b)** Iteration 15. **c)** Iteration 30. **d)** Iteration 42.

be the best staircase of the run, shown in Figure 6.3d. This optimisation run also has half as many iterations as the optimisation run on right QPC, so it is possible that the iteration merely needed more time.

If we move to look at how the different pinch off curves look like at different iterations throughout the optimisation run in Figure 6.4, we see that the voltages of the seven pixels do seem to converge towards a set of voltages. We also see that the pinch off curves are much more alike at the later iterations than in the early iterations. This indicates that the algorithm is working as intended. The algorithm shows again that it prefers to pinch

off at the most negative voltage allowed. Even though the staircases we see in these pinch curves are not as pronounced as for the right QPC, we definitely still see some resemblance to staircases. Some of these features though are outside the evaluation window of $0.01\frac{e^2}{h}$ to $11\frac{e^2}{h}$, because of this these features are not influencing the optimisation. The fact that the algorithm makes use of the ability to move the evaluation and sweep window, and that this ability has an effect in reducing the score, is encouraging. This is because in future, tuning an extremely long series of conductance steps may become possible by tuning in a local voltage range, moving the sweep window, and tuning the next set of steps.

7 Summary and Outlook

In this thesis, I have shown that we were able to fabricate a device using nanofabrication lithography techniques in a different paradigm; that of pixelated gates that increase the spatial tunability of the resulting potential landscape, and that can be tuned using autonomous algorithms. Specifically, we showed that a new gate-voltage optimisation algorithm allows us to observe quantized conductance staircases. It was found that only certain configurations of gates gave convincing optimisation results when using specific procedures to account for gate hysteresis, which we attribute to non-idealities of the particular device. When deactivating the QPC gates, we were not able to measure fractional quantum Hall plateaus, which we attribute to fabrication-induced reduction of 2DEG mobility. We speculate that the quality of the 2DEG was compromised during an annealing step with rather high temperature.

Looking at what improvements could be done for future experiments (where the problems concerning ohmics, hysteresis and lack of fractional quantum Hall plateaus have been fixed), one may consider to replace our single-layer gates by a two-layer process. The first gate layer could be a screening gate with an array of holes, over which a second layer implements one individual gate above each hole. Such a design may alleviate potential problems associated with the pixel connections, which in our single-layer design are not screened. Extending the thought of a screening gate and the concept of pixel gates, one could also explore a much larger grid of pixels and demonstrate new types of experiments that could be performed with a device like this.

8 Appendix A

8.1 Fabrication Recipe

This fabrication recipe is based on the recipe found in Federico Fedele Ph.D thesis [13] and the ohmic recipe was found in the Master and Ph.D thesis of Christian Olsen and Douglas T. McClure [31, 28].

Markers Clean

- 3 Solvent Cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA
- Dry with N2 gun
- Ash 2 min in O2 atmosphere

Markers Spin

- Prebake 5 min at 185°C
- Spin A4 at 4000 rpm for 60 sec
- Bake 2 min at 185°C

Markers Exposure
The exposure file is prepared using the software Beamer, using these parameters:

- 100 keV Elionix
- 2 nanoamps
- 720 $\mu C/cm^2$
- 600 um WF
- 60000 dots per WF
- pitch is 1
- 0.36 us dwell time
- In the wecass schedule file use 1.2 dose coefficient. This may vary

Markers Develop

- 60s in MIBK:IPA ratio 1:3
- 15s in IPA
- Dry with N2 gun
- Ash 2 min

Metal Deposition and Lift-Off

- 6 nm Ti
- 100 nm Au
- 2 hours in 80°C NMP

Mesa Clean

- 3 Solvent Cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA
- Dry with N2 gun
- Ash 2 min in O2 atmosphere

Mesa Spin

- Prebake 5 min at 185°C
- Spin EL9 at 4000 rpm for 60 sec
- Bake 1 min at 185°C

Mesa Exposure
The exposure file is prepared using the software Beamer, using these parameters:

- 100 keV Elionix
- 40 nanoamps
- 295 $\mu C/cm^2$
- 600 um WF
- 20000 dots per WF
- pitch is 1

- 0.06637 us dwell time

Mesa Develop

- 90s in MIBK:IPA ratio 1:3
- 20s in IPA
- Dry with N2 gun
- Ash 2 min

Prepare Test Chip

We need a chip to check the etch rate of the solution. This can be done on a scrap piece of wafer that does not have a heterostructure.

- Clean with same 3 solvent cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA
  - Ash 2 min in O2 atmosphere
- Spin AZ1505 at 4000 rpm 60s
- Bake 115°C for 1 min
- Expose any pattern on the Heidelberg, that lets you measure the mesa height. We used nine 100x100 um squares.
- Develop with MF-123 for 30 sec
- Stop development in MQ for 15 sec

Prepare Etch solvent

The etch mixture consists of H2SO4:H2O2:H2O with a ratio of $1 : 8 : 240$. This mixture should have an etch rate of about 3nm/s. The mixture is stirred using a magnetic stirrer to keep the mixture uniform. While etching the chip is also lightly stirred in the mixture. First we etch the test chip. Then we strip the resist and measure how much has been etched using either a profilometer or a Sensofar. Then we adjust the etch time accordingly, while taking into account that the etch rate will decrease as time has passed.

Mesa Etch

- Etch the chip
- Rinse in MilliQ for 30 sec
- Strip resist with 3 solvent cleaning
- Measure the height of the Mesa to see that the 2DEG has been cleared

Ohmics Cleaning

- 3 Solvent Cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA
- Dry with N2 gun
- Ash 2 min in O2 atmosphere

Ohmics Spin

- Prebake 5 min at 185°C
- Spin A8 at 4000 rpm for 45 sec
- Bake 4 min at 185°C
- Spin A8 at 4000 rpm for 45 sec
- Bake 6 min at 185°C
- Spin A4 at 4000 rpm for 45 sec
- Bake 8 min at 185°C

Ohmics Exposure

- 100 keV Elionix
- 40 nanoamps
- 295 $\mu C/cm^2$
- 600 um WF
- 20000 dots per WF
- pitch is 1
- 1200 $\mu C/cm^2$
- 0.27 us dwell time

Ohmics Development

- 90s in MIBK:IPA ratio 1:3
- Rinse 15s in IPA 15 sec

- Ash 2 min

Ohmics Deposition and Lift-Off

Before we deposit the metal stack, we clean the deposition area in situ with argon plasma for 120 seconds.

We then deposit the metal:

- 5 nm Pt
- 200 nm Au
- 100 nm Ge
- 73 nm Pt
- 100 nm Au
- 50 nm Ge
- 55 nm Pt
- Lift off in 80°C NMP for 2 hours

Ohmics Anneal

The ohmics are then annealed in order to make a better contact to the 2DEG. We anneal the sample in a RTA, rapid thermal annealer, in Forming gas (N2/H2) atmosphere at 530°C (this is too high, don't use this ohmic recipe) for 100 seconds. This ohmic stack and anneal recipe is from Douglas McClure's Phd thesis. A similar recipe can be found in Christian Olsens Master thesis. This recipe uses an annealing temperature of 440°C for 60 seconds.

ALD - Oxide layer We deopsit 15 nm of Hafniumoxide

Clean the chip

- 3 solvent cleaning
- 2 min 1,3-Dioxolane
- 2 min Acetone
- 2 min IPA
- Ash 2 min
- Deposit 15 nm HfO2

QPC Cleaning

- 3 Solvent Cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA

- Dry with N2 gun
- Ash 2 min in O2 atmosphere

QPC Spin

- Prebake 5 min at 185°C
- Spin A2 at 4000 rpm for 60 sec
- Bake 3 min at 185°C

QPC Exposure
The exposure file is prepared using the software Beamer, using these parameters:

- 125 keV Elionix
- 1 nanoamps
- 1248 $\mu C/cm^2$
- 500 μm WF
- 200000 dots
- Pitch 1
- Remember to divide dose time with 4. Because of multipass.
- Set multipass to four passes
- 0.0195 μs dwell time, This has been divided by 4.
- In beamer we use Bias to shrink the design with 4 nm with the X-Y mode. This varies depending on the outcome of the Bias x Dose test
- In the wecass schedule file use 2.65 dose coefficient. This varies depending on the outcome of the Bias x Dose test

QPC Develop
For the QPC we use cold development. This gives us more leeway because it slows down the development process.

- 4 min in MilliQ:IPA ratio 3:7, 9 mL MilliQ, 21 mL IPA, cooled to -5°C
- Dry with N2 gun
- Ash 45 sec

QPC Metal Deposition and Lift-Off

- 5 nm Ti

- 18 nm Au
- 1 hour in 80°C NMP

Bond Pads Clean

- 3 Solvent Cleaning
  - 2 min 1,3-Dioxolane
  - 2 min Acetone
  - 2 min IPA
- Dry with N2 gun
- Ash 2 min in O2 atmosphere

Bond Pads Spin

- Prebake 5 min at 185°C
- Spin EL9 at 4000 rpm for 60 sec
- Bake 3 min at 185°C
- Spin A4 at 4000 rpm for 60 sec
- Bake 3 min at 185°C

Bond Pads Exposure
The exposure file is prepared using the software Beamer, using these parameters:

- 125 keV Elionix
- 40 nanoamps
- 1248 $\mu C/cm^2$
- 500 um WF
- 200000 dots
- Pitch 1
- 0.0195 us dwell time

Bond Pads Develop

- 60s in MIBK:IPA ratio 1:3
- 15s in IPA
- Dry with N2 gun

- Ash 2 min

Bond Pads Deposition and Lift-Off

- 10 nm Ti
- 250 nm Au
- 2 hours in 80°C NMP

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