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MSc. Thesis

Center for Quantum Devices

Investigating InAsSb Nanowires for Majorana Fermion Devices

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Abstract

In recent years Majorana fermions have been identified as a possible platform for performing fault-tolerant quantum information processing due to their non-abelian exchange statistics and topological protection against decoherence. In hybrid nanowire/superconductor systems Majorana fermions are proposed to emerge as quasiparticle excitations, Majorana zero modes. This thesis concerns measurements on Majorana zero mode devices on InAsSb/Al hybrid nanowires. One of the prerequisites for the emergence of Majorana zero modes in hybrid nanowire/superconductor systems is a large spin-splitting. Recent theory predicts InAsSb nanowires to exhibit significantly larger spin-splitting compared to InAs or InSb, in which transport signatures of Majorana zero modes have previously been reported. Here, we present transport measurements for two different types of $InAs_{1-x}Sb_x$ nanowires with molar fractions of $x = 0.35$ and $x = 0.8$. The study into the $InAs_{0.65}Sb_{0.35}$ nanowires is unique as they are in the wurtzite crystal structure, a crystal structure not previously reported for InAsSb. We find that the wurtzite crystal structure has a lower electron affinity than regular zinc-blende InAsSb nanowires, i.e. the wurtzite nanowires exhibit are more responsive to electrostatic gate potentials. The gateability may be crucial for the properties of future InAsSb devices. By using Coulomb and tunneling spectroscopy transport signatures associated with Majorana zero modes are detected in two different device geometries. This is the first report on Majorana zero modes in InAsSb nanowires.

Acknowledgments

I would like to thank my supervisors Peter Krogstrup and Jesper Nygård for their guidance and helpful discussions during my thesis studies. I would also like to thank Charles Marcus for inviting me to join the InAsSb Majorana device subgroup, which is the subject of my thesis, and numerous interesting discussions on the topic. Joachim Sestoft is arguably the person who have had the biggest impact this thesis as all experiments were planned and executed in close collaboration with him. As a friend and a collaborator I could not have hoped for a better person share ups, downs, and late night lab work with. The last person who can not be forgotten in the context of this thesis is our in-house magician Shivendra Upadhyay whose knowledge, patience and help has been crucial for all fabrication steps.

For general discussions of Majorana device physics Mingtang Deng and Daniel Sherman have always had an open door when a question popped up, which I am grateful for.

For a young scientist Thomas Kanne has an immense knowledge on nanowires and if there were ever a question regarding the material aspects, he has been my go-to guy day and night.

Finally the Qdev Bagel club consisting of Joachim Sestoft, Thomas Kanne, August Mikkelsen, Alexander Whiticar and Anders Kringhøj have besides physics discussions helped to get the mind of experiments every once in a while. This has been essential for my personal sanity during my thesis studies.

Finally I would like to thank my significant other, Anna, for her understading during these times where late night measurements at times have seemed more important

than being at home. Without your support I would not have made it this far.

Preface

During my thesis studies at the Center for Quantum Devices I have been a part several different projects. These include nanowire characterization using Transmission Electron Microscopy, growth dynamics of ternary nanowires and Al-shell growth on nanowires, transport measurements on SIS-devices, Majorana devices and Interferometer devices. However, for this thesis I have focused on the studies of Majorana zero modes in InAsSb/Al hybrid nanowires to try to present a concise and consistent thesis.

The thesis consist of five parts. An introduction which relates the work carried out to the historical and future perspectives of quantum information processing. A theory section explaining the basics of the theoretical work that the experimental findings of this thesis is founded on, as well an introduction to the materials and devices explored. The experimental methods used for fabrication and measurements is outlined before the results are presented and discussed. In the conclusion I will put the obtained results into context and briefly discuss the next steps in the field.

Contents

List of Abbreviations

ALD - Atomic Layer Deposition

EBL - Electron Beam Lithography

EDX - Energy Dispersive X-ray Spectroscopy

FET - Field Effect Transistor

HR-TEM - High Resolution Transmission Electron Microscope

IPA - Isopropanol

MBE - Molecular Beam Epitaxy

MF - Majorana Fermion

MIBK - methyl isobutyl ketone

MZM - Majorana Zero Mode

NDC - Negative Diffrential Conductance

NIS - Normal metal - Insulator - Superconductor

NISIN - Normal metal - Insulator - Superconductor - Insulator - Normal metal

NW - Nanowire

PEC - Proximity Error Correction

PMMA - poly methyl-methacrylate

Qubit - Quantum bit

SEM - Scanning Electron Microscope

SOI - Spin Orbit Interaction

TEM - Transmission Electron Microscope

UHV - Ultra High Vacuum

VLS - Vapor-Liquid-Solid

WZ - Wurtzite

ZB - Zinc-Blende

1 Introduction

Classical Computers

Semiconductor devices have been the cornerstone in the field of information technology since the development of the first Silicon field effect transistor (FET) at Bell Laboratories in the 1940s. Information technology using FETs uses binary language and is operated by applying an electrostatic potential across a current carrying junction which can be either opened (bit (1)) or closed (bit (0)) by the electrostatic potential. Since the demonstration of the first FET, optimization of the FET fabrication processes has in resulted in the miniaturization of the individual components (bits), that are connected in integrated circuits used for performing computational tasks. This has led to an exponential increase in computational power, commonly known as Moore's Law [1], as more and more bits are utilized. This exponential increase in computational power has been accompanied with a decrease in the size of computers which has changed from occupying whole buildings to a point where a very fast computer can easily fit into our pockets. Both of these effects are directly caused by our ability to miniaturize the individual components and place these in closer proximity to each other. However, we are presumably at the end of Moore's Law for two different reasons. First, the high number of components on a chip dissipates large amounts of energy which makes it increasingly more difficult to prevent overheating of the circuits. Second, and more fundamentally, the components are becoming so small that the classical physics that governs the FET are affected by the quantum physics that become more and more pronounced as the size of the individual components decrease. Quantum mechanics dictates the lowest size limit

for classically operated transistors as the individual components will be disrupted by e.g. quantum tunneling if this limit is surpassed. In effect this means that in the near future classical computers will once again have to increase in size for the computational power to increased.

Although computers and information technology have arguably been the invention that have had the largest impact on human civilization during the 20th century, there are still areas in which the performance can be fundamentally improved. Certain problems are next to impossible to solve for classical computers due to the intrinsic nature of the computation. If given an optimization problem a classical computer will iterate through all possible solutions before giving the optimal solution, though this process is sped up by implementation of specialized algorithms. Nonetheless the computational effort associated with such a problem scales exponentially with the number of input parameters which often makes approximations necessary for the computer to converge on a solution. Although a classical computer could in principle solve the optimization problem and yield an exact solution, the computational time required to solve a large problem makes it unfeasible. Similarly, integer factorization, the foundation for classical encryption, is notoriously hard to solve for a classical computer given a large enough number to factorize. The problem is not intrinsically impossible to solve, but the computational power required is simply not within reach.

Quantum Computers

In the 1980s a solution to the aforementioned limitations on computations was proposed by Richard Feynmann [2], amongst others [3, 4], when it was suggested that we

exploit quantum properties to make quantum mechanical bits (qubits). A computer operated using qubits is referred to as a quantum computer. This type of computer has several advantageous attributes compared to its classical counterpart. A qubit operates using a well-defined two level system e.g. the spin of an electron with spin up $|\uparrow\rangle = |0\rangle$ and spin down $|\downarrow\rangle = |1\rangle$ as the two levels. Due to the quantum phenomenon of superposition the qubit, when not measured, can be in any state that is a linear combination of these two states

$$\psi = c_1 |\uparrow\rangle + c_2 |\downarrow\rangle \tag{1}$$

where c_i are amplitudes with a total probability of being in one of the states equal to 1

$$P_i = |c_i|^2$$
$$P_{spin\ qubit} = |c_1|^2 + |c_2|^2 = 1.$$

This is in stark contrast to the classical bit which at any given point has to be in *either* the $|0\rangle$ or $|1\rangle$ state. A schematic representation of the possible states in the qubit is seen in Fig. 1. ϕ and θ can assume any value, so every point on the surface of this sphere (known as the Bloch sphere) is a superposition of the states $|0\rangle$ and $|1\rangle$ and can be described by Eq. 1. In a spin based quantum computer, quantum gates are used to manipulate and control the position of the qubit-state on the surface of the Bloch sphere. Only the states $|0\rangle$ and $|1\rangle$ can be detected in a measurement, but

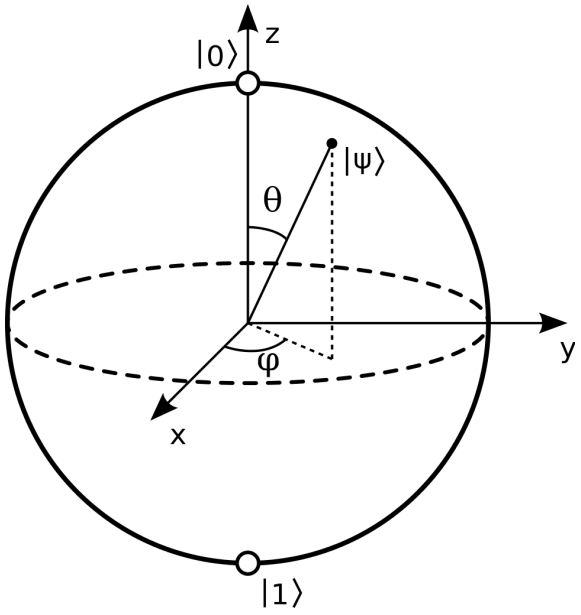


Figure 1: Schematic representation of the possible states in a qubit, known as the Bloch Sphere. Figure adapted from [5]

any superposition of the states on the surface of the sphere can be projected onto the z-axis and result in a measurement of $|0\rangle$ or $|1\rangle$.

A system of qubits additionally exploits another quantum phenomenon, namely quantum entanglement, by which the state of every qubit in the system can be determined by performing a measurement on a single qubit. For any given system with n two-level components (bits or qubits) there are 2^n different configurations. A key difference between the classical and the quantum computer is thus that the classical bit system is in one of the 2^n states at a given point while the qubit system is in all of the states simultaneously. This will allow the qubit system to perform the required computations on all configurations simultaneously, whereas the classical system has to iterate through each individual configuration.

David DiVincenzo's famous publication from 2000 [6] lists the requirements for build-

ing a universal quantum computer as:

- A scalable physical system with well characterized qubits.
- The ability to initialize the state of the qubits to a simple fiducial state, such as $|000...\rangle$.
- Long relevant decoherence times, much longer than the quantum gate operation time.
- A universal set of quantum gates.
- A qubit specific measurement capability.

To this day one of the largest successes of solid state quantum computers have been factorizing the integer 21 into its prime factors 3 and 7 [7]. This was done using Shor's algorithm, proposed by Peter Shor in 1994 [8], which factorizes integers into its constituent primes in polynomial time, which is an exponential speedup compared to classical algorithms, and would with an universal quantum computer be able to break any applied modern day encryption.

But still, despite the obvious advantages of quantum computers, we are still using the classical counterpart. The reason for this is the inherent difficulty in maintaining and controlling the state of quantum systems, as quantum mechanics is intrinsically probabilistic compared to the deterministic nature of classical physics. So far qubits have been proposed in a wide of variety systems e.g. ^{29}Si or ^{31}P in Ultrapure Si [9, 10], Nitrogen-vacancies in Diamond [11], Spin $\frac{1}{2}$ systems in 2-Dimensional Electron Gasses [12], etc. Despite all of these ingenious approaches, a universal quantum computer is still expected to be decades into the future, due to several

scientific and engineering obstacles. For one the thermal energy in the system has to be sufficiently low, to make it improbable for the system to be thermally excited from the low energy state to the higher one

$$k_b T \ll \Delta E_{0-1}$$

with k_b being Boltzmanns constant, T being absolute temperature, and ΔE_{0-1} being the level spacing between the two levels of the qubit. If this criterion is not met, a state can not be controllably maintained in the desired state, and the encoded information is lost. For qubit systems this typically requires the system to be cooled to temperatures $T \ll 1$ K, which will be discussed in sec. 3.2. Scaling of the system, which is crucial for having sufficient qubits to operate, is an extremely difficult task since the qubits are placed close to one another, to allow them to become entangled, but the electrical leads performing operations and readout on the each qubit has to be decoupled from the rest of the system to avoid undesired inter-qubit cross talk.

Both of the aforementioned requirements can be solved or circumvented, but as the individual components are not entirely adiabatic, noise is introduced in the system which has to be taken into account and filtered, which is a field of study in itself [13, 14]. There are several other difficulties on the path towards robust quantum computation, but the last one I want to touch upon, as it is relevant for this thesis, is quantum decoherence. Any condensed matter quantum system is at least loosely coupled to its surroundings, which gives a finite probability of altering the quantum state through interactions, referred to as quantum decoherence. Decoherence time describes the period a quantum state is maintained within a quantum system, and,

being a probabilistic system, the average time the system is coherent is known as the lifetime of the system. Lifetimes of different systems vary from nanoseconds to tens of seconds (in extreme cases). As stated in the DiVincenzo criteria, a usable qubit has to have a decoherence time that is much longer than the gate operation time, and though gates can be operated quite fast, a long decoherence time is still desirable.

In the last few years a new method to dramatically suppress quantum decoherence in qubits has emerged by the proposed use of condensed matter Majorana fermions as logic qubits in condensed matter systems. The topic of this thesis will be on the observation of Majorana zero mode transport signature in InAsSb/Al hybrid Nanowires, as Majorana zero modes are proposed to be Majorana Fermions. A short literature review on the most significant experimental results on Majorana zero modes will be given at the end of sec. 2.

2 Theory

2.1 Majorana Fermions and Majorana Zero Modes

In this section the basic concepts of Majorana Fermions and Majorana Zero Modes will be outlined as well as the requirements for realizing these exotic states in condensed matter systems.

Majorana Fermions (MFs) were proposed by Ettore Majorana in 1937 [15] as a solution to the Dirac equation [16] using only real numbers, compared to the conventional solution which has a real and an imaginary part. This solution suggests that charged spin 1/2 particles can in principle be their own antiparticle. This solution was seen as an oddity since the standard model prescribes that particles and their antiparticles, among other differences, possesses opposite charge. Majoranas formulation of the Dirac equation was consistent with the theories of general relativity and electromagnetism and because of this work, fermions that are their own antiparticles were dubbed Majorana fermions [17]. The result implies that the creation ($\gamma^\dagger$) and annihilation (γ) operators for MFs are identical, contrary to (standard) Dirac fermions

$$\gamma_{MF} = \gamma_{MF}^\dagger$$
$$\gamma_{Dirac} \neq \gamma_{Dirac}^\dagger.$$

When Ettore first published his results they were regarded as a curiosity of physics

and difficult to realize in nature, but to this day it is still debated whether neutrinos are Dirac fermions or MFs [18, 19].

For many decades following the acceptance of the possibility of MFs in particle physics, the concept was not further investigated as it was mostly seen as a theoretical construct. However, a report published by Kitaev in 2001 [20] postulated that exotic quasi-particle excitations in condensed matter systems could be analogous, and possess the properties, of MFs. In Kitaevs famous "Toy-model" pairs of MFs along a 1-Dimensional (1D) semiconductor system with superconducting p-wave pairing could leave a pair of bound MFs living at zero energy, one at each end of the 1D channel.

MFs have another interesting property, compared to Dirac fermions; they follow non-abelian exchange statistics. Dirac stated in his original theory, that due to the antisymmetric nature of the wavefunction of fermions, interchanging two particles adiabatically changes the sign of the wavefunction. Interchanging them again thus leads to a system identical to original one, independent on the nature of the exchange. Dirac fermions follow abelian statistics. On the contrary, the wavefunction of particles that follow non-abelian exchange statistics is dependent on the method the particles are interchanged, and simply interchanging two non-abelian particles twice does not necessarily leave the system in the original state. These exchange statistics are the foundation of MF based quantum information processing, a concept referred to as braiding. Proof of condensed matter MFs still has not been confirmed. The decisive proof is to verify the non-abelian exchange statistics either through braiding or a non-trivial fusion rules outcome [21]. The quantum gates in Majorana based quantum computing are the path-dependent braiding operations that require a min-

imum of 2 sets of MFs and a suitable network structure. A T-structure that can host MFs in each 'leg' is the simplest such structure [22].

Majorana Zero Modes

The following section is mainly based on [21], [23] and [24]. Majorana Zero Modes (MZMs), sometimes referred to as Majorana bound states, are quasi-particle excitations predicted to emerge in condensed matter systems, that may be MFs. At first proposals for the realization on MZMs in condensed systems concerned spinless p-wave superconductors. Most famously is the toy-model known as the Kitaev chain as depicted in Fig. 2. In this model each 'box' (index i) represents a fermion that is split in two constituents. In the top of the figure the two constituents of each fermion is paired together ($\gamma_{i,1} - \gamma_{i,2}$), whereas in the bottom the constituents are paired with a neighboring fermion constituent ($\gamma_{i+1,1} - \gamma_{i,2}$).

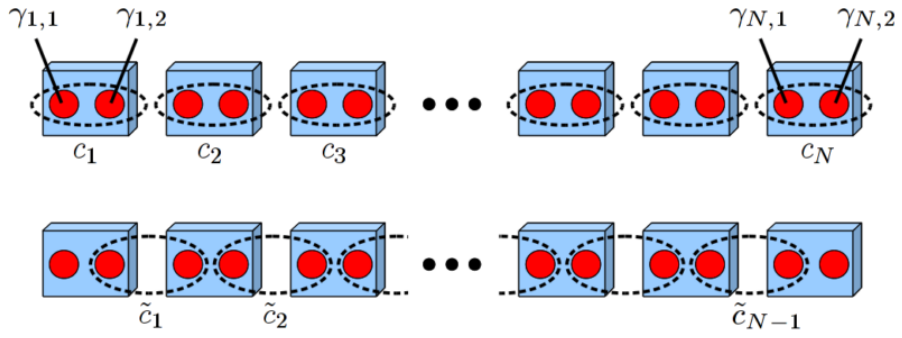


Figure 2: Schematic representation of Kitaev's toy-model. In the tp figure, each box represents a fermion that is split in two paired fermion constituents. In the bottom, the constituents (at i) are paired to a constituent from a neighboring fermion ($i = \pm 1$). The bottom scheme represents the p-wave pairing situation, which leaves a single pair consisting of $\gamma_{1,1} - \gamma_{N,2}$ at the very ends of the chain. Figure adapted from [21]

This model describes a tight-binding chain of superconducting p-wave pairing which

in turn is described by the Hamiltonian

$$\mathcal{H} = -\mu \sum_{i=1}^{N} n_i - \sum_{i=1}^{N-1} \left(t c_i^\dagger c_{i+1} + \Delta c_i c_{i+1} + h.c. \right) \tag{2}$$

with μ being chemical potential, t being hopping amplitude between neighboring sites, Δ the superconducting gap, n_i the number operator (defined as $n_i = c_i^\dagger c_i$)), and $h.c.$ the hermitian conjugate. c_i ($c_i^\dagger$) describes annihilation (creation) of an electron at site i. Majorana fermions can be described by the corresponding Majorana operators (γ) are obtained by splitting the fermionic operators into its real and imaginary components

$$c_i = \frac{1}{2}(\gamma_{i,1} + i\gamma_{i,2}) \tag{3}$$

$$c_i^\dagger = \frac{1}{2}(\gamma_{i,1} - i\gamma_{i,2}). \tag{4}$$

By isolating $\gamma_{i,1}$ or $\gamma_{i,2}$ in c_i or $c_i^\dagger$ and substituting it into the other confirms that our creation and annihilation operators are indeed identical.

$$c_i = \frac{1}{2}((2c_i^\dagger - i\gamma_{i,2}) + i\gamma_{i,2})$$

$$c_i = c_i^\dagger$$

Inserting the Majorana operators into Eq. 2 and evaluating the simplest case with $\mu = 0$ and $t = \Delta$ the Hamiltonian assumes the form

$$\mathcal{H} = -it\sum_{i=1}^{N-1}\gamma_{i,2}\gamma_{i+1,1} \tag{5}$$

which describes a pairing of Majoranas at neighboring sites $(i - i \pm 1)$. Just as above the fermionic operators of the neighboring Majorana operators can be described by

$$\tilde{c}_i = \frac{1}{2}(\gamma_{i+1,1} + i\gamma_{i,2}).$$

Inserting $\tilde{c}_i$ in our Hamiltonian yields

$$\mathcal{H} = 2t\sum_{i=1}^{N-1}\tilde{c}_i^\dagger\tilde{c}_i \tag{6}$$

which describes states living at an energy of $2t$. However, the end states in either end $(\gamma_{N,2} + \gamma_{1,1})$ of the chain that are not part of Eq. 5 can be expressed with the fermionic operator $\tilde{c}_{MF}$,

$$\tilde{c}_{MF} = \frac{1}{2}(\gamma_{N,2} + \gamma_{1,1})$$

The absence $\tilde{c}_{MF}$ from the Hamiltonian in Eq. 5 means that these states are residing at zero energy.

In a conventional superconductor the electrons are paired in Cooper-pairs yielding an even number of fermions, but Eq. 6 suggests the the ground state of such a superconductor is two-fold degenerate and can have either an even $(n_i = \tilde{c}_i^\dagger c_i = 0)$

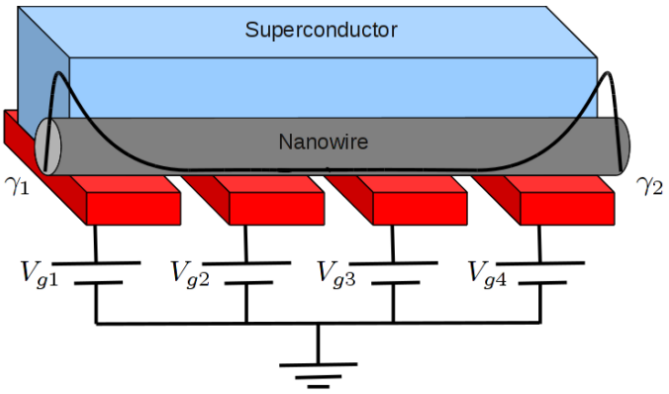


Figure 3: Simple representation of the requirements for realizing MZMs in condensed matter systems. A NW with strong spin-orbit interaction and proximity induced superconductivity. The gate electrodes are used to tune the chemical potential in the NW. The wavefunction is simplified, and often exhibits oscillations as described by [25]. Figure adapted from [21].

or odd ($n_i = \tilde{c}_i^\dagger c_i = 1$) number of fermions. If odd, the odd fermionic state will reside at both ends of the chain, with wave functions decaying exponentially with distance from the end, as depicted by the black curve in Fig. 3.

A fascinating and important property arising from the delocalized end-states is topological protection against decoherence. Decoherence occurs as a result of interaction with the local environment, and since the wave function is highly delocalized, decoherence can only occur as a result of a global perturbation in the ideal case of an infinite chain. In a realistic device with a length of about 1 μm the end states are still protected. How well the end-states are protected depends on several factor including length of the chain and the chemical potential in the NW [26].

The above arguments concerned the special case $\mu = 0$ and $t = \Delta$ but Kitaev showed that the results are valid, and thus that zero-energy states can be present in this system, as long as $|\mu| < 2t$.

The results explained above were rapidly recognized to play a crucial role for realizing MZMs in a condensed matter system, aside from the obvious experimental difficulty; the lack of a p-wave superconductor.

However, after a decade of theoretical research two independent theoretical reports from 2010 suggested MZMs could emerge in 1D semiconductors with large spin-orbit interaction and Landé g-factor, coupled to an s-wave superconductor, under the right conditions [27, 28]. This latter finding sparked the pursuit for MZMs in condensed matter systems, as the experimental and material requirements were already at hand.

To understand the emergence of MZMs in NWs let us consider a 1D semiconductor with considerable spin-orbit interaction (SOI), coupled to an s-wave superconductor, aligned in a parallel magnetic field. Given a good semiconductor/superconductor coupling the states in the semiconductor are aligning to the superconductor density of states making the semiconductor subject to an effective proximitized superconductivity [29]. The Hamiltonian for describing such a system is

$$\mathcal{H} = \sum_{\sigma=\uparrow,\downarrow} \int dx \left[\Psi_\sigma^\dagger(x) \left(\frac{\hbar^2 k_x^2}{2m^*} - \mu - \alpha_{SOI} k_x \sigma_y + \frac{g\mu_B B \sigma_z}{2} \right) \Psi_\sigma(x) + \Psi_\downarrow(x) \Delta \Psi_\uparrow(x) + h.c \right] \tag{7}$$

with $\sigma_{x,y}$ being Pauli spin matrices, $\hbar$ the reduced Planck constant, $\hbar k_x$ is momentum along the 1D semiconductor axis (x), m^* effective mass, $-\alpha_{SOI} k_x \sigma_y$ is SOI, and α_{SOI} being the spin-orbit strength, g is the Landé g-factor, μ_B is the Bohr magneton and B is the parallel magnetic field, giving rise to the Zeeman splitting, and $\Psi_\downarrow(x)\Delta\Psi_\uparrow$

is the term for superconducting pairing.

When applying the above criterion the SOI shifts the respective spin-bands by $\pm k_x$, when the 1D length is chosen to be along the x-direction. The energy associated with the SOI is $E_{SOI} = (m^* \alpha_{SOI})/(2\hbar^2)$. The spin-orbit splitting results in the two spin-bands only having a single degeneracy point at $k_x = 0$ as seen in Fig. 4**a**. Applying a magnetic field perpendicular to the spin-orbit field lifts (lowers) the upper (lower) sub band and a gap is opened between the two spin bands at the degeneracy point (Fig. 4**b**) meaning only a single spin is allowed in each band, though the spin is dependent on momentum as depicted by the arrows. The energy offset for the bands induced by the magnetic field is given by

$$E_{\pm} = \frac{\hbar^2 k_x^2}{2m^*} \pm \sqrt{\left(\frac{g\mu_B B}{2}\right)^2 + (\alpha_{SOI} k_x)^2}$$

with $\pm$ describing upper or lower band. Assuming $E_{SOI} \ll g\mu_B B$ the spins in the respective bands will be nearly polarized yielding the desired "spinless" bands as seen in Fig. 4**c**. If the bands are sufficiently split and μ is small, the upper band can be neglected, while the lower sub band is described by

$$\Psi_- = \frac{1}{\sqrt{1+\gamma^2}}(\Psi_\downarrow + i\gamma\Psi_\uparrow) \tag{8}$$

where $\gamma = \alpha_{SOI} k_x / g\mu_B B \ll 1$. Applying proximitized superconductivity introduces electron-hole symmetry in the system and a gap is opened around E = 0, as seen in Fig. 4**d**. Using $\Delta \ll g\mu_B B$, the superconducting term from Eq. 7 can be expressed

only in terms of the lower sub band from Eq. 8 to give an expression for the lower sub band

$$\mathcal{H}_- \sim \int dx \left[\Psi_-^\dagger(x) \left(\frac{\hbar^2 k_x^2}{2m^*} - \mu_{eff} \right) \Psi_-(x) + i\Delta_{eff} \Psi_-(x) \hbar k_x \Psi_-(x) + h.c \right] \tag{9}$$

with p-wave pairing amplitude $\Delta_{eff} = \alpha_{SOI}\Delta/(g\mu_B B)$ and effective chemical potential $\mu_{eff} = \mu + (g\mu_B B)/2$ [22].

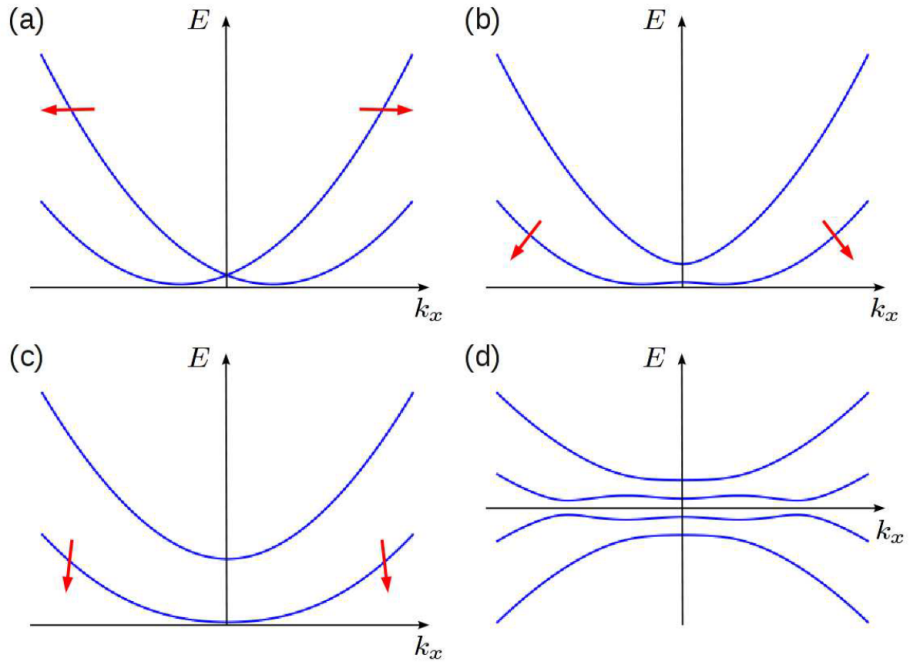


Figure 4: Schematic representation of the $E(k_x)$ bands in a 1-Dimensional semiconductor with SOI and finite paralell magnetic field. **a)** SOI split the originally degenerate spin bands leaving a single degeneracy point at E = 0. **b)** At small finite magnetic field, the degeneracy is lifted, and each band now holds only one momentum dependent spin. **c)** At larger finite field the spinless regime is reached as the spins in each band aligns either parallel or anti-parallel to the field. **d)** Superconductivity is introduced and a gap of Δ is opened. Figure adapted from [21].

To verify that the 1D semiconductor system indeed hosts MZMs the Hamiltonian is

compared to the 1D continuum version of the Kitaevs p-wave pairing chain

$$\mathcal{H}_{1D}^{pw} = \int dx \left[\Psi^{\dagger}(x) \left(\frac{\hbar^2 k_x^2}{2m^*} - \mu \right) \Psi(x) + \Psi(x) |\Delta| \hbar k_x \Psi(x) + h.c \right]. \tag{10}$$

These Hamiltonians have to satisfy that they can be continuously transformed into each other without closing the induced gap to confirm MZMs in the 1D system. As this condition is satisfied it follows that MZMs can emerge in the 1D hybrid semiconductor/superconductor system under suitable conditions.

With these theoretical considerations in mind a suitable material that meets the requirements can be evaluated. The material requirements are: a 1-Dimensional system, with strong spin orbit interaction, large Landé g-factor, and proximitized superconductivity. III/V semiconductor nanowires (NWs) with heavy elements (i.e. In, As, Sb) are a prime candidate they have intrinsically high g-factors [30], strong spin orbit interaction [31, 32], as well as proximitized superconducting gaps in epitaxially matched NW/superconductor interfaces have recently been reported [33, 34].

2.2 Semiconductor Nanowires

Semiconductor Nanowires are crystals of semiconducting materials which are spatially confined in 2 Dimensions with diameters of tens to hundreds of nanometers and a an unrestricted length typically on the order of μm. The small diameter of NWs makes it reasonable to approximate them as 1-dimensional systems. It should be noted that metallic [35], insulating [36], and superconducting [37] nanowires also exist, but they will not be discussed for the purpose of this thesis. Additionally,

semiconductor NWs can be pure group IV or an III/V or II/VI alloy. For the purpose of this thesis III/V NWs will be the focus.

Semiconductor NWs are heavily studied systems as their properties are suitable for a wide variety of applications e.g. biosensors [38, 39] or photovoltaics [40, 41]. The nanoscopic diameter of NWs makes quantum phenomena pronounced which leads to NWs having different properties with respect to their bulk counterpart e.g. bandgap for semiconductors. This makes NWs an ideal system to investigate quantum mechanical properties arising from spatial confinement.

Nanowire Growth

All III/V NWs presented in this thesis are grown by Peter Krogstrup in a Varian Gen II solid source Molecular Beam Epitaxy (MBE) system at the Niels Bohr Institute. The growth of the NWs is catalyzed by Au-particles which under the right conditions mediates non-equilibrium Vapor-Liquid-Solid (VLS) growth. The VLS-growth method was first reported by Wagner and Ellis in the 60's [42] where they describe single-crystalline structure growth mediated by a liquid alloy and carrier gasses. In MBE-VLS growth the growth wafer is carefully cleaned before being loaded into the Ultra High Vacuum (UHV) chamber of the MBE. Catalyst particles are either pre-patterned or deposited as a thin film in situ and subsequently annealed to form droplets. Alternate seed materials [43] and self-catalyzed growth [44, 45] are also used for VLS growth but will not be considered further. At a temperature of $\sim 400 - 500$ °C the Au-particles become liquid and form an alloy with the growth substrate. Growth is commenced by opening valves to the solid source effusion cells

containing pure elements used for growth. The UHV allows for a long mean free path for the atoms released from the effusion cells, effectively creating a directed flux. The impinging atoms of this flux supersaturate the alloyed Au-particle, form nucleation centers, and are subsequently precipitated as near-perfect crystals beneath the catalyst particle. By changing which elements are introduced to the growth chamber, as well as their relative flux, axial hetero structures and ternary alloys [46, 47] can be grown. These more complex systems allows for the possibility to engineer the properties and functionality of the NWs [48]. During VLS growth there are varying competing processes that contribute to the growth, and an exact mechanism is not yet fully understood though several groups are studying the dynamics and kinetics of NW growth [49, 50, 51]. As MBE-growth is an out of equilibrium process, trying to predict what happens during a growth comes down to determining which outcome minimizes the energy. InAs can grow in both the wurtzite (WZ) and zinc-blende (ZB) crystal structures, depending on growth parameters. Along the [0001]WZ/[111]ZB growth direction the only difference between these crystal structures are the stacking sequence (ABAB-stacking for WZ, ABCABC-stacking for ZB). During growth InAs can change from one crystal structure to the other depending on which is energetically favorable.

After the axial growth of NWs (the core) a shell can be grown radially to form core-shell hetero structures. The growth substrate holder in the MBE at NBI allows for rotation and since the effusion cells are stationary, two types of shell growth can occur; full-shell (with substrate holder rotation) or half-shell (no rotation). The radial hetero structures allows for further engineering of the NWs properties and both superconducting and semiconducting shells can be grown [52, 33].

This thesis concerns measurements on $InAs_{1-x}Sb_x$ NWs with a half-shell of Al (InAsSb/Al). Using this material is motivated by a recent theoretical report which suggests that InAsSb NWs is a promising candidate for hosting MZMs [53] as it exhibits a large spin-orbit splitting. Although the report states that optimal material is CuPt-stacked $InAs_{0.5}Sb_{0.5}$ NWs, the material overall shows great promise.

To grow InAsSb/Al NWs a [111]B InAs substrate is used. Au-catalyst is deposited through one of the methods mentioned above. The substrate is heated to liquify and alloy the catalyst particles. When a certain temperature is reached, NW-growth is commenced by opening the valves to the In and As effusion cells, respectively. After a period of InAs axial growth, the Sb effusion cell is opened and InAsSb is grown. The temperature of these cells, and the opening angle of the valve controls the relative fluxes of the elements. For the NWs the ratio between group III and V is 1:1. However, the incorporation rate of group V species is not linearly proportional to the flux ratio between the different elements i.e. growing a specific As/Sb ratio requires knowhow on VLS growth of this alloy. After the NWs have grown for the desired period of time the In valve is closed and the axial growth terminates when the catalyst particle is depleted of In. To grow the Al half-shell, the substrate rotation is halted and the substrate temperature is lowered to $\sim$ -30 °C. The valve to the heated Al effusion cell is opened and a half-shell is grown. The resulting NWs consist of a hexagonal semiconductor core, with Al covering two or three facets.

Device Geometries

For realizing MZMs in this hybrid NW/superconductor materials two different device geometries are explored, each exhibiting different transport signatures of MZMs as explained in the following.

2.2.1 Copenhagen Geometry

The Copenhagen Geometry is a normal metal - insulator - superconductor - insulator - normal metal (NISIN) device. In this geometry the proximitized semiconductor/superconductor segment of the NW is tunnel-coupled to the normal metal leads and can be thought of as a superconducting quantum dot with transport occurring through tunneling of cooper pairs. When a parallel magnetic field is applied the energy of the energetically unfavorable odd charge state is lowered through the Zeeman energy to allow transport via single particle tunneling. This is shown schematically in sec. 2.2.3. Experimentally this phenomenon is observed as the spacing between coulomb resonances being halved as a function of gate voltage in a parallel magnetic field, corresponding to a transition from $2e$ periodicity (cooper pairs) to $1e$ (single particles). This effect can be measured using Coulomb spectroscopy.

A scheme of the device geometry is seen in Fig. 5**a**. The semiconductor/superconductor island can be isolated from the normal metal leads by applying a negative bias on the cutter gates ($V_{cut1,2}$). The chemical potential of the island can be adjusted by the local plunger gate (V_g).

2.2.2 Delft Geometry

The Delft geometry is a normal metal - insulator - superconductor (NIS) device. Transport of charge carriers between NW and superconductor, at energies below the superconducting gap, Δ, can occur through the process of Andreev reflection. When an electron with energy $\mu + E_e < \Delta$ and momentum $+k$ impinges on the interface it has no states to enter. However, through simultaneous retroreflection of a hole with momentum $+k$ at energy $\mu - E_e$ a Cooper pair with charge $2e$ can be transferred to the superconductor at the fermi level. As the electrons in the NW are highly confined the Andreev reflections can become bound states known as Andreev Bound States(ABS). The ABS, which emerge from the superconducting coherence peaks, move towards the center of the gap when exposed to a parallel magnetic field. At a certain field magnitude they merge at $E = 0$, as evidence of topological superconductivity [54], and maintain this energy until the closing of the superconducting gap. Using tunnel spectroscopy ABS can be probed in the NIS geometry.

A scheme of the Delft geometry device is seen in Fig. 5**b**. As in the Copenhagen geometry V_{cut} is used to tune the coupling between the source contact (S) and the semiconductor/superconductor segment while V_g is used to change the chemical potential in this segment.

2.2.3 State of the art

Following the proposal by Lutchyn *et. al.* [28] mentioned above, the first experimental observations of MZMs transport signatures was published by Mourik *et. al.* in

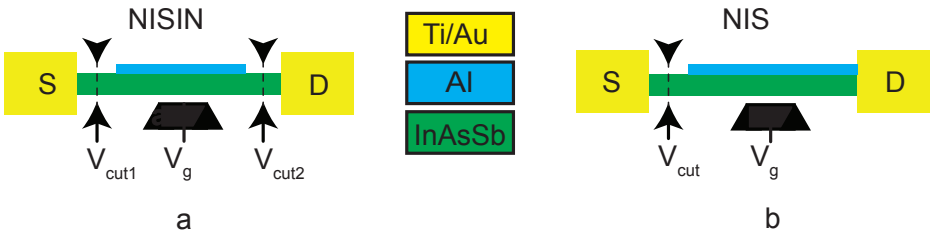


Figure 5: **a)** Schematic representation of the Copenhagen geometry (NISIN) device. The cutter gates, $V_{cut1,2}$, are used to tune the coupling to the source (S) and drain (D) contacts, while the plunger gate, V_g, is used to tune the chemical potential in the NW. **b)** Schematic representation of the Delft geometry (NIS) device. The cutter gate, V_{cut}, is used to tune the coupling to the source (S) contact while the plunger gate, V_g, is used to tune the chemical potential in the NW. Figure slightly redone from [55].

2012 [56]. Using InSb NWs with a NbTiN superconducting contact as a NIS device geometry, conductance through a zero-energy state was reported at a parallel magnetic field of 100 mT and was stable over large variations of fields and gate voltages. The observed MZM transport signatures from [56] is shown in Fig. 6 where the emergence of a zero-bias conductance peak as function of magnetic field is apparent. In this report the superconductor is evaporated onto the NW which yields a 'soft' superconducting gap, i.e. sub gap conductance is non-zero. Nonetheless, transport signatures of MZMs emerge which backs Kitaevs postulate that more than one band can be present. The ABS that are evolved into the zero-bias conductance peak can not be seen in this plot.

In a 2016 publication by Albrecht *et. al.* [57] measurements on the NISIN device geometry on epitaxial InAs/Al NWs were reported. The transport signatures of MZMs in the geometry, along with a schematic representation of the $2e$ to $1e$ transition explained above, is shown in Fig. 7. In 7**a** intensity plots of differential conductance as function of source-drain bias and gate voltage is seen at different

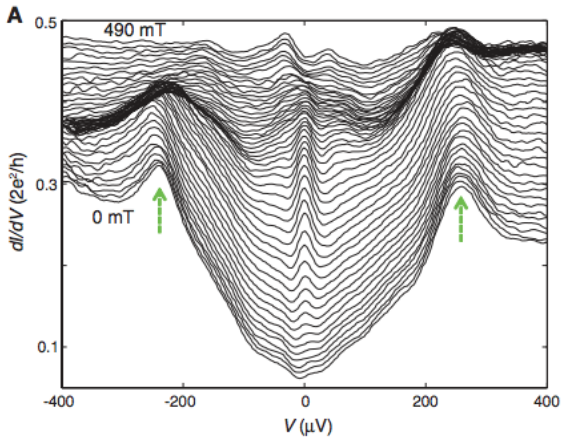


Figure 6: Waterfall plot showing a zero-bias conductance peak emerging as function of magnetic field from 0 - 490 mT in an Au-InSb/NbTiN NIS device. At the higher fields the zero-bias peak disappear as well as the peaks associated with proximitized superconductivity (marked by the arrows) Traces are offset for clarity. This was the first reported transport signature of MZMs in hybrid NW systems. Figure adapted from [56].

parallel magnetic fields, $B_{\|}$. The two zero-bias conductance resonances at $B_{\|} = 0$ mT evolves into four zero-bias conductance resonances at $B_{\|} = 220$ mT. Fig. **7b** explains this schematically. At $B_{\|} = 0$ the device is in the superconducting state and the degeneracy points between subsequent even occupation numbers (N_G=0,2,4..., black parabolas) has a lower energy than the odd occupancy (blue parabolas). The Zeeman energy lowers the energy of the odd charge state as the magnetic field is applied. At $B_{\|} = 80$ mT (green parabola) transport occur through the odd charge states as the energy is lowered sufficiently to make this more favorable than the even-even degenracy point. At $B_{\|} = 220$ mT the odd charge states is lowered to the same energy as the even charge states and the periodicity of the zero-bias conductance peaks is doubled as seen by the conductance peaks at the bottom of Fig. **7b**. In this publication the exponential length-dependent protection of the zero-bias conductance peaks was also demonstrated by measuring NISIN devices with different

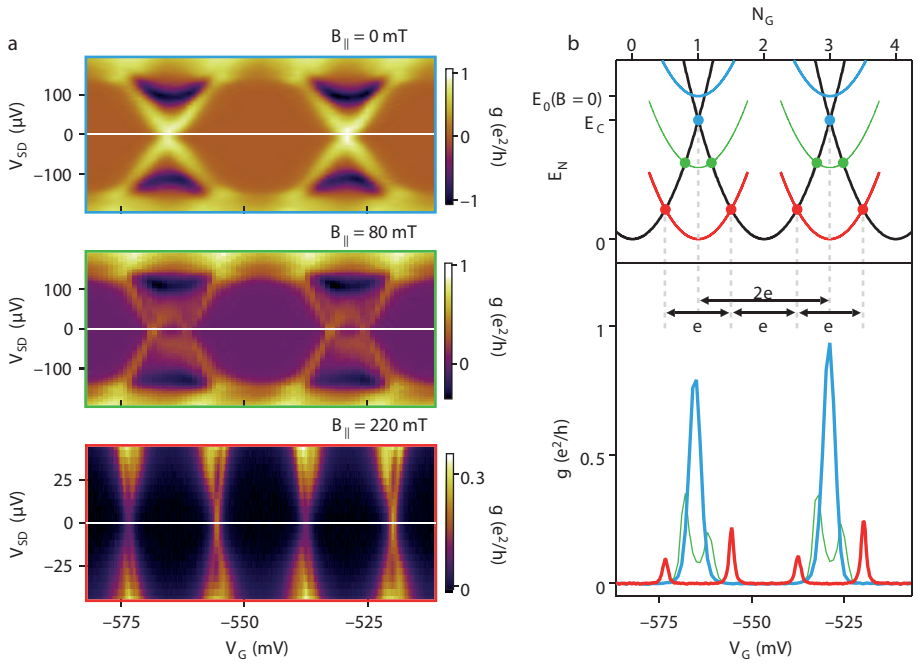


Figure 7: Intensity plot of differential conductance as function of source-drain bias and plunger gate voltage in an Au-InAs/Al-Au NISIN device. See text for details. Figure adapted from [57].

lengths of the proximitized semiconductor/superconductor segment.

3 Experimental Methods

3.1 Device Fabrication

In this section the general procedures for device fabrication are described. Irregardless of device geometry three different approaches to fabrication of electrostatic gates was explored to obtain the best response in the devices:

- Side gated devices with electrostatic gates located in the imminent vicinity of the NW acting with the vacuum as dielectric
- Top gated devices with electrostatic gates placed on top of the NWs using Al_2O_3 as dielectric
- Bottom gated devices with electrostatic gates predefined on the chip before NW deposition using Atomic Layer Deposited HfO_2 as dielectric.

3.1.1 Electron Beam Lithography Procedures

In the following the common procedures for nano-fabrication using Electron Beam Lithography (EBL) is described, while the deviations caused by the different gating schemes presented above will be commented afterwards. In order to do the transport measurements on the NW devices described in Sec. 2.2.2,2.2.1 electrical leads and electrostatic gates have to be deposited. All devices were fabricated on Si chips[1] with either 100 nm or 200 nm of SiO_2 as insulating layer.

[1]The general design of the device-chips (i.e. bonding-pads, leads, and registration marks) used for this thesis was fabricated by Jeremy Yodh or Saulius Vaitiekenas

NW deposition

There are different approaches to how NWs can be transferred from the growth substrate to the device chip. For this thesis two different methods were used.

- *Dry deposition*: Dry deposition is used to transfer a large amount of NWs to the device chip without any specificity in placement of the NWs. A sharp triangular shape is cut from a cleanroom wipe and held between tweezers and is very gently brought in contact with the growth substrate. Subsequently the cleanroom wipe is, again gently, brought into contact with the area of the Si/SiO_2 chip that is to be used for device fabrication. Ideally, thousands of NWs are placed randomly in the desired area. The process has to be gentle to affect the growth substrate and NW crystals as little as possible. This method is only recommended for non-positioned NW growths.
- *Micromanipulator deposition*: Using a micromanipulator and a needle with a tip radius of 100 nm, individal NWs can be identified and picked up from the growth substrate using an optical microscope and subsequently placed on the device chip. This method is used to transfer individual wires and allows for precise NW placement and on the device chip. This method is the optimal approach to transfer wires from a positioned array or if a specific placement or orientation on the device chip is required.

Design

After NW deposition the device chip was imaged using either an optical microscope or a Scanning Electron Microscope (SEM) so that the position of the NWs could be

imported to the correct location in the design file containing the 'blank' layout of the chip. All designs in this thesis was drawn in DesignCad23 using the device chip design file as template for further designs. After having drawn the desired design the Designcad file is exported to Beamer which was used to perform Proximity Error Correction (PEC) to avoid overexposure during lithography, and export a file to be read by the electron beam lithography system. Finally, registration, exposure schedule and beam dose was performed in the exposure program, Wecas.

Resist spinning

All fabrication steps for the devices in this thesis require lithography for one purpose or the other. Prior to lithography resist is spun on the chip. Several spinning techniques were explored to obtain as good a resist layer as possible, i.e. uniform and without residual resist under the chip. The resist used for all devices was a 4% poly methyl-methacrylate (PMMA) with an average molecular weight of 950 KDa. The optimized recipe used for fabrication was as follows:

- Load chip in spinner, blow with N_2.
- Initiate program with 5s at 500 rpm followed by 45s 4000rpm.
- During acceleration from 500 rpm to 4000 rpm deposit 12 μl resist.
- Hard bake at 185° on hotplate for 120 s.

This yields a $\sim$ 200 nm layer of PMMA uniformly distributed over the $\sim$ 5 mm$\times$5 mm chips utilized for all devices. Depending on device and lithography step either one or two layers of PMMA is spun.

After resist-spinning the chip is loaded into the 100 kV Elionix ELS-7000 EBL system and after beam conditioning and registration the design is exposed. For all exposures the following settings were used: beam-current = 500 pA, writefield size = 600 μm^2, 240.000 dots pr writefield, dot dwell time 0.14 μs corresponding to a dose of 1120 C/cm^2. Using these settings a feature resolution of $\sim$ 10 nm can be achieved.

Aluminum Etching

As mentioned in Sec. 2.2 a full- or half-shell can be grown on the NWs after semiconductor growth, and will be grown on the entire length of the NWs. However, as touched upon in Sec. 2.1 only a segment of the NWs is supposed to have an Al-shell. To remove Al, resist defined etch windows are designed and exposed as above. The exposed resist is developed by stirring the chip in an 1:3 methyl isobutyl ketone(MIBK)/Isopropanol (IPA) for 60 s, and subsequently in pure IPA for 30 s. A beaker of Transene Al etchant type D is heated to 50°C and the chip is swirled rigorously in that beaker for 10 s and immediately after transferred successively in 5 beakers of MiliQ water for 10 s, 30 s, 40 s, 50 s, and 60 s, respectively, to neutralize the acid. After rinsing in IPA and blow drying with N_2 the chip is ashed for 60 s in a plasma asher to remove residual carbon. The plasma ashing also attacks the resist and 60 s of plasma ashing corresponds to removing 10 nm of resist.

Metal Deposition

After Al-etching, a beaker of acetone at room temperature is used to remove the remaining resist before spinning two new layers of PMMA. The desired design for the contacts and/or gates is drawn, exposed, developed and ashed as above. Subsequently, the chip is loaded into an 10 kV AJA metal evaporation system and RF milled for 260 s at 50 W to remove semiconductor-oxides. Depending on the gate-type of the device, one of two metal evaporation schemes were followed.

- Side gates and bottom gates: Evaporation of 5 nm Ti, used as a sticking layer, followed by evaporation of 120-150 nm Au. Gates and contacts are deposited in the same lithography step.
- Top gates: At first 5 layers of 3 nm Al is deposited, while exposing the chip to ambient air for 300 s in between each evaporation to oxidize the Al yielding an insulating layer of $\sim$ 15-20 nm Al_2O_3. Subsequently Ti/Au is evaporated as above. An additional step of lithography is required to expose the contacts. Contacts are deposited as side/bottom gates[2].

After metal deposition lift-off of the remaining metal covered resist is performed in acetone at room temperature for $>$ 30 min followed by an IPA rinse and 60 s plasma ashing to remove resist residues. The procedures of EBL explained above are schematically represented in Fig. 8 from the resist in spun to the remaining resist and metal is lifted off. The end result is that only the EBL exposed area is covered by metal or used as Al-etch windows after the chemical development.

[2]Chips with prefabricated bottom gates were fabricated by Joachim Sestoft. The bottom gate arrays were fabricated by the described method and subsequently covered by $\sim$20 nm of HfO_2 by Atomic Layer Deposition (ALD).

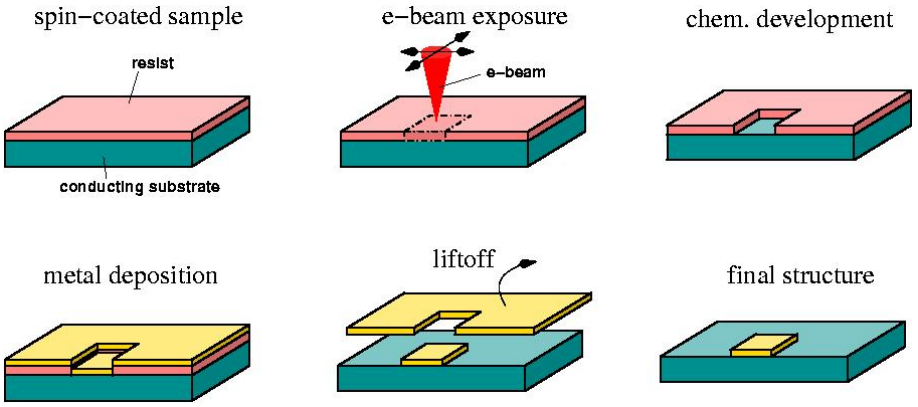


Figure 8: Schematic showing the individual steps in EBL procedures. Resist is spun, exposed, and developed to define areas on the substrate for metal deposition. After metal evaporation the entire substrate (and resist) is covered with metal and the metal covered resist is removed leaving metal only in the exposed regions. Image adapted from [58].

Immediately before loading a chip into the dilution refrigerator for measurements, the chip is glued to a Qdev daughter board with Ag-paint and the pinouts of the daughter board are bonded to the bonding pads on the chip by 50 μm Al-tread. The chip is loaded into a puck, which in turn is loaded into the dilution refrigerator.

3.2 Measurements in a ^{3}He/^{4}He Dilution Refrigerator

In this section the working principles of a dilution refrigerator will be outlined, as well as the measurement technique used in this thesis. For a more detailed explanation of the physics behind the dilution refrigerator see e.g. the textbook by Pobell [59]. All measurements in this thesis are carried out in a cryo-free ^{3}He/^{4}He Triton Dilution Refrigerator, henceforth simply referred to as *fridge*, with a mixing chamber base temperature of T_{mc} ∼30 mK measured by the ruthenium-oxide secondary thermometer which is very precise at mK temperatures. Performing the experiments

at mK temperatures is crucial as the thermal energy, k_bT, at higher temperatures will result in thermal broadening of the signal which may wash out the desired features in the signal, or simply obscure the physics of interest as described in Sec. 1. The fridge is dependent on the properties of mixing ^{3}He and ^{4}He at low temperatures. Both isotopes are liquid at mK temperatures. Due to the different number of neutrons in the core ^{3}He carries $\frac{1}{2}$-spin while ^{4}He has 0-spin. ^{3}He thus follows fermi-statistics while ^{4}He follow boson-statistics. The sub-kelvin cooling power is caused by the fact that ^{3}He exhibits a finite solubility in ^{4}He even in the $T \Rightarrow 0$ K limit.

When the puck is loaded it is brought into thermal contact with the mixing chamber, which is the coldest part of the fridge. In the mixing chamber the liquid isotopes of He will undergo a phase separation, at the λ-point at 2.17 K (at 1 atmosphere), into an almost pure ^{3}He-phase and a ^{4}He-rich phase (dilute phase). The dilute phase retains a maximum ^{3}He-solute concentration of $\sim 6.6\%$ in the $T \Rightarrow 0$ K limit. This is a quantum phenomena governed by the zero-point energy of the atoms, their weight, and the average interatomic distance in each of the two phases. The dilute phase of the mixing chamber has a flow passage to a still on which a pump is operating. As the ^{3}He/^{4}He mixture is being pumped on in the still, the ^{3}He evaporates first and thus create an osmotic gradient of ^{3}He from the dilute phase in mixing chamber to the still, which in turn causes ^{3}He to go from the pure ^{3}He-phase to the ^{4}He-rich phase. Due to the fermi statistics of ^{3}He, moving from one liquid phase to the other requires energy due to the enthalpy of mixing, and this energy is taken from the thermally coupled puck, providing cooling power. The evaporated ^{3}He from the still is after condensation fed back into the mixing chamber so the process can

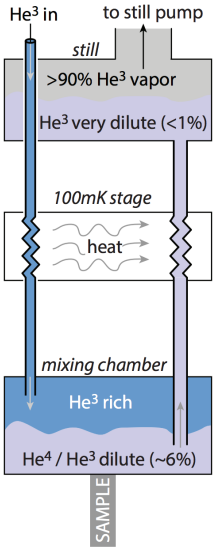


Figure 9: Schematic of the ^{3}He/^{4}He mixing chamber/still cooling loop used to cool and maintain the sample at mK temperatures. ^{3}He moves from the ^{3}He-rich phase to the dilute phase when the still pump is operating and cools the sample. Figure adapted from [60].

continue "indefinitely". Furthermore, the input and output of the mixing chamber is thermally coupled so that the dilute leaving the mixing chamber helps to cool the ^{3}He entering the mixing chamber. A schematic of the sub-kelvin cooling loop can be seen in Fig. 9

It should be noted however that it is the electron temperature (T_e), not the temperature measured by the ruthenium oxide, that determines the effective temperature of the measurements. The cables leading the electrical signal into the fridge are thermally coupled to the mixing chamber to achieve as low an electron temperature as possible.

The electrical lines going into the fridge can be connected to the outside world via a breakout box which gives access to both gates and contacts. For the source-drain bias a DC-signal is merged with an AC-signal. The AC-signal was supplied by phase

sensitive SR830 Lock-in Amplifier which is also used for collecting data. The AC-signal was used to probe the differential conductance ($g = \frac{dI}{dV}$) of the devices and had an amplitude of $10 - 20$ μeV. This amplitude should be higher than the thermal energy in the system i.e. T_e. The DC-signal was provided by a Digital Analogue Converter (DECADAC) and was used to change the source-drain over the desired range, typically -0.5 mV to 0.5 mV. The DECADAC has a range of -10 V to 10 V and was also used to apply a potential to the local gates.

Additionally, the fridge is equipped with a superconducting vectoring magnet with $B_{max(z)} = 6$ T, $B_{max(x,z)} = 1$ T. The device chip lies in the z-y plane and the x-direction of the vectoring magnet is not used in the measurements.

4 Results and Discussion

Many devices were fabricated and measured and a full overview is seen in appendix A. However, for the results section the focus will be on the devices and NWs which yielded the most prominent results.

4.1 Qdev 253

The Qdev253 batch of NWs is a very interesting growth from a materials and experimental point of view. The NWs are grown using thinfilm deposited annealed Au-catalysts on an InAs [111]B substrate. During the initial growth the wires grow as pure InAs in the WZ crystal structure. After a period of growth the NWs were forced to kink (i.e. the Au-droplet moves to one of the facets of the NW and mediates horizontal growth) by a 20 s Ga-pulse from the Ga effusion cell. A 45°-tilt Scanning Electron Microscopy (SEM) image of a kinked Qdev253 NW on the growth substrate is seen in Fig. 10. Worth noting is the slight upwards bending of the wire, as well as the continuous Al-phase on the top facet after the kink. Both will be discussed later.

After the NWs are kinked and grow in the $\{1\bar{1}00\}$WZ direction, the {0001}WZ/ {111}ZB symmetry is broken, and the wire is 'locked' in the crystal structure it had at the kink. After a period of InAs growth following the Ga-pulse, Sb is gradually introduced into the system and the NWs grow as InAsSb. Examining these NWs by Transmission Electron Microscopy (TEM) reveal that the InAsSb part after the kink is predominantly in the WZ crystal structure. Though bulk InAs condenses in the ZB crystal structure, it often form WZ when grown as NWs depending on

Figure 10: False-colored 45°-tilt SEM image of a Qdev253 WZ NW on the growth substrate. The Sb concentration in the NW gradually increases until it reaches its final concentration of $InAs_{0.65}Sb_{0.35}$ as illustrated by the green to red transition. Scale bar is 500 nm. Image credit Thomas Kanne.

the growth conditions [61, 62] as mentioned in Sec. 2.2. Introducing Sb into the system makes the WZ crystal structure energetically unfavorable and reports on InAsSb NWs reveal that these are in the ZB crystal structure except at very low Sb concentrations [63].

In the Qdev253 growth, however, several micrometers of WZ InAsSb growth occur, which is the first report on continuous growth of this material. The physical properties of materials, e.g. band gap [64], are dependent on their crystal structure. This growth thus allows for an interesting study on WZ InAsSb NWs, as this is a unique material. After growth of the InAsSb segment, the temperature is lowered to accommodate Al growth.

The majority of the NWs are kinked and the InAsSb segment is in the WZ crystal structure along $\{1\bar{1}00\}$, except for some that re-kink after the Ga-pulse to grow in the ZB structure as this should be energetically favorable. The molar fraction is determined to be $x \approx 0.35$ by Energy Dispersive X-ray Spectroscopy (EDX) in a

Phillips CM20 TEM, using pre-determined Cliff-Lorimer factors for InAs and InSb in the same TEM (not shown here).

The kinked NWs have different morphologies depending on crystal structure. The $\{1\bar{1}00\}$ WZ grows with a cubic morphology, whereas the re-kinked ZB NWs return to a hexagonal morphology. The Al is grown in the crystal orientation which minimizes the energy. For the WZ NWs the energetically optimized Al-match appears to be when the Al grows in a [111] out of plane orientation (perpendicular to the kinked NW growth direction), which results in an well-matched epitaxial growth along the NW growth direction, as seen in the High Resolution(HR)-TEM image in Fig. 11. This epitaxial NW/Al interface is seen all along the InAsSb WZ NWs.

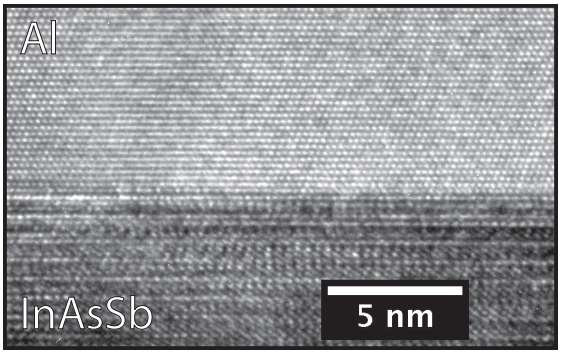


Figure 11: HR-TEM image of the epitaxial interface between InAsSb/Al in the Qdev253 NWs. The Al grows as a single continuous phase, with a few grain boundaries, for a few μm along the NW growth direction. Image credit Thomas Kanne.

As mentioned above it is assumed that the quality of the epitaxial semiconductor/superconductor interface play an important role in realizing MZMs in NW devices. Another important effect attributed to the Al-epitaxy is the slight upwards bending of the NWs. As the lattice parameter for the Al is slightly smaller than in the $InAs_{0.65}Sb_{0.35}$ NW a compressive strain is introduced into the NW, effectively causing it to bend towards the Al-phase. Thus, the WZ NWs can be distinguised

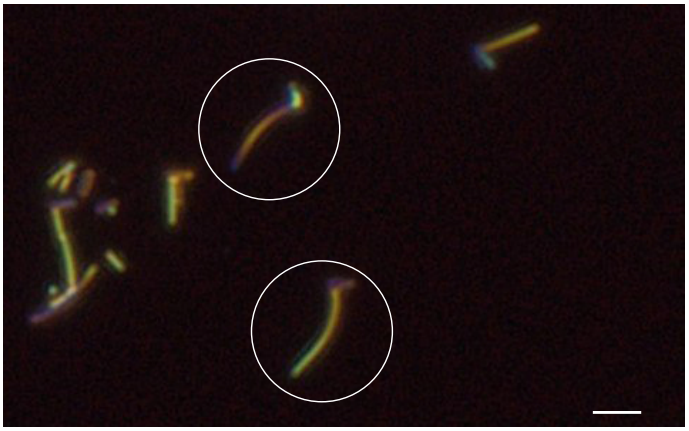


Figure 12: Dark-field optical microscope image of QDev253 NWs on the device substrate. The white circles shows the WZ NWs to be used for devices. Scale bar is 1 μm.

even in an optical microscope as seen in the dark-field image of Qdev253 NWs on a device chip in Fig. 12. This is crucial for the device yield, as devices are only fabricated on the desired NWs (WZ). In InAs NWs the smaller lattice parameter, compared to InAsSb following Vegards Law, introduces a tensile strain in the NWs causing them to bend away from the Al-phase [33].

The WZ InAsSb NWs are of great interest as WZ III/V NWs are reported to have larger band gaps than ZB [64] and have shown a type-IIC band alignment going from ZB to WZ in InAs NWs [65] which is also predominant when going from InAs to $InAs_{1-x}Sb_x$ [48]. Although the latter result is not specifically for WZ InAsSb, it is a reasonable assumption that WZ InAsSb NWs will exhibit trends analogous to those seen in the ZB crystal structure. In Fig. 13 calculated valence E_v and conductance E_c bands as function of molar fraction, x, in $InAs_{1-x}Sb_x$ is shown.

Assuming that WZ InAsSb acts a other III/V NWs, and keeping the type-IIC band alignment in mind, this means the conduction band edge for a WZ NW has a lower electron affinity compared to ZB structures which in combination with the larger

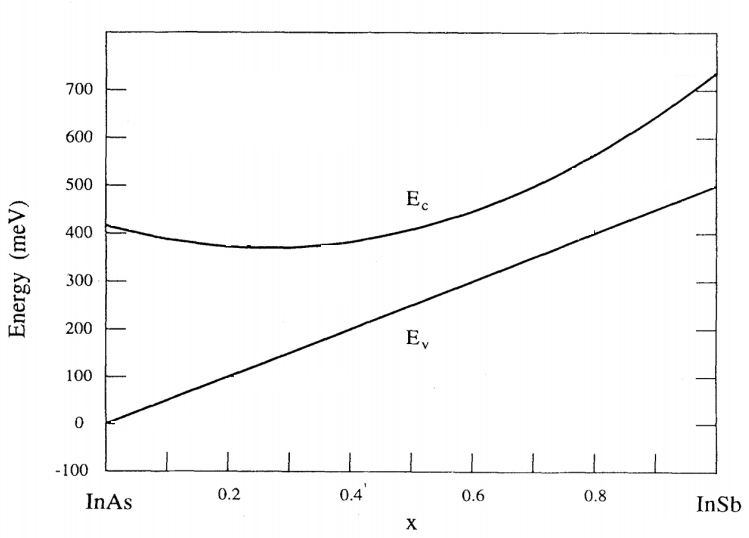


Figure 13: Calculated band structure for ZB $InAs_{1-x}Sb_X$. Figure adapted, and slightly modified, from [48]

bandgap will result in WZ InAsSb NWs to exhibit a larger electrostatic gate response. Blocking transport through InAsSb NWs, using only side gates, has not previously been possible in our lab.

4.1.1 Delft Geometry

In Fig. 14 a false-colored SEM image of a measured side-gated Delft geometry device on a WZ Qdev253 NW from the *Camp Nou* chip is seen. The Al is etched away to facilitate the normal metal/NW contact. The remaining Al form the NW/superconductor segment (proximitized segment) with a length of 700 nm. A cutter gate ($V_{cut1,2}$) is placed on either side of the NW to be able to apply a large enough negative voltage to only allow a tunneling current between the normal metal lead and the proximitized segment. The side gate is used to control the chemical potential in the proximitized segment. The plunger gate is placed on the opposite

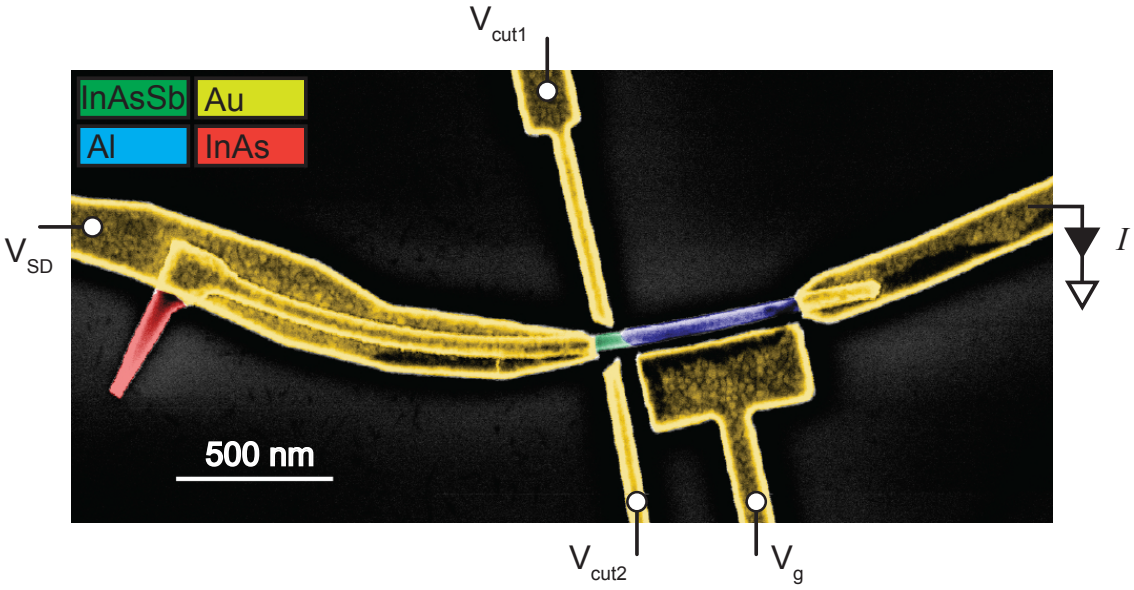


Figure 14: False-colored Scanning Electron Micrograph of a Delft geometry device on a Qdev253 WZ NW.

side of the Al-covered top facet, for the plunger gate to have the largest effect on the chemical potential in the NW, i.e. the Al does not screen the gate potential.

After loading the sample into the fridge and cooling to base temperature zero-bias differential conductance, is measured as a function of cutter gate voltage, V_{cut1}, as described in sec. 3.2.

As seen by the trace in Fig. 15**a** applying several volts of negative gate voltage on both V_{cut1} and V_{cut2}, the differential conductance through the device can be completely turned off. As mentioned above, InAsSb ZB NWs usually do not have such a high response from side gates which makes the WZ NWs promising for these experiments.

As described in sec. 2.1 the NW has to have induced superconductivity for MZMs to emerge. To test this, source-drain bias (V_{SD}) sweeps were preformed in the

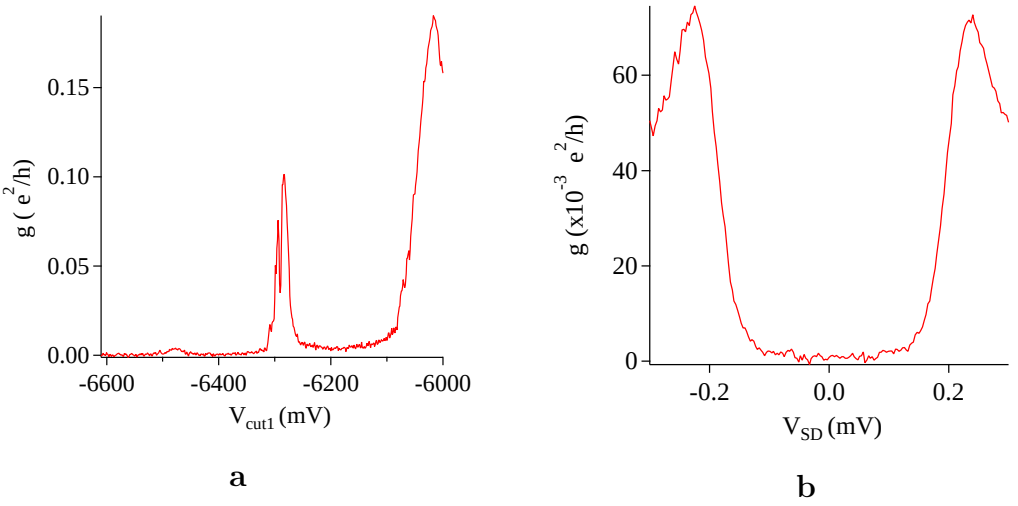


Figure 15: **a**) Plot of differential conductance, as function of cutter gate voltage (V_{cut1}). At the largest negative gate voltages the conductance through the device is turned off. Other gates are $V_{cut2} = -7000$ mV, $V_g = 0$ mV. **b**) Plot of differential conductance, g, as function of source-drain bias (V_{SD}). The trace shows a hard gap with near-zero conductance in the whole region $V_{SD} = -0.1 - 0.1$ mV. Other gates are: $V_{cut1} = -5000$ mV, $V_{cut2} = -7324$ mV, $V_g = 0$ mV.

region where the zero-bias differential conductance was zero, and as seen in Fig. 15**b** the differential conductance trace indeed resembles a hard-gap with gap size, $\Delta \sim 220$ μeV. This Δ is slightly larger than the value of $\Delta = 180 - 190$ μeV reported in the literature for InAs NWs proximitized by Al [34, 57]. The larger Δ could be caused by a thinner Al-phase on these NWs, as shown by reports on Al thin films [66]. It should be noted that the quality (slope of the conductance peaks) of induced superconducting gaps in NWs appear to be slightly better for a full-shell superconductor compared to a half shell [34]. For Majorana devices however, a half shell is superior as the superconductor does not screen the external potential as much, making it feasible to tune the charge carrier density in the NW.

With the device tuned into the right regime, all prerequisites for MZMs are existing;

1D semiconductor with proximitized superconductivity, large spin-orbit coupling, and large Landé g-factor. To localize sub-gap states gate sweeps using $V_{cut1,2}$ or V_g are performed at $V_{SD} = 0$ or a finite $V_{SD} < \Delta$.

In Fig. 16 an intensity plot of differential conductance as function of V_{SD} and V_{cut1}, which clearly exhibits subgap states, is seen. Over a V_{cut1} range of 250 mV the symmetric states emerge from the continuum, intersects at $V_{SD} = 0$ mV, almost reaches the other side of the superconducting gap before returning to their original continuum.

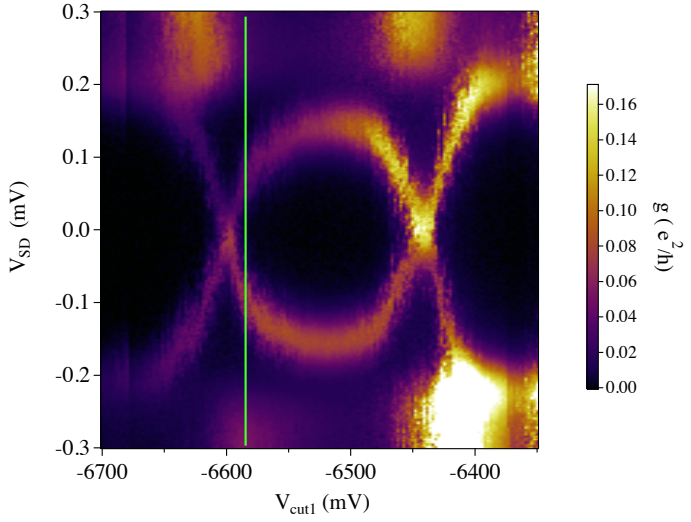


Figure 16: Intensity plot of differential conductance, g, as function of source-drain bias (V_{SD}) and cutter gate voltage (V_{cut1}). The superconducting gap and the subgap states discussed in the text are clearly visible. Other gates are: $V_{cut2} = -6000$ mV, $V_g = 0$ mV. The green line corresponds to the gate configuration used in Fig. 19

To examine if these states could be driven into a zero-bias peak in a parallel magnetic field ($B_\parallel$), a finite magnetic field angle sweep in the device-plane was performed and $B_\parallel$ was found to be 20° with respect to the z-axis, in accordance with an estimate based on device and chip carrier orientation. This can be determined as

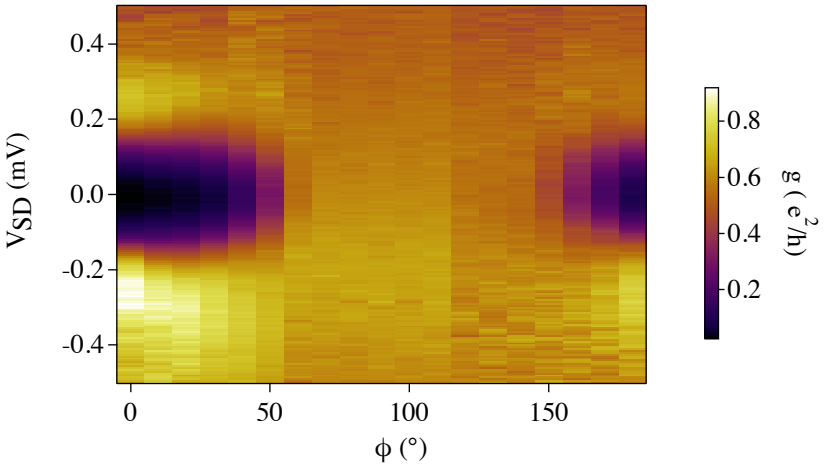


Figure 17: Finite magnetic field angle sweep at $|B|$ =200 mT. The parallel field direction is found to be 20° with respect to the z-axis.

superconductivity breaks down at a critical field B_c. A perpendicular magnetic field has the largest effect on superconductivity. Performing an in-plane 180°-sweep at finite magnetic field will show an oscillation of the magnitude of the superconducting gap, Δ. The parallel field direction is found by determining at which angle Δ has the largest value in a finite field of $B < B_c$. An angle sweep for this device is seen in Fig. 17 from which the parallel field direction was determined.

When the observed subgap states were evolved in the parallel magnetic field however, they did not respond. As seen in Fig. 18**a** of the same region of gate space at $B_{\parallel} = 400$ mT the superconducting gap has diminished as expected for a superconductor, but the subgap states maintain their position. At 1000 mT the conductance features in this region of gate space are significantly different. At this field magnitude two V_{SD}-independent conductance resonances are observed at similar gate voltages to the zero-field intersections between the subgap states as depicted in Fig. 18**b**. These conductance resonances are also observed at the same gate voltages above

the superconducting gap in Fig. 18**a** and are attributed to Coulomb resonances in a quantum dot formed in the constriction between the normal metal lead and the proximitized segment.

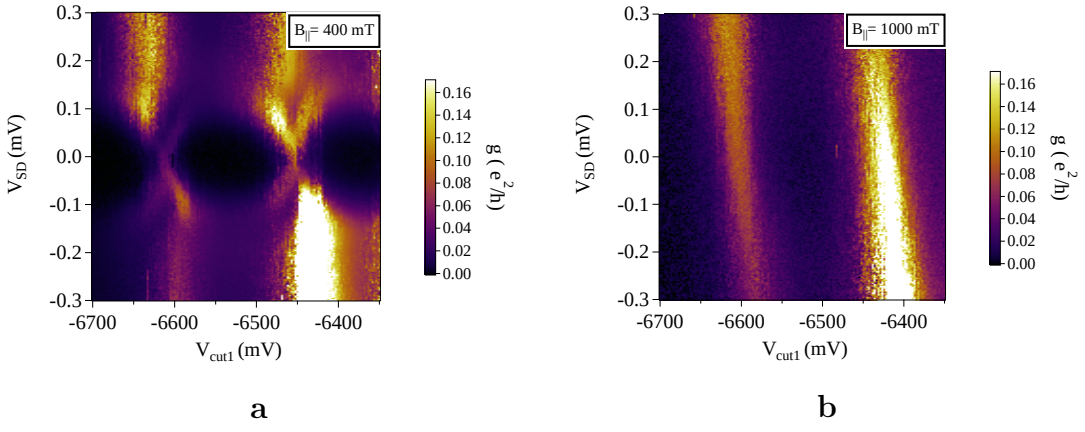


Figure 18: Intensity plots with the same gate configuration as in Fig. 16 at finite magnetic fields. **a**) $B_{\|} = 400$ mT. The superconducting gap has diminished, but still persists. The subgap states are at the same energy as the $B_{\|} = 0$ mT case and have merged with the continuum. **b**) $B_{\|} = 1000$ mT. All features have disappeared save for the two Coulomb resonances.

To verify that these subgap states were indeed not of the desired nature an intensity plot of differential conductance as function of V_{SD} and $B_{\|}$ was performed at $V_{cut1} = -6555$ mV, corresponding to the green line in Fig. 16. This plot is seen in Fig. 19 where the subgap states are located at $\sim \pm 0.1$ mV at $B_{\|} = 0$ and stay at that voltage until the closing of the superconducting gap.

The subgap states observed in this device are believed to be Yu-Shiba-Rusinov (YSR) states which are observed in quantum dots coupled to a superconductor [67, 68, 69, 70]. The characteristics of YSR-states depend on the coupling between the superconductor and the quantum dot, and since all aforementioned measurements are performed at similar gate configurations, no change in the YSR-states are

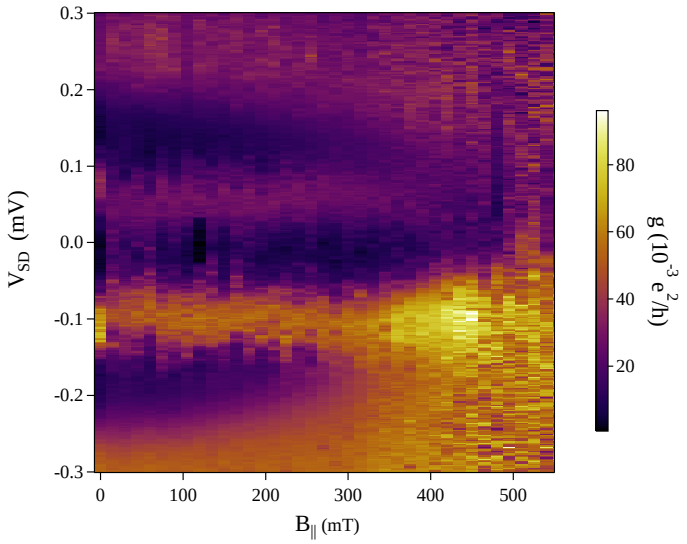


Figure 19: Intensity plot of differential conductance as function of source-drain bias and parallel magnetic field magnitude. The energy of the subgap states are unaffected by the magnetic field.

expected as function of magnetic field.

4.1.2 Copenhagen Geometry

In Fig. 20 a false-colored SEM image of a Copenhagen geometry device on a Qdev253 WZ NW from the *Camp Nou* chip is seen. As in the Delft geometry the $V_{cut1,2,l,u}$ gates are used to tune the tunnel coupling between the proximitized segment, with length $L \approx 500$ nm, and the normal metal leads while V_g is used to change the charge carrier density of this segment. As in the Delft geometry the plunger gate is beneath the wire using the same argument as above.

As in the previous section the first criteria to hunt for MZMs are for the device to be in the low conductance regime with an induced superconducting gap. In the trivial regime the Copenhagen geometry is essentially a superconducting quantum

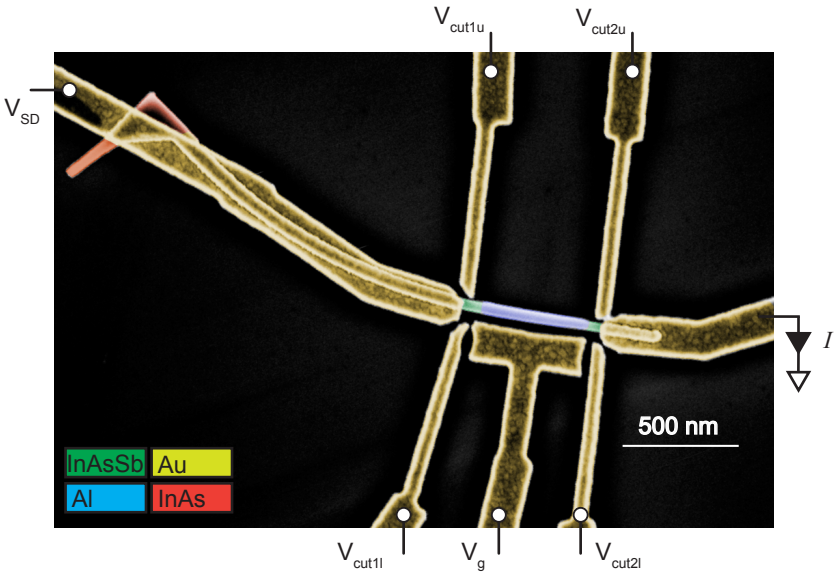


Figure 20: False-colored Scanning Electron Micrograph of a Copenhagen geometry device on a Qdev253 WZ NW with proximitized segment length of 500 nm. $V_{cut1,2,l,u}$ tunes the coupling between the normal metal leads and the proximitized segment while V_g tunes the charge carrier density of this segment.

dot, and similarly the transport signatures for MZMs in this device are evolved from the superconducting quantum dot characteristics as described in Sec. 2.2.3. After tweaking the gates to get the NW into this regime, zero-bias gate sweeps using either a cutter gate or the plunger gate are performed to find a region in gate space with Coulomb blockade features. As this NW had an intrinsically low conductance, a region like this could be found by applying a negative voltage of -240 mV on V_{cut2u} and perform a sweep with V_{cut2l}. In Fig. 21**a** a plot of a zero-bias differential conductance as function of V_{cut2l}-gate sweep showing a low conductance region with quantum dot-like transport features. At slightly more negative gate voltage the zero-bias differential conductance through the device is turned off entirely. Subsequently an intensity plot of this region was performed to determine if the zero-bias conductance peaks were a result of Coulomb blockade physics. This intensity plot

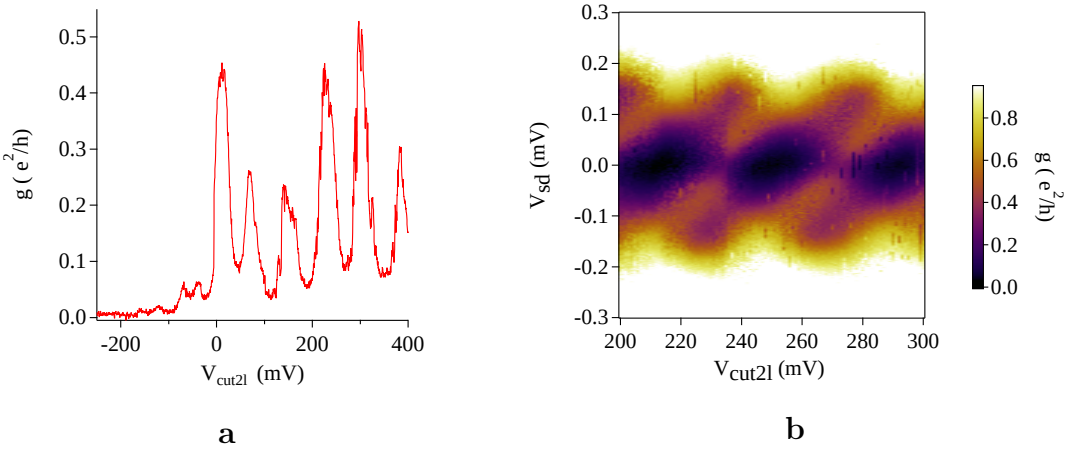


Figure 21: **a**) Plot of differential conductance as function of V_{cut2l}. At -200 mV, the conductance through the device is off. Transport features resembling Coulomb resonances are seen at slightly positive V_{cut2l} voltages. V_{cut2r} = -240 mV. **b**) Intensity plot of differential conductance as function of V_{SD} and V_{cut2l} exhibiting Coulomb diamond features. V_{cut2r} = -240 mV.

is shown in Fig. 21**b** with transport features that resemble Coulomb diamonds.

Due to the induced superconductivity in the NW the Coulomb peak periodicity is $2e$ as Cooper pairs tunnel on and off the island. To drive the NW into the $1e$ regime a parallel magnetic field is applied, to lower the energy of the odd occupation charge state. The parallel field direction was found as in the previous device and was determined to be 40° with respect to the z-axis. 200 mT increments from 0-1000 mT were followed by acquisition of intensity plots at the same gate configuration as Fig. 21**b**. In Fig. 22 two such plots are seen at 400 mT (**a**) and 1000 mT (**b**). It is apparent that the periodicity of the zero-bias Coulomb peaks does not change over this magnetic field range. At $B_{\|}$ =1000 mT the differential conductance in the device is almost completely constant at all source-drain biases and gate voltage which means superconductivity is destroyed and the device is in the normal conduction regime.

Although the Qdev253 NWs held much promise to use for Majorana devices from

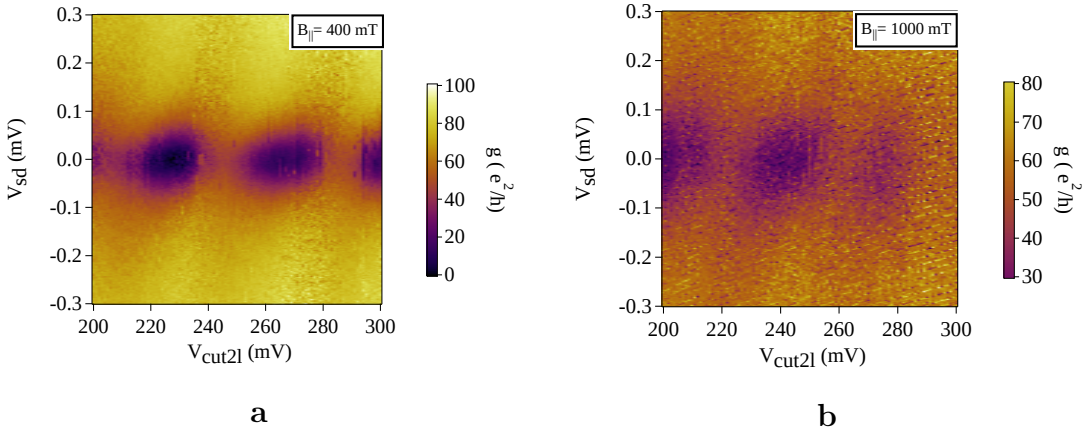
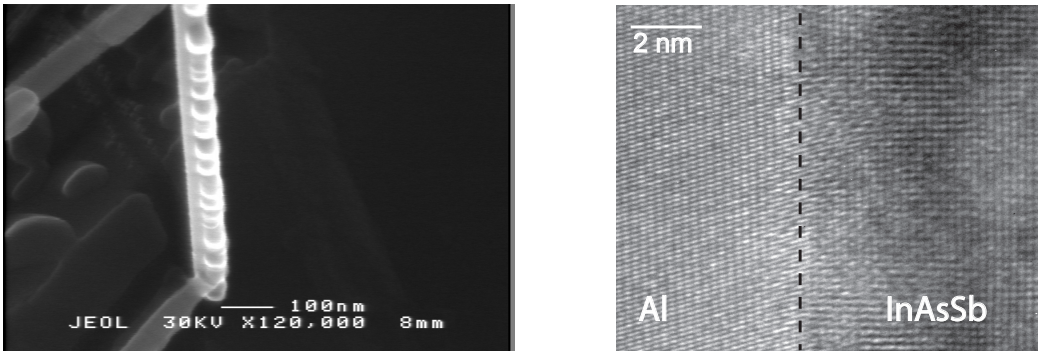


Figure 22: Plots with the same gate configuration as in Fig. 21**b** at finite magnetic field. **a**) $B_{||}$ = 400 mT. The superconducting gap has diminished, but still persists. V_{cut2r} = -240 mV. **b**) $B_{||}$ = 1000 mT. The differential conductance is almost constant implying the device is in the normal conductance regime. V_{cut2r} = -240 mV.

both an experimental and theoretical perspective, none of the devices on either of the three chips measured yielded the desired results. Nonetheless, these devices exhibited better response to the side gate potentials than previously observed on InAsSb NWs, an effect attributed to the unique crystal structure and the resulting bandstructure. Nano-lithography procedures are notoriously invasive and next to impossible to maintain exact control over, so this batch on NWs should not be entirely neglected before more statistics are obtained. Similarly a study into optimization of the device fabrication on these NWs, and InAsSb NWs in general, could improve the results. A such study has nevertheless not been the focus of the work presented in this thesis.

4.2 Qdev 310

The Qdev310 InAsSb NWs are a more conventional batch than the Qdev253 presented above. The growth is commenced by pure InAs growing on a InAs [111]B substrate. After a period of axial growth the Sb effusion cell is gradually opened and the NWs grows as ZB $InAs_{0.2}Sb_{0.8}$, determined by EDX (not shown), for several micrometers. Following NW growth, the temperature of the substrate is lowered to accommodate Al growth. In Fig. 23 an SEM image of a Qdev310 NW on the growth substrate is seen (**a**) along with a HR-TEM image of the InAsSb/Al interface (**b**). In contrast to the Qdev253 WZ Al-phase, it is apparent that the Al-phase on these NWs is less uniform and there is also a slight rotation of the Al with respect to the InAsSb facets. Nonetheless, the HR-TEM image shows an epitaxially matched semiconductor/superconductor interface.



a **b**

Figure 23: **a**) SEM image of a Qdev310 NW on the growth substrate. The Al-phase appears a bit rough and globular. **b**) HR-TEM image of the epitaxially matched InAsSb/Al interface, though the Al is rotated a few degrees with respect to the NW facets. Image credit Thomas Kanne.

4.2.1 Delft Geometry

In Fig. 24 as false-colored SEM image of one of the measured bottom gated Qdev310 Delft geometry devices from the chip *Honeybadger3.2* is seen[3]. Two of the bottom gate 'fingers' are shorted together to form a plunger gate, while the third acts as a cutter gate.

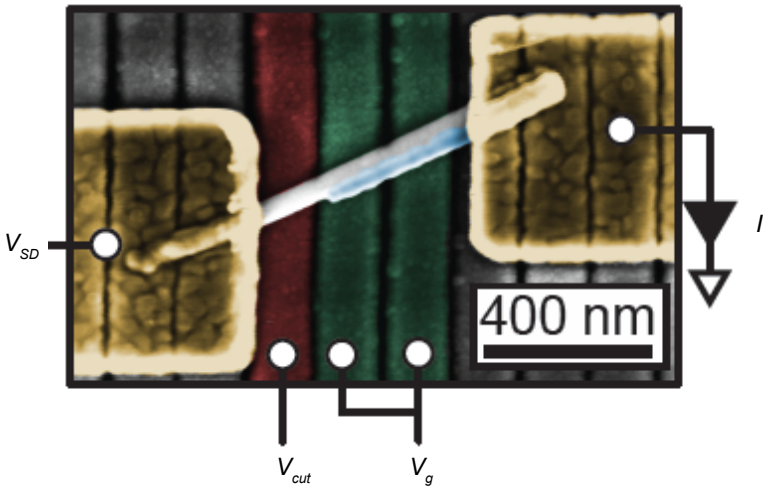


Figure 24: False-colored SEM image of a Qdev 310 bottom gated Delft geometry device. Figure from [55].

As the bottom gates are closer to the NW using the bottom gate scheme the lever arm of the gates is sufficient to block transport through the device. In Fig. 25**a** a zero-bias V_g sweep shows the differential conductance through the device turning off. Transport features resembling hard gap is observed at this gate configuration though with a low but finite sub gap conductance (not shown). Tweaking the gates further to increase the 'hardness' (i.e. slope of conductance peaks and sub gap conductance) of the gap yielded the hard gap seen in Fig. 25**b** with Δ= 225 μeV.

[3]The devices on this chip were fabricated by Joachim Sestoft. All measurements were performed in collaboration with Joachim Sestoft.

Again slightly larger than the Δ previously reported for InAs/Al. The sub gap conductance oscillates around g = 0 e^2/h and could be attributed to measurement noise.

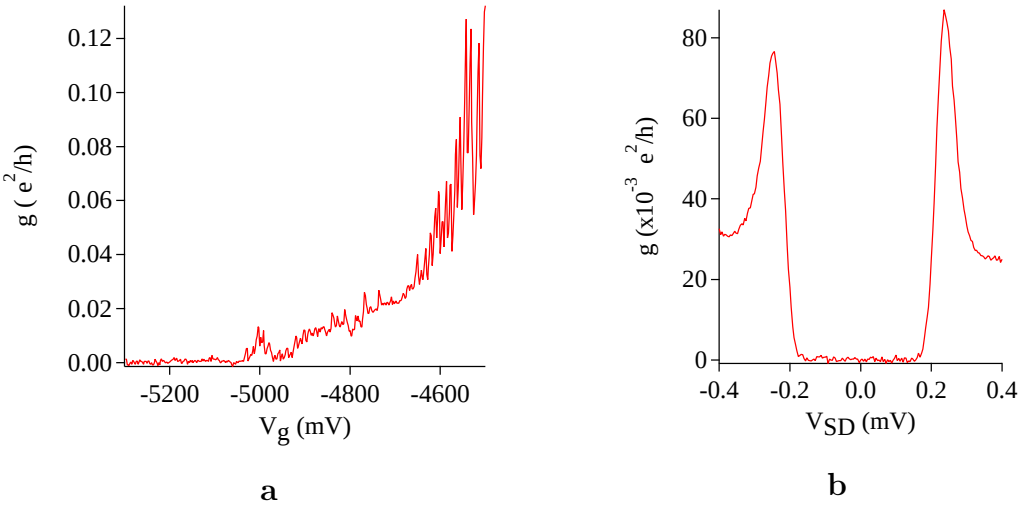


Figure 25: **a**) Plunger gate sweep showing the zero-bias conductance through the device being turned off. V_{cut} = -3500 mV. **b**) Source-drain sweep of the device showing a hard superconducting gap with Δ = 225 μeV. V_{cut} = -4500 mV, V_g = -7000 mV.

As before these transport features are the first requirements for MZM hunting. In an attempt to localize sub gap states, finite $V_{SD} < \Delta$ gate sweeps were performed. A region with below gap conductance peaks was localized and an intensity plot of differential conductance as function of source-drain bias and plunger gate voltage was acquired as seen in Fig. 26 [4] which resembles Andreev Bound States or strongly coupled YSR-states. Interesting to note is how the intensity of the superconducting conductance peaks decrease when the sub gap states enter the gap. It appears that the subgap states are part of the conductance resonance before moving into the gap, which could indicate that these states are indeed ABS.

[4]There is a $\sim$ 50 μV offset on the V_{SD} axis in the acquisition, which is attributed to the DECADAC voltage source.

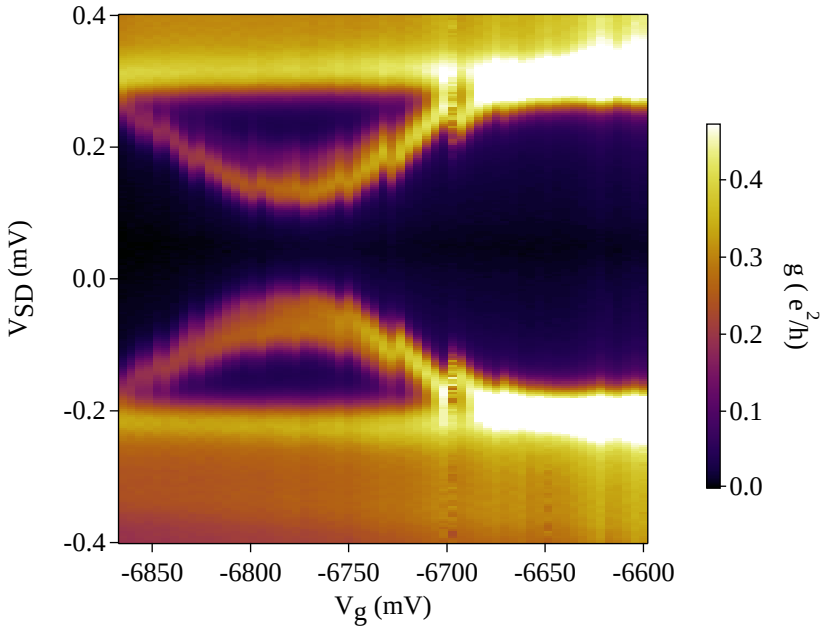


Figure 26: Intensity plot of differential conductance as function of source-drain bias and plunger gate voltage. V_{cut} = -3500 mV.

V_g was fixed at a value -6810 mV and an intensity plot was acquired of g as function of V_{SD} and $B_{\parallel} = 152°$ (determined as before) . This plot is seen in Fig. 27 where the subgap states at E = 100 μeV move towards zero energy as the parallel magnetic field increases. It is however difficult to distinguish whether the states join and pin to zero before the superconducting gap is closed at 900 mT. It appears that the subgap states at zero field have a spin degeneracy where one spin state moves towards, and eventually fuses with, the continuum while the other moves towards zero energy.

As mentioned in the previous section the parallel field direction could be estimated from the SEM images of the device. Prior to experimentally determining the parallel field direction and the acquisition of Fig. 27 a similar plot with an estimated magnetic field direction, B_{guess}, was performed. Further investigation revealed that B_{guess} was actually off by $\sim$30° with respect to the parallel direction. Nonetheless,

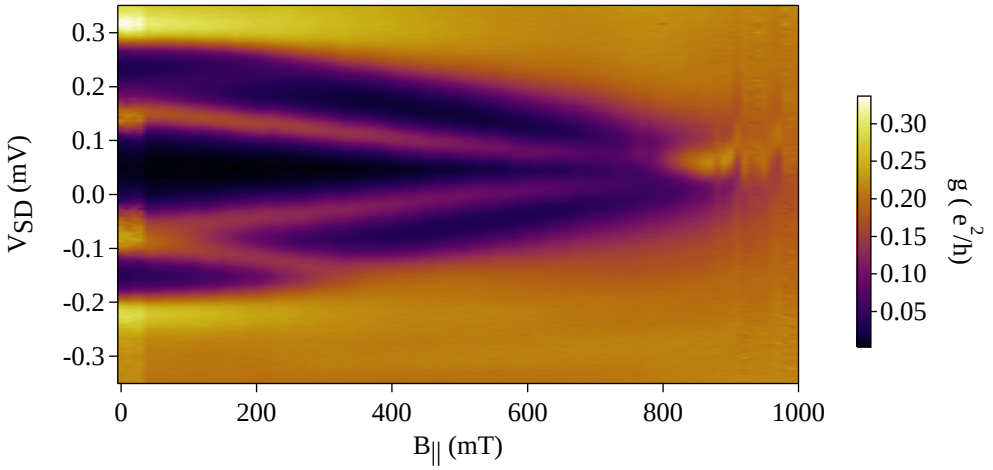


Figure 27: Intensity plot of differential conductance as function of source-drain bias and parallel magnetic field. The subgap states move towards zero energy as the magnitude of the magnetic field increases. V_{cut} = -3500 mV, V_g =-6810 mV, $B_{||} = 152°$.

this plot is seen in Fig. 28 where many of same features as in Fig. 27 are seen. With this field direction the subgap states merge and pin to E = 0 at $|B_{guess}| = 300$ mT and stay at that energy until the closing of the superconducting gap at $|B_{guess}| \approx 500$ mT. This is an unexpected result, as the parallel magnetic field component for this field direction is significantly smaller than for $B_{||}$. In accordance with expectation the superconducting gap closes at a lower finite field for this field direction.

Both Fig. 27 and 28 exhibit transport signatures of MZMs in the NIS geometry, which have not previously been reported on InAsSb NWs. The transport features seen in Fig 28 are identical to those obtained by Mourik in Sec. 2.2.3 plotted in a different way.

Although the subgap features drifted a bit in gate space over time, these measurements were very reproducible although the transport features depended on the exact gate configuration. In Fig. 29**a-d** intensity plots of differential conductance of these

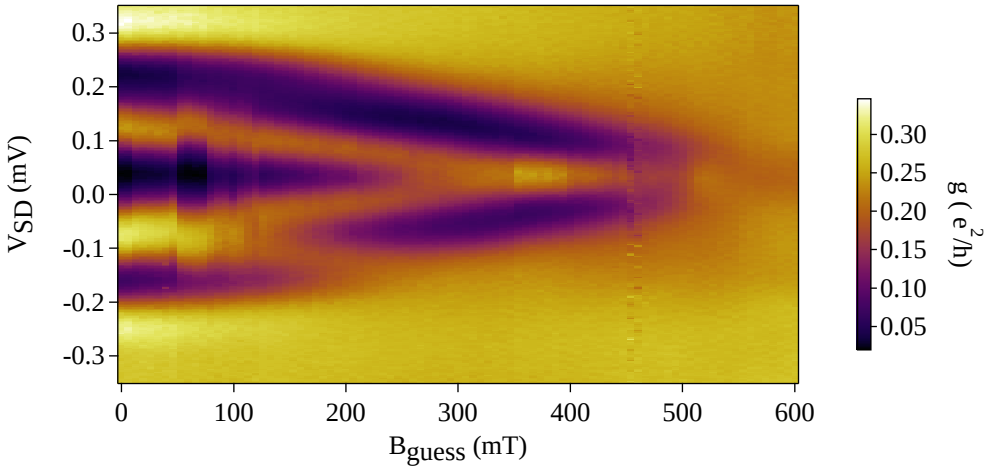


Figure 28: Intensity plot of differential conductance as function of source-drain bias and magnetic field magnitude. The subgap states pin to zero at B_{guess} = 300 mT at stay at this energy until the closing of the superconducting gap at B_{guess} = 500 mT. V_{cut} = -3500 mV, V_g=-6885mv, $|B_{guess}| = 5°$.

subgap states, in different conductance regimes, as function of source-drain voltage and $|B_{\|}|$ are seen, all exhibiting different transport features. The plots are obtained at different gate configurations, and generally show that these subgap states are intrinsic to the device and can be found at different liniear combinations of the gates. The evolution of the subgap states as function of the magnetic field is nonetheless different for each measurement, except for the apparent two-fold spin degeneracy of the states at $B_{\|} = 0$. In **a**, where the device is almost pinched off, the states move towards zero energy as the magnetic field increases. At $|B_{par}| = 400$ mT, they merge into a zero-bias conductance peak, and stay at that energy until the closing of the superconducting gap at $|B_{\|}| \approx 800$ mT. The conductance through the device in this measurement is only a fraction of that seen in Fig. 27 and 28 but the transport signature of the NIS MZMs still persist in this different conductance regime.

In Fig. 29**b** the magnetic field response seems to be higher as the sub gap states

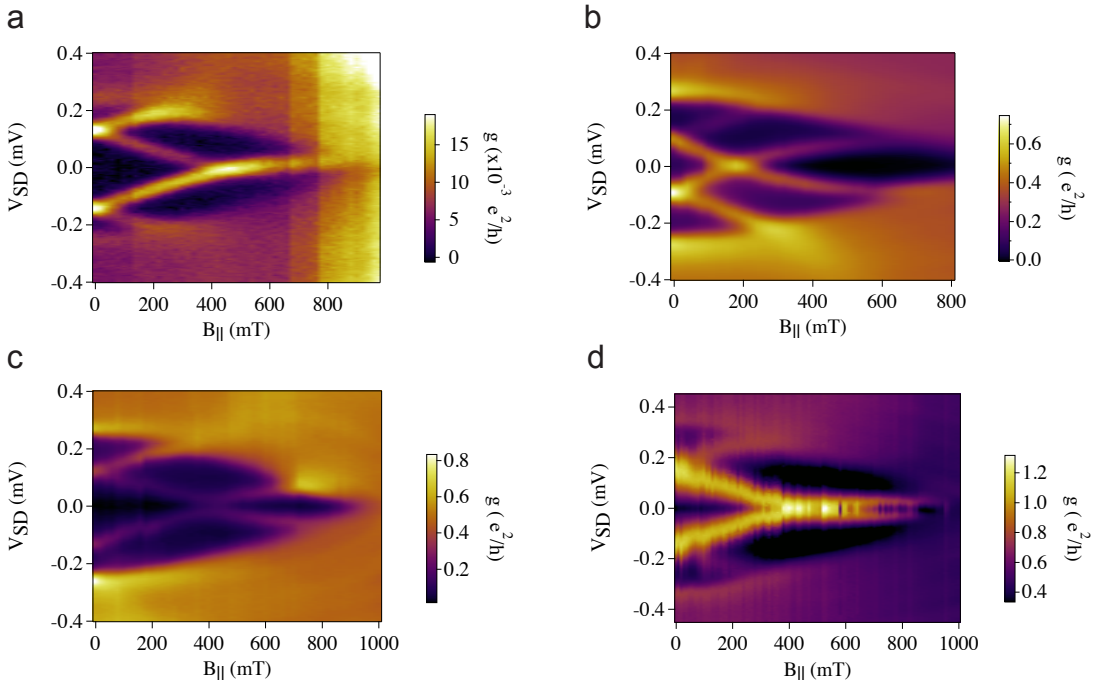


Figure 29: Intensity plots of differential conductance as function of source-drain bias and parallel magnetic field magnitude in different conductance regimes. **a**) V_{cut} = -9000 mV, V_g = -3885 mV. The device is in a low-conducting regime. The quite stable zero-bias peak is a transport signature of MZMs. **b**) V_{cut} = -7500 mV, V_g = -4738 mV. The states cross at $|B_{\|}|$ = 200 mT and continue their trend until merging with the vacuum. **c**) V_{cut} = -3500 mV, V_g = -8578 mV. The subgap states move towards zero energy as the magnetic field increases. An anti-crossing occur at $|B_{\|}|$ = 400 mT and the states move towards, and eventually merges with, the continuum. **d**) V_{cut} = -3500 mV, V_g = -8650 mV. The device is a high-conductance regime. The subgap states merge at $|B_{\|}|$ = 400 mT and split again at $|B_{par}| \approx$ 600 mT. Oscillations like these are mentioned in the literature.

meet at $V_{SD} = 0$ at $|B_{\|}|$ = 200 mT, however they continue moving as function of the magnetic field and eventually merge with the continuum on either side at $|B_{\|}|$ = 600 mT. Fig. 29**c**, an avoided crossing is observed instead of a merging at $|B_{\|}|$ = 400 mT.

In Fig. 29**d**, for which the gate configuration is very similar to **c**, where the conductance is roughly two orders of magnitude higher than **a**, the subgap states exhibit

the same trend as in Fig. 29**a** at first. After merging at $|B_{\parallel}| = 400$ mT a gap is reopened around E = 0 at $|B_{\parallel}| \approx 600$ mT. This effect is predicted theoretically for MZMs in proximitized NWs [25].

From the response to the magnetic field, Landé g-factors can be extracted from the Zeeman term

$$\Delta E_z = \mu_B g \Delta B$$

with ΔE_z being the change in energy, μ_B the Bohr Magneton, and ΔB the change in magnetic field magnitude. Simply put, the g-factor can be determined from the slope of the subgap states as function of the magnetic field magnitude. For this device the extracted g-factors varied between 5-20. The high g-factor helps explain why the apparent emergence of MZMs in these wires occur at quite low magnetic fields compared to similar experiments on NIS devices on InAs NWs performed in our lab (not published).

4.2.2 Copenhagen Geometry

In Fig. 30 an SEM image of a measured top gated Copenhagen geometry device on a Qdev310 NW from the *Honeybadger2*[5] chip is seen. The length of the proximitized segment is 1.2 μm.

As mentioned earlier the transition to topological superconductivity in this device geometry is observed as the transition from $2e$ periodic Coulomb resonances to $1e$ in

[5]The devices on this chip were fabricated by Joachim Sestoft. All measurements were performed in collaboration with Joachim Sestoft.

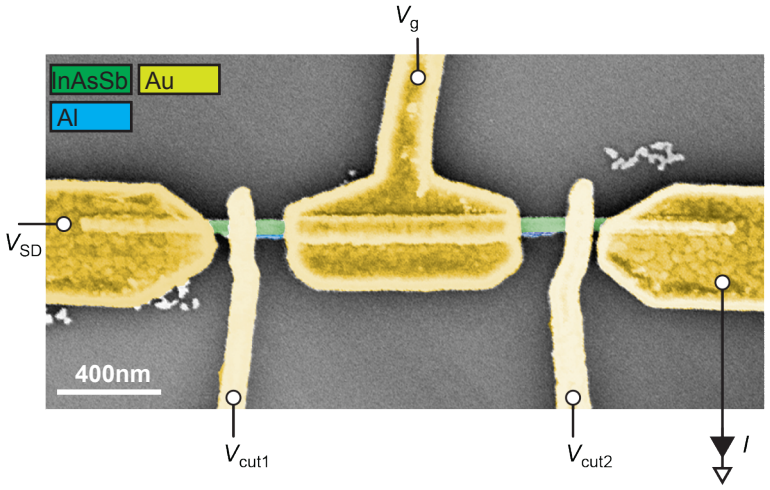


Figure 30: SEM image of a top gated Copenhagen geometry device on a Qdev310 NW. Figure from [55]

a finite magnetic field. First transport features desired in this device are proximitized superconductivity and Coulomb blockade physics. In Fig. 31**a** a plot of differential conductance as function of source-drain bias, with all gates being 0, exhibiting proximitized superconductivity is seen. Fig. 31**b** shows the differential conductance as function of plunger gate voltage, in a region that exhibits Coulomb blockade and Coulomb resonances, which in combination with the proximitized superconductivity should have a $2e$ period.

To drive the device into the $2e$ to $1e$ transition, the parallel field direction was determined, as before, to be $B_{\parallel} = 45°$. The lowering of the odd charge state, as function of magnetic field magnitude, should show the period of the zero-bias Coulomb resonances being halved. In Fig. 32 intensity plots of differential conductance as function of source-drain bias and plunger gate voltage at $|B_{\parallel}| = 0$, 150, 300 mT are shown. At zero field evenly spaced Coulomb diamonds are seen. The even spacing is expected for a proximitized segment of this length [57]. At the edge of the superconducting

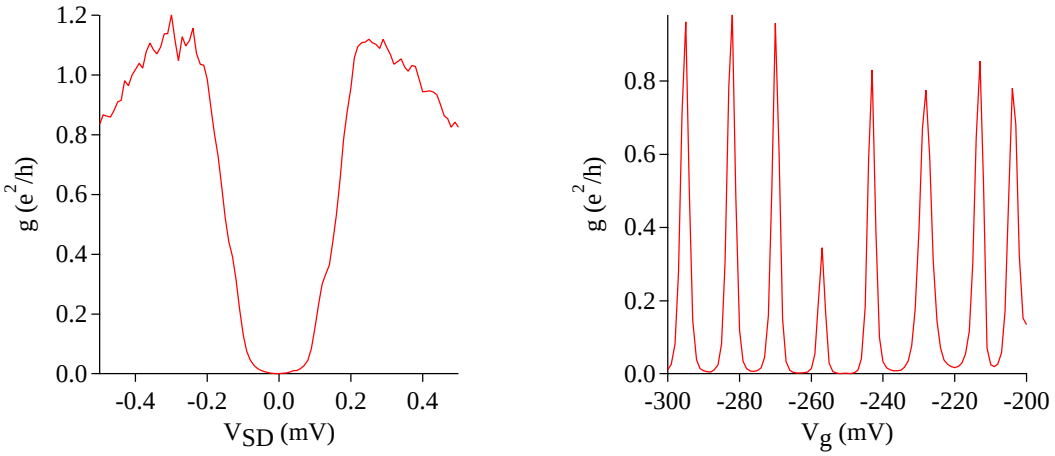


Figure 31: **a**) Plot of differential conductance as function of source-drain bias showing a superconducting gap. This device exhibits a low intrinsic conductance. Other gates are 0. **b**)Plot of differential conductance as function of V_g. This region exhibits transport features of Coulomb blockade- and resonances, presumably with $2e$ periodicity. Other gates are 0.

gap inside the conductance regions, areas of large Negative Differential Conductance (NDC) are seen. The observed NDC is in accordance with recent experiments on Majorana islands [57, 71] and has previously been studied in mesoscopic superconducting quantum dots coupled to normal metal leads [72]. As $|B_{\|}|$ is increased to 150 mT the width of the superconducting gap decreases while the NDC and the Coulomb resonances prevail. At $|B_{\|}| = 300$ mT the device has transitioned from $2e$ to $1e$ and the periodicity of the zero-bias resonances has doubled. This is in accordance with theory on MZMs and corresponds to previous report by Albrecht *et. al.* on InAs/Al Majorana devices of this geometry. The $2e$ to $1e$ transition is a transport signature of MZMs and has not previously been reported in InAsSb.

In Fig. 33 an alternate way of showing the $2e$ to $1e$ transition is seen. The plot shows a zero-bias intensity plot of differential conductance as function of V_{cut} and

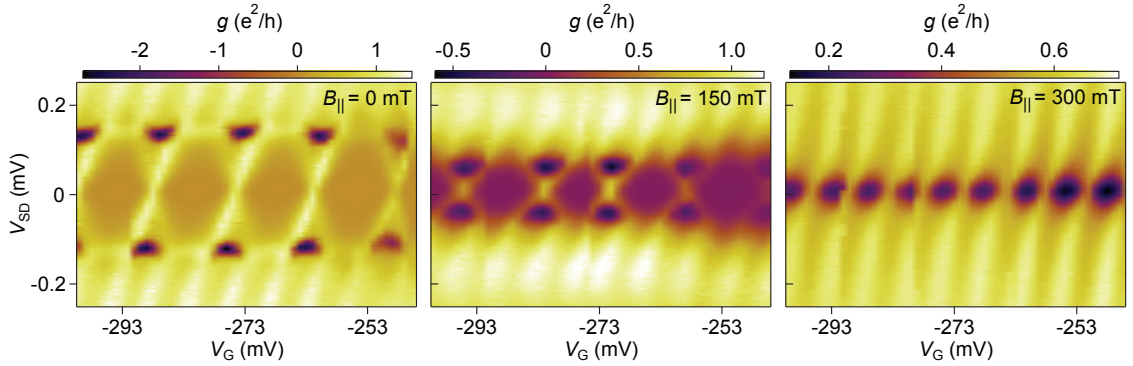


Figure 32: Intensity plots of differential conductance as function of source-drain bias and plunger gate voltage at $B_{\parallel} = 0$, 150, 300 mT. period between the zero-bias differential conductance resonances is halved from $B_{\parallel} = 0$ to $B_{\parallel} = 300$ mT, indicating a transition from $2e$ to $1e$. All other gates are 0.

$|B_{\parallel}|$. At low fields Coulomb resonances are seen. As the field increases the differential conductance drops significantly and the conductance resonances split at $B_{\parallel} = B^* =$ 150 mT. At $B_{\parallel} = B^{**} =$240 mT the conductance resonances regain intensity and have half the gate distance between them corresponding to $1e$. The $1e$ conductance resonances after B^{**} have half the conductance of the $2e$ resonances.

As shown above, transport signatures of MZMs have been thoroughly measured and probed in the Qdev310 InAsSb/Al NWs. These signatures were observed in both of the investigated geometries as well as with two different gating schemes. As expected the side gated devices on these NWs did not have a good enough gate response and did not yield any notable results.

Interestingly these NWs seem to defy the argument often found in the literature that the better the epitaxial interface is, the more suited are the NWs for Majorana devices. The Al-phase in the Qdev310 NWs is not entirely uniform, sometimes discontinuous, and rotated a few degree with respect to the NW facets; a stark contrast to the Al-phase seen in the Qdev253 NWs. This could be an indication

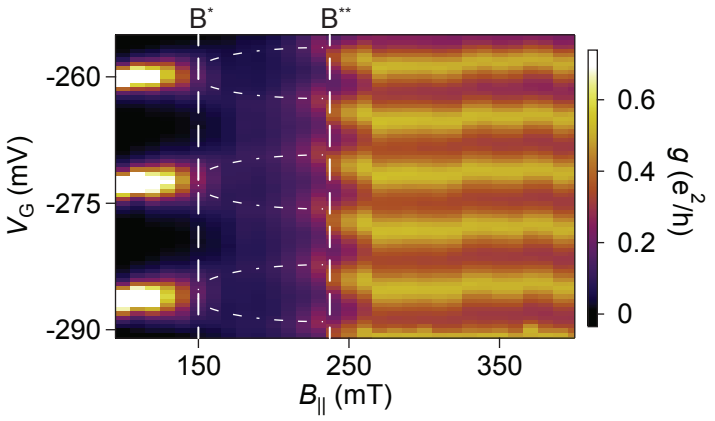


Figure 33: Intensity plot of differential conductance as function of plunger gate voltage and parallel magnetic field magnitude. Between B^* and B^{**} to transition from $2e$ to $1e$ occur.

that a clean semiconductor/superconductor interface is a decisive parameter for the properties of this interface more than the exact epitaxial matching. A study on the Al-epitaxy effects on measurements of MZMs could prove vital for understanding how different parameters alter the properties of Majorana devices. Similarly, a study on different As/Sb ratios be key in determining an optimal material for realizing MZMs in condensed matter devices.

5 Conclusion

This thesis presents two major results on InAsSb NW devices. First, we find that WZ InAsSb has a lower electron affinity than in the ZB crystal structure, making WZ InAsSb NWs more responsive to electrostatic gate potentials. A further study into the exact band structure, theoretically and experimentally, of WZ InAsSb NWs could make these eligible for new applications. Second, InAsSb/Al hybrid NWs are a viable condensed matter platform for realizing MZMs. Neither has been reported previously.

Data exhibiting indications of MZMs are observed in several devices. Only the most prominent results obtained during the InAsSb/Al NWs MZM study have been presented during this thesis.

From the data presented in this thesis it is not possible to conclude if InAsSb NWs are superior to InAs or InSb NWs for realizing MZMs. To determine which InAsSb alloy is optimal for Majorana devices a more thorough study of different As/Sb ratios is required. If the meta-stable CuPt-stacked $InAs_{0.5}Sb_{0.5}$ NWs could be grown, MZM experiments using these would be very interesting. Exploring alternative superconductor shell materials, e.g V or NbTiN, could also be a decisive factor in which hybrid NW/superconductor system is optimal for Majorana devices.

The transport signatures of MZMs found in both explored device geometries do not prove that the observed states are Majorana fermions. To reach this conclusion the non-abelian exchange statistics of MZMs has to be demonstrated. This requires either braiding in a network hosting two sets of MZMs or detecting the non-trivial fusion rule outcome of two sets of MZMs. Both are experiments that lie ahead and

have not been the subject of this thesis.

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6 Appendix A

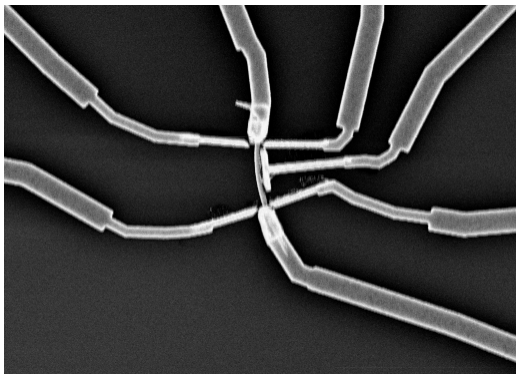
List of devices

In the following I will give an outline of the not previously mentioned device chips I have fabricated during my thesis studies as well as those fabricated by others on which I have been helping with measurements. The devices will be presented with its chip nickname.

Devices Fabricated

AG1

Side gated Delft and Copenhagen geometry devices on the Qdev253 InAsSb/Al WZ NWs.

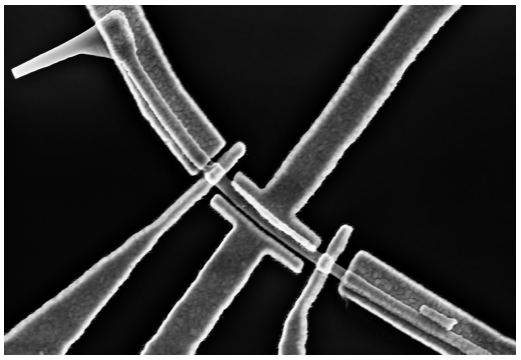


SEM image of a Copenhagen geometry device from the AG1 device chip

Device was overexposed and not measured.

AG2

Top gated Delft and Copenhagen geometry devices on the Qdev253 InAsSb/Al WZ NWs.

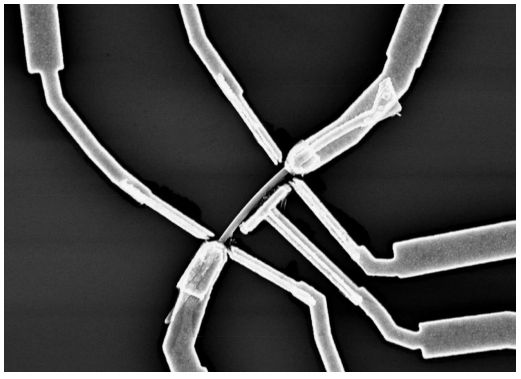


SEM image of a Copenhagen geometry device from the AG2 device chip

Devices were measured but were very switchy. This was attributed to charge traps in the Al_2O_3 dielectric. No relevant data acquired.

AG3

Side gated Delft and Copenhagen geometry devices on the Qdev253 InAsSb/Al WZ NWs.

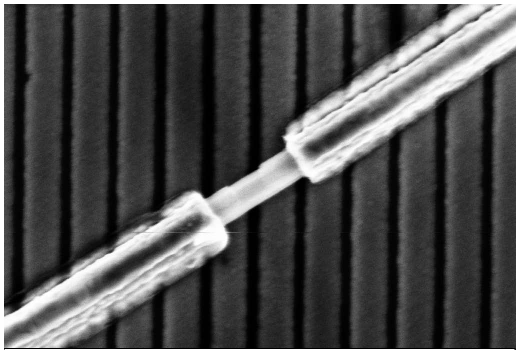


SEM image of a Copenhagen geometry device from the AG2 device chip

Gates and contacts were leaking, probably to back gate due to too much force being used for bonding.

Ceres Park

Bottom gated SIS devices on the Qdev 422 InAs/GaSb(full-shell)/Al(half-shell)

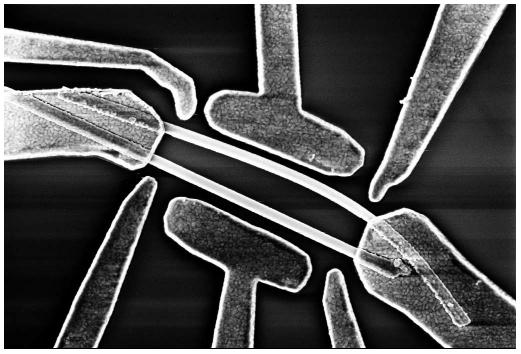


SEM image of a SIS device from the Ceres Park chip

Devices were measured but did not yield the desired results.

White Heart Lane

Side gated Interferometer devices on the Qdev418 InAs/Al NWs.

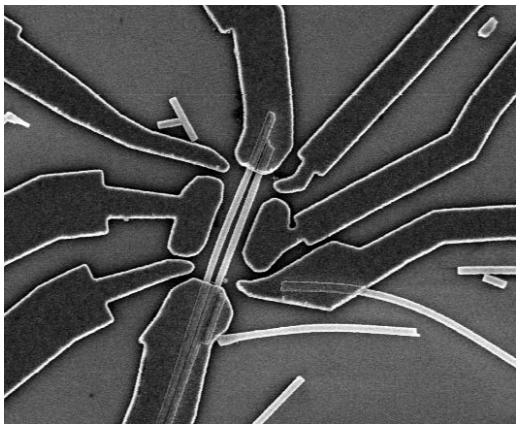


SEM image of a device from the White Heart Lane device chip.

First generation of Interferometer devices. Sample was measured for a short while. Only 1 device had all contacts and gates working. No relevant data obtained.

Emirates

Side gated Interferometer devices on the Qdev418 InAs/Al NWs.

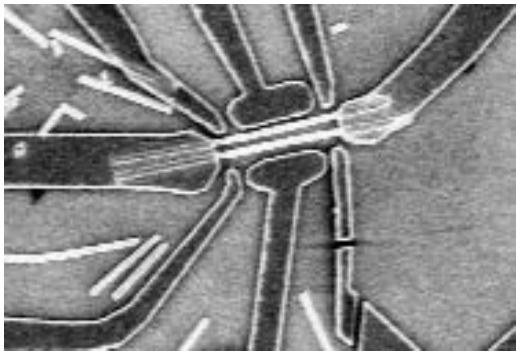


SEM image of a device from the Emirates device chip.

No functioning devices.

Stade de France

Side gated Interferometer devices on the Qdev 418 InAs/Al NWs.



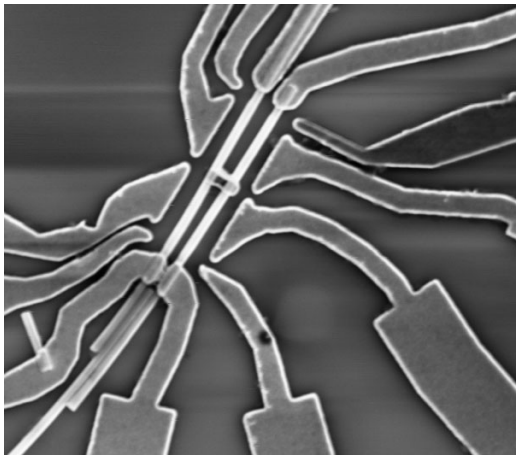
SEM image of a device from the Stade de France chip

No devices had all gates and contacts working.

Bernabeu

Side gated Interferometer devices on the Qdev418 InAs/Al NWs.

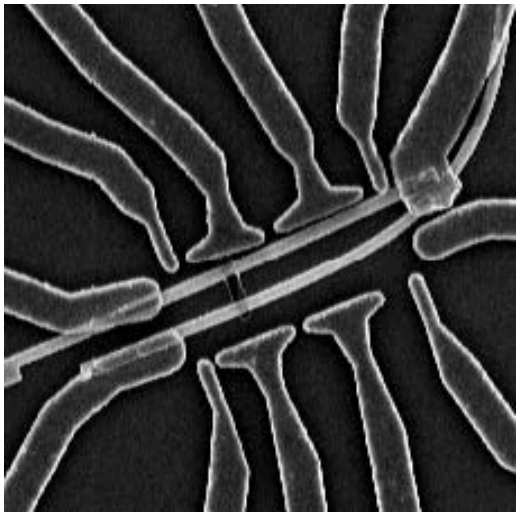
Sample was measured without obtaining any relevant data. Device was unloaded when the device geometry was found to be insufficient for the desired measurements.



SEM image of a device from the Bernabeu chip.

Wembley

Side gated 2^{nd} generation Interferometer devices on the Qdev418 InAs/Al NWs.



SEM image of a device from the Wembley chip

Misalignment in the EBL exposure, presumably due to lensing effect of resist at the chip edge.

Measured Devices Fabricated by Collaborators

Orangutang3

Side gated Copenhagen and Delft geometry devices on the Qdev310 InAsSb/Al NWs. No relevant data. Devices fabricated by Joachim Sesoft.

Honeybadger3.1

Bottom gated Copenhagen and Delft geometry devices on the Qdev310 InAsSb/Al NWs. No relevant data. Devices fabricated by Joachim Sestoft.

MAY1

Side gated Copenhagen and Delft geometry devices on the Qdev189 InAsSb/Al NWs. No relevant data. Devices fabricated by Jeremy Yodh.