FACULTY OF SCIENCE
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Master's thesis

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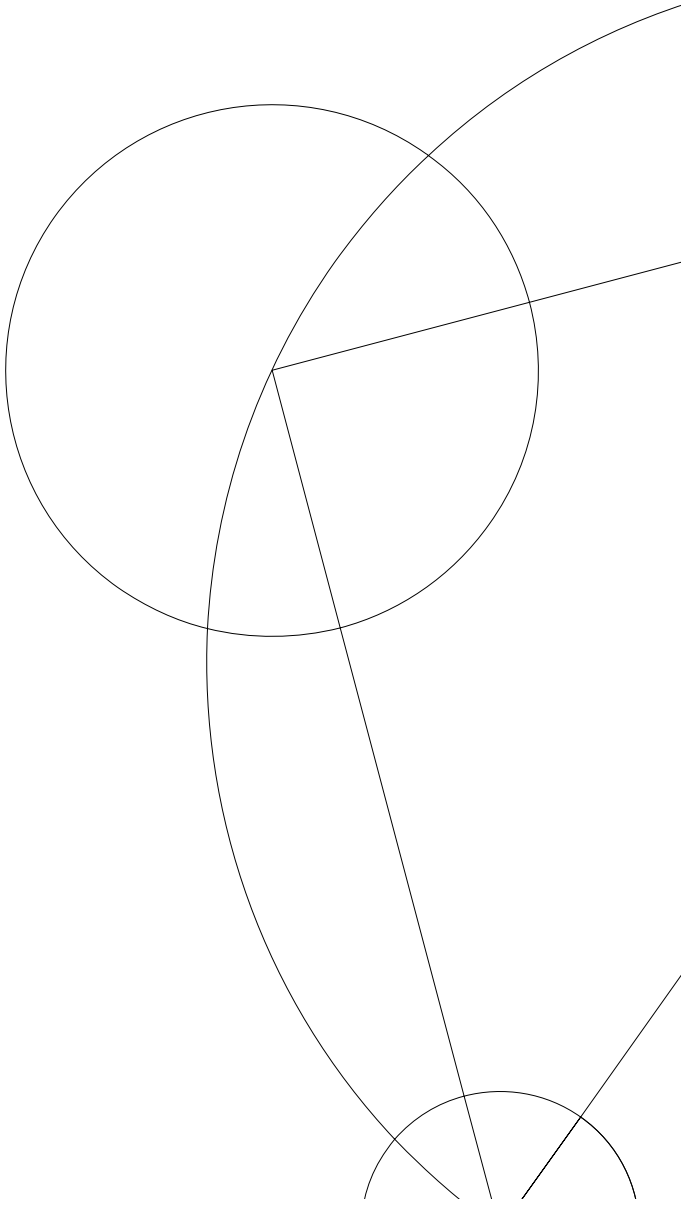
Scaling electron spin qubit devices implemented in GaAs quantum dots



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ABSTRACT

Scaling towards multiple qubits is the next major challenge for the field of solid state electron spin qubits. Implementing a solid interconnection mechanism plays a key role in the viability of spin qubits for quantum computation and quantum error correction. A fabrication recipe is developed that allows for creation of arbitrary gate defined quantum systems in two dimensions in GaAs. A number of device designs that allow multiple qubit operation are fabricated. Experimental results from two different device designs are presented. A linear device with 12 working quantum dots designed for exchange coupling of three resonant exchange only qubits via quantum systems is shown and it's performance characterized. Operation of exchange only qubits was not possible within the device due to poor performance of the charge sensors and capacitive cross-coupling of the electrostatic gates. A different device, designed as a flexible platform for implementation of multiple types of spin qubits coupled via a quantum system is also characterized. A tunnel coupled triple quantum dot is configured within the device, and a double quantum dot with the capability for single shot readout is demonstrated. A number of experimental challenges are identified and possible solutions are suggested, together with a few ideas for future experiments within similar systems.

CONTENTS

LIST OF FIGURES

1 INTRODUCTION

Over the past sixty years we have seen incredible advancements in computing power. With the pursuit of the Moore's law, computer components are getting ever smaller with the number of transistors growing faster than ever. However, even with billions of logic bits in a conventional CPUs there is still a number of computational problems that cannot be solved, even by transitioning to smaller process nodes[1]. Due to probabilistic nature of physics and quantum mechanical phenomena such as particles or systems existing in superpositions, the deterministic classical computers struggle.

As originally proposed by Richard Feynman[1] in 1981, to simulate a quantum system, it only makes sense to use a quantum system. Come in the quantum bit, or qubit. Similarly to a classical bit, a qubit can take the values of 1 and 0, denoted $|1\rangle$ and $|0\rangle$, but since it is a quantum system, a qubit state can be in a superposition of ones and zeros. By adding multiple qubits a quantum computer can be in a superposition of all possible states states at the same time. This property is called quantum parallelism.

Utilizing quantum parallelism makes solving certain computational problems significantly more efficient. Factorizing prime numbers of length N suddenly takes only N^2 amount of time as opposed to $e^{N^{1/3}}$ for the classical system, as discovered by P. Shor[2] and jump started the field quantum computation. Other famous algorithms include Grover's quantum search[3] which allows the reduction of database access calls by 50% compared to classical algorithms. For natural sciences quantum computation promises exponential gains in the speeds for quantum simulation[1].

In essence any quantum mechanical system with two levels can be used for quantum computation. To build a complete quantum computer, however, it needs to fulfill the requirements postulated by D. DiVincenzo[4]. In needs to be a well characterized system, where one knows all it's energy eigenstates and the interactions with the control apparatus and other qubits, that can be scaled in a trivial(or semi trivial) manner. It has to be possible to initialize a known quantum state, for example set all registers to zero, or prepare a state of interest. It must not decay on the timescale of the gate operations, i.e. it's decoherence times must be *much* longer than the quantum gate operation times. And finally it must be able to perform a set of "universal" quantum gates, a simplest of which is comprised of all single qubit operations and a single two qubit gate, like XOR or cNOT, with the possibility to read out each qubit individually.

Since the emergence of the field many schemes for implementing qubits have been proposed and demonstrated, including ions trapped in electrostatic fields[5], atoms in ultracold gases[6], Nitrogen Vacancy centers in a diamond[7], superconducting RC circuits[8], nuclear spins excited by NMR[9] and of course electron spins[10] [11][12][13][14][15][16].

[1] A technical terms used to describe processor manufacturing technology. A process node refers to the physical size of the transistors on a CPU. As of writing of this thesis the current Intel process node is $22nm$, moving into $14nm$ early 2015

1.1 Experimental challenges in implementation of multiple qubits

Scaling qubit systems is important not just for increasing the computational power of a quantum computer. Any interaction with the environment can cause an unwanted change of a state of the qubit causing errors. In a classical system these errors can be corrected through redundancy, but in quantum systems the "No cloning theorem"[17] prevents one from simply copying the state. An existing approach to correcting errors in quantum systems is to connect several "physical" qubits as a single "logical" qubit[18]. The detection and correction of errors can then be interlaced with the operation of the logical qubits.

To reduce the number of errors from decoherence or dephasing one wants the qubits to be well isolated from the environment, while operation and measurements the qubits have to be well coupled to the control electronics which could be a major source of errors. In tightly packed architectures control interactions with the qubit would also affect it's neighbour. One intuitive way of avoiding this cross coupling is by separating the qubits. A two spin qubit interaction through induced electric fields has recently been demonstrated[15]. The viability of this capacitive coupling method for long range coupling is questionable, because of the significant fall off of the interaction strength with distance. To solve this challenge recent proposals suggest the use of a mediator to increase the range. For example, to couple two qubits via a generally faster exchange interaction with a quantum dot as a mediator[19][20]. Some studies indicate that a large multilevel quantum dot will also protect the system from some types of electrical noise due to screening[21].

This thesis is a description of the fabrication and an attempt to test novel device architectures that allow for coupling of multiple spin qubits through a mediator. Utilizing long range coupling not only is a solution to the problem of cross coupling from the control electronics, but also an answer to the problem of fitting the required components close to the qubit. From the perspective of tuning, working with multi-electron quantum dots is a huge advantage, since it eliminates the need for optimization of the geometries for the capability to reach a single electron occupancy. Long range coupling also opens options up for scaling these system towards multi-qubit architectures and error correcting configurations.

1.2 Outline of this thesis

The necessary background as a reference for the reader is presented in chapter 2. The experimental setup used to perform the measurements is then presented in chapter 3. The following chapter 4 gives an overview of the fabrication process as well as the experiences from the development of the fabrication procedure. Chapters 5 and 7 describe the general procedures for transitioning from the cleanroom and into the cryostat, with chapter 6 giving a more detailed description of the most commonly performed tasks during the measurement phase. Finally, chapter 7 gives an overview of the experience from the measurement phase in the dilution refrigerator, highlighting the encountered challenges. The work done for the thesis is then summarized and possible solutions to the problems from chapter 7 are suggested.

2 SPIN QUBITS IN GAAS HETEROSTRUCTURES

The basic building block for for solid state electron Spin Qubits is the electron. To enable the use of physical properties of an electron as a computational tool one needs full confinement and control. The initial confinement to two dimensions is achieved through structure of the material[22]. Electric fields from the metallic gates further restrict the electron movement, confining them to one or even zero dimensional spaces. Single[10], double[23] or multiple electron[11][21] properties and interactions can then be used for forming the basis for quantum computation[4]. This chapter presents the theoretical background for the physical implementation of Solid State Spin Qubits and the basis for the experiment presented in this thesis.

2.1 2DEG and the heterostructure

The main workhorse in the modern day low dimensional experimental solid state physics is the *2 dimensional electron gas*(2DEG). 2DEG is a thin layer of highly mobile electrons that are free to move within a plane. Their movement in the third dimension perpendicular to the plane is quantized and as a result restricted. For this reason 2DEGs are sometimes referred to as *quasi two dimensional*. The main benchmark for the quality of the 2DEG in the material is the *electron mobility*, defined as:

$$\mu = \frac{\sigma}{en_e} \tag{1}$$

where μ denotes the electron mobility, σ is the conductivity, e is the electronic charge and n_e is the electron density in two dimensions. Electron mobility describes how far the electron can travel in the 2DEG without encountering any hard scattering events[2]. Mobilities as high as $3 \cdot 10^7 cm^2/Vs$ can be achieved in a good wafer at cryogenic temperatures[3] which corresponds to a mean free path of $0.3mm$ in GaAs[24]. Very high mean free path is important because in this case transport through the devices measured for this thesis can be considered ballistic.

Wafers with very high quality of 2DEG that are used for spin qubit experiments are grown in a Molecular Beam Epitaxy(MBE) chamber on top of the GaAs substrate as shown in figure 1. GaAs and AlGaAs have nearly the same lattice spacing which does not interrupt the crystalline periodicity allowing for high electron mobilities. The 2DEG is present between the GaAs and the AlGaAs layers. The electrons are confined in a potential well formed on one side by the repulsive barrier due to the conduction band offset of 0.3V between the two layers. The other side is an electrostatic potential formed due to an electric field in the growth direction coming from the partially ionized donors in the n-doped AlGaAs layer. As indicated in the figure, bound state below the Fermi energy will be occupied at low temperatures. Additional layers of AlGaAs encapsulate the dopants that act as scattering centers[22].

[2] scattering angles more than 90°

[3] The mobilities are usually measured at $4K$. Cryogenic temperature refers to the base temperature of a conventional cryostat. Normally around $4K(1.5K)$ for a ^4He cryostat and $< 100mk$ for a $^3He -^4 He$ dilution refrigerator

The sheet of 2DEG is contacted by annealing a gold-germanium eutectic[4] at high temperatures. This provides an Ohmic contact allowing current to travel from electrical connections in the cryostat, into and out of the wafer. These contacts are referred to as "ohmics".

When cooled down to low temperature the 2DEG forms at the interface naturally[5]. Further constriction of the electrons within the sheet requires their local removal. This is done through use of electrostatic gates on the surface of GaAs. By applying negative voltage these gates change the local electric potential experienced by the electrons underneath. This depletes the 2DEG underneath, i.e removes all free electrons from the area.

One could imagine using both the negative depletion gates in combination with accumulation gates with positive voltage that attract electrons and make the effective electrostatic potentials steeper. GaAs lacks a natural insulating oxide which makes this approach problematic. The Schottky barrier between the metal and GaAs is too low at only 0.9V and cannot sustain large positive voltage without tunneling events occurring. One solution is to deposit a small layer of hafnium oxide(HfO_2) underneath the metallic gates using the Atomic Layer Deposition(ALD) technique.

No native insulating oxide also means that charge noise and telegraph[6] noise are present. This happens most likely due to electrons tunneling through the Schottky barrier between GaAs and the metal gates at larger negative voltages[25]. Experimentally there exists a way of offsetting this effect by applying positive bias to depletion gates during cooldown, called bias cooling. One explanation for this, is that at positive bias the local energy minima near the top of the heterostructure are filled with electrons which prevents any additional charge from tunneling in. Several devices with oxide between the GaAs and the metal have been measured, where no switching noise has been seen after cooling down without bias cooling(for experimental details see section 6.1).

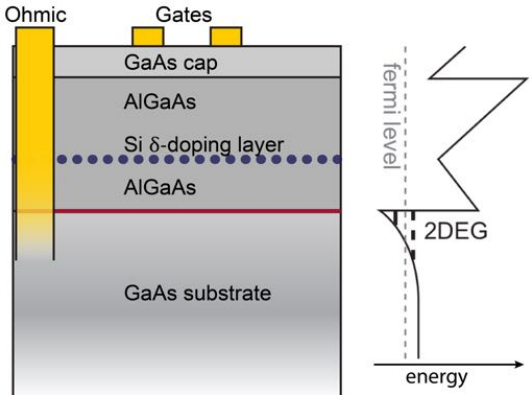


Figure 1: *A schematic plot of a GaAs heterostructure. Layers of GaAs and AlGaAs are grown on top of a GaAs substrate. The 2 dimensional electron gas(2DEG) is present on the interface between GaAs and AlGaAs, confined by the repulsive conduction band offset of the two semiconductors and an electric field from the dopant layer. Electrostatic gates are deposited on the surface to confine the 2DEG by depleting it through electric fields. Ohmic contact to the 2DEG is made though a Germanium-Gold alloy annealed into the material*

[4]alloy of gold and germanium which has a lower melting point than either of the two metals on their own

[5]2DEG is present at low temperatures without need for electric or magnetic fields to accumulate electrons in the quantum well.

[6]called switching noise in the lab

2.2 Quantum dots

Applying voltages to the depletion gates creates constrictions within the 2DEG. When a small number of conduction electrons are confined to a small island of 2DEG a zero dimensional system is formed, called a Quantum Dot. The confinement is of the order of the de Broglie wavelength of the electrons $\lambda = h/2m_e^\star E$ where E is the kinetic energy of the electrons which causes discrete energy levels to form. In this sense quantum dots are often thought of as artificial atoms. Much like in atoms, each energy level is spin degenerate, which means it can be occupied by two electrons of opposite spin[26].

Due to Coulomb repulsion of the electrons inside the dot, the energy required to add an additional electron to the dot with self-capacitance C is the charging energy $E_c = e^2/C$. The energy required to add an additional electron to the next orbital in the quantum dot is called the addition energy, which is defined for a given occupancy of the dot(N):

$$E_{add}(N+1) = E_c + \Delta E = \mu(N+1) - \mu(N) \tag{2}$$

where $\Delta E = E_{N+1} - E_N$ is the energy of the next excited orbital and $\mu(N) = U(N) - U(N-1)$ is the electrochemical potential of the dot. $U(N)$ is the total energy of the dot with (N) electrons which is defined through the constant interaction model[7] and is:

$$U(N) = \frac{(-|e|N + \sum_i C_i V_i)^2}{2C} + \sum_j^N E_j \tag{3}$$

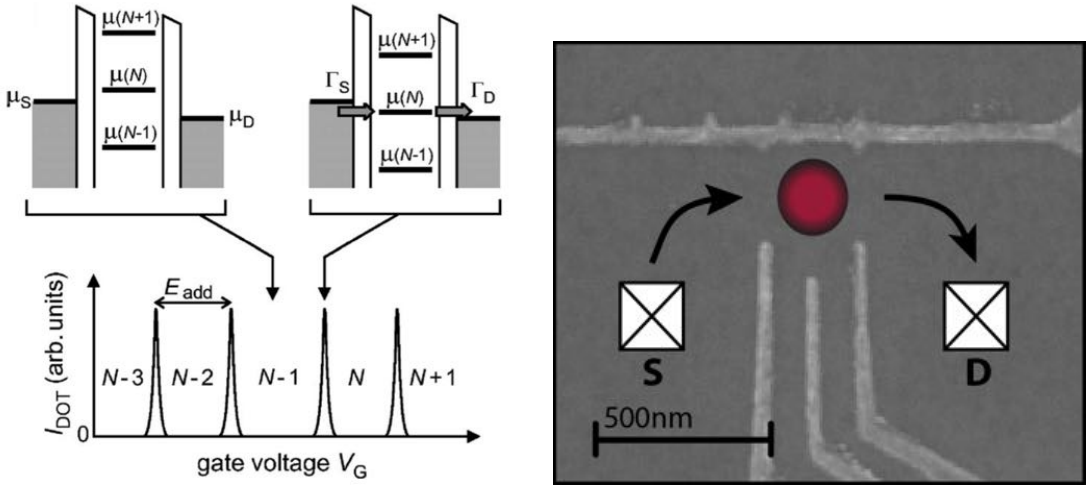
where i denotes the i'th metallic gate and E_j is the energy of the occupied single-particle state $|\psi_j\rangle$[27].

The quantum dot is coupled to a sea of electrons on either side: the source and drain reservoirs. The tunneling to and from the quantum dot is dependent on the alignment of the electrochemical potentials of the leads and the dot. Applying bias voltage between source and drain opens up a bias window. If there is an electrochemical level within the dot that fits within the bias window, tunneling will occur($\mu_S > \mu(N) > \mu_D$). Outside of this condition no current flows through the dot and the quantum dot is in a Coulomb blockade[28]. The electrochemical potential levels can be controlled by applying voltage to the gate electrode, which in our case we usually call a plunger gate. The electrochemical potential depends linearly on gate voltage, so by sweeping the gate it is possible to control both the transport through the dot and it's occupation.

2.2.1 Tuning up a auantum dot and charge sensing

It is possible to use the properties of quantum dots to augment charge sensing. Traditionally the occupation of a dot is measured by measuring transport through the dot. This gives rise to Coulomb oscillations, where the measured current changes as the levels inside the dot pass through the source-drain bias window. A second (sensor) quantum dot in close proximity can sense the change in electric potential as a result of the first quantum dot changing occupancy. This change acts effectively as gate voltage for the sensor dot changing the conductance through it. If the sensor dot is tuned to a regime where it is very sensitive to any change in gate voltage, the conductance difference can be accurately measured assigning a certain target occupation to a certain conductance level. This techniques has been originally developed for a Quantum Point Contact[29] and later shown to be possible for a quantum dot acting as a sensor[30].

[7] constant interaction model assumes that Coulomb interaction among the electrons in the dot and the environment are expressed through a single capacitance, which is the sum of all capacitances in the system. Additionally it assumes that the level spectrum is independent of the number of electrons



(a) (b)

Figure 2: *Conductance through a quantum dot. a) Top left: No energy levels are within the bias window and the current through the quantum dot is suppressed, i.e. Coulomb blockade. Top right: An energy level is within the bias window and the tunneling current between the source and drain reservoirs is possible. Bottom: A plot of the current through a quantum dot as a function of V_G. A relative occupation of the quantum dot can be determined. Figure from [26] 2(b) Micrograph of a part of a device used to create the quantum dot by depleting the 2DEG under the electrostatic gates(light gray). Current is measured from source to drain electrode.*

Measuring conductance is generally slow, since one need a large number of averaging to get a discernible signal. For fast measurement of the dynamics of the system a new generation of charge sensing has been developed that uses impedance mismatch at a resonance frequency of a tank RLC circuit and the quantum channel. This technique is called radio frequency reflectometry[31] and is described in more detail in section 3.4. The reflectometry data presented in this chapter is equivalent to the data that can be taken with the charge sensing technique described above.

To tune up a quantum dot, one follows a simple algorithm illustrated in figure 3. To do this efficiently requires some experimental experience, however the thought process behind it is rather intuitive. The first step is usually an attempt to reduce the number of variables in the system. In our designs this is done though defining a static depletion region that serves as a base for all subsequent tunings, i.e setting the global "backbone" gate. This is done by measuring transport across the gate and increasing the gate voltage until electrical transport is no longer possible. After the "backbone" is set, the left and right tunnel barriers are swept for different values of the plunger gate, until coulomb oscillations are seen as shown in figure 3.

2.2.2 Double quantum dots and multiple quantum dots

Now lets extend the system described in the previous chapter to two quantum dots positioned directly near each other(in series). For this system plunger gates V_L and V_R control the electrochemical potentials of left and right dot respectively through capacitive coupling.

Conductance for this system can be measured for V_R as a function of V_L as shown in figure 4. This plot is commonly referred to as a charge stability diagram. Current flow is only possible at points where the energy levels of both quantum dots align within the bias window[32]. For a sufficiently large bias window one would see a set of lines, i.e. Coulomb peaks, as the energy levels enter and exit the bias window and electrons are able to tunnel through. Similarly to a single dot, each line indicates that the number of electrons in the ground state changes by one.

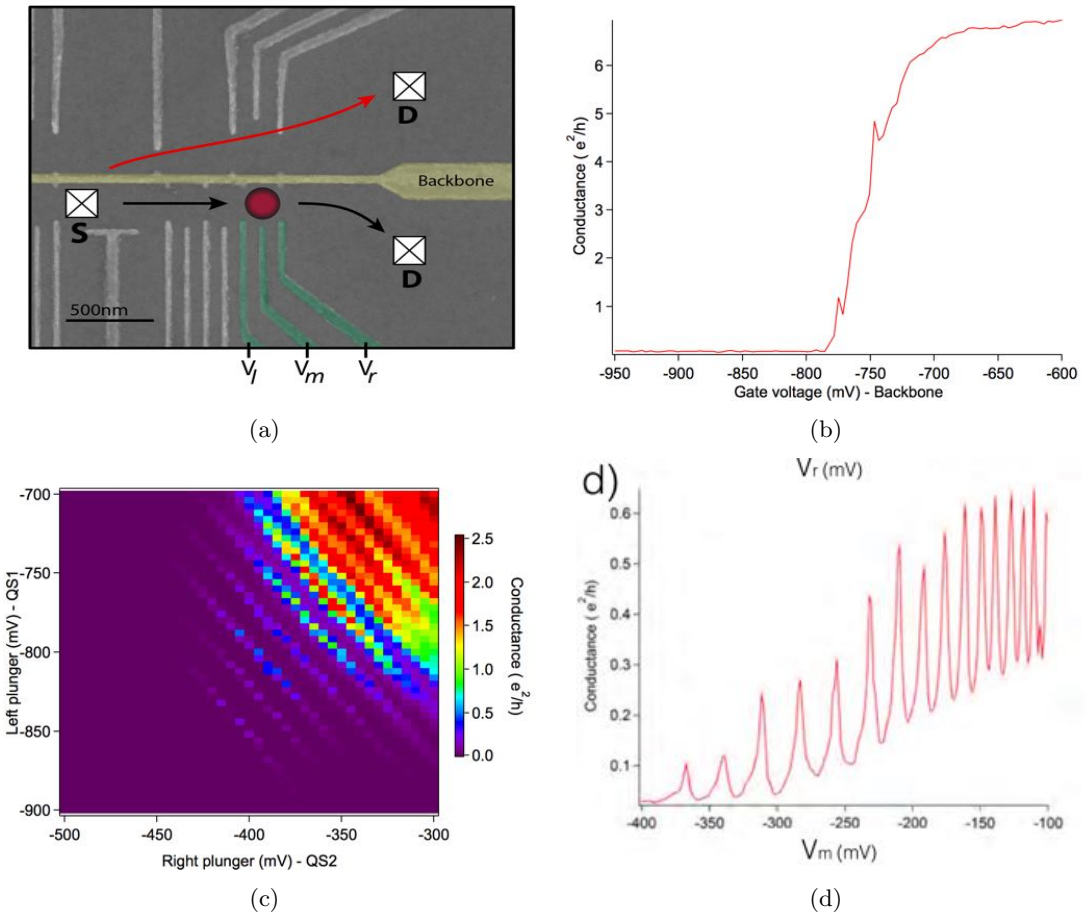


Figure 3: *Tuning a Quantum dot. First, the backbone gate(yellow) is ramped to negative voltage and depletes the 2DEG. DC transport is measured along the red arrow. When the backbone is pinched-off a quantum dot is tuned up using the depletion gates V_l, V_r and V_m (green) while measuring transport through the quantum dot region(black arrows). 3(a) Micrograph image of the device. Circle indicates the position of the quantum dot, current is measured between the Ohmic contacts: source and drain. 3(b) Pinch-off curve of the backbone. When measuring transport with source and drain on either side of the backbone (red arrow), applying more negative voltage on the gate depletes the underlying 2DEG and the conductance drops to zero. 3(c) Measuring transport on either side of the quantum dot (black arrows) as a function of the voltage on the tunnel barrier gates V_l and V_r for a static V_m. The conductance goes from a continuum to discrete quantization as the tunnel barrier height increases. 3(d) Coulomb oscillations of a quantum dot. Transport through a quantum dot is measured as a function of the middle plunger gate V_m. The middle gate changes the chemical potential of the energy levels in the dot bringing them in and out of alignment with the source-drain bias window as illustrated in figure 2.*

If the bias window is small, transport is only possible at the crosspoints as it is exactly where the energy levels in both quantum dots align.

In a model situation where both quantum dots are completely uncoupled, the plot will show perfectly horizontal and vertical lines only. In this case both gate voltages only influence the chemical potentials within the corresponding quantum dot. This is however almost never the case.

In a realistic system V_R will capacitively couple to the chemical potential of the left quantum dot and vice versa. As a result the lines in the charge stability diagram will be tilted as a change in occupancy of one dot influences the electrochemical potential of the one next to it, as shown in figure 4(a). Each cross point will be split into so-called *triple points*. At each triple point

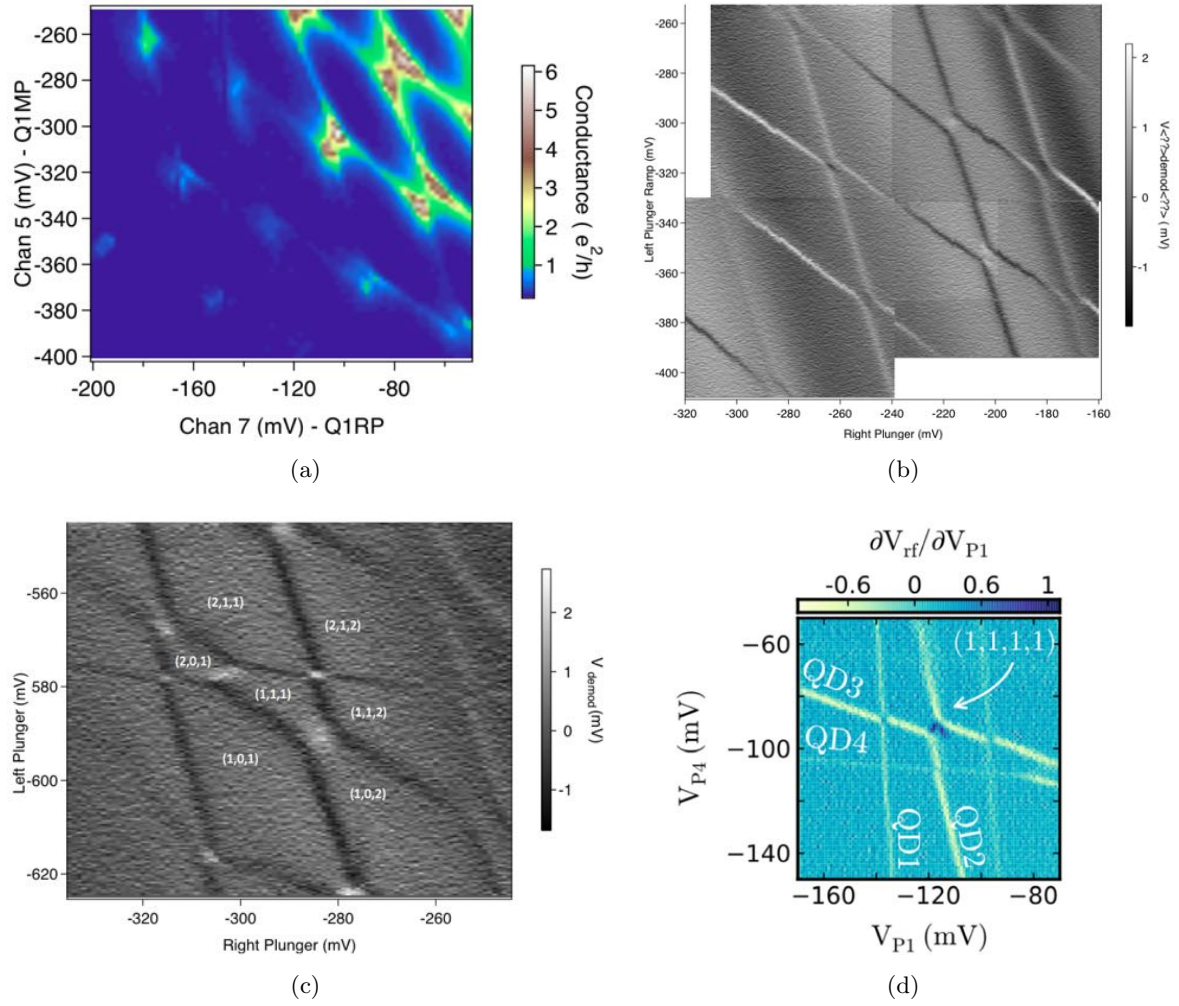


Figure 4: *Multiple quantum dots. 4(a) A double quantum dot measured in DC-transport. The conductance is higher where more energy levels fit into the bias window. As the quantum dots become smaller, the energy levels become farther apart due to an increase in self-capacitance and fewer energy levels fit into the bias window. This happens at more negative values of the plunger gates. 4(b) Charge stability diagram measured for a double dot in charge sensing. A differential plot of V_{right} as a function of V_{left}, each line signifies a change in occupation by one. Due to a finite capacitance between the two quantum dots, each crossing is split into two triple points. Finite inter-dot tunneling also bends the transition lines around the crosspoints. 4(c) Charge stability diagram measured for a triple quantum dot as a function of V_{right} and V_{left} for a fixed V_{middle}. Additional quantum dot is seen by presence of an additional set of transitions with a different slope, controlled mostly by the middle plunger. 4(d) Experimental data from [33] for 4 quantum dots in series for plunger 1(P1) as a function of plunger 4(P4). 4 different slopes of transition lines indicate presence of 4 quantum dots.*

there are three different charge states that are energetically degenerate. The distance between each set of triple points is determined by the capacitance between the quantum dots[32]. If the tunnel coupling is large, the lines near the triple points will start to bend as seen in figure 4(b).

With low bias windows electron transition line will no longer be visible when measured in transport due to slow tunneling. In charge sensing however, the transitions will still be mapped out due to much higher sensitivity. This is particularly important when considering systems with more than two quantum dots in series. Tunneling will be heavily suppressed and will require measuring for longer times than experimentally viable.

The same principles apply with additional quantum dots in series. Additional transition signatures in form of additional sets of lines will appear on the charge stability diagram. In the same fashion triple[16] and even quadruple[33] quantum dot arrays have been realized.

By going to very negative voltage values[8] in the charge stability diagram, quantum dots can be completely emptied of electrons. This allows for unambiguous determination of the occupation of the quantum dot system.

2.2.3 Pauli spin blockade in double quantum dots

A single energy level inside a quantum dot can be occupied by two electrons. These electrons in a single orbital must have an opposite spin according to the Pauli principle, that states that the wavefunction of a two electron state has to be anti-symmetric. This state is called a singlet. For a triplet state, both spins are aligned, and since the Pauli exclusion principle still holds, one of the electrons must occupy an excited orbital. As a result there is an energy difference J commonly referred to as exchange splitting, between the states $(0,2)S$ and $(0,2)T$[9].

In a presence of a large tunnel coupling t_c the electron wavefunction is no longer localized to a single quantum dot. This means that a $(1,1)$ state, where there is one electron in each dot, can also be in a singlet- or a triplet-like state, with spins either aligned or opposite to each other. The exchange splitting in this system depends strongly on t_c and the charging energy of a single quantum dot E_C and can be made arbitrarily small with proper tuning of the electrostatic gates.

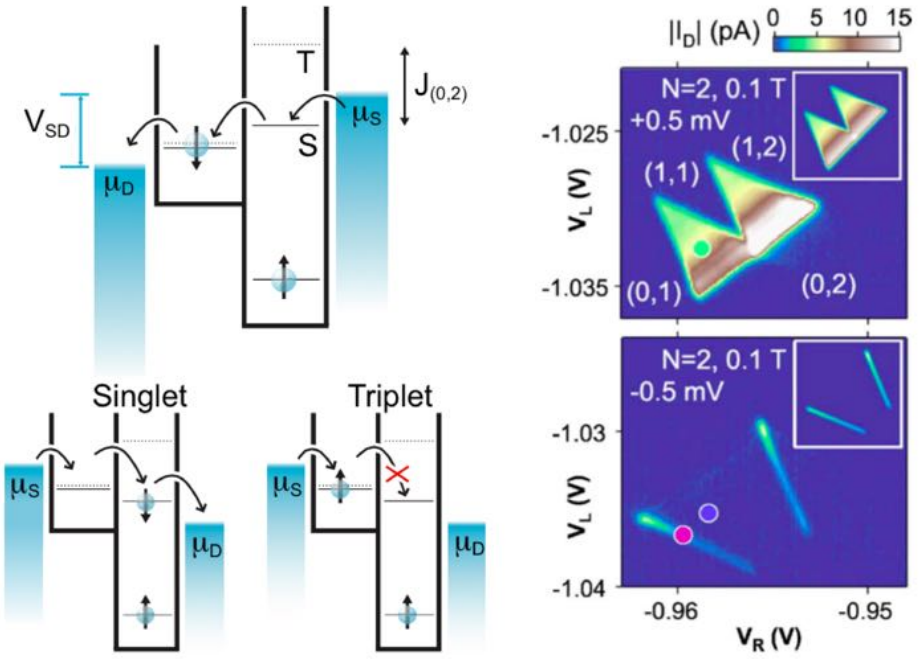
Since the electron spin is conserved during tunneling, the exchange splitting can play a major role in the electron transport as seen in lateral quantum dots by Johnson, et al.[34]. In DC transport the current will be rectified in a phenomenon called Pauli spin blockade.

Imagine a double dot in a $(1,1)$ state and a single electron is tunneling from the left dot to the right dot due to the applied bias. The system is tuned such that there is always a single electron in the right dot. Because of the small exchange splitting in the $(1,1)$ charge configuration, there is almost no difference energetically between loading a $(1,1)S$ or a $(1,1)T$ state. If the initial configuration is a singlet-like $((\uparrow,\downarrow))$, after a tunneling event, the electron from the left dot will for a singlet-like $(0,\uparrow\downarrow)$ in the right dot and will be able to further tunnel through the lead. In an opposite scenario, where the initial state is a triplet-like $((\uparrow,\uparrow)$ the tunneling is not possible, since $(0,\uparrow\uparrow)$ triplet-like state is energetically inaccessible. The bias prevents the electron from tunneling backwards so the current will effectively drop to zero until a spin flip occurs[34]. This is illustrated in figure 5. By applying a reverse bias the spin blockade is lifted and current flow is again possible.

Using charge sensing it is possible to measure changes in occupation of the double dot. Utilizing Pauli spin blockade is essential in a technique called spin-to-charge conversion, where one can measure the state of the system, singlet or triplet, by looking at whether the tunneling event has occurred or not through charge sensing.

[8] this can be offset by bias cooling as described in section 6.1

[9] in this case we assume only two electrons in the double dot. $(0,2)$ refers to the right quantum dot occupied by two electrons and similarly $(1,1)$ refers to both quantum dots each containing a single electron



(a) spin blockade (b) bias triangles

Figure 5: *Spin blockade. 5(a) Top: electron tunneling through a double dot at negative bias. The chemical potentials within the double quantum dot are aligned so transport is possible. Bottom left: Electron tunneling through a double dot at positive bias. Exchange splitting between singlet and triplet* $(1,1)$ *charge state is negligible, so electrons in both spin orientations can be loaded into the left quantum dot. If the loaded state is anti-parallel with the electron in the right dot the tunneling through the double dot is possible. If the loaded state is parallel with the electron in the right dot, the tunneling is suppressed due to the* $(0,2)T$ *state being inaccessible in energy. Figure from [35] 5(b) Bias triangles showing current flow(green circle) around the triple points for two neighboring transitions. At the transition from* $(1,1)$ *state to* $(0,2)$ *the current is heavily suppressed(blue circle) due to Pauli spin blockade at negative bias and is only possible at the sides of the bias triangles due to the exchange of electrons with the leads(pink circle). Figure adapted from [34]*

2.3 Qubits

The basic building block of quantum information is called a *quantum bit*, or *qubit*, similarly to the classical bit of information. Just like the classical bit, it can be in a state 0 or 1, denoted in the Dirac notation as $|0\rangle$ and $|1\rangle$, but unlike the classical bit it can also be in a linear combination of states, or superposition:

$$|\Psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{4}$$

where α and β are complex numbers. When the qubit is measured, with the probability of $|\alpha|^2$ it will be in a state $|0\rangle$ and with a probability of $|\beta|^2$ in a state $|1\rangle$, satisfying the relation:

$$|\alpha|^2 + |\beta|^2 = 1 \tag{5}$$

since the probabilities must sum to one. Any qubit state is thus a unit vector in a two dimensional complex vector space spanned by the orthonormal *computational basis* states $|0\rangle$ and $|1\rangle$.

A handy visualization tool for the state of a qubit in any given superposition is a three dimensional unit sphere called the Bloch sphere(figure 6). Since the sum of the square of the coefficients is equal to one, we can rewrite the state of a qubit using spherical coordinates[36] into:

$$|\Psi\rangle = \cos\frac{\theta}{2}\alpha\,|0\rangle + e^{i\phi}\sin\frac{\theta}{2}\,|1\rangle \tag{6}$$

Any single qubit operation can be intuitively visualized on the Bloch sphere. For example a NOT gate exchanges states $|0\rangle$ and $|1\rangle$ which is effectively a rotation around the x axis by π radians. When measuring a quantum superposition, it will collapse into either $|0\rangle$ or $|1\rangle$.

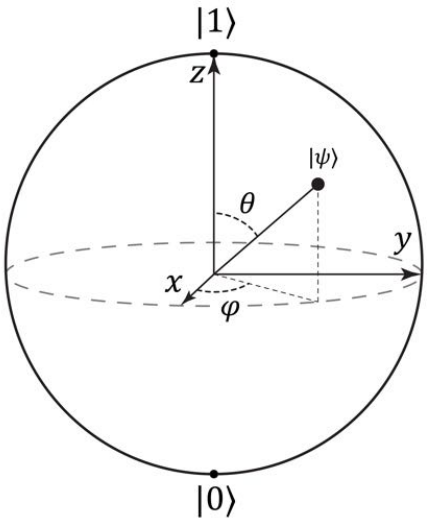


Figure 6: *A Bloch sphere representation of the computational basis states of a qubit. Any single qubit operation can be visualized as the rotation around the axes in the sphere*

This is called a projective measurement. This is why an individual measurement of the system reveals nothing about the quantum state. To determine the probability of collapsing into the measurement state[10] one needs to repeat the measurement on an ensemble of identically prepared qubits[36].

[10]measurement basis can be chosen at random. To obtain α and β one would need to chose the measurement basis to be the computational basis

2.3.1 Loss-DiVincenzo qubits

Using an electron spin for quantum computation has been first suggested by Daniel Loss and David DiVincenzo in 1998[10]. This idea is what is now referred to as Loss-DiVincenzo qubit(LD-qubit) has kicked off the field of spin qubits. It uses the electron spin states $|\uparrow\rangle$ and $|\downarrow\rangle$ as computational basis, the qubit states $|0\rangle$ and $|1\rangle$.

Full control of such qubit is achieved through electron spin resonance(ESR). A large magnetic field B_0 is applied which splits the states $|\uparrow\rangle$ and $|\downarrow\rangle$ by the Zeeman energy. A small oscillating magnetic field applied on resonance with the spin-flip transition energy and perpendicular to B_0 drives rotations around the x and y axis on the Bloch sphere. In the rotating frame the driving field is static. The rotation axis is controlled solely by the phase of the driving field. Two qubit gates can be introduced by introducing exchange interactions with the neighboring quantum dots[27].

LD qubits have been implemented [26] and singe shot readout have been demonstrated[37]. The biggest challenge for implementation of LD qubits is in the generation of the oscillating magnetic fields. Some approaches utilize a stripline manufactured directly on top of the quantum dot[12]. However this approach is impractical for further scaling because of the space required and the heat output of several neighboring striplines. Using electric dipole spin resonance (EDSR) to generate magnetic fields via the spin orbit interaction has also been demonstrated[38], however this approach is mostly pursued in materials with stronger spin orbit interaction.

One of the more promising approaches for GaAs has recently been demonstrated by introducing nanoscale magnetic materials onto the device[39]. This creates a small magnetic field gradient and the electron can then be shaken electrically inside the gradient making it feel an oscillating field. Because of ease of electrical control, each qubit can get a unique resonance frequency. This makes it easy to individually address the qubits in a multi-qubit configuration by simply navigating in the frequency space. Devices designed for this thesis were specifically designed with a possibility of placing micromagnets in this way.

2.3.2 Singlet-Triplet qubits

A so called Singlet-Triplet qubit is implemented using 2 electrons in two neighboring tunnel coupled quantum dots that are described in section 2.2.2. Two electrons in the same dot within a double dot can be treated simply as two electrons in a single dot with the second dot not being present at all[26]. In this case there are 4 possible states[11]:

$$S(0,2) = (|\uparrow_2\downarrow_2\rangle - |\downarrow_2\uparrow_2\rangle)/\sqrt{2}) \tag{7}$$

$$T_+(0,2) = (|\uparrow_2\uparrow_2\rangle\,, \quad T_0(0,2) = (|\uparrow_2\downarrow_2\rangle + |\downarrow_2\uparrow_2\rangle)/\sqrt{2}), \quad T_+(0,2) = (|\downarrow_2\downarrow_2\rangle \tag{8}$$

one singlet states and 3 triplet states. Similarly for one electron in each dot:

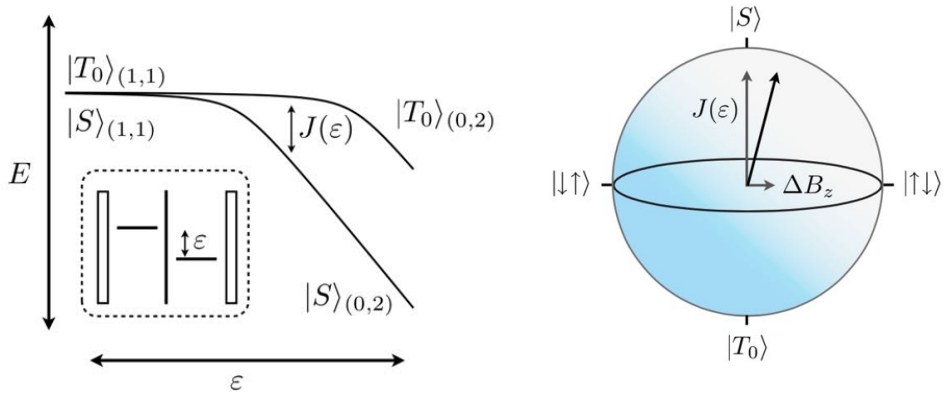
$$S(1,1) = (|\uparrow_1\downarrow_2\rangle - |\downarrow_1\uparrow_2\rangle)/\sqrt{2}) \tag{9}$$

$$T_+(1,1) = (|\uparrow_1\uparrow_2\rangle\,, \quad T_0(1,1) = (|\uparrow_1\downarrow_2\rangle + |\downarrow_1\uparrow_2\rangle)/\sqrt{2}), \quad T_+(1,1) = (|\downarrow_2\downarrow_2\rangle \tag{10}$$

The electrochemical potentials of both quantum dots are aligned and the occupation is controlled electrically through the detuning parameter(tilt) $\epsilon = \eta\Delta V$ for $\Delta V = \sqrt{\Delta V_L^2 + \Delta V_R^2}$, where ΔV is the voltage detuning and subscripts L and R denote the electrostatic gate. η is

[11] this case looks at a situations wit two electrons in the right dot. A situation with the two electrons in the left dot is treated identically.

the lever arm which can be calibrated through DC measurement of the transport through a spin blockaded double dot[35]. In the presence of a finite tunnel coupling charge states $(1,1)$ and $(0,2)$ hybridize and since the interdot electron transitions preserve spin, the singlet and triplet states will only couple to singlet and triplet states respectively. Because of a large difference in exchange splitting between $(1,1)$ and $(0,2)$ the singlet-triplet qubit has a level structure shown in figure 7.



(a) ST anticrossing

(b) Bloch sphere representation

Figure 7: *Singlet Triplet qubit. 7(a)Charge states* $(1,1)$ *and* $(0,2)$ *hybridize in the presence of a finite tunnel coupling. Symmetric state* $T_0(1,1)$ *and antisymmetric state* $S(1,1)$ *are chosen as the logic states* $|0\rangle$ *and* $|1\rangle$*. 7(b) Bloch sphere representation of the logic states in a singlet-triplet qubit. The rotation in the xy plane on the Bloch sphere is driven by the exchange splitting* $J(\epsilon)$*. Rotations between logic* $|0\rangle$ *and* $|1\rangle$ *are performed by a magnetic field difference* ΔB_Z *between the two electrons[40]. Figures adopted from [27]*

At a finite magnetic field triplet states $|T_+\rangle$ and $|T_-\rangle$ are split away from the triplet ground state $|T_0\rangle$ by the Zeeman energy ΔE_Z and can be arbitrarily far away from the singlet and triple ground state anticrossing. At this stage they act as leakage states and can be avoided by moving fast in ϵ with respect to their anticrossings.

Symmetric state $T_0(1,1) = (|\uparrow_1\downarrow_2\rangle + |\downarrow_1\uparrow_2\rangle)/\sqrt{2})$ and antisymmetric state $S(1,1) = (|\uparrow_1\downarrow_2\rangle - |\downarrow_1\uparrow_2\rangle)/\sqrt{2})$ with magnetic quantum number $m = 0$ are used as the logic states $|0\rangle$ and $|1\rangle$ for ST(singlet-triplet) qubit. The rotation in the xy plane on the Bloch sphere is driven by the exchange splitting $J(\epsilon)$. Rotations between logic $|0\rangle$ and $|1\rangle$ are performed by a magnetic field difference ΔB_Z between the two electrons[40]. This gives universal control of the qubit as has been experimentally shown by Petta, et al.[41].

Initialization and readout are done via the detuning axis, ϵ. By moving to the "right" in the energy diagram a singlet $(0,2)$ state is prepared. Moving into the $(1,1)$ region turns on the rotations around the z axis. When moving back into the $(0,2)$ region fast, only a singlet state will be able to tunnel into a $(0,2)$ charge configuration while the triplet will be stuck in $(1,1)$. This is easily picked up by the charge sensor. Single shot readout has been successfully demonstrated for this qubit by Barthel, et al[42].

The main difficulty when operating Singlet-Triplet qubits is in introducing a magnetic field gradient. Among other approaches this has been done through the use of a micromagnet in a similar fashion to a LD qubit.

2.3.3 Exchange-only qubits

The idea for using 3 electron spins for computation was first suggested by D. DiVincenzo, et al[11]. A fundamental advantage of the proposed scheme is the ability to control the qubit purely by way of electrical pulses as opposed to introducing ways of creating magnetic field gradients or oscillating magnetic fields. A functional exchange-only qubit out three electron spins in three tunnel coupled quantum dots has been implemented experimentally by Laird, et al[14] and further improved by changing to a linear design by Medford, et al[16][43].

There are 8 possible 3 electron states, four with spin $S = 1/2$ and another four with $S = 3/2$. If an external magnetic field is applied, this will split these eight states into four subspaces with spins that project into $m_S = \pm 3/2, \pm 1/2$.

For the qubit we choose to work in the $S = 1/2$, $m_S = +1/2$. The triple quantum dot is controlled via gate voltages on left and right plungers, V_l and V_r respectively. The occupation is defined through the usual convention (N_l, N_m, N_r) and is controlled by the detuning parameter:

$$\epsilon = \frac{(V_r - V_r^0)}{2} - \frac{(V_l - V_l^0)}{2} \tag{11}$$

where $\epsilon = 0$ is set in the symmetry point for a $(1, 1, 1)$ occupation. In a linear geometry the exchange interaction is possible between the left-middle, $J_l(\epsilon)$, and middle-right, $J_r(\epsilon)$, quantum dots. At the symmetry point where $J_l = J_r$ we choose the logic qubit states to be the singlet like:

$$|0\rangle = \frac{1}{\sqrt{6}}(|\uparrow\uparrow\downarrow\rangle + |\downarrow\uparrow\uparrow\rangle - 2\,|\uparrow\downarrow\uparrow\rangle) \tag{12}$$

and the triplet like

$$|1\rangle = \frac{1}{\sqrt{2}}(|\uparrow\uparrow\downarrow\rangle - |\downarrow\uparrow\uparrow\rangle) \tag{13}$$

Logic states can be mapped adiabatically into the singlet and triplet-like states in the $(1, 0, 2)$ and $(2, 0, 1)$ regions which additionally opens up exchange splittings $J_l(\epsilon)$ between the singlet-like $|S_l\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\uparrow\rangle - |\downarrow\uparrow\uparrow\rangle)$ and triplet-like $|T_l\rangle = \frac{1}{\sqrt{6}}(|\downarrow\uparrow\uparrow\rangle + |\uparrow\downarrow\uparrow\rangle - 2\,|\uparrow\uparrow\downarrow\rangle)$, and $J_r(\epsilon)$ between the singlet-like $|S_r\rangle = \frac{1}{\sqrt{2}}(|\uparrow\uparrow\downarrow\rangle - |\uparrow\downarrow\uparrow\rangle)$ and triplet-like $|T_l\rangle = \frac{1}{\sqrt{6}}(|\uparrow\uparrow\downarrow\rangle + |\uparrow\downarrow\uparrow\rangle - 2\,|\downarrow\uparrow\uparrow\rangle)$ as shown in figure 8. On a Bloch sphere these exchange interactions are 120°apart and allow full qubit control electrically, by shifting in detuning[44]. States with $S = 3/2$ are nearby in energy but require a magnetic field to drive transitions to and from this subspace, and thus can be ignored in this context.

Qubit operation is done through turning the exchange on and off while at the symmetry point to drive qubit rotations. Readout is performed through a similar scheme to the ST qubit, utilizing spin-to-charge conversion by restricting tunneling for the triplet like state into the outer dots. Since the system is symmetric, this can be done for both middle-left and middle-right quantum dots. Demonstration of universal control and single-shot readout has been performed successfully by Medford, et al.[16].

2.4 Coupling multiple spin qubits

So far the qubits types described in the thesis focused primarily on control of a single qubit. As well as these qubit types can perform all single qubit gates, it is still not enough for universal quantum computation, criteria for which are described by D. DiVincenzo in 2000[4]. One of the criteria is to be able to perform a universal set of quantum gates. There are many sets out there that have been developed by mathematicians around the world. One of the simplest is the ability to perform **all** single qubit gates, i.e. ability to reach any point on the Bloch sphere, and a **single** conditional two qubit gate, be it a Control NOT(cNOT) or a Control Phase(cPHASE).

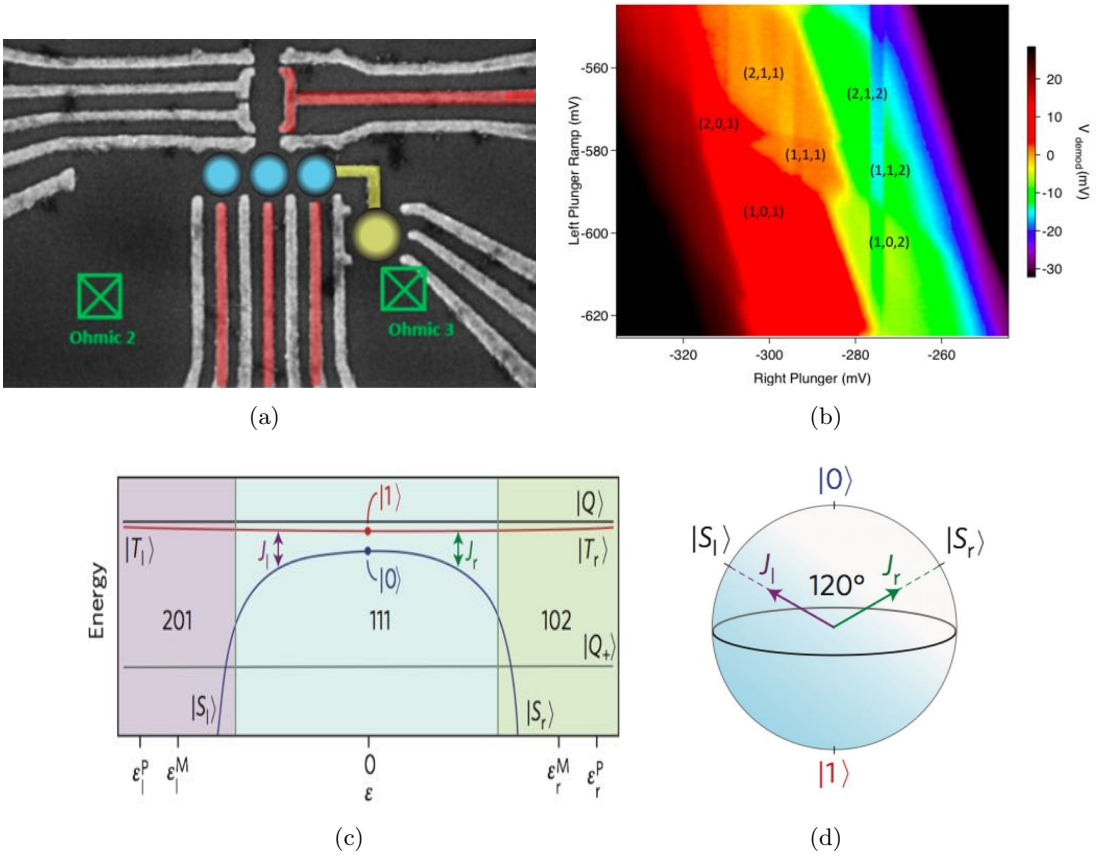


Figure 8: *Exchange only qubit.8(a) Micrograph image of the device. Circles indicate the positions of the quantum dots(blue) and the charge sensor dot(yellow), transport is measured between the Ohmic contacts(S-D). 8(b) Charge stability diagram measured by reflectometry. The absolute occupation can be measured by completely emptying the quantum dot from electrons and then counting up the transitions. 8(c) Level structure of a triple quantum dot in the* $S = 1/2$, $m_S = \pm 1/2$ *subspace. Singlet like* $S(1,1,1)$ *and triplet like* $T(1,1,1)$ *states are chosen as computational basis* $|0\rangle$ *and* $|1\rangle$ *respectively. Moving in detuning towards the hybridized states in charge states* $(2,0,1)$ *and* $(1,0,2)$ *opens up respective exchange splittings* J_l *and* J_r *that can be used to drive qubit rotations. Leakage states* $|Q\rangle$ *and* $|Q_+\rangle$ *are* $S = 3/2$ *and do not couple directly. Figure from [16] 8(d) A Bloch sphere comprised out of logic states* $|0\rangle$ *and* $|1\rangle$ *of an exchange only triple-dot qubit. Rotations on the Bloch sphere are driven by full electrical control using the two exchange axis 120° apart making full single-qubit control possible. Figure from [16]*

A cNOT gate is a conditional operation of the *target* qubit which depends on the state of the *control* qubit. An example would be if the target qubit changes from $|0\rangle$ to $|1\rangle$ if and only if the control qubit is in the state $|0\rangle$. A CPHASE is essentially the same, but with the qubit phase being changed conditionally. There are two main mechanisms suggested for coupling two qubits: capacitive coupling and exchange coupling.

Capacitive coupling utilizes the spatial properties of the wavefunction of the state. For a ST qubit the weight of the wavefunction will be different depending on which logic state the system is in. In a triplet like $T(1,1)$ state, the wavefunction is mostly evenly distributed across the double quantum dot, but in a singlet like $S(0,2)$ state, the weight of the wavefunction is shifted to the side[15]. Thus at a nonzero J in the qubit it will impose different electric fields on the second qubits depending on it's state, i.e. charge configuration. Since J is controlled though electric field, the precession of the second qubit will change depending on the configuration of first qubit, which allows for an implementation of a cPHASE gate. This has been shown

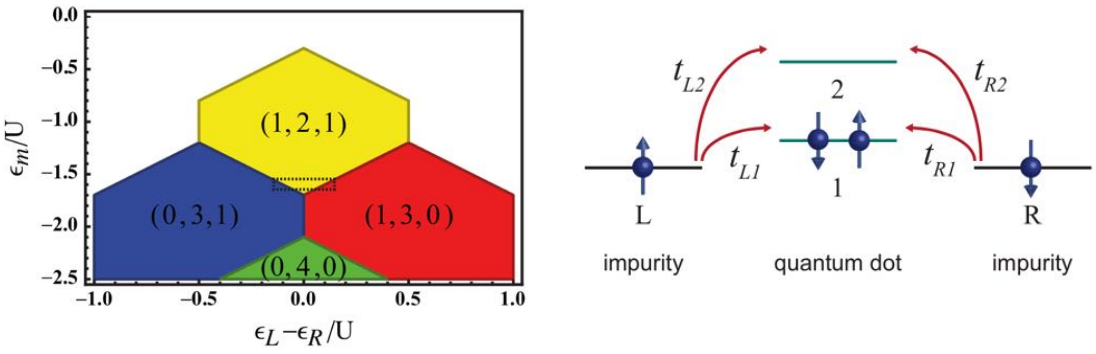
experimentally by M. Shulman, et al[15].

2.4.1 Long range coupling

Another of the famous requirements for physical implementation of a quantum computer is scalability[4]. Spin qubit systems are normally implemented with nanosized electrostatic gates in semiconductors, which promises great scalability. Unfortunately, the scalability criteria is severely limited by the crude implementation of control and measurement equipment that is required at the current stage of this technology. This includes wires having to be lead down to the device from macrosale and auxiliary quantum systems having to be placed nearby for sensing and readout. Additionally, in a perfect quantum computer all qubits are entangled, which considering the 2 dimensional nature of the quantum devices that are being made currently presents a great challenge.

Long range coupling of spin qubit systems is of great interest not only because of the scalability difficulties. Coupling via exchange interaction is generally preferred because it is fast, robust and is protected against multiple types of noise, additionally it can be controlled electrically[11][44][40]. Unfortunately exchange interaction, being a form of long range Coulomb interaction, decays exponentially with distance[20]. To increase the range of the exchange interaction a mediator is needed. One of the proposed mediator systems is an additional quantum dot.

Long range tunneling between the outer quantum dots in a triple dot linear array has been experimentally shown recently[45][46]. The system is configure such that the middle dot levels are far detuned from the resonance of the outer dot levels so that sequential tunneling is suppressed. By applying a microwave excitation to the system electron tunneling between the outer quantum dots is possible through a virtual occupation of the middle dot. In this case the tunneling is assisted by photons(PAT, photon assisted tunneling) when the microwave excitation hits the resonance of a frequency that matches the detuning between the neighboring quantum dots $\epsilon_0 = nh\nu$, where ϵ_0 is the detuning, h is the plack constant, ν is the microwave frequency and n is an integer.



(a) (b)

Figure 9: *Srinivasa, et al[20] scheme for long range coupling via an RKKY-like exchange interaction. 9(a) The system is tuned to a* $(1,2,1)$ *charge state with the nearest accessible charge states being* $(1,3,0)$ *and* $(0,3,1)$*. The operation point is indicated by the dashed rectangle. 9(b) Energy level diagram at the operation point. An effective exchange interaction between the outer quantum dots is possible, with magnitude depending on the tunneling amplitudes and energy detunings, which can be controlled electrostatically. The relevant tunneling amplitudes are shown. Reverse tunneling amplitudes correspond to the complex conjugate of the respective tunneling amplitude. Figures adapted from [20].*

Another approach has been proposed by Srinivasa, et al[20]. In this proposal a multilevel

quantum dot can serve as a mediator for a RKKY-like exchange interaction of the two single-electron spin qubits. The system is setup akin to a triple dot(see figure 9) and the barriers are tuned, by applying voltages to the electrostatic gates, to a regime where sequential tunneling is impossible. In a weak tunneling regime, where tunneling is heavily suppressed from the side quantum dots to the middle quantum dot, and the exchange $J_{Li} = J_{Ri} = 0$, an effective exchange interaction between the outer quantum dots is possible:

$$J = -2(\frac{t^{\star}_{R2} t_{R1} t^{\star}_{L1} t_{L2}}{\Delta_R \Delta_M \Delta_L} + c.c.) \tag{14}$$

and is dependent on the tunneling amplitudes[12], the energy difference between the qubit (doubly occupied state for the middle dot) levels and the intermediate states $(1, 3, 0)$ and $(0, 3, 1)$ relative to an energy origin E_0, which is defined for the system in a $(1, 2, 1)$ charge state in a weak tunneling regime. Experimentally, tunneling amplitudes can be controlled by changing gate voltages, and the energy level differences can be controlled via detuning. This allows for J to be tuned with the lower limit being set only by the tunnel coupling[20]. Using a multilevel quantum dot, the energy difference in the middle dot Δ_M can be tuned in a discreet fashion[20]. In a large multi-electron quantum dot, the step size can also be adjusted, because the level spacing changes with the number of electrons in the quantum dot[26]. Some studies also indicate that such exchange coupling will also be protected against some types of noise due to the screening of the Coulomb interactions by the large number of paired electrons inside the quantum dot[21].

Independently S. Mehl and D. DiVincenzo are also working on coupling multiple spin qubits via a quantum system[19]. In their approach they find that efficient entanglement of two ST_0 qubits is possible if a large discrete quantum system is used as a mediator. One of the interesting results is the effect of parity, i.e. if the quantum state is unoccupied or doubly occupied versus single occupied. An entanglement operation via an even occupied state can be performed by just one entangling gate with gate fidelities greater than 10^{-3}, which is a requirement for surface code error correction[47]. For entangling via a single occupied quantum state requires at least two entangling gates. Additionally, the system in the single occupied regime is much more susceptible to errors.

The core assumption is that the physical parameters of both qubits are identical and that they are equally coupled to the quantum state. In case of different coupling, for a state with an even occupation these effects can be corrected by changing the $4th$ order exchange term in the Hamiltonian to reflect the asymmetric tunneling rates. For a state with an odd occupation this is not possible, in fact for strong asymmetry the system no longer satisfies the requirement for surface code error correction[19].

Another major error generating mechanism is the difference in the local magnetic field gradient magnitude due to hyperfine interaction. Similarly to the asymmetric exchange, the single occupied quantum state is critically affected, while the double occupied or empty state is protected against these fluctuations, since the states with unpaired electrons are only virtually occupied. Local shifts in magnetic field gradient magnitudes can reach $5mT$ for GaAs which results in error rates breaking the surface code threshold. It is possible to reduce the error rate to below the threshold by using spin-less materials or by adjusting gate sequences in a feedback loop as recently demonstrated by Shulman, et al.[48].

[12] complex conjugate of the tunneling amplitude corresponds to reversing the tunneling direction

3

EXPERIMENTAL SETUP

This section describes the experimental setup used for low temperature Spin Qubit experiments. It covers the general wiring of the cryostat as well as the measurement tools and techniques, and a brief description of the data acquisition setup.

3.1 Triton dilution refrigerator

Temperature is of utmost importance when working with quantum phenomena. Thermal energy is a contributor to noise and decoherence effects through a number of processes such as lattice vibrations and energy level broadening. Just to work with 2 dimensional quantum dots, the temperature should be low enough to form a 2DEG. Higher temperatures also contributes to random excitations within the level structure of the dots leading to charge noise. Spin relaxation is also dependent on temperature, with higher temperatures leading to smaller characteristic T_1 times[49].

To avoid these problems as best as possible, the samples are being cooled down to very low temperature, typically with base temperatures around 20mK. This is done using ^{3}He-^{4}He dilution refrigerators supplied by Oxford Instruments - Triton200.

3.1.1 Dilution refrigeration

The principle behind dilution cooling is as follows. At cryogenic temperatures the mixture of ^{4}He and ^{3}He is a liquid. If cooled down below a critical temperature of $0.87K$, the mixture will separate into two phases. The lighter ^{3}He-rich liquid will rise to the top because of it's lower density and the heavier ^{4}He-rich liquid will sink to the bottom. As the temperature is decreased, the top ^{3}He phase will become pure ^{3}He. It was discovered experimentally, to great surprise of the physicists at the time, that the concentration of ^{3}He in the ^{4}He phase does not go to zero, but rather stays at a value of 6.6% even for $T = 0$. This fact can be used for cooling by transporting ^{3}He across the boundary from the concentrated ^{3}He-rich phase into the diluted ^{3}He-poor phase in ^{4}He. One can think of this as an evaporation process by which heat is removed. In a simplified treatment, assuming one mole of ^{3}He crosses the boundary, for heat to be removed the enthalpy difference between the concentrated and the dilute phase should be positive:

$$\Delta H = T\Delta S = T[S_{dil}(T) - S_{con}(T)] \tag{15}$$

since there is no change in volume:

$$dH = TdS, \quad where \quad S = \int_0^T \frac{C}{T} dT \tag{16}$$

According to results in experimental measurements for specific heat done by Greywall [50], specific heat for the dilute phase is larger than that of concentrated phase. Flow of ^{3}He across the phase boundary is then an increase of entropy and will cool the system.

That is, however, a very naive treatment of the problem, since the non-separability of the dilute mixture at low temperature by itself is a mystery that challenges the third law of thermodynamics. The correct treatment of the problem must treat the mixtures as quantum liquids. The ^{4}He isotope has a nuclear spin $I = 0$ and will undergo superfluid transition at around $2.177K$. At temperatures below approximately $0.5K$ it is almost completely in it's ground state, so it's entropy and specific heat go to zero.

^{3}He is a spin $\frac{1}{2}$ particle and obeys Fermi statistics and the Pauli principle even when diluted in ^{4}He. The condensate of ^{4}He can be thought of as an inert superfluid background, which contributes to the total volume of the liquid, but has negligible specific heat capacity and will alter the Ferni temperature and the effective mass of ^{3}He[13].^{4}He atoms occupy less space than ^{3}He because of the larger zero motion of ^{3}He as an effect of smaller atomic mass. When dilute ^{3}He atoms would be closer in space than in the concentrated phase and would have a larger binding energy. This means that up to a certain concentration it is favorable for ^{3}He to stay in the dilute phase, hence the finite concentration even at $T = 0$[51].

3.1.2 ^{3}He-^{4}He dilution refrigerator

A general ^{3}He-^{4}He dilution refrigerator works by transporting the ^{3}He across the phase boundary between the condensed and the dilute phase of ^{3}He-^{4}He mixture.

Figure 10 shows a schematic of a dilution unit of a typical cryostat[14]. The cooling occurs when the mixture consisting of mostly ^{4}He and small quantities of ^{3}He enters the concentrated phase of the mixing chamber, where subsequently ^{3}He enters the dilute phase. The concentration in the dilute phase is being constantly lowered by transporting ^{3}He to the Still chamber driven by osmotic pressure difference. The still is at approximately $0.7K$, so the vapor pressure of ^{3}He would be much higher than of ^{4}He. ^{3}He will then leave the mixture into the gas phase and will be pumped away. This keeps the still at low temperature in the same fashion as a ^{3}He cryostat would.

The returning mixture at 1.5K needs to condense into liquid and this is done through the use of a so-called main flow impedance. It builds up sufficient pressure, usually in the range of $50 - 200mbar$ to make sure ^{3}He does indeed condense at the temperature of $1.5K$. The cooling power from evaporating ^{3}He in the still is used to cool down the returning mixture to below $0.7K$ through a series of heat exchangers to prevent it from evaporating. The mixture coming up from the mixing chamber and additional flow impedances ensure that the returning mixture is at a low enough temperature when it enters the concentrated phase of the main mixing chamber. This way the mixture continuously circulates to provide cooling to the sample usually mounted at the bottom of the mixing chamber.

3.1.3 Triton 200

Triton 200[52] is a closed loop cryogen-free dilution refrigerator. Cryogen-free in this respect means that the precooling of the incoming mixture is done though the use of a Pulse Tube Refrigerator. It can cool down a sample to a base temperature of around 18mK providing up to $400\mu W$ of cooling power. It has a magnet able to provide fields of up to 5T in the vertical direction.

The system hangs from a top plate which is mounted on a vibration dampening frame. The top plate separates cold parts of the system from room temperature and is also the access point to all system services such as pumping lines, electrical connections, thermometry, etc. From the outside the system is protected by the Outer Vacuum Chamber or the OVC, which keeps

[13] effective mass is essentially a measure of interaction with the environment

[14] a model representation, the actual implementation will be slightly different

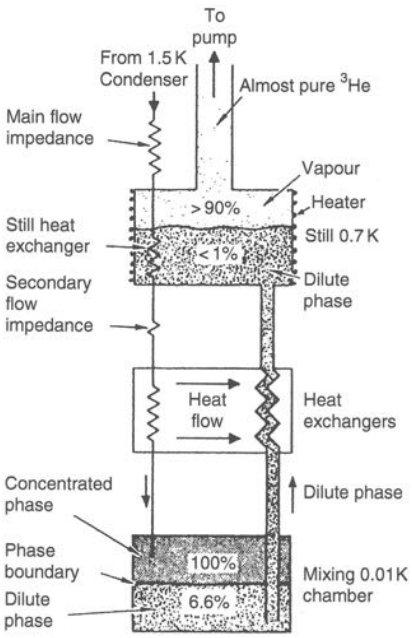


Figure 10: *A schematic representation of the ^{3}He-^{4}He dilution unit. The cooling is provided by ^{3}He crossing the phase boundary inside the mixing chamber due to the enthalpy difference between the incoming concentrated and the outgoing dilute liquid. Driven by osmotic pressure difference, the outgoing mixture is used to cool down the incoming mixture through a series of heat exchangers. In the still at higher temperature the vapor pressure of ^{3}He is substantially higher than that of ^{4}He, so it leaves the dilute phase into the gaseous phase. The gas is then pumped away providing more cooling for the incoming mixture. Figure taken from [51]*

the pressure inside the system at around $10^{-5}mbar$. This prevents thermal exchange with the surroundings. Inside the OVC there are layers of radiation shielding protecting the insides of the cryostat and the sample from unwanted heat and noise.

The bulk of heat is removed from the system via a closed loop helium expansion cycle in the Pulse Tube Refrigerator. It works by expanding the 99.999% pure helium. The returning low pressure helium from the cold head is then compressed by a compressor situated in the chiller rooms. The heat from the compression is removed by water cooling in the chase after which the compressed helium is returned to the cold head via the high pressure helium flex line and a rotary valve. The cold head is located in the top part of the cryostat and is where the adiabatic expansion of helium takes place allowing cooling to cryogenic temperatures. The cooling happens on two stages pulse tube 1^{st} stage(PT1) and pulse tube 2^{nd} stage (PT2). These operate at temperatures of around 50K and 4K respectively.

The mixing chamber (MC) is cooled through two cooling loops. The pre-cool circuit, figure 11 in red, cools the mixing chamber from room temperature to below 10K. It uses the two heat exchangers located on PT1 and PT2 to cool down the still, 100mK plate and the mixing chamber to low enough temperatures that ^{3}He condensing could happen. At temperatures below $10K$ the precooling circuit is shut off and evacuated using a turbo pump.

When the system is at a cold enough temperature and the precooling loop is evacuated the condensation of ^{3}He can happen. The mixture is cooled by a heat exchanger on the $4K$ PT2 stage. On a traditional system, the mixture would normally be cooled down further to $1.5K$ using a ^{4}He pot. On a cryogen-free system this is unavailable and the mixture is instead condensed using Joule-Thompson (J-T) stage. Using a very efficient heat exchanger inside the still pumping line and an impedance, the mixture will undergo isenthalpic expansion.

After the J-T stage, the mixture enters the dilution unit where the ^{3}He is transported across the phase boundary between the concentrated and the dilute phase providing further cooling. The sample holder is thermally connected to the bottom of the MC-plate and sits inside the magnet coil.

The system is equipped with a bottom loading mechanism, which allows fast sample exchanges without warming up the whole cryostat. By utilizing this load lock, it is only necessary to collect the mixture from the dilution unit into the mixture collection tank before an exchange could happen. When exchanged, the MC will typically warm up to only 65K. In this way sample exchanging process takes only a few hours as opposed to the time it requires for a full cycle[15].

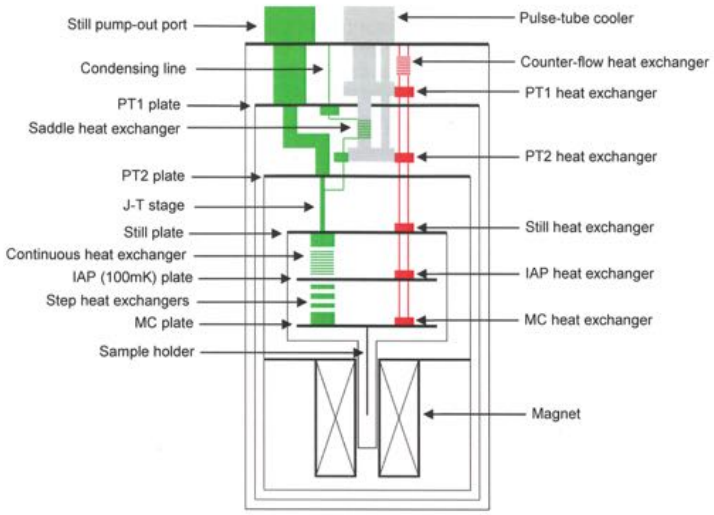


Figure 11: *Schematic of internal layout of the cryostat. Shows the main temperature stages as well as the precooling circuit(red) and the dilution circuit(green). The system is cooled down by a Pulse Tube Refrigerator from room temperature. The mixing chamber is pre-cooled by the precooling circuit from room temperature to below 10K. The precooling circuit is then shut off and evacuated and the subsequent cooling and operation is done through the dilution circuit. Figure from [52]*

3.1.4 Cold traps

Even though the mixture is in a closed loop, a number of contaminants can still be present in it. At room temperature metal and plastic surfaces inside the loop will release a number of contaminants like water, nitrogen and various oils from the o-rings in the system. To remove these contaminants special impurity traps are utilized. There are three so-called cold traps within the loop. Two of them are placed on the PT1 and PT2 plates and the third one is outside the cryostat. Since these traps are at temperatures below the freezing points of any hydrocarbons or even nitrogen, these contaminants will freeze out on the surfaces in the trap instead of freezing inside the much more delicate circuitry of the dilution unit. The traps inside the cryostat are cooled by the pulse tube. The outside trap sits in a liquid nitrogen dewar which has to be refilled periodically for the trap to remain cold. One can remove the contaminants from the loop by warming up the external cold trap after disconnecting it from the system.

[15] warming up the system typically takes on the order of 12-16 hours. Subsequent disassembly, sample exchange, assembly, re-pressurization and cooling back to base temperature takes on the order of $2-3$ days.

3.2 DC wiring and measurement equipment

3.2.1 DC Wiring

Spin qubit experiments require two different ranges of electrical operation. For defining the confining potential of the quantum system with the electrostatic gates one needs heavily filtered and attenuated lines. These lines should be able to keep their settings at timescale of weeks without spontaneous drifts or jumps. Because of their static nature they can also be heavily filtered to reduce incoming noise.

The DC part of the cryostat(see figure 12) wiring consists of two Constantan looms consisting of 48 lines. These start with two Fisher connectors at the top of the cryostat and then go all the way down to the coldfinger. The looms are anchored to each cryostat stage by copper clamps which are essentially two pieces of copper pushing against the loom to create good thermal contact. After the mixing chamber plate the looms go around a set of copper poles, also called bobbins, and are held in place by GE varnish, an adhesive that still works at extremely low temperatures. The idea here is again to provide cooling to the sample and thermalize the electrons by being in thermal contact with copper. After bobbins, the loom is connected to a series of RC and RF filters taking out the majority of the incoming electrical noise.

The RC filters consist of a set of surface mounted low pass filters with a cutoff frequency of 80MHz. These are Mini-Circuits LFCN-80 and they are connected in series with two $2k\Omega$ resistors and 2 $5nF$ capacitors to ground. Noise under approximately 10GHz gets absorbed by the RC filters rather than being reflected. For higher frequency noise, the lines go through the RF filters which are a set of Mini-Circuits LFCN-80, LFCN-1450 and LFCN-5000 in series, with cutoff frequencies of 80MHz, 1450MHz and 5000MHz respectively. These reflect high frequency noise that is not filtered by the RC filters.

Since the DC wires provide the majority of the cooling to the sample, at the mixing chamber plate constantan loom is replaced with a higher quality copper loom. We assume the lattice temperature to be at the same temperature as the mixing chamber plate: base temperature of around 20mK. Apart from lattice temperature another important metric is the electron temperature. This is measured indirectly by looking at the width of a Coulomb peak in transport measurement. By fitting a Gaussian one finds the upper bound for the electron temperature in the sample [53]. Electron temperature for this cryostat has been measured to be around 100mK[16].

3.2.2 DC measurement electronics

DC measurement electronics starts with the DecaDac manufactured by Jim McArthur at Harvard Electronics lab. This DAC(digital to analog converter) has a range of $\pm 10V$ and is stable on the timescale of weeks and provides a solid source of voltage for the experiment. The DAC is powered by an optical power adaptor cable from the measurement PC. This decouples the DAC from the noise generated by the PC and it's ground. After the DAC a voltage divider and a low pass filter box is attached. 5:1 divider and a low pass filter with a theoretical cutoff frequency of around 6Hz[17] is used for setting the gates, higher division factors are used to set the Ohmic potential, typically on the order of 1000:1.

[16] Electron temperature between $100 - 150mK$ has been measured for a previous experiment. At some point during the experiments described in this thesis, the mixing chamber temperature jumped to a higher value of around 40mK as opposed to 20mK, at which the measurements were taken. $100mK$ plate temperature was also higher than normal at around 200mK with all electronics turned on. It is likely that the electron temperature was in fact somewhat higher than measured previously for subsequent cool downs

[17] Most of the divider boxes on the setup were made by me and have a measured division factor of 4.3 and 3dB point at around 32Hz. This is due to the finite resistances and capacitances from other parts of the box, such as the casing, connecting wires and solder.

A low noise BNC cable connects the lines further to a $1.9MHz$ low pass filter which is then attached to a breakout box. There are two breakout boxes on the setup and they are the main interface with the looms inside the cryostat, and by extension the sample. Each breakout box is connected by a shielded cable to Fisher connectors on the top plate of the cryostat and further as described in figure 3.2.1.

Measurement instruments can be connected to the BNC ports of the breakout box. Since the DC wiring is heavily filtered there are two kinds of instruments that are usually connected to the breakout box ports. Those that source/measure voltage and those that source/measure current.

Typical transport measurement consists of a voltage source(S) and an amp meter(D). For voltage source we use the DAC. The voltage it produces is divided down so the typical working range is on the order of millivolts for gates and microvolts for Ohmics.

Resulting currents are then in the pico to nano ampere ranges which is too small to reliably measure with a room temperature amp meter directly. Ithaco 1211 current preamplifiers accept a current input and convert it to an easily measurable voltage. They have a variable sensitivity from 10^{-3} to 10^{-12} ampere/volt and the optimal for the experiments was 10^{-7}. Averaging out high frequency noise can be done by a controllable RC rise-time. The typical setting for the experiment was around $3 - 10ms$. Resulting voltage was in the millivolt range and is measured by HP 34401A Digital Multimeters.

Keithley 2400 Source Meter was sometimes used as an alternative voltage source or to be used as a sanity check. It can both source current and voltage at the same time within a particular compliance value and will give the same, albeit more noisy results.

If the signal is too noisy another tool to use could be an SR830 Lock-in amplifier. A lock in amplifier picks up only the signal for a particular frequency using homodyne detection. However, due to heavy filtering of the lines it can only be operated at fairly low frequencies, which results in long measurements. To avoid interfering with 50Hz noise, frequency a prime number away from 50Hz is recommended. Fot the Mayo board the frequency most commonly used is 137Hz, for Sydney board[18], because of additional inline resistance from the on-board filters the maximum feasible frequency was 13Hz.

3.3 High freqency wiring and equipment

Controlling the qubit requires substantially higher bandwidth than what is possible through the heavily filtered loom. Coaxial lines are used for sweeping through voltage space using fast gates and to send down arbitrary waveforms for qubit operation.

3.3.1 RF wiring

There are two sets of coaxial cables present in the cryostat(see figure 12). The central LOS(line of sight) insert carries 8 semi-rigid NbTi/NbTi[19] coaxial lines all the way down to the mixing chamber plate. After the mixing chamber plate a custom piece of Cu/Cu coaxial cables are used ending at the coldfinger. For filtering and thermalisation all coaxial lines are attenuated at the thermal stage plates with the largest attenuation being at the 4K plate since it has the most cooling power. Another insert at the side carries two out of 8 possible additional lines configured for reflectometry(see 3.4).

The input line for reflectometry(Tx) is configured in a similar fashion to the rf-lines(figure 12) with most of it's attenuation at the top stages of the cryostat where the cooling power

[18]Mayo board and Sydney board refers to the PCB sample holder used in the experiment mounted after the coldfinger of the cryostat. Detailed description can be found in 5.1

[19]refers to Niobium-Titanium alloy inner and outer conductor

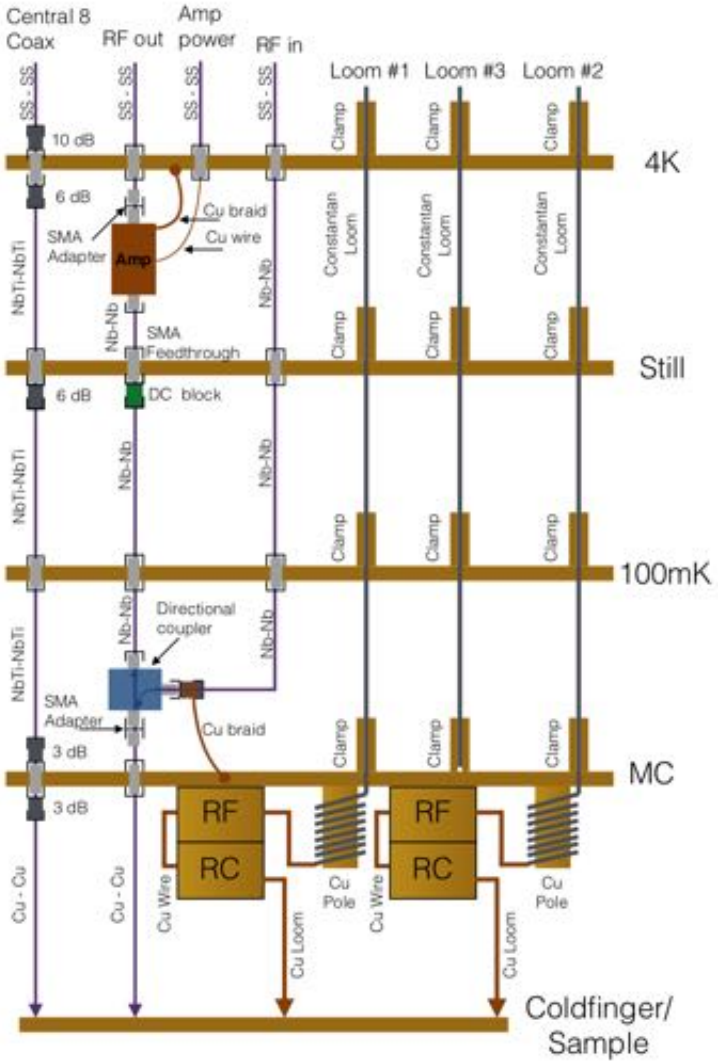


Figure 12: *Schematic of internal wiring of the cryostat. Main stages are shown as well as all types of lines down to the coldfinger. DC wiring part consists of 3 looms. At each thermal stage the loom passes through a copper clamp for thermalization. At the MC plate the loom goes around a copper pole - bobbin for additoinal thermalization. After the bobbins the loom connects to a set of RF and RC filters before finally reaching the coldfinger connectors. Only loom 1 and loom 2 come out to the coldfinger. Loom 3 stops at the mixing chamber stage. The RF wiring consists of 2 line of sight(LOS) ports. The first LOS insert carries the high frequency lines used for operating electrostatic gates. Attenuation is present at the 4K and the Still plate of the cryostat due to the best cooling power at these stages. The second LOS insert carries two coaxial lines for reflectometry. The incoming RF-in line is attenuated at the top stages similarly to the rest of the coaxial lines. After the 100mK plate it passes through a directional coupler and only the reflected signal enters the RF-out line. The signal in the RF-out line is amplified by the cryogenic amplifier. The amplifier itself is powered through one of the remaining six coaxial lines in the insert and a Cu wire. Figure from [54]*

is largest. After the 100mK plate it connects to a directional coupler. For thermalization of the reflectometry lines, the attenuation can only be present on the way down and until the directional coupler. Any attenuation between the directional coupler and the sample and between the sample and the measurement device will reduce the valuable signal. After the attenuators and the directional coupler itself the reflected signal goes into the output line(Rx) line and is

amplified through a cryogenic amplifier. The output line does not carry any attenuation.

3.3.2 RF equipment

Agilent HP 33250 Function/Arbitrary Waveform Generators are capable of outputting arbitrary waveforms at a sampling rate of up to 200MS/s with a waveform length of up to 16.4 Kpts. These are programmed in software to deliver a sawtooth waveform and together with a DC offset are a primary tool for fast sweeping in voltage space. The range of the sweep is set by the amplitude of the sawtooth, while the acquisition speed is set by the frequency. A typical frequency range for fast acquisition is between 100Hz to 1KHz. Two synchronized Agilent 33250 were used for the experiment.

Output from the Agilent 33250 is synchronized and combined with a faster arbitrary waveform generator(AWG) - Tektronix AWG5014a. It is a 4 channel AWG capable of sampling rate of up to 1.2GS/s, total waveform length of up to 64Kpts and a rise time of approximately 1.4ns. This allows for fast control of spin qubits such as implementation of Hahn echo sequences to extend coherence times[55]. Additional sequencing support where multiple waveforms can be sent, stored and sequenced allows for full electrical control[41][16].

3.4 Demodulation circuit and reflectometry

Observing charge dynamics requires fast measurement. DC lines are specifically protected against high frequency noise, which combined with self capacitance of the lines in the cryostat and the characteristic quantum channel resistance on the order of $100k\Omega$ makes this impossible[20]. To bypass this limitations reflectometry technique has been utilized. It has been pioneered by Schoelkopf[56] and further adapted for use in spin qubit experiments by D. Reilly[31] and gives an effective bandwidth in the MHz range.

3.4.1 Reflectometry

Consider an RF signal propagating down a line with a certain impedance. If the signal hits another line with different impedance a part of the signal will be reflected. The observed voltage is expressed by a *voltage reflection coefficient* Γ, given by:

$$\Gamma = \frac{z(\omega) - z_0}{z(\omega) + z_0} \tag{17}$$

where z_0 is the characteristic impedance of the transmission line of 50Ω. The reflected power is proportional to $|\Gamma(\omega)|^2$.

The load impedance is implemented through the use of a tank circuit with impedance:

$$z(\omega) = i\omega L + \frac{R}{1 + i\omega RC} \tag{18}$$

Here L is the inductor value, C is the stray capacitance from device, wires, the 2DEG etc. R is the resistance of the circuit. Reflected power would be minimal if the tank circuits impedance is also at 50Ω. This would happen at the matching resistance:

$$R_m = \frac{L}{50 - \Omega C} \tag{19}$$

and matching frequency:

[20] simple model of $f_{3dB} = \frac{1}{2\pi RC} \approx 1kHz$ is the characteristic low pass frequency

$$\omega = \frac{1}{\sqrt{LC}} \tag{20}$$

If a charge sensor is implemented as a resistive element of the tank circuit with a characteristic resistance close to the matching condition, the circuit will be very sensitive to any change of the resistance in the sensor channel due to transitioning electrons expressed in reflected power.

In theory we can predict the matching resistance fairly accurately, however in practice it is not always that straightforward. Inductance can be controlled precisely by changing the surface mounted components which are available commercially between $100 - 1200nH$. Capacitances on the other hand are largely out of our control. The idea is to reduce stray capacitances as much as possible by placing surface mounted components closer to the device, making shorter bond wires, avoiding crossing over device with some bonds and even reducing the size of the mesa. Resistance can be controlled at will by gate voltage, however, there are only certain regions in gate space for which the sensor is sensitive to it's target. In an unlucky scenario, one could have a single sensitive spot in gate space with matching condition happening at vastly different resistance values. In this case one would have to qualitatively adjust the surface mounted components to "move" the matching condition to a desired region. Figure 13 shows the reflected power as a function of conductance through the charge sensor.

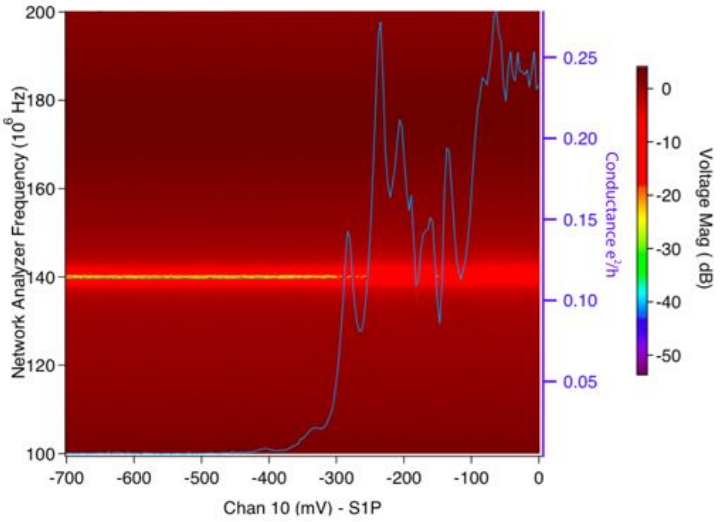


Figure 13: *Reflectometry matching condition. As the conductance through the charge sensor is modulated by gate voltage, a tank circuit goes through a matching condition. At the matching condition the reflected power is minimal, expressed by demodulated voltage. The difficult part is to "move" the matching condition to a resistance of the sensor where it is sensitive as a charge sensor, typically at the slope of the conductance curve.*

We have also seen devices where the resonance deepens with increasing resistance of the quantum channel. The model above assumes the resistance to be dominated by the quantum channel. With ohmic resistances above $1k\Omega - 2k\Omega$ the model breaks down, since now one can think of the sensing channel being in parallel with a number of capacitive paths to ground. This means that the impedance of the channel is now governed by these capacitive paths to ground and the reflection coefficient wont change when the resistance in the quantum channel becomes very large[27]

3.4.2 Demodulation circuit

At the core of the setup is the demodulation box. The incoming signal is split and then recombined using *homodyne detection* to pick up the small changes in the device. Homodyne detection works by combining two sine wave (two parts of the same signal) and essentially multiplying the two waveforms. The resulting output will look like:

$$sin(a) \cdot sin(b) = \frac{1}{2}(cos(a-b) - cos(a+b)) \tag{21}$$

which is a superposition of the two "parts". For example mixing a 5MHz sine wave with a 6MHz sine wave, the outgoing signal would be a mix of 1MHz wave and 11MHz wave. If two waveforms of the same frequencies are mixed, the resulting outcome would contain a measurable DC signal that depends directly on the amplitudes of a and b, plus an a+b high frequency component that can be filtered away.

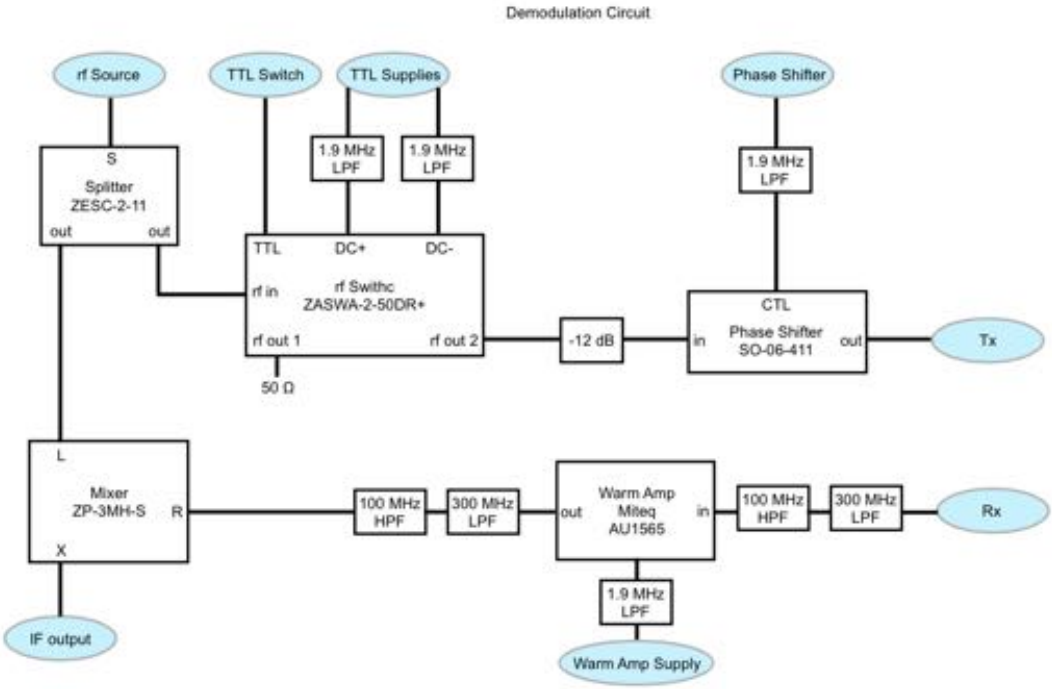


Figure 14: *The demodulation circuit used for the experiment[35]. Using homodyne detection the idea is to measure the DC-offset of the difference part of the incoming signal. Incoming signal from the source is split by the splitter and is further passed into the Tx line(reflectometry input) through an rf Switch and a phase shifter. The rf switch is connected to the AWG through a TTL Switch. The reflected signal from the Rx line(reflectometry output) is amplified by a room temperature amplifier. Amplified signal is combined with the original signal in a mixer, after which it is sent into the measurement device. The sum signal is filtered by a series of low pass filters. Figure from [27]*

The insides of a demodulation box are illustrated in figure 14. As the carrier waveform enters the box, it is split in two. One part, the "reference" signal goes straight to the mixer where it will eventually be recombined with the outgoing signal from the cryostat. The second part goes into Tx line of the cryostat through a switch, a phase shifter and a series of attenuators and DC blocks. The rf switch is connected to the AWG5014 and serves the purpose of turning the carrier frequency on only at times of reading out the state of the quantum system and not to disturb the system during operation by turning the carrier off. The phase shifter adjusts the phase of the carrier to be *in phase* with the "reference", since otherwise the DC signal will be severely

diminished or even canceled out. DC-blocks are of the *inside-outside* kind and are designed to decouple the demodulation box from any DC ground and low frequency noise that is present in the demodulation box. A series of attenuators is used to reduce the power of the signal for thermalization and to not disturb the sample too much[21].

After being reflected from the sample and amplified by the cryogenic amplifier the signal enters the Rx input on the demodulation box. It is then effectively band filtered by a 100MHz high-pass filtered to remove any kind of DC noise originating from inside the cryostat and a 300MHz low pass filter to remove any higher frequency noise. The signal is then amplified again by a room temperature amplifier before being recombined at the mixer. After the mixer the sum and the difference signals go out of the IF output on the box. Since we are only interested in DC component of the difference signal, the sum signal is filtered away first by a resistive 30MHz Picosecond filter and then by a 1.9MHz low pass filter. This filtered signal is then amplified again by a room temperature preamplifier SRS SR445a before entering the Alazar digital oscilloscope for measurement.

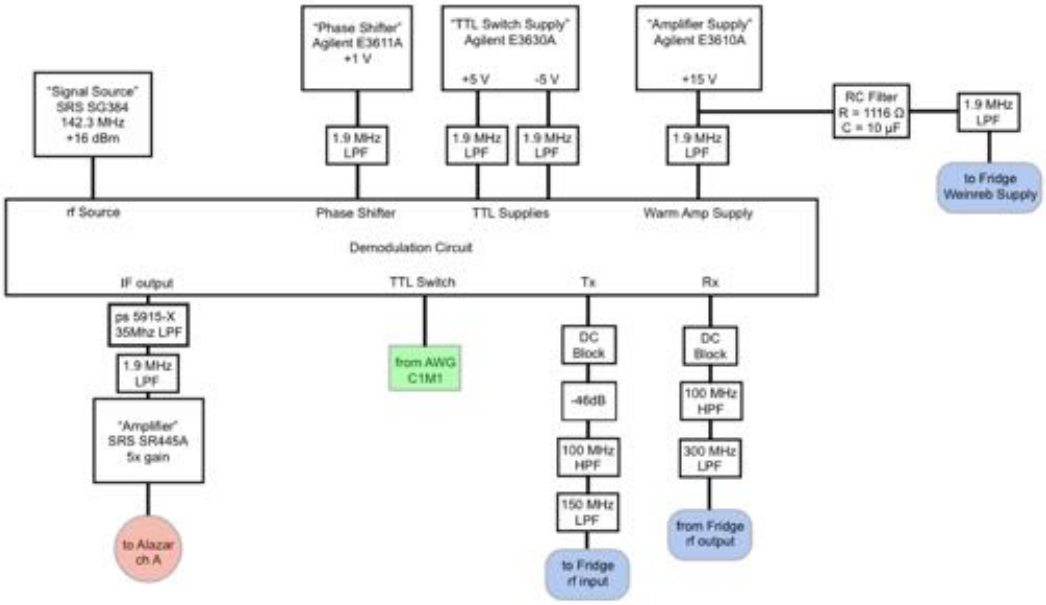


Figure 15: *The carrier waveform is generated by the signal generator SRS SG384 and sent into the demodulation box. From inside the demodulation box the signal is sent through the Tx line down into the cryostat(Fridge). The reflected signal enters the demodulation box through the RX line. After mixing with the "reference" signal inside the demodulation box the combined signal is output from the IF output. Figure adapted from [27]*

3.4.3 AlazarTech ATS9440 digital oscilloscope card

Achieving fast readout though reflectometry requires fast data acquisition and fast data storage. The main advantage of the Alazar card is it's ability to quickly offload the acquired data into the computer at speeds of up to 1.6Gbps though a PCI-Express 8x slot. It writes the data directly into the RAM, meaning in theory unlimited acquisition times[22] The card itself is capable of

[21] too high power may lead to heating and as a result thermal broadening of the transitions

[22] unfortunately at the moment of writing this thesis hardware limits us to 128GB RAM using server grade hardware, but with capacities of up to several gigabytes per machine are coming in a relatively close future. This will however utterly destroy the Igor acquisition suite, since the rule of thumb experiment files sizes should be under 400MB!

up to 125MSa/s on up to 4 channels simultaneously with each channel having a bandwidth of 65MHz. It can also store up to 2GSa in it's onboard memory.

When triggered, the Alazar cad acquires a certain number of samples. This number of samples is called a *record*. These will typically be averaged using the onboard FPGA. When enough records are acquired the card registers it as one *buffer* and starts offloading it into the RAM while simultaneously acquiring the next set of samples. A single buffer can store up to 2^{19} samples when using a single channel[57].

3.5 Software control and acquisition

The whole experiment is controlled through the Igor software suite running on a single PC. The bulk of communication with the equipment for slow measurement is done through IEEE-488 short range communications bus or GPIB(General Purpose Interface Bus), developed by Hewlett-Packard in 1960s. It is a robust standard that can be stacked in series to connect up to 31 devices. The GPIB card inside the computer connects through a fiber-optic cable to reduce noise to the main GPIB bundle that goes to all other instruments. Using the GPIB Communications protocol implemented through Igor *procedure files*, i.e. device drivers, it is possible to control the equipment and acquire data using software commands.

Communications with the DACs is done through the Serial port, which is connected to the equipment via a fiber-optic cable to remove DC noise. Communication and control of the AWG is done though a LAN connection and the built in VISA protocol in Igor. The Alazar card is controlled through an Igor extension written by J. Medford.

The general state of the software suite is quite complicated. It has been originally written by Alex Johnson[58] around the year 2003 and has been used and modified ever since. The core acquisition is still done using the original routines where applicable. Newer equipment, including the Alazar card, has been added to the code in a rather careless fashion by people who just needed their experiments to work. As a result the documentation is lackluster and many of the routines' purpose has been lost.

4

DEVICE AND DEVICE FABRICATION

Fabrication of the device and to some extent device design are usually dismissed by experimentalists as tedious and boring. Considering how many factors are at play during this process it is unsurprising that they get overwhelmed and put in a defensive stance when it comes to trying out new ideas or adjusting recipes. I would urge anyone taking on the task not to be overly conservative, but neither be trigger happy with new fabrication ideas. Control is key and a controlled process is a reliable process that is easy to steer in the direction of a satisfying result. Respect the "fab" and the experience of the people before you, but don't limit yourself by that experience.

This chapter will focus on device fabrication reasoning and many tricks that have been found to work. This is a collection of knowledge that is too important to go into the appendix, yet not important enough to make it into the conclusions section.

4.1 General overview

The genera strategy for making the device is based on standard GaAs fabrication techniques. A detailed recipe in included in appendix A. The process begins by cleaving(cutting) and cleaning a piece of wafer. Then, to insure electrical isolation between the electrostatic gates, the unwanted 2DEG is etched away by an an acid solution. This chemically removes the material down to the bulk substrate(see sec. 2.1) only leaving the necessary paths for the ohmic contacts. This step is called mesa etch. The mesa area is usually defined using UV-lithography technique.

When the mesa is ready, the next step it to contact the remaining 2DEG by thermally annealing the stacks of metal to make ohmic contacts. The contacts are defined by means of UV or Electron Beam (E-beam) lithography and the metals are then deposited by standard means of e-beam or thermal evaporation. During the annealing step, the whole wafer is heated up to around $420^{\circ}C$. At this temperature a specially designed metal eutectic sieves down into the material creating ohmic contact to the 2DEG. Any metal gates present on the wafer at this point will also be annealed, including alignment marks, and this will distort and deform the features. It is therefore important to fabricate the Ohmic contacts before defining the fine features.

The next and final part of the fabrication is the patterning of the electrostatic gates that make a quantum device. Similarly to the ohmic contacts, the electrostatic gates are defined using e-beam lithography. Metal is deposited by e-beam evaporation. The gates consist of a Titanium sticking layer and a thicker layer of gold. The thickness of the gold layer varies depending on the part of the device, with outer areas being as thick as $200nm$.

When all electrostatic gates are finished it might be useful to image one of the devices using a Scanning Electron Microscope (SEM) to confirm their quality. A superstition is going around about the negative effects of SEM imaging. These negative effects have never been observed on any device fabricated in Center for Quantum Devices, although there is no reason to subject them to further processing if one is confident in his yield.

4.2 The wafer

The devices used for this thesis were made on a GaAs heterostructures supplied by C.Gossard and M. Manfra. The heterostructures themselves are explained in section 2.1.

The wafers are grown in a molecular beam epitaxy(MBE) chamber[24]. Physically the MBE chamber is round and because of it's shape the temperature distribution across the wafer is not completely uniform. Parts of the wafer farthest from the center would generally be colder than the center. This results in a sweet spot of the best quality material in the middle of the wafer of around 2 inches or approximately 5 cm in size[23]. That is the quality of the material expressed in uniformity, electron mobility, donor and impurity concentration decays towards the edge. It is worth noting that we did not test this in our lab and have no reason to believe that it makes a dramatic difference in device performance. The ohmic resistance has been seen to increase by up to a factor of 3. It is also recommended to avoid a ring around a millimeter wide which appears approximately $0.5cm$ from the edge. It can be seen on the back of the wafer once it has been cleaned. Ohmic contacts placed directly on top of this ring were not making contact to the 2DEG in batches PT_25-29 and PT_19-24.

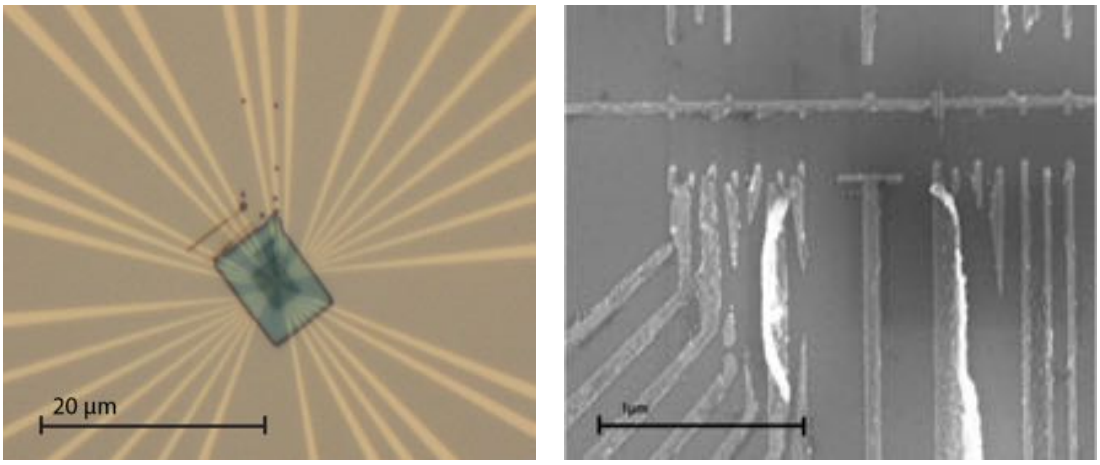
4.3 Resist

A resist is a light sensitive polymer solution that changes it's chemical properties when exposed to high doses of radiation. It is used during lithography process to define the features that will undergo chemical or physical processing. To obtain a uniform layer of the resist the wafer is spincoated. After spincoating it is usually baked for a few minutes on a hot plate, so the resist dries up and gets firmer. A kind of light that causes a chemical reaction will determine the type of the resist. For instance S1813 resist is a photoresist, because it reacts with hard UV light, while e-beam resist PMMA is resistant to UV and will only react when exposed to a beam of electrons.

After the resist is patterned in a lithography system, it will be subjected to a developer solution. If the resist is *positive* the developer will remove(dissolve) the exposed areas and if the resist is *negative* the developer will remove the unexposed areas. Better resolutions are generally obtained using positive resists(feature sized down to a few nm), while negative resists are generally more resistant to wet chemicals(feature size down to $2\mu m$). A general lithography process is described in figure 19. It is important to note that some resists can act as both positive and negative [59]. For example, figure 16(a) shows a device with overexposed positive resist PMMA. Because of a extreme dose of radiation it has became cross-linked. In this case the can't be removed with a solvent or by oxygen plasma ashing, hereby acting as a negative resist.

An important factor to think about when picking a resist for a particular step is it's height after spincoating. The height of the resist after spinning for a certain amount of time depends on the physical properties of the resist and it's concentration. A 4% PMMA solution will have a final thickness of just under $200nm$ while a 2% solution will have a thickness of around $50nm$. This is important if the distance between parallel features is very small. In general, if the width of the resist stack after development is much smaller than it's height, it will most likely collapse on it's side and ruin the pattern(see figure 16(b)). We have seen good results with 4%PMMA and gate pitch of around $70nm$. This results in a resist stack after development of around $40nm$ wide and $180nm$ high. This is possible with the correct development time and exposure with low amount of backscattering, such as using a 100KV system. Baking times could also be varied to

[23] As confirmed by M. Manfra during a conversation at the IARPA site visit in November. When the wafer is grown, the growers take a piece from the center for testing. The data supplied with the wafer is thus only accurate in that fairly small region



(a) (b)

Figure 16: *16(a)Optical image of the device that has been imaged with resist on. This caused PMMA to become cross linked from overexposure[59] and it is virtually impossible to remove. 16(b) An SEM picture of a metallized device where the resist has been overdeveloped or overexposed. Resist stacks became much narrower than the height, which caused them to collapse on it's side.*

influence the strength of the resist. It is recommended to bake the resist for around 2-5 minutes so it becomes dry. We have seen improvements in e-beam resist strength when baking it for upwards of 20 minutes for very tight exposures with $50nm$ gate pitch.

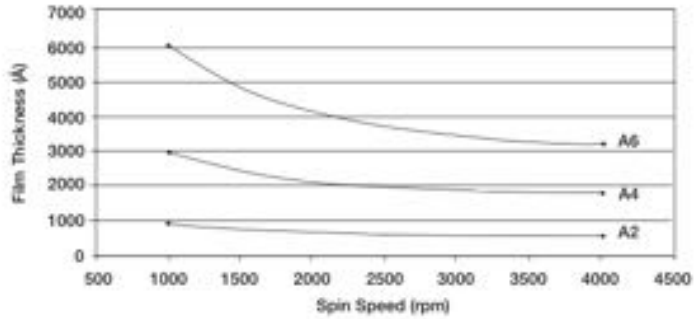


Figure 17: *A spin curve for the 2%(A2), 4%(A4) and 6%(A6) PMMA resists used in the cleanroom. Depending on the resolution needed, one would use a different concentration of PMMA. It is generally not recommended to vary the spin time due to reproducibility concerns. A general rule of thumb is that the feature pitch should be comparable to the height of the resist. If this is not met, the resist may collapse after development and the evaporation step will ruin the device. Data taken from [60]*

4.4 Lithography

Photolithography and E-Beam Lithography is a process in nanofabrication used to write a pattern into bulk material. It uses light to transfer a patter from a design file or a mask onto the light sensitive material, which can then be processed to obtain high resolution patterns.

Photolithography uses hard UV light that is sent through a photo mask onto a wafer coated with UV sensitive resist. The main limitation of UV lithography is that the resolution is limited by the diffraction limit of the used wavelength. Theoretically this means that the best achievable

resolution possible with a good mask aligner that uses $365nm$ wavelength is around 180nm[24]. In practice however, most cleanroom mask aligners claim being able to achieve resolutions of around $1-2\mu m$. The main benefits of optical lithography is the speed and scalability. It is easy to produce large quantities of UV light and expose whole wafers through a mask. This method is however much less flexible for prototyping, since one would need a new mask for each new device design[25].

As impressive as optical lithography can be in terms of scalability and throughput, it is not relevant on an experimental physics cleanroom level. For prototyping on a small scale with very high degree of customizability and very high resolutions we use Electron Beam Lithography. It utilizes high intensity focused beam of electrons to write patterns into E-beam sensitive resists such as PMMA. Electrons are produced from a thermionic source or a Field Emission Gun similarly to a Scanning Electron Microscope(SEM). In fact, most E-beam lithography systems are modified SEM's and can be operated as such, for example for imaging purposes.

With an electron wavelength of around $1.23nm$ one can in theory approach resolutions of down to several nanometers. In practice, however, there are two main factors limiting the attainable resolution. Electrons emitted from the source are called primary electrons. When primary electrons hit matter several different events are likely to occur. The electrons could be transmitted, absorbed by breaking a C-C bond, or have a chance of being scattered in a multitude of directions due to Coulomb interaction with electrons or nuclei of the incident layers, i.e. the resist, substrate, etc.[63][64] If the electrons are scattered elastically with an angle less than $\phi_0 < 90$ deg, they will effectively broaden the beam during it's propagation through the resist. Beam broadening will limit the feature resolution of the exposed pattern. Primary electrons will also occasionally backscatter($\phi_0 > 90$) from inside the resist or the substrate and can expose parts of the resist up to a $100nm$ away. Effect from elastic forward- and backscattered electrons can be minimized by either decreasing the thickness of the resist or using higher energy electrons by switching to a machine with higher acceleration voltage. The effects of the acceleration voltage are illustrated in figure 18. At higher acceleration voltage the electrons penetrate further into the material before being scattered. This means that the beam broadening happens further down in the material, instead of in the resist layer.

Primary electrons will also interact inelastically with loosely bound electrons in the outer shells of the solid. This event will transfer sufficient kinetic energy to an encountered electron and send it flying off through the solid with a possibility of hitting the resist. These lower energy electrons are referred to as secondary electrons and set the main limit on pitch resolution in a phenomenon called the proximity effect.

In experimental physics the substrate parameters are often fixed[26]. The two most effective optimization parameters left are therefore the lithography system and the resist, with the resist often being the main bottleneck for the lithographic process[65].

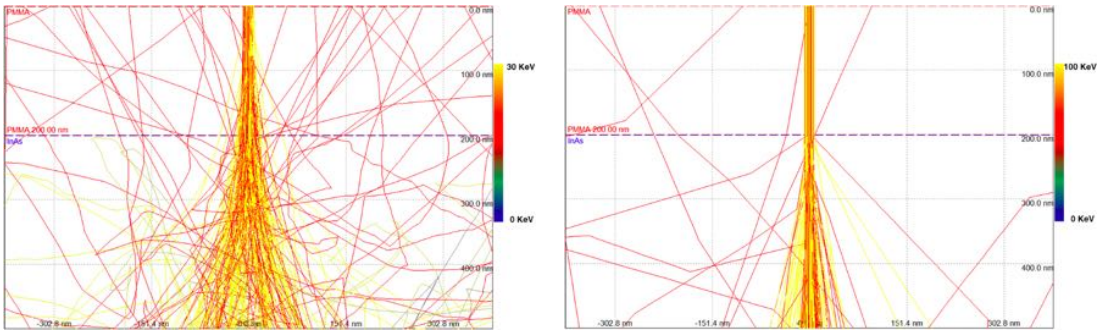
4.4.1 Lithography systems at QDev

MJ150 mask aligner optical lithography system can handle wafers up to 6 inches in diameter. It uses $365nm$ wavelength generated from a mercury source. The best obtainable resolution is

[24]Intel has recently announced being able to do optical lithography with a resolution of 11nm using a technique called immersion lithography[61]. In that technique light travels through a series of lenses and then a pool of water before finally hitting the wafer. It uses the refractive index of water and then the resist to focus light to tiny spot sizes[62]. This is difficult to implement and requires specialized hardware. It is not relevant in prototyping tasks given the availability of E-beam lithography

[25]There exist mask-less optical lithography systems referred to as laser writers. They gain in flexibility, but lose in speed, since exposures take orders of magnitude more time per pattern. Laser writers are still subject to the same limitations in terms of resolution as other optical lithography systems

[26]if the experiment is on GaAs, so it does not make any sense to switch to Si for the sake of lithography!



(a) (b)

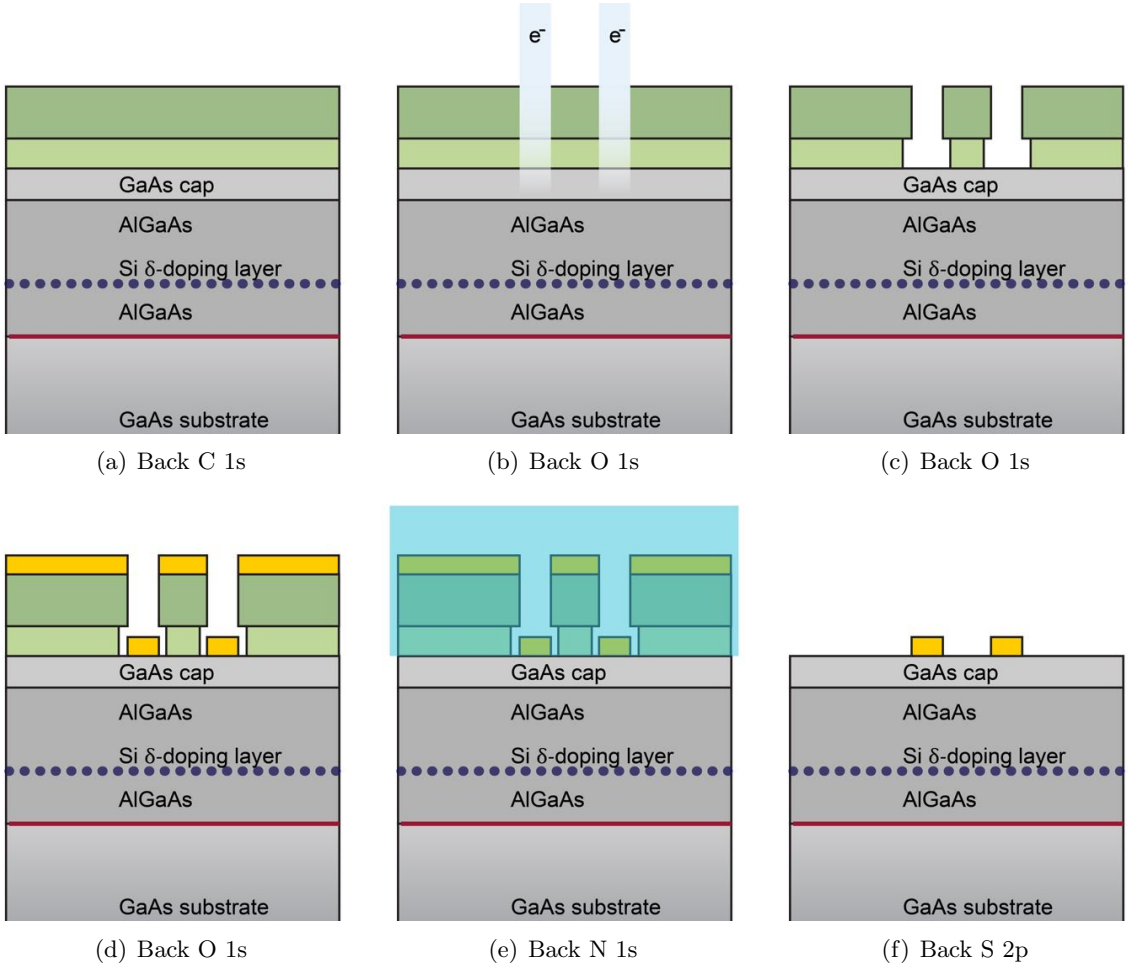
Figure 18: *A Monte Carlo simulation for beam broadening as a result of elastic and inelastic scattering of electrons when interacting with the sample. A beam of lower energy gets notably broadened. Adopted from [66] 18(a) 30KeV electron beam.18(b) 100KeV electron beam.*

around $1\mu m$. It can be used in two main modes being soft contact and hard contact. In hard contact, the wafer is pressed against the mask manually before exposure. In soft contact a wafer is held in place by vacuum using an o-ring between the stage and the mask. When the vacuum is engaged, the stage snaps into place. Because of the precision required in aligning the wafer to the pattern[38], the snapping motion was ruled as unacceptable and the stage lifting had to be operated manually.

Originally our recipe required three optical lithography steps to make devices: mesa patterning for wet etch, ohmic contacts and bonding pads patterning and the last connecting layer of electrostatic gates. Conventional optical lithography with a mask aligner requires the removal of so-called edge beads from the chip. These naturally form during spin coating. Edge bead removal techniques require an area of up to several millimeters and thus are not feasible considering the value of the material and typical sizes of the chips that are used in fabrication. When doing a mesa etch edge beads are generally not a problem, although they might lead to cracking of the chip when pressing it against the mask. When trying to align features to each other this becomes a whole different story. In this case, removing edge beads helps greatly, since the wafer piece will be "springy" with them. Because of the difficulty of multiple layer alignment we opted to use E-beam systems instead for ohmic contact patterning and all electrostatic gate sections. This requires more E-beam steps which is significantly more time consuming, yet still can be done within a few days. There are two main E-beam systems in Center for Quantum Devices. Raith E-line is a $2-30kV$ system and Elionix, a $100kV$ system. Elionix system was used for all E-beam as it does not suffer from the same proximity effect limitations as the Raith. The Raith E-line has ocasionally been used for large features, where lower acceleration voltage does not limit the outcome, if there was no available time slot for the Elionix.

4.4.2 E-line vs. Elionix

The only reason for this chapter even being here is to make a statement that both systems can perform any exposure that we would throw at it. Figure 20(a) is an example of what could be achieved after a few months optimization and dose tests. Exposing single pixel lines on the E-line it was possible to achieve successful lithography comparable in quality to an Elionix exposure. The main limitation of the system however is the lack of automatic height and focus correction. For a 30KV system the depth of focus is much smaller than for a 100KV system. The wafer would normally sit at an angle and exposures several millimeters away from the calibration point will be out of focus. Nevertheless the E-line proved to be a capable system, even though I would



(a) Back C 1s (b) Back O 1s (c) Back O 1s

(d) Back O 1s (e) Back N 1s (f) Back S 2p

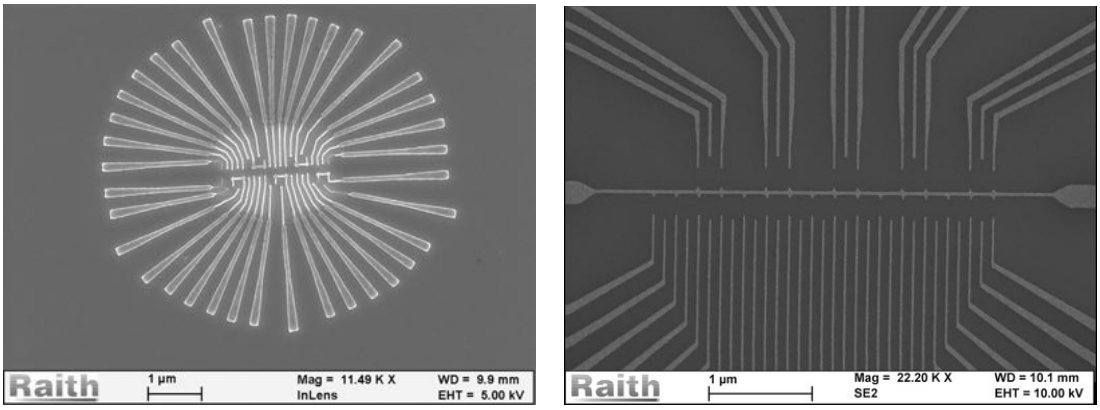
Figure 19: *A general overview of electron beam lithography process with bi-layer resist. The procedure for a monolayer resist would be identical. 19(a) Two layers of positive E-beam resist is applied to the wafer by spincoating. The bottom layer is chosen to be more sensitive to the electron beam. 19(b) A pattern is exposed onto the resist. The beam of electrons breaks the C-C bonds locally in the polymer. 19(c) The wafer is "developed" by a special solution that removes the resist from the exposed region of the wafer. Since the bottom resist is more sensitive to the electron beam, a larger portion of it is removed creating an undercut. 19(d) Metal is evaporated onto the developed wafer. Since the evaporation is unidirectional, the metal will only cover areas directly in line of sight of the source. 19(e) The wafer is submerged in a solvent that dissolves all remaining polymeric resist lifting off the metal that is not in direct contact with the wafer. 19(f) After lift off only the metal on the surface of the wafer remains following the original pattern.*

recommend doing high resolution lithography on Elionix.

4.5 Metal evaporation

Metalization of the sample and liftoff are usually done as the final part of the lithography process. The main idea is described in figure 19. There are several important factors to consider when determining which metals and how much to evaporate. Obviously, for pure electrical connections chemistry dictates the use of noble metals like Au and Pt, for superconductivity - metals that become superconducting like Al or Ti and so on...

After picking the metal the first consideration should be about the substrate. It is important to ensure that the metal sticks to the surface. For this reason a sticking layer is deposited and



(a) (b)

Figure 20: *20(a) A prototype L-shape test device consisting of 15 quantum dots and 5 sensors made on the 30KV Raith E-line electron beam lithography system. The lithography was reliable, but only near the calibration point. It was not possible to make an array of such devices reliably. 20(b) 15 in a row device made on a 100KV Elionix electron beam lithography system. This design has been fabricated reliably in arrays of up to 9 devices and some have been finished into full devices.*

it's primary function to ensure that whatever is deposited on the surface of the substrate will stay in place. The sticking layer is just thick enough to ensure that the coverage is complete and uniform, in our case - $5nm$ of Ti.

Then one should consider the resists tolerance of heat. Evaporating metal on the surface heats up the sample and bakes the resist further. Lets say you want to evaporate on photo resist which is baked at 115C. Evaporating $50nm$ of gold only takes a few minutes. During this time the surface wont heat up beyond 100 degrees. Evaporating a full micrometer of Cr on the other hand might hard bake the resist and make it impossible to remove during liftoff.

Evaporation is unidirectional. What this means in practice is that anything casting a "shadow" will prevent the shadowed part from being covered by metal. Therefore the angle of the target plate on which the device will be positioned is very important and any hairs, junk or shifting resist will affect the result. Avoiding junk and hairs is easy by following standard cleanroom practice. Moving resist is something that should not happen normally if the guidelines in the resist chapter 4.3 are followed. There is a number of situations when one might want to exploit this feature. For example, the shadow evaporation is often used to create superconducting islands in cooper pair splitters.

5

PREPARATION FOR EXPERIMENT

This chapter describes the sample preparation as a last step before the measurement. This section contains tips on how to choose the right sample board, bond the sample and load it into the cryostat for tuning and subsequent operation.

5.1 Sample boards

Device fabrication refers to producing the device on a wafer. Obviously if one tries to do any measurement or experiment one needs to interface the sample with the experimental setup. This is usually done by mounting the sample onto a specially made sample board, then put into a puck and into the cryostat. In QDev there are two kinds of sample boards used for Spin Qubit experiments.

5.1.1 Mayo board

The "Mayo Board" is the main PCB used for the experiments primarily within Spin Qubits. It was manufactured by Mike Shea at the Mayo clinic and features 51 potential DC connections and 11 coaxial SMP connections, figure 21.

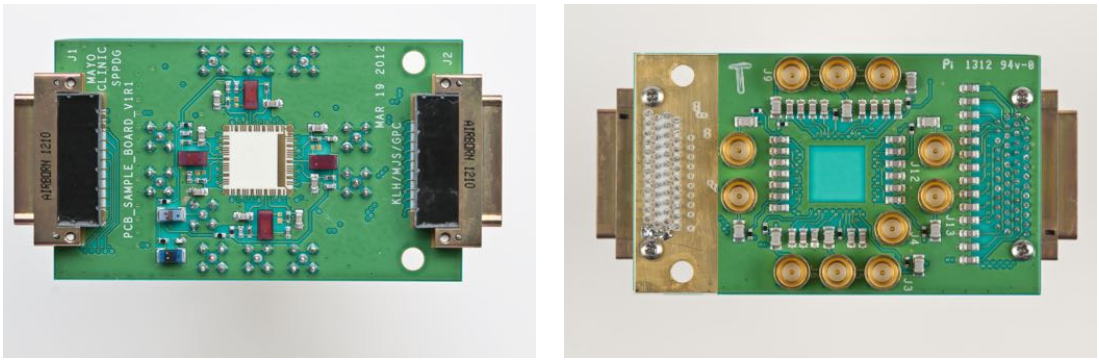
The DC connections are provided via two 51-pin nanoD connectors on each side of the board which are internally shorted, so the board can essentially act as a passthrough. This allows electrical contact from two different sources and is especially important during bias cooling. All DC-only lines are connected to a decoupling capacitor to ground to eliminate any high frequency noise from propagating onto the device. 10 of the DC connections are connected to a high frequency line through a bias tee. Each of these 10 lines comes out to two bondpads that are connected by a 12kΩ resistor in parallel, which means that both bonding pads can be used for DC operation.

There are 10 SMP ports on the board itself that allow for fast operation of the device. A bias tee connects each of these to a DC bias line. This way only the bonding pad which is directly connected to the high frequency line can be used with high frequency signals. All fast lines are also matched in length from the smp sockets to the bonding pads to eliminate propagation delays and phase mismatches. Since high frequency lines in the cryostat are also matched, it is recommended to use coaxial cable pieces of equal length when connecting the board to the internal connections of the puck.

One of the high frequency lines is split into 4 RLC circuits or "tank circuits" in parallel. These are used for sub-microsecond measurement of up to four charge sensors on the device via reflectometry. The detailed description of reflectomentry can be found in section 3.4. Tank circuits can be configured by the user to achieve different resonance frequencies. The more detailed description of the configuration will follow in section 5.2

There are several limitations of the "Mayo board" that are inherent to it's design. It can only handle 10 fast RF lines plus and additional RF line for fast sensing, even though there are

14 lines available in the cryostat[27]. The sample is also mounted directly onto the main board and there is no easy mechanism to replace it without tearing off the bond wires and potentially damaging both the sample and the motherboard itself. Both of these issues are solved with the "Sydney board".



(a) (b)

Figure 21: *The Mayo board.21(a) Top view of the motherboard. Surface mounted inductors are highlighted in red. The board can accept up to 51 DC through the nanoD connectors on the sides and 11 RF connections through the SMP ports on the bottom. One of the RF connections is used for up to 4 resonant sensor circuits. The device is mounted in the middle using glue and bonded to the surrounding bonding pads on the wirebonder. 21(b) Bottom view of the Mayo board.*

5.1.2 The Sydney board

The "Sydney board" is a next generation of sample boards that is based on two main ideas: high degree of connectivity and configurability and non-destructive sample swap possibility. This sample board is developed by J. Colless at the University of Sydney and adapted for use in our experiments by N. Okulova and the author.

The full capacity of the board is up to 74 DC lines, 36 coaxial fast lines operable at around 5GHz and 4 Microwave lines operable at frequencies of above 10GHz[67]. "Sydney board", shown in figure 22, consists of a main and expensive motherboard and an additional cheap daughter board that can be designed and configured on a per sample basis.

All DC lines go through a set of RC filters and end up at a set of connections under the daughter board. 36 of these lines are connected to 5GHz coaxial multiport connections through a bias tee. All lines are matched in length to eliminate signal delays or phase mismatches. The 4 microwave lines have a different set of bias tees and are routed on the top layer to reduce any negative effect they might have on the rest of the board. The number of accessible connections are ultimately limited by the wiring of the cryostat (48 DC and 14 coax), however with the right adaptor any line can be accessed should it be needed for a particular experiment.

The daughter boards can be designed with a particular experiment in mind using any PCB design software like Altium. They are connected to the motherboard via an interposer piece, which is a machined piece of plastic designed to hold special push-pins called Fuzz Buttons™. It is important that the bottom of the daughterboard follows the footprint of the interposer, but otherwise one is free to reroute the lines in a convenient fashion inside the custom board. This is shown in figure 23.

Sydney board can be mounted into the IARPA puck using a custom mount piece designed by the author. DC lines are adapted through custom assemblies designed by N. Okulova.

[27] at the moment of writing this thesis

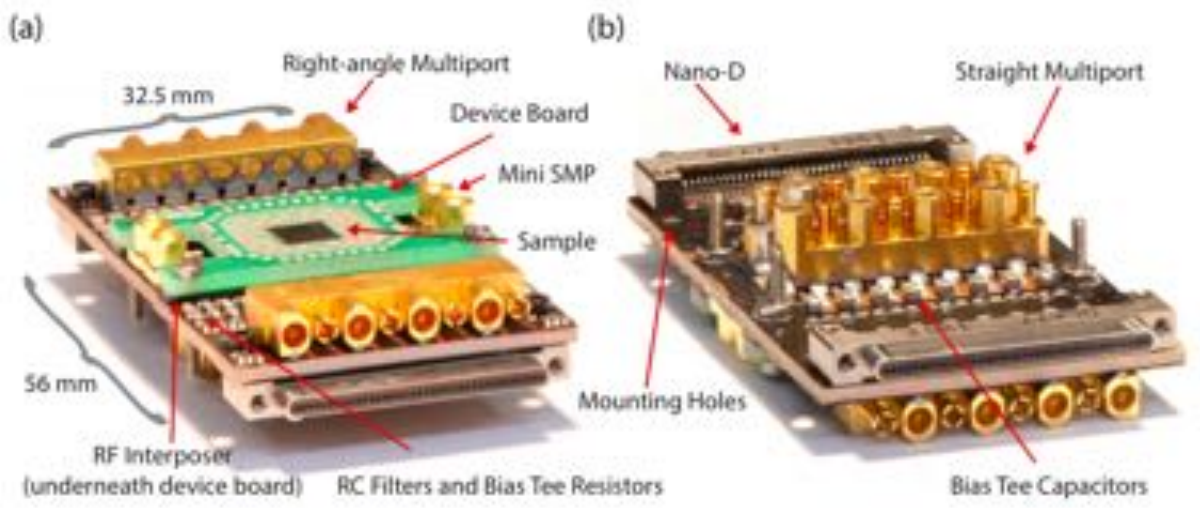
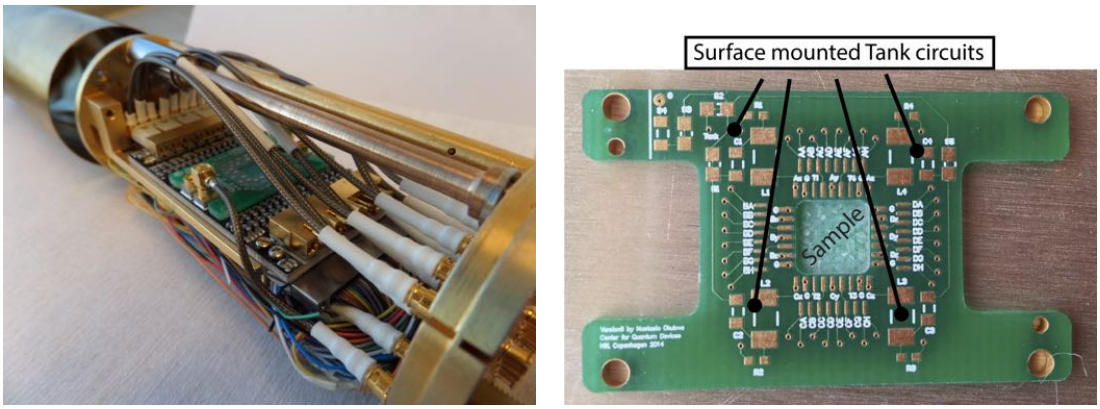


Figure 22: *Overview of the Sydney board. It features up to a total of 74 DC connections through two 37pin nanoD connectors on each side of the board. 36 lines are connected to a coaxial high frequency port through a bias tee, rated ar 5GHz. 4 microwave ports rated up to 12GHz are situated on the top of the motherboard. The sample board is easily swappable for increased flexibility. Figure from [67]*



(a) (b)

Figure 23: *23(a) A sydney board assembled inside the IARPA slug. The DC assembly is tucked under the board. The motherboard is held in place by a set of custom made mounting hardware. 23(b) An example of a swappable daughterboard used for Spin Qubits experiments. The board is designed by N. Okulova with the intention to replace the Mayo board. It features 48 accessible DC lines, 14 fast lines and 4 surface mounted tank circuits that can be configured by the user of the board.*

5.2 Board preparation

Before mounting the sample it is important to ensure that the boards work and fit inside the puck. Following general testing procedures is recommended at least once per each new board taken out of the drawer. In case of a defect this potentially save a lot of time trying to find the problem with the sample cold in the cryostat.

Until recently the lab has been using semi-rigid coax with the "Mayo board". In this case it is important to shape it correctly and test that it fits in beforehand. I would also recommend testing the lines with a network analyzer in case any piece has been unintentionally broken. A broken coax is not necessarily visually apparent, but will expressively show up during a transmission or reflection test.

The next is the configuration of the surface mounted tank circuits. The simple model for the resonance frequency of a tank circuit is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{22}$$

We are measuring mismatch of impedance and at resonance frequency the impedance is given by

$$z \approx \frac{R}{LC} \tag{23}$$

It is known from previous measurements that the most sensitive point is at a conductance value $G = 0.2\frac{e^2}{h}$ and it is dominated by the conductance of the quantum channel. The capacitance is dominated by the capacitances of the bond wires, capacitance of the 2DEG etc. By default the "mayo board" is equipped with varactors that can increase the capacitance to help achieve the matching condition. However it has been determined counter productive, since the self-capacitance of the device is already high as it is and further increasing it though the varactors is impractical. Varactor lines have thus been used as normal DC lines by disconnecting them from the tank circuits by simply removing the surface mounted diode.

The capacitance is largely out of control and can only be optimized through device design. The resistance is mostly dependent on the tuning requirements of the quantum structures such as QPC's or quantum dots. This leaves one way to change the resonance frequency of the tank circuit: by replacing the surface mounted inductors.

For our experiment the default mounted inductors on the mayo board have been replaced with 820nH and 1200nH, which achieves resonance frequencies of 177MHz and 215MHz, which is within the desired range of 100MHz to 400MHz. The remaining two lines were completely disconnected since we only needed two readout lines. For the Sydney board, the most successful configuration was 620nH and 820nH resulting in resonance frequencies around 190MHz and 240MHz.

5.3 Sample preparation

When the boards are configured the sample is ready to be mounted. There is a number of ways to glue the sample to the surface of the sample board. Originally silver paste was used as an adhesive. There were concerns however about the conductive silver paint acting as a capacitor plate and increasing the already unwanted stray capacitance of the device. We opted for a solution of 8% PMMA. For the sample to stay on well it is important to let the adhesive dry out completely. This can be done by either leaving it in a well ventilated place for a few hours or if one wants to save time and avoid contamination - put it into light vacuum. For this purpose plasma oven has been utilized. It pumps out the air down to a pressure of around $10^{-2}bar$, and the sample can be left there for around 10-15 minutes without turning on the plasma.

Bonding is a straightforward process as long as one follows the general guidelines and sets the machine to the correct parameters. The very first touchdown of the bonder head carries a risk of an electrostatic discharge which will potentially blow up the device. One has to make sure both the bonder and the sample are at the same potential. GaAs is conductive at room temperature, so it is advisable to make the first bond to a leftover alignment mark. This bond can later be removed without damaging the real bond pads or it can be left there to provide additional cooling from the ground. Boards are usually grounded with the special shorted connectors[28].

[28]Grounding Sydney daughterboards is non trivial, but one can usually operate floating if one exhibits more caution. Do not leave it unattended for long periods of time and avoid static buildup.

Before starting the bonding process it is crucial that one plans ahead and sketches a bonding diagram. This is not a problem when working with just a few wirebonds, but when working with devices like ones presented in this thesis, one uses the maximum capabilities of the sample boards and this makes the bonding layouts highly non-trivial. In general one wants to keep the reflectometry lines as short and straight as possible. The same is true for the fast lines, but they are usually a second priority. It is also desirable to avoid bondwires going across the device where possible, since one wants to reduce the capacitance as much as possible. There is a certain art to bonding and laying out a good bonding strategy, unfortunately it is something one has to figure out on their own.

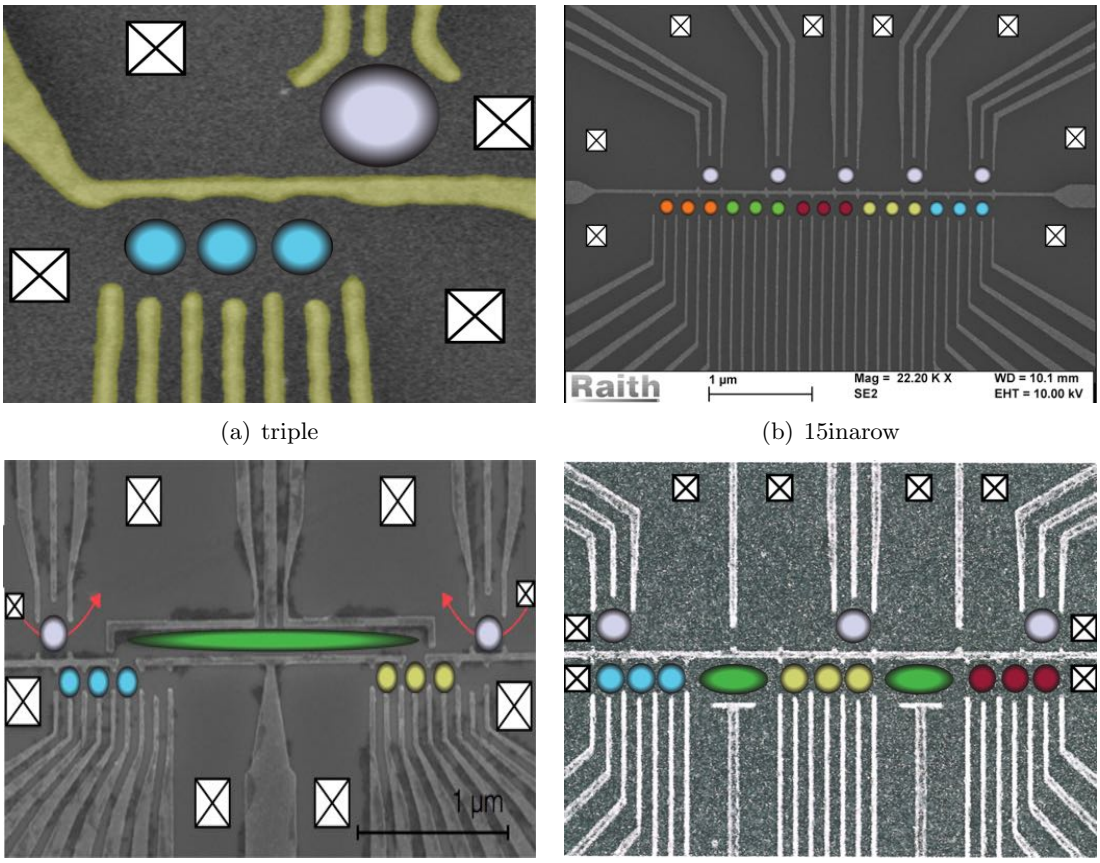
When transporting and loading the sample into the cryostat, there are generally two employed strategies. First is to keep everything grounded at all times. This requires planning beforehand to ensure that connecting and disconnecting connectors does not interrupt the link to ground. Alternatively, some prefer working at a floating potential and only worrying about the relative differences in potential between the pieces. Either strategy has been seen to work. The most important advise here is to be consistent.

5.4 Device geometry back catalog

Over the course of this project many device designs have been created. Some of them were successful, others served as a stepping stone or proof of principle. Several different geometries were explored which aimed to house different qubit types and ways of scaling up to a potential quantum computer.

First designs were variations on the idea of the original J. Medford triple dot resonant exchange qubit[16][43]. The most straightforward continuation was to extend the chain of Quantum Dots and repeat the pattern in a linear fashion as shown in figure 24. This would allow either capacitive or exchange coupling through the edge dots as described in 2.4.1. Designs of up to 15 quantum dots in a row were fabricated with the idea of being able to contain up to 5 qubits. Several of these we cooled down over the course of the project. However there were several key challenges with this approach. Tuning up 4 Quantum Dots in series has been demonstrated[68], however the strategy for tuning up more than that is largely unknown. The charge stability diagram for 4 quantum dots in series get complicated and anything beyond that becomes impractical to work with. Hence one would fall back to tuning up each qubit separately. Our strategies for tuning up a triple dot rely on being able to load and unload electrons. In a situation where the neighboring "qubit" is tuned up, the transport will be heavily restricted thus preventing us from easily loading or unloading electrons during the tuning process. In an experiment of device NO7 (linear 15 quantum dots in a row) made by Nastasia Okulova and measured with the help of the author, we were able to form quantum dots at each position by themselves, however attempting to go beyond one triple was challenging. Two triple dots were tuned up, however the difficulty of operation prevented any further study of the system.

Since each qubit needs a load/unload channel for tuning a logical step would be to make a device that allows just that. Figure 24(c) and 24(d) show next generation of devices, where each triple dot get it's own set of ohmic channels for loading and unloading. Design in figure 24(c) is coupled by a floating gate coupler that will increase the capacitive copling between the two qubits. Additionally, depending on the position of the three dots within the 4 dot framework, one can choose between coupling through the side or the middle quantum dots. Design in figure 24(d) employs similar strategy, but adds an additional possibility of coupling the two neighboring qubits through a high-fidelity exchange interaction using a multi-level quantum dot[20]. This is achieved by closing the ohmic channel using the corresponding gates to form large discrete level systems.



(a) triple

(b) 15inarow

(c) doubledogbone

(d) triplesausage

Figure 24: *SEM images of device geometries fabricated over the course of the project. Color circles indicate quantum dot positions, squares define ohmic contacts. Light purple circles are idicate the positions of the sensor dots used for reflectometry and charge sensing. 24(a) A triple dot device originally made by J. Medford. It features a triple quantum dot which contains the qubit and an auxillary quantum dot used for charge sensing. 24(b) A linear design built on the same principle as the original triple dot device. Contains 15 total (5 sets of 3) quantum dots that were expected to contain 5 qubits and 5 quantum dots used as charge sensors. 24(c) Double qubit device. Contains 2 sets of 4 quantum dots intended to be used as a triple dot. Two triple dots are connected by a floating gate coupler intended to increase the capacitive coupling between the qubits. 4 lithographically defined quantum dots on either side allow coupling between either middle or side quantum dot. Adapted from [54]. 24(d) Triple qubit design featuring 3 exchange-only quantum dots. Each qubit has a reservoir of electrons on either side that allow loading and unloading independently of the other qubits. After tuning, the reservoir can be closed by the coupler gates to form a discrete system that can efficiently mediate exchange interaction between the adjacent qubits.*

5.5 Qubit is sotware concept

"Qubit is Software" is an idea proposed not so long ago in an attempt to unify different qubit technologies in one device, figure 25. In theory, there is no reason why given the right tuning parameters $S - T_0$ qubits couldn't occupy the same position as an LD qubit. Even an exchange only qubit based on a triple quantum dot geometry would be possible within the confinements of the same device. Devices exploring this idea have been fabricated, but encountered several technological limitations. Given that Spin Qubit technology is in it's infancy, current fabrication strategies involve optimizing devices for a particular experiment. Optimal parameters in terms of material, dimensions and even gate layouts differ quite heavily. For instance, it has been

experimentally observed that being able to tune up double quantum dots in either leftmost or rightmost positions of a gate defined triple dot design might not translate into an ability to tune up a single triple dot within the same geometry of given dimensions. In the future however, once we are able to print any number of qubits on the same chip reliably, this idea should be revisited.

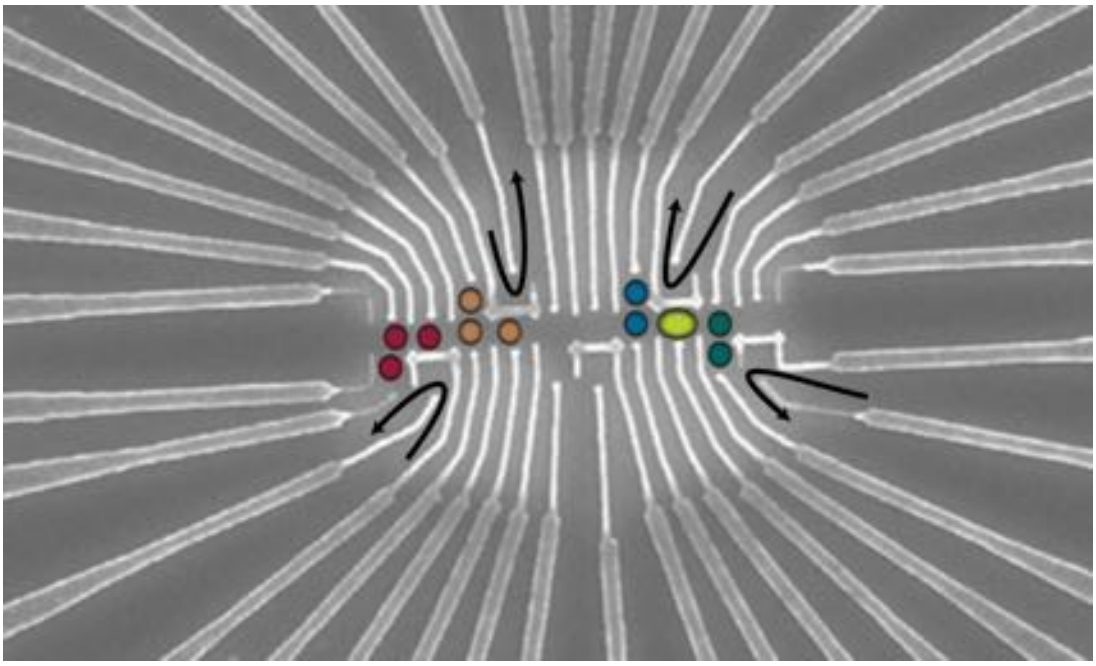


Figure 25: *Micrograph of a prototype device design illustrating "Qubit is Software" concept. One could imagine a number of spin qubit types realised within the same device, differing only by tuning parameters. In this case two triple-dot exchange-only qubits are tuned up (red and orange), each with it's own sensor(black lines) and two double dot ST_0 qubits coupled via a Jelly bean coupler(yellow). Both sides could then be coupled capacitively or via exchange through an additional Jelly bean coupler in the middle. The opportunities are endless.*

6

EXPERIMENTAL TECHNIQUES

This section describes some of the most common experimental procedures performded during the phase of setting up the experiment.

6.1 Bias cooling

To prevent charges from tunneling through the low Schottky barrier in GaAs[25] as explained in section 2.1 positive voltage is applied while at room temperature and all the way until the base temperature when the 2DEG is formed and charges are "frozen in". This has been done for most cooled down devices ranging from 350mV and all the way down to 50mV. A general rule of thumb is to bring the operating voltage of the gate to zero volt. This is achieved by first cooling down the device with no bias applied and measuring the negative voltage at which the underlying 2DEG is depleted(taking pinch-off curves). On the subsequent cooldown a positive voltage would be applied of the same absolute magnitude to linearly shift the *pinch-off* point to a more positive point in gate space. Some experience indicates that applying a finite positive bias to the gates during cooldown might be sufficient, because GaAs is conductive at room temperature and the electrons would fill all the available states even in the presence of a small field.

In practice this is a non trivial operation that requires some planning before execution. The cryostats are loaded through the bottom which means that electrical contact with the breakout boxes will only happen when the sample puck engages the coldfinger. Additionally, unless the cryostat has been warmed up to room temperature prior to loading, the coldfinger itself would be at around $50K$. 2DEG in GaAs is formed at around $70K$[24] which means that one would have a limited and fairly short amount of time to apply necessary bias to the right gates. Instead this is done through the bottom nanoD connectors on the Puck Loading Stick(PLS). Spare breakout boxes can be connected to the bottom of the PLS and then biased through the bias line using a voltage source like the Keithley 2400 Source Meter. Corresponding lines on the top should also be biased by the same source and left open. This will prevent any voltage drop through the device, once the puck engages.

Because GaAs is conductive at room temperature, a sizeable leakage current can be measured running from the biased gates through the material and into other pads, like ohmics, that should be left grounded. This is illustrated in figure 6.1. After the puck engages, the current will start to drop as the sample begins to cool down. In a few minutes GaAs will become insulating and 2DEG will form. At this point the current will flatten out at a very low value. Once this happens, one can in principle disconnect the voltage source as the charges have become immobile and the require effect has been achieved.

6.2 Device testing methodology

After the fabrication step is finished and the device itself is bonded up and ready to be cooled down it is difficult to know whether the intended experiments would be possible with it. The

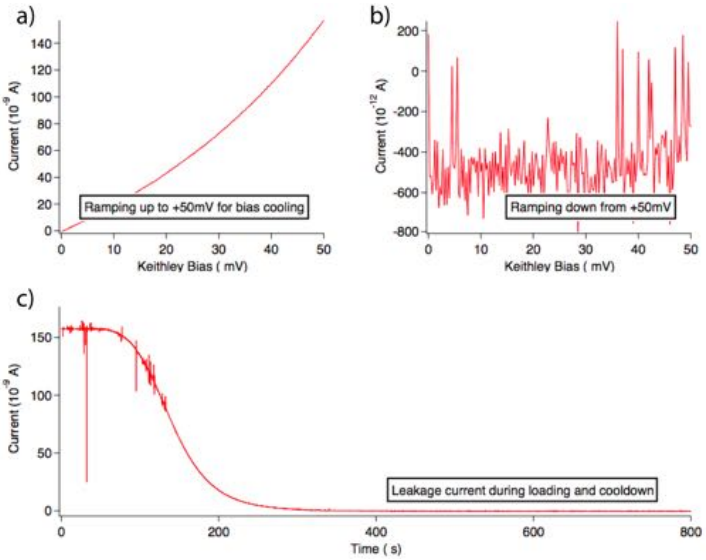


Figure 26: *Bias cooling. a) Ramping up the voltage source to a desired value at room temperature produces leakage current of around* $140nA$*. b) Monitoring leakage current during loading and after contacting the coldfinger. The leakage current quickly drops to near zero as the GaAs becomes insulating as the sample cools down after contacting the coldfinger at* $60K$*. The noise spikes are an effect of physical c) Ramping the voltage source down to zero at base temperature does not have an effect on the leakage current indicating that the procedure was successful. We consider leakage current on the order of picoamperes is effectively zero.*

first cooldown would normally be a test cooldown that determines whether the device is operational and whether it has the potential to work. This section will describe the initial tests that determine whether the device stays cold or goes into the trash bin.

6.2.1 Ohmic and electrostatic gate tests

Step one is ensuring that the Ohmic contacts and the electrostatic gates are working as intended. For the Ohmics a criteria for "working" is a low resistance contact to the 2DEG at base temperature. A test is performed by setting all ohmic contacts to ground and sourcing current into each ohmic individually using the Keithley 2400 source meter(referred to in the lab lingo as simly keithley). $\pm 100\mu V$ is sufficient. A typical "good" ohmic resistance is on the order of a couple hundred ohms, with typical resistance around 500 Ohms. Since the ohmics would be grounded on the break out box, an additional resistance of around 8kOhms would show up since the line passes through the RC filters twice, one on the way down and one on the way up[29]. The 2DEG sheet resistance will also contribute, however it is insignificant on the order of Ohms[30]. Needless to say, the Ohmic contacts is the most important part of the device and should they fail, the device is useless.

The electrostatic gates are the second most important part of the device. The "working" criteria for electrostatic gates are: no lithographic errors such as being shorted to a separate gate and ability to deplete the 2DEG. Two tests are usually performed. The first tests for lithographic errors in form of the shorting to other gates. For this test, all gates are set to ground on the breakout box and a small voltage is sourced onto each gate separately using the Keithley 2400 sourcemeter. The beauty of the keithley is that it can both source a voltage and

[29]since all ohmics are grounded together (in parallel) the actual resistance might be different, yet still in the same ballpark

[30]as measured once using a 4 terminal lock in measurement

measure the current. If the gate is shorted to anything else, a current will show up, in which case the leakage can be localized by means of elimination. The easiest way to perform the test is to use the bias line and the bias switch on the breakout box.

The second test tests the functionality of the electrostatic gates with respect to their ability to deplete the 2DEG. A setup with a voltage source(keithley or dac) and an amperemeter(see sec. 3.2.2) is required. Voltage is applied to the gate, while the transport though the 2DEG is measured. If the gate is functional the current will drop as the 2DEG is depleted. The point at which the current flow stops, i.e. *the pinch-off* point can be moved in the subsequent cooldown through the bias cooling techique described in section 6.1.

6.2.2 Reflectometry tests

Testing the capability of performing fast measurements is crucial, and is possible at the early stage of the device testing. Since the idea is to match the channel impedance to the line impedance, the sensor gates are pinched off while the reflected signal is monitored using a Network analyzer(see figure 13). As the sensor channel resistance increases, the reflected signal will move from maximum reflection when the channel is open and through a resonance where almost nothing is reflected. This test does not necessarily represent the conditions when the relfectometry sensing would be implemented for sensing an actual qubit in the device, but will give the information of whether the any lines are broken and at which channel resistance the matching condition is satisfied. The best sensing has been empirically determined to be at around $0.2e^2/h$[31]

7 EXPERIMENTAL MEASUREMENTS

When planning the experiments in your head, the way forwards looks pretty clear and intuitive. Reality is however much more grim. It is very hard, if not impossible, to foresee the implications that might arise when the measurements begin, and as such one enters a regime with multiple iterations and hitting the head against the wall in an attempt to make sense of the measurements.

After a long time with perfecting the fabrication procedures, several device geometries emerged as promising ideas for what could be implemented. As described in section 5 several ideas had to be changed or adjusted to accommodate for various deadlines and hardware limitations. This way a "15 in a row" design was scrapped after receiving preliminary results from a parallel group. One of the goals was to test if a large multilevel quantum dot would serve as a good long range coupler and mediator for multiple spin qubits. It was determined, that making such a quantum dot in that particular design was difficult if at all possible, since the dimensions were originally optimized for single electron or simply small quantum dots. The next logical step was to introduce a geometry where small quantum dots could easily be tuned up and could coexist with easily tunable large quantum dots. Hence, the triple-triple design was born(figure 24(d)). Equipment availability and maintenance are very important parts of an experimentalists life. After some time it was discovered that the cryostat had to be fixed and the device taken out. After fixing the cryostat, a decision has been made to switch to a different type of devices, that could still house the intended experiment and also potentially other concepts. Both experimental attempts are presented in this chapter, with the rationale behind the decisions that were made during the measurement process.

7.1 Triple-triple design

The first device that satisfied all the criteria for being "alive" had the codename JB_TTL_14. A fourth batch of it's kind with the first ones having broken gates or the dimensions being too small to be able to tune up quantum dots. The idea for this device was to potentially be able to implement 3 exchange only qubits, each separated by a large mediator quantum dot - the jelly bean. In the end it was possible to tune up a triple dot in each intended position individually, however, tuning up all three was not possible. Additionally problems with charge sensors and fast lines in the cryostat eventually lead to the device being replaced.

7.1.1 Initial testing and first cooldown

After cooldown all electrostatic gates were tested and found functional. Additionally, when testing the reflectometry, it was possible to pick up all 3 resonances from the 3 sensors.

Living off the experience from cooling down several devices of the same type, it was possible to roughly predict the required positive voltage for the bias cooling. It was seen previously on the same material that bias cooling does make the devices less noisy. It was decided to apply +200mV positive bias on initial cooldown.

Initially the device appeared very quiet with no spontaneous shifts or charge fluctuations. However, upon having spent time with the device it became apparent that electrostatic shifts on the order of hours or even days were present. These long time fluctuations eventually disappeared after working, shifting gate voltages, on an area of the device for around a week. What this meant originally is that attempting to set up long overnight scans with high resolution was very difficult once we moved on past DC transport measurements. Charge sensors tuned up in the evening would be driven out of their narrow sensitive region by a random jump, meaning the data acquired would be useless noise.

7.1.2 Tuning up triple dots

After "aging" finished it was possible to tune up triple quantum dots in every triple dot position on the device. The general strategy was first to form a large quantum dot using only the outside *wall* gates, the gates that control tunneling to the leads, then break it up into smaller quantum dots until eventually getting into a triple dot regime.

Following the procedure described in sec. 2.2.1 a single quantum dot could be formed. This is easiest done measuring DC-transport through the quantum dot. The bias was usually set to around $50\mu V$. After the wall-wall scan was taken, wall voltage is set symmetrically such that the conductance is at approximately $0.2e^2/h$. This should already form a single quantum dot.

The voltages on all of the gates inside the triple dot region, all plungers and two barriers, are then slowly ramped more negative. From this point on the scans are taken with the outer plungers, called left and right plunger because of their placement in leftmost and rightmost quantum dot respectively. This makes the quantum dot smaller and at a certain point multidot signatures will appear in form of additional transition lines. At this point it might no longer be possible to pick up enough signal in DC transport, so one would usually switch to charge sensing.

As the middle gates become more negative, one might see transitions that are broken up into pixelated areas. This is called latching and happens because the tunneling event is slower than the measurement time. If this happens, the most restrictive gates, in this case the outer walls, should be made more positive, by approximately a few millivolts. If the quantum dot does not easily break up into several quantum dots, a good idea is to explore the voltage space of the middle plunger by taking (left-right) plunger-plunger scans while stepping the middle plunger by 10-20mV.

Since all gates a capacitively coupled it is advised to set the voltages on all electrostatic gates to approximately half their pinch-off value. This will help offset the negative effects of cross-capacitance for subsequent tuning, by reducing the absolute voltage difference between tuning the first qubit alone and tuning additional gates of the neighboring qubit. The effects of cross capacitance can be quite large, for instance when tuning the left qubit it was found that changing the voltage on the left plunger in the middle qubit effectively corresponded to changing the voltage on the right plunger of the qubit 3 by 1/7 of the voltage.

7.1.3 Forming multiple triple dots

After tuning up the first triple dot in the position of Qubit 3, the next logical step was to tune up a triple quantum dot at the position of Qubit 2. Gates within the Qubit 3 were set to the reference positions of around half way to depletion. However, regardless of how hard we tried, it was not possible to form a large quantum dot in the position of Qubit 2. The next strategy was to completely remove the voltage from all other qubit gates. Upon setting the gates within qubit 3 to zero, we could suddenly see Coulomb oscillations while in DC trasport from the large

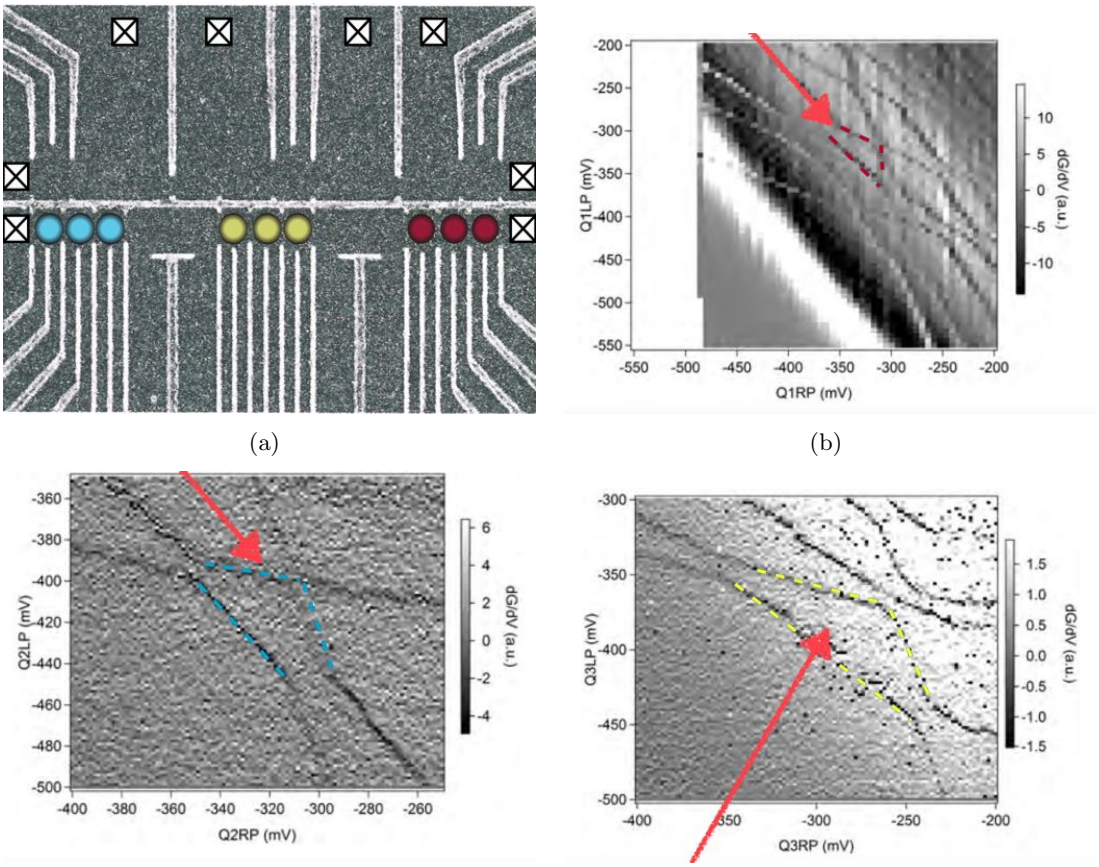


Figure 27: *Tuning up device TTL_14.27(a) Micrograph image of the device. Circles indicate the positions of the quantum dots, transport is measured between the Ohmic contacts(S-D). 27(b) First triple dot formed 27(c) Second triple dot formed 27(d) Third triple dot formed. Colors match the outlines of the* $(1, 1, 1)$ *region. Figures 27(b), 27(c) and 27(d) adopted from [54]*

quantum dot in qubit 2. It seems that the cross capacitance from the gates in qubit 3 were obstructing our ability to tune up any quantum dots in the position of qubit 2.

Surprisingly, voltages on the gates within Qubit 1 did not have the same effect. After extensive tuning it was possible to tune up two triple quantum dots simultaneously in the position of Qubit 1 and Qubit 2. The electrostatic cross coupling between the two qubits was very strong, as mentioned previously. Moving the plunger gate within qubit 2 by 150mV would correspond to moving the plunger in Qubit 1 by approximately 20mV.

Another problem encountered during the cooldown was the "oscillating potential" that would change the required voltages to deplete a channel by up to 200mV. These drifts were slow on the order of days and could be removed by setting all qubit gates to zero for a few minutes. One possible reason for it could be the large patches of electron gas in the position of the large jelly bean couplers forming a kind of a floating metal and slowly changing it's potential disrupting the tuning process.

7.2 Butterfly design

The butterfly design(shown in figure 28) is intended as a flexible platform for a number of ideas. The two sides of the device are symmetric on the device level. Quantum dots can be formed in all or either of the three positions of the each side of the device denoted as Qubit 1 and Qubit

2. For instance one can imagine tuning up two full exchange-only triple quantum dot qubits on each side of the device operated independently. Alternatively a ST_0 qubits could be formed in either left-center or right-center quantum dot positions. The coupling between the two sides of the device can be made capacitive through floating metal, by restricting tunneling to and out of the middle jelly bean region, or it could be implemented through a discrete system through an exchange interaction similarly to the RKKY-like interaction described in section 2.4.1. The quantum dot in the middle, i.e. the Jelly bean can be tuned independently of the qubits by it's own set of plunger gates. The electrostatic gates colored in red indicate a fast rf-line connected through a bias tee. This enables control of the quantum dots via fast pulsing.

The sensing is performed through two quantum dot based charge sensors on either side of the device. To further increase their sensitivity a capacitive dog-bone is placed between the outer quantum dots within the Qubit regions and the sensor. Attempting two qubits interactions through a capacitive dogbone has a negative influence on the qubit coherence times, however can be safely implemented for sensing[69][15]. Both sensor quantum dots can be operated using the reflectometry technique(section 3.4) for fast sensing and potentially single shot readout.

Additionally gates M1 and M2 would connect to a micromagnet, in this case Co, which can be magnetized by applying an external magnetic field and will introduce a magnetic field gradient necessary for LD[39] and ST[70] qubit operations.

7.2.1 Tuning up the jelly bean

To verify that the coupling via the middle is possible a single quantum dot has been tuned up the in Jelly bean region. First the backbones B1 to B4 were pairwise pinched off to ensure that it was possible to control transport through the middle channel. The pich-off curves for such a system become pich-off plots, since it is important to step both gates together. Similarly to making a gate controlled QPC, we set the conductances on for each pair of backbones approximately around $0.8e^2/h$ after which we attempted to tune up a single quantum dot by measuring transport as a function of gates QS1 and QS2 while stepping QS3 in steps of 10mV. It was possible to quickly tune up a large quantum dot as shown in figure 29.

When initially checking the Jelly bean, the gate voltages required were rather large[31]. When we later returned to the Jelly bean with qubit gates set to approximate voltages required for double and triple dots, the required voltages have shifted dramatically. This indicates a large capacitive cross coupling between the qubit and the Jelly bean gates which might be problematic for fine tuning. Upon making the plunger gate QS3 more negative the Jelly bean quantum dot would also break up into several smaller dots. The voltage on QS3 at which the Jelly would break down into small dots was around $-50mV$. This is a problem because it essentially means that the gate does not deplete the 2DEG underneath it but rather pushes it aside. This can be solved in two ways: reduce the positive voltage when bias cooling or omit it from the bias cooling completely, or fabricate a new generation with this gate positioned further away from the opening in the backbones[32].

7.2.2 DC spin blockade in a double dot

A double dot could successfully be tuned up in the qubit 1 region of the device. The backbones were left at a setting where a Jelly bean could exist, but with tunneling into the Jelly bean

[31] large with respect to our self set maximum of approx 1V. This value is passed on through generations of experimentalists and is thus more of a superstition. Although nobody wants to be left with a blown up device, so it's rather hard to find someone to test this limit.

[32] interestingly enough this conclusion was reached before this device saw the cold darkness of the fridge. The batch of devices with that exact adjustment has been fabricated, but had failed due to equipment error and was not viable for cooling down. Due to time constraints, the cooled down devices were from an older generation.

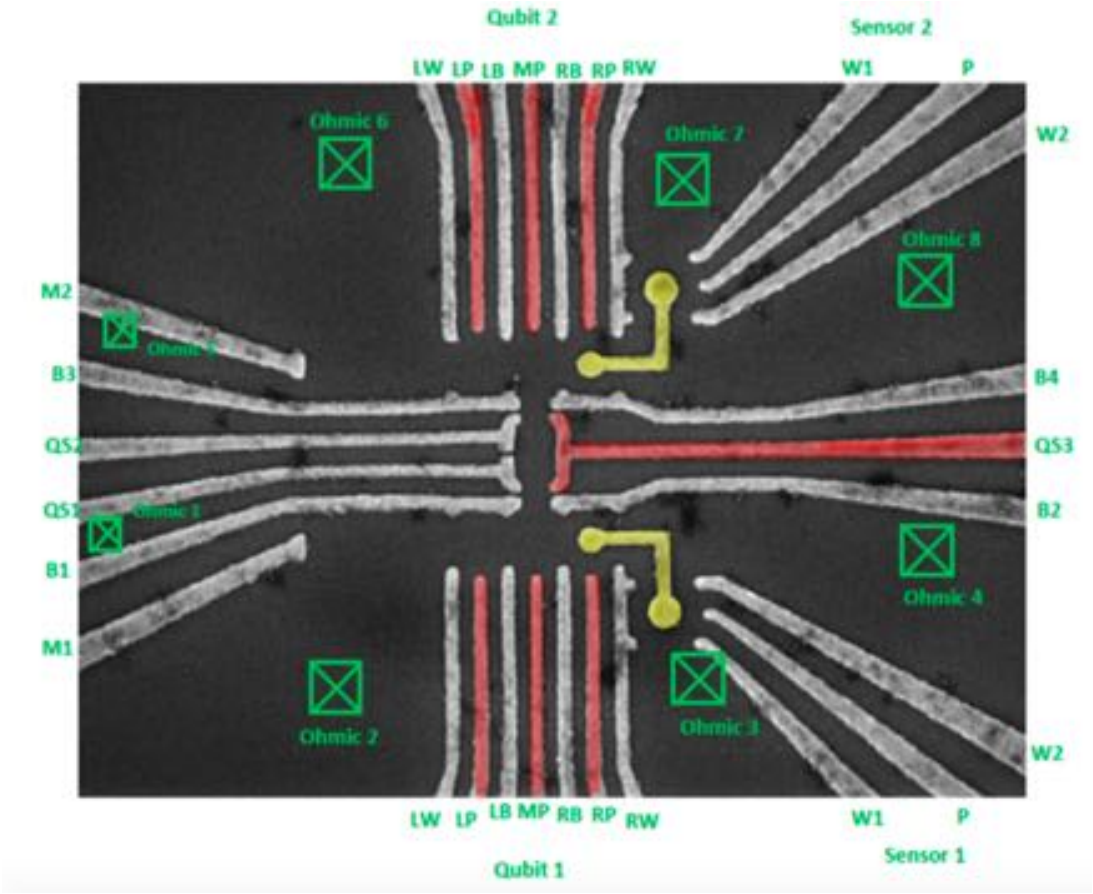


Figure 28: *Micrograph image of the butterfly device. It is designed as a flexible platform for multiple spin qubits experiments. Each side of the device features 3 gate defined quantum dot positions with a sensor quantum dot on the side connected by a floating capacitive dogbone(yellow) to the rightmost quantum dot. Qubit gates are named after the exchange-only convention. From left to right: Left Wall(LW), Left Plunger(LP), Left Barrier(LB), Middle Plunger(MP), and so on. The 4 gates in the middle that are used in the most static fashion are called Backbone('s) and are numerated backbone1 through 4. The two sides are coupled through a quantum dot in the middle that is referred to as a Jelly bean coupler. The jelly bean has it's own set of electrostatic gates - QS1, QS2 and QS3. Gates M1 and M2 were originally intended as a grounding gate for the micromagnets. Gates highlighted in red are fast gates. Ohmic arms are shown as green boxes and numerated accordingly.*

region heavily suppressed by increasing the negative voltage on the backbones by 10mV. This way, should we ever have needed to allow tunneling between the Jelly bean and the double dot, adjusting the tunnel barrier would not interfere much with the double dot tuning.

The double quantum dot was tuned using the same methodology as described previously for a triple dot. The wall-wall scan measured in transport gives the right values for the formation of a single large quantum dot. Subsequently, making the middle tunnel barrier more negative breaks up the large quantum dot into two small ones. Figure 30 shows the result.

An attempt was made to tune up a system as a Singlet-Triplet qubit. In plane magnetic field of 200mT was applied to split the degenerate triplet like levels away from the $S(1,1)$-$T_0(1,1)$ anticrossing. The magnetic field gradient between the quantum dots is provided by the random Overhauser nuclear field gradient originating from the nuclei inside the quantum dot[41]. For readout the conventional spin to charge convention was employed.

The tunnel rates were suppressed to a point where tunneling is only possible at the tripple point. Pauli Spin blockade could then be localized in DC transport by reversing the bias a

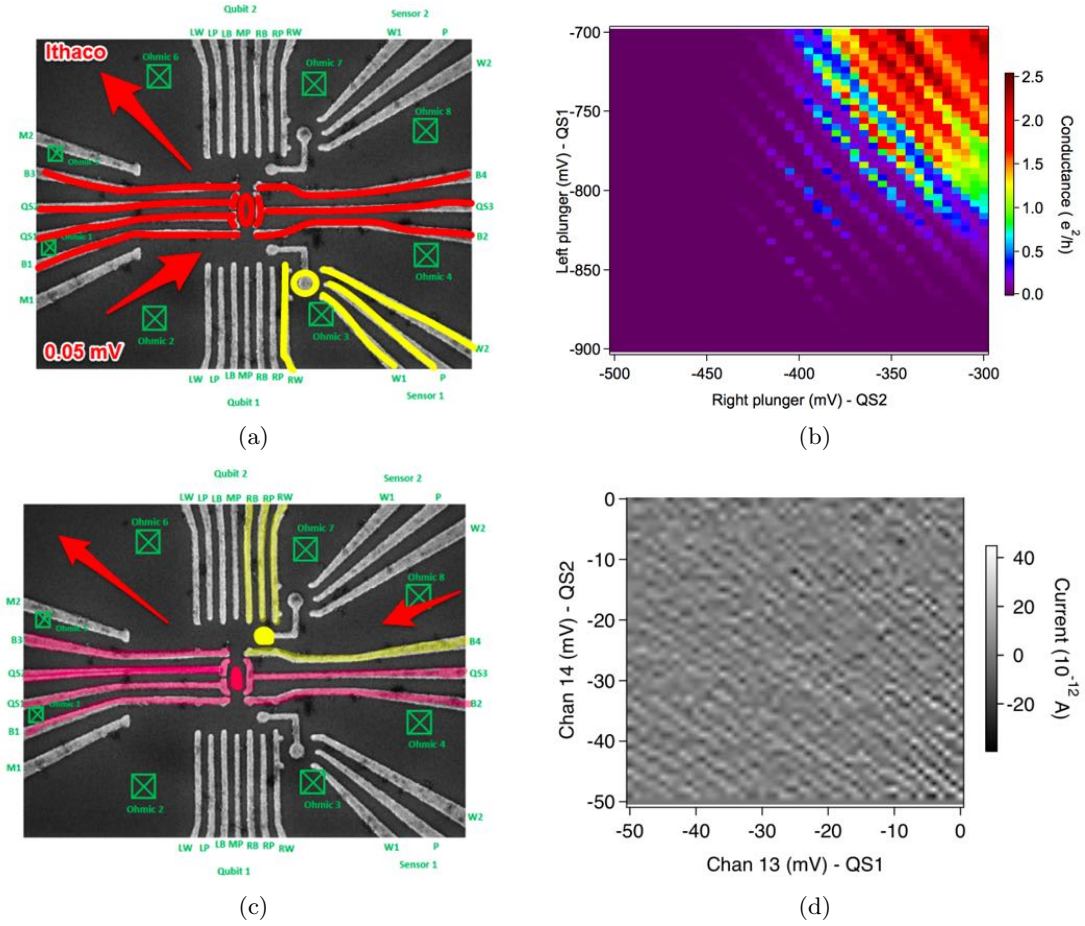


Figure 29: *Tuning of the Jelly bean couple dot29(a) Micrograph image of the device. Circles indicate the positions of the quantum dots, transport is measured between the Ohmic contacts(S-D) along the directions of the arrows. Yellow quantum dot can be operated as a charge sensor. 3(c) A quantum dot forming in the jelly bean region with all electrostatic gates that are not involved in tuning set to zero. Bias $+0.2mV$ 29(c) Charge sensing of the jelly bean using a quantum dot on the opposite side to Qubit 1 location of the device. Transport through the sensor is measured along the red arrows from S to D. Bias $0.05mV$ 27(d) Charge sensing the jelly bean with all other electrostatic gates set near their operation voltage. The capacitive cross coupling from the other gates pushed the operating voltage of the jelly bean close to zero as can be seen from the differentiated conductance plot. Diagonal lines correspond to transitions in the jelly bean. Level spacing is very small, and indicates a large quantum dot being formed.*

inspecting the bias triangles. At the bias of $\pm 0.4mV$ a spin blockaded transition was found as shown in figure 30. The transport is possible at negative bias, but is suppressed for the same transition if the bias is reversed. Electron relaxation by coupling to the leads is possible, this is visible by transport being possible around the edges of the blockaded triangles triangles.

7.2.3 Pulsed spin blockade and Single Shot capability

Seeing a Spin blockade in dc transport is great, however, if one wants to use the phenomenon for spin-to-charge conversion the state of the system needs to be determined faster, in a single shot. Single shot readout is one of the requirements for quantum computations[4]. With single shot readout the state of the system is determined in a single shot, rather than taking an average of a lot of events.

Having found the blockaded transition the fast control circuitry is connected. We connect

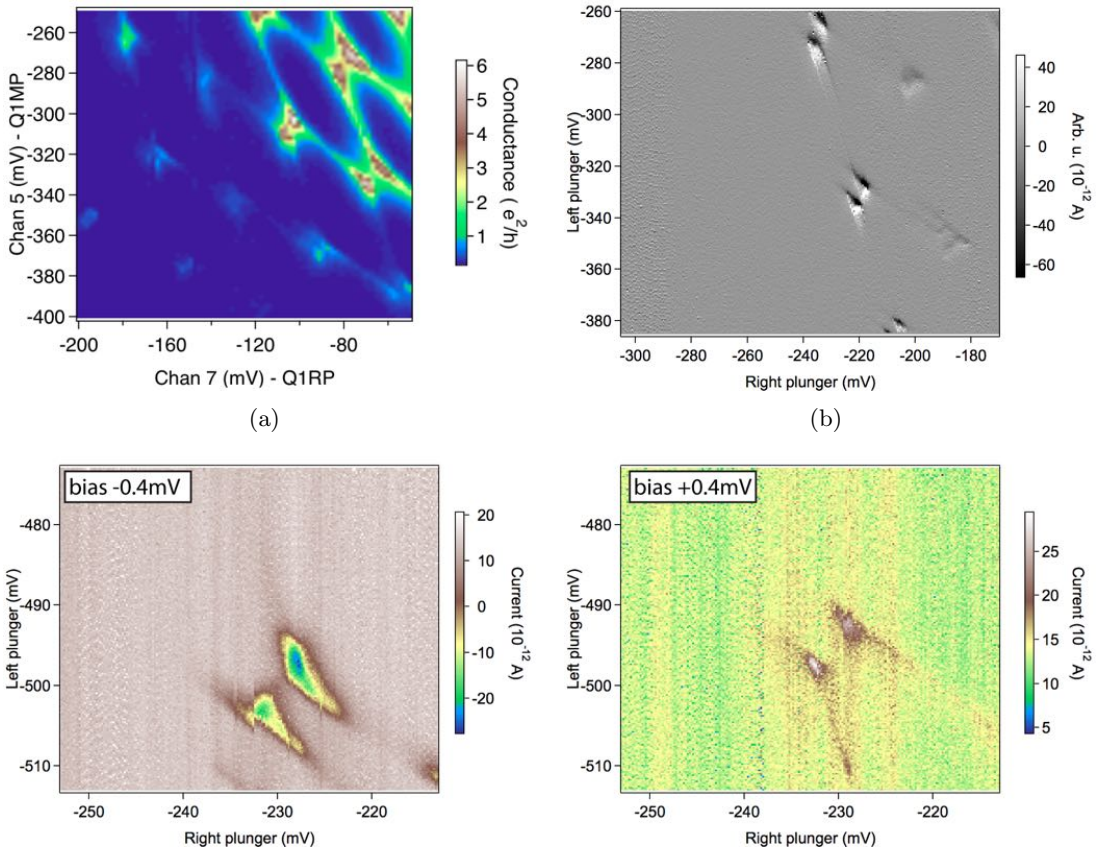


Figure 30: *Pauli spin blockade in DC trasport 30(a) DC transport through the double dot. At more negative regions of gate voltage space the level spacing is larger and fewer levels fit into the bias window. Transport becomes only visible at triple points. 30(b) Differentiated conductance plot showing transitions of interest. 30(c) One of the transitions in a double dot. At negative bias the current runs through 30(d) Upon reversing the bias at the same transition it is apparent that the current flow is blocked and is only possible at the side of the bias triangles where electrons can exchange with the leads.*

the Tektronix AWG5014a through a splitter to the fast gates on the device. The pulse is calibrated by applying a "10mV" square pulse to the gate in software[33] with a duty cycle of 70-30. When taking a charge stability diagram with the pulse on, one would see a doubling of the corresponding transition, with the more pronounced one being the $+10mV$ and the more washed out one being the reference. The software division factor is then changed until the spacing between the doubled transition lines corresponds to 10mV in gate space.

Through using pulse sequencing we are able to create a custom waveform that will take us around the transition. The pulse shown in table 1 is constructed.

The measurement is done in the blockaded region by parking in the correct position of the gate voltage space. The electron is first thrown away by exchanging it with the lead, crossing into the $(0,1)$ like region during the Relax/Exchange step. An electron is then loaded into a $(1,1)$ like state during a Load step. Since the electron which gets loaded is random, sometimes it will end up in a singlet like $S(1,1)$ like state and otherwise in a triplet like $T(1,1)$ like. A final

[33]since there is a number of attenuators and filters on the line before the sample the actual amplitude at the sample will be different. "In software" means that the AWG will output a with an amplitude it thinks is 10mV. In reality a software division factor is what needs to be calibrated.

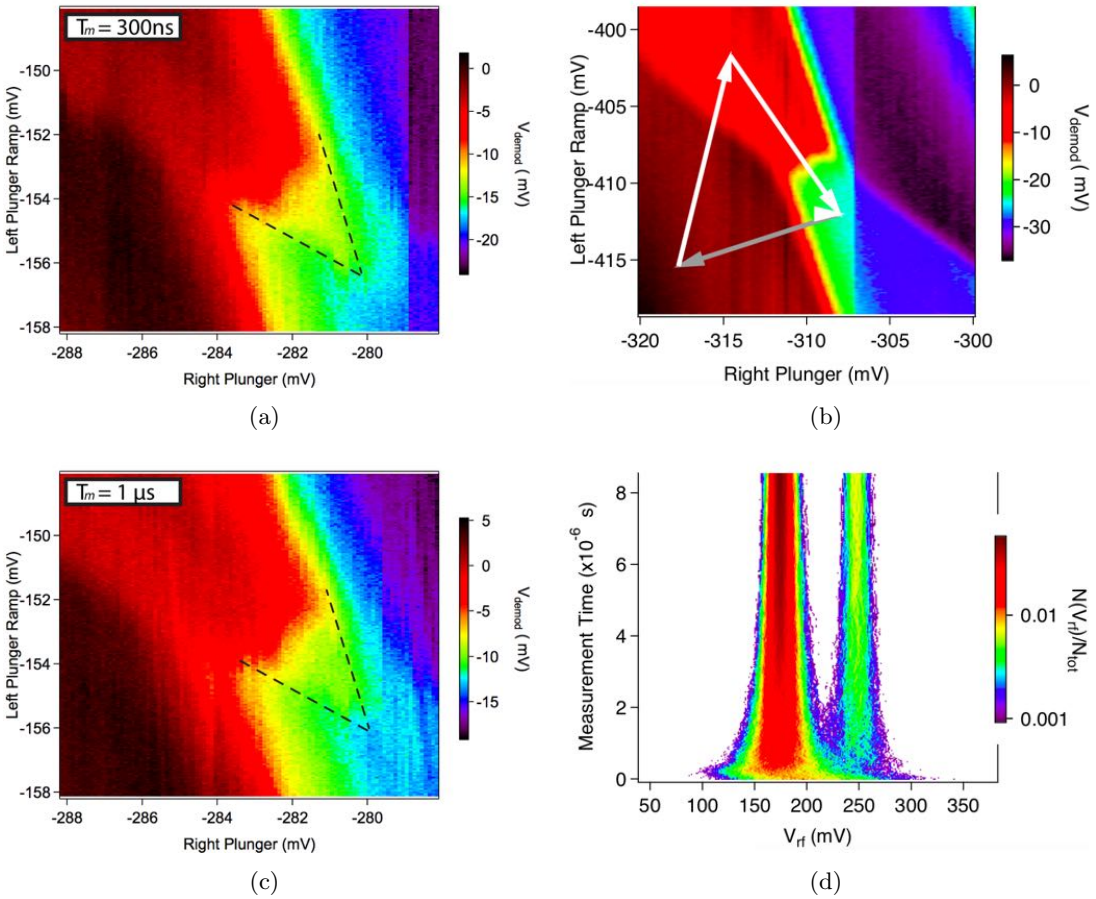


Figure 31: *RF spin blockade in device NO9b.31(a) and 31(c) Transition between* $(1,1)$*-like at the top left and* (0.2)*-like at the bottom right(actual occupation is proportionally higher). When a triplet-like* $T(1,1)$ *is loaded into the double dot, the transition is blockaded for the subsequent gate pulse. For* $300ns$ *measurement time the charge state extends into the* (0.2)*-like region. For* T_m *of* $10\mu s$ *the electron spin relaxes and can tunne through, so the extended region disappears. 31(b) A schematic of the pulse sequence overlaid onto the* $(1,1)$*-*(0.2)*-like transition. The gray arrow is the initial pulse that throws out an electron out of the double dot. The second pulse then loads a new electron from the leads into the* $(1,1)$*-like region. The last pulse takes the electron back into the measurement point in the* $(0,2)$*-like region where the measurement is taken by reflectometry. 31(d) Optimizing single shot readout. A histogram over the tunneling events following as a result of the pulse sequence described in table 1. After approximately* $3\mu s$ *integration time the singlets and triplets can be clearly distinguished.*

Table 1: Pulse table for finding a pulsed spin blockade

Point	Time	Carrier waveform
Measure	Varied	ON
Relax/Exchange	$300ns$	OFF
Load	$150ns$	OFF

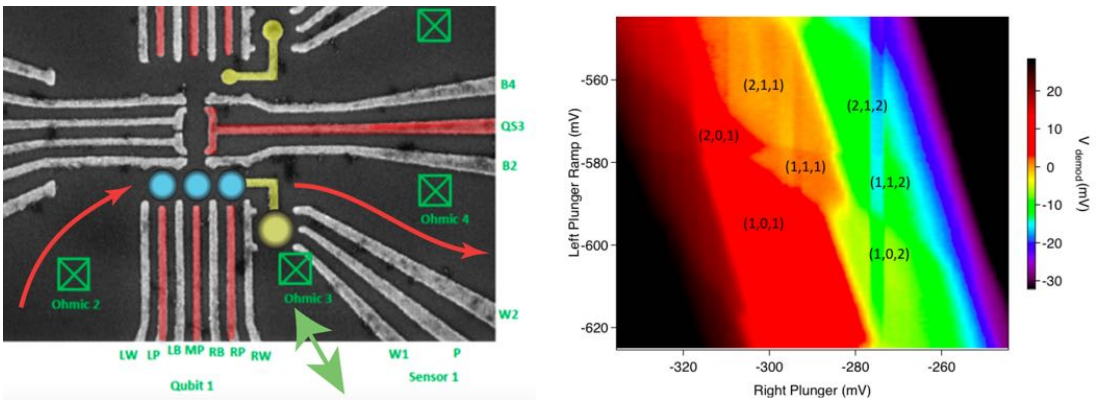
pulse then takes the electron to the measurement point. Depending on it's state, the singlet like will be able to tunnel into a $S(0,2)$ like state, while the triplet will get stuck. The measurement will show the corresponding charge sensing signal "spilling over" into the $(0,2)$ like region. This is exactly what is see in figure 31(a). The measurement time is varied eventually, but can be set

to $300ns$ initially. In the measurement region we average the signal, so the measurement time has to be shorter than the spin relaxation time T_1. After measuring for $10\mu s$ the spin blockaded region disappears completely as shown in figure 31(c).

Figure 31(d) shows the two DC signal levels of the charge sensor in relfectometry, with the lower corresponding to a singlet-like configuration and a higher to a triplet-like. Singlets and triplets can be reliably distinguished after integrating for approximately $3\mu s$.

7.2.4 Tuning a triple dot

As a proof of principle a triple quantum dot was tuned up in the lower qubit 1 region of the device(figure 32). A spin blockade is possible in a similar fashion to the one in the double dot. Additionally one would expect to see blockaded triangles on both sides of the triple dot. A diagonal pulse was applied corresponding to changing the detuning by $\pm 15mV$ which corresponds to approximately half the width of the $(1,1,1)$ region. After extensive tuning no signs of spin blockade were seen. This could be due to rather poor signal to noise ratio and power broadening of the lines due the reflectometry signal. The carrier signal power was later reduced from $-72dBm$ to $-76dBm$ that solved the power broadening issue, however there was still a lot of noise from an unidentified source. The war on noise is described in more detail in the subsection 8.2.



(a) (b)

Figure 32: *Tuning a triple-dot in the "butterfly device". 32(a) Blue circles indicate the position of the quantum dots, Yellow circle is the position of the charge sensing. Greed double-pointed arrow indicates reflectometry setup. DC transport can be measured along the red lines. 32(b) A charge stability diagram taken with reflectometry as a function of voltage on left plunger(LP) as a function of right plunger(RP). A distinct "house" structure indicating* $(1,1,1)$*-like region with the total occupation higher than 3 electrons.*

8

CONCLUSIONS

8.1 Lessons learned from device JB_TTl_14

The capacitive cross-coupling of the electrostatic gates was spatially different in the last cooldown of JB_TTl_14. This could indicate that it was an effect of the bias cooling. When cooled with a positive bias the general idea is to trap some negative charge in the GaAs under the electrostatic gates. This prevents unwanted tunneling due to low Schottky barrier and makes the surface gates stronger. The un-evenness could disappear in subsequent cooldowns[34].

The random floating of the patches of the 2DEG could also be eliminated by adding an ohmic channel to each jelly-bean. An ohmic set to ground will remove the possibility of the 2DEG patch charging up and will also allow for easier tuning of the qubits in DC transport without having the need to open up other qubits. This has in-fact been implemented in later iterations.

Some preliminary data also exists[54](taken by J. Beil and me) on the screening of the electric fields from the neighboring electrostatic gates by placing a large sheet of metal over the device separated by a layer of Hafnium oxide. It utilizes the fact that an electric field from a dipole decays faster over distance than from a monopole[35]. The data looks promising, but it is worth noting that the sample size was small and the performance of these devices as qubit was not characterized due to a fabrication problem at the time[36]. One could easily imagine the sensitivity of charge sensors dropping by the same amount as the gate cross-coupling.

8.2 Lessons learned from device NO9b

8.2.1 Experimental difficulties and comments on the experimental setup

Electrical noise was a major limiting factor during the experiment. When I inherited the experimental setup, it was nearly impossible to even measure transport trough a device, with current spikes in the μA range. Most of the noise sources have since been found. Some were more obvious than others. The biggest noise source was the ground loop with the demodulation box. The demodulation box is a very noisy environment as it is. It sits on the same ground and has electrical connections to the computer via the Alazar card. Normally it is isolated from the cryostat in the DC range by use of inside-outside DC blocks. The ground connection originated from a voltage controlled phase shifter, which is normally adjusted by hand through a dedicated power supply, but which was connected to the DAC via a BNC cable for convenience purposes. Others were more tricky. Pieces of faulty equipment are usually hard to troubleshoot since it requires significant disassembly of the experimental setup. This way a faulty Ithaco current preamplifier which was a source of $50Hz$ noise was localized and removed from the setup. There

[34] this device has in fact been cooled down again without the participation of the author. However, the number of active gates was reduced significantly down to only two qubits in positions 1 and 2. The main goal of the experiment was to work on the triple dot in qubit 1, so the uneven cross-capacitance was never tested.

[35] induced mirror charge in the screening gate makes the gate an effective dipole

[36] the zero setting on the lithography system was mistakenly changed and everyone's fabrication had overdose problems until it was localized

is still a sizable amount of electrical noise in the system which could not be localized at the time. One of the theories suggests it could be a faulty isolation of the magnet ground inside the cryostat. I would recommend for the next user to carefully examine the cryostat before starting a new experiment.

When running rf-reflectometry we have experienced broadening of the transition lines. One of the possible explanations for this was the power of the RF-carrier signal going down the cryostat. The power at the sample after passing through all of the installed attenuation was originally determined to be $-72dBm$. This corresponds to a V_{rms} of around 56 microvolt. K_bT at 1K is equal to $86\mu V$. This means the sample was heated significantly from the point where the carrier was turned on. This has been seen by taking a scan of the same region in voltage space twice in a row, with the transitions in the second scan were significantly more washed out. The power was reduced to $-76dBm$ which corresponds to electron temperature, assuming perfect thermalization, of around $400mK$. This was still higher than we would like, but when attempting to go lower, the signal to noise ratio would drop to a point where measurements were impossible.

8.2.2 Cross coupling

A few conclusions can be made about the geometry of the device based on it's performance during the last cooldown. Capacitive cross-coupling is still a major problem, similar to the linear triple-triple device. During the work on this thesis several schemes for reducing or even completely eliminating this cross coupling have been suggested, however their implementation required significant time investment. One of the strategies was covered in [54]. A large sheet of metal can be placed on top of the device. When voltage is applied to the gate, a mirror charge would be created partially screening the electric field emanating from this gate to reduce it's effect on neighboring gates and 2DEG.

Another approach is more about the robustness of the tuning process rather than an attempt to suppress the cross-coupling. The idea is to introduce a new gate running down the middle of the quantum dot region. This gate would be biased with a positive voltage akin to accumulation gate techniques in Silicon. This would allow a more aggressive manipulation of the gate voltages on the negative depletion gates without the risk of completely removing the non-depleted quantum dot region. Due to low Schottky barrier in GaAs(see sec. 2.1) this would require deposition of an oxide layer between the positive accumulation gate and the substrate. This approach is in the works currently with fabrication recipe developed by P. Nissen and is showing promising results.

8.2.3 Device geometry

The set of gates controlling the tunneling rates to and from the Jelly bean would mostly be set by the tuning parameters of the Qubits. As such, the intention was to tune up a large quantum dot in the Jelly bean by adjusting voltages on the 3 electrostatic gates. When the qubit regions were in a state with formed quantum dots, the operating range of the Jelly bean plungers was very close to zero volt. This is bad, since the depletion of the 2DEG by these gates alone only happens at around $-200mV$. In this case, instead of making the quantum dot smaller, applying negative bias to the plunger gates breaks the dot up into smaller quantum dots as see in figure 33. This problem is easily solvable by increasing the physical dimensions of the device, in this case the spacing between the plunger gates lithographically. Interestingly, this has been predicted before the cooldown of this device and a newer generation has been fabricated with increased dimensions. Unfortunately the batch has failed because of fabrication problem.

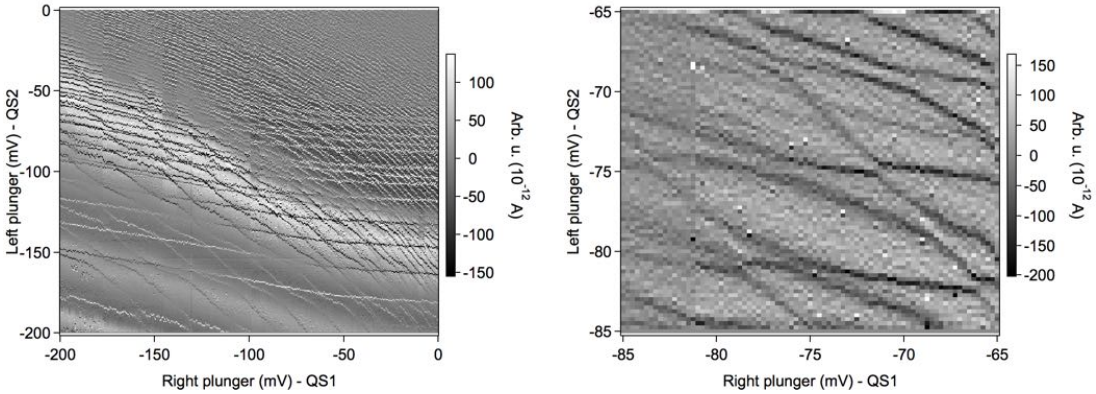


Figure 33: *Breakdown of the large quantum dot in the Jelly bean as a function of plunger gates QS1 and QS2 33(a) Charge stability diagram measured in charge sensing. After reaching approximately $-60mV$ on the plungers, the quantum dot begins to break down into smaller tunnel coupled quantum dots. 33(b) A zoom in on the region indicated in figure a) clearly showing multidot signatures(in this case something that looks like a triple-dot). The plunger gate QS3 operates close to zero($-40mV$ here). This unwanted behavior could be removed by spacing the plunger gates further apart.*

8.3 Final words

In the end we were able to develop a reliable recipe for fabricating any imaginable architecture within the cleanroom at Center for Quantum Devices on GaAs. We were also successful at fabricating various device designs that fit a wide range of ideas for implementation of solid state Spin Qubits, starting from *simple* linear "8 in a row" designs, intended for 8 quantum dots in a row to "15 in a row", exploring new design philosophies with the "L-shape" designs intended to be able to house any implementation of a quantum dot spin qubit, to finally converging on the "butterfly" and the "triple-triple" designs that are intended to explore the possibility of long range coupling of multiple physical qubits. After fabrication we were also able to show tunable and controllable double and triple quantum dots that are at the core of the implementation of spin qubits. If we are to scale, we need to connect multiple qubits by a reliable connection.

Through trial and error, we were able to uncover the experimental challenges in scaling these systems to one day be able to build a quantum computer. The main challenge comes from how interconnected the environment on such devices is. The capacitive cross-coupling can be a killer in tightly packed devices, much more so than for the single qubit demonstrations. Removing or reducing this cross-coupling by means of screening[54] or by improving the resistance to cross-coupling via bipolar gate designs is needed.

By increasing the complexity of quantum devices, we also increase the amount of control electronics required. A greater number of measurement devices and connections to the sample significantly increases the amount of electrical noise and heat that is sent down into the cryostat. If the implementation of a multi-qubit device becomes successful in the near future, control electronics might become a problem and with it the scalability advantage, that spin qubits currently possess. Development of more advanced hardware, like the Sydney Board(fig 22) and miniaturized circuits will become a major milestone.

Mediators are bound to play a greater role in the future for interconnecting potential networks of qubits(see sec. 2.4.1). There is a number of very interesting experiments to do with the coupling schemes proposed by Srinivasa, et al.[20] and Mehl, et al.[19]. For instance, verifying the RKKY-like exchange interaction between two qubits would be a major achievement. Additionally, one can tune this exchange electrically by adjusting tunnel rates or level spacing in the

multi-electron quantum dot without disturbing the qubit state dynamically, implementing an ON-OFF switch. Similarly for the entanglement operation, an ON-OFF action can be achieved by parking in an error prone regime and changing occupation of the mediator independently of the qubit. Additional control knobs are present in the form of the asymmetric exchange interaction, that should also be tunable by gate voltage independently of the qubit state. Even in a case, where the limit is imposed by a fabrication error, it should be possible to remove the asymmetry via balancing the tunneling amplitudes to and from the quantum state coupler. Exploring the interaction between different kinds of qubits is also an interesting direction. One experiment could be to couple an electrically controlled resonant exchange-only qubit via a mediator to a Loss DiVincenzo qubit made with a micromagnet. One could imagine using the fast operation of the exchange-only qubits on the order of GHz[43] with the long relaxation times of a completely isolated LD qubit in a small magnetic field which can be on the order of seconds[71]. The mediator can then be turned ON or OFF when needed to store some information in the LD qubit.

Some of these ideas are already on their way within the Spin Qubits team with the new generations of devices potentially opening doors into a new phase implementing solid state quantum dot based electron spin qubits.

A

FABRICATION RECIPE

This chapter contains the fabrication recipe that was developed for the multidot devices with and without a screening gate. Since this recipe was developed together with Johannes, I stole parts of the written recipe from his thesis.

The starting point was the recipe of Jim Medford which he used to fabricate JB19-2b in the Harvard CNS cleanroom. The change in the fabrication environment and equipment meant that the recipe had to be readjusted to work. Additionally, we are producing much larger devices which gives rise to problems which were not encountered by Jim.

The main difference in the workflow compared to the original recipe is the replacement of the photolithography steps with e-beam lithography. This does increase the manufacturing time, however is not a major concern since the patterns are fairly small and the most demanding exposures can be done within a few hours at most.

Overview

A general overview of the fabrication process is as follows:

1. Cleave chip
2. Mesa patterning
3. Mesa etch
4. Ohmics patterning
5. Ohmics deposition
6. Ohmics annealing
7. Fine gates patterning
8. Fine gates deposition
9. Outer gates patterning
10. Outer gates deposition
11. Insulating oxide deposition (ALD) of HfO2
12. Screening gate pattern
13. Screening gate deposititon
14. Screening gate connector patterning
15. Screening gate connector deposition

Cleave chip

I advise anyone starting their fabrication to carefully consider the dimensions of all the devices in a batch together on one piece of wafer. The devices I fabricated were $3.2cmby3.3cm$, so the fitting dimensions for a piece of wafer were chosen to be $7.5mmby11mm$ for 6 devices at a time. This makes the chip small enough to go into the first clip in the elionix while giving me enough "failure protection". By this I mean cracking the sample at the edges, dropping etc.. I also advice against making square chips, since it is important to keep track of the orientation.

Mesa pattern

In order to electrically isolate the different devices on a chip and to reduce parasitic capacitance, unnecessary 2DEG around the devices is etched away. The arms of the mesa are then left as a connection for the ohmic contacts to the device. When preparing an etching solution it important to follow all safety procedures. Yes, you are not working with HF, but it is still dangerous. Another important aspect to think about is that the etch rates will be slightly different each time. The reasons for this are found in reaction kinetics (duh) and also human error. Remember, we want to etch with a few nanometers precision, so even a drop can make a difference over the course of a minute. To determine the etch rate use a junk piece of simple GaAs. Experience shows that etch rates between the junk material and the "real" material will be different, however this is insignificant.

Etch past the 2DEG. In general it's hard to go wrong with etching too much. The only issue might be having to spend more time at the evaporator, since the outer gate layers have to climb the mesa.

For a paranoid fabber, every step starts with a 3 solvent clean. I personally find the "first solvent" only necessary when starting out with a new piece or when a wafer has been forgotten in the drawer for a while. TCE is a grease cutter, and I dont expect any greasy fingers on my device at any point in time!

1. 3 Solvent clean
   (a) Sonicate in Trichloroethylene (TCE) for 5min
   (b) Sonicate in Acetone for 5 min
   (c) Sonicate in Isopropyl Alchohol for (IPA) 5 min
   (d) Blow dry with N2
2. Bake chip on a 185C plate for at least 4 minutes. In the meantime, get the resist ready.
3. Place the chip on a glass slide and let it cool down for at least 15s
4. Spin Shipley S1813 photoresist
   (a) 10s, 500 rpm to have time to drop the resist on the rotating wafer. Never on stationary! Shiv will hate you!
   (b) 60s 4000 rpm
   (c) Take the chip off the spinner. If the resist got on the bottom of the wafer a neat trick is to wrap a glass slide in a cleanroom wipe and use a corner soaked in acetone to carefully remove the resist at the bottom of the wafer.
   (d) Bake 115 C, 2 min
5. Expose in the mask aligner for around 12s. Do it on a junk chip first to see if the dose is still good.

6. Develop the wafer.
   (a) 60s DC-26
   (b) 20s rinse in micro-pore water
   (c) Blow dry with N2
7. O2 plasma clean. 15s in the old microwave oven. Examine in the optical microscope resist residues if unsure about the time

Mesa etch

1. Prepare etch bath H2SO4:H2O2:H2 1:8:240 mL. Stir thoroughly. If left alone, cover the bath by a glass tray/lid. Evaporating water will make the etch stronger over time.
2. Etch for 60s. Do it for the test chip first!
3. Sonicate in acetone for 2 min
4. Sonicate in IPA for 2 min
5. Blow dry with N2
6. Measure the etch rate with the profilometer[37]
7. Etch the real chip knowing the etch rate from the junk chip. Give it 5nm more to begin with. In my experience the real wafer is usually etched faster.
8. Sonicate in acetone for 2 min
9. Sonicate in IPA for 2 min
10. Blow dry with N2
11. Clean in warm (55 C) acetone or hot (70 C) NMP for around 2hours in a closed beaker. If you can leave the chip overnight in cold acetone - do it.

Ohmic patterning

Ohmics are patterned together with the bond pads. We use e-beam for this, since aligning the Ohmic pattern in the old mask aligner is a nightmare. Besides, you can use large appertures and high beam current. This was a full wafer will be done within an hour.

1. 3 Solvent clean. Just like before. TCE, Acetone, IPA
2. Place chip on a 185 deg hotplate for at least 4 minutes
3. Let the chip cool down
4. Spin El-9 Copolymer. Ohmics work best with a bilayer resist.
   (a) 10 s, 500 rpm
   (b) 60s 4000 rpm
   (c) Clean the bottom of the chip

[37] you measure the height in the profilometer obviously, then do the math. It's not too hard!

(d) Bake at 185 for 3min

5. Spin 4%PMMA (A4) e-beam resist

   (a) 10s, 500 rpm

   (b) 60s 4000 rpm

   (c) Clean the bottom of the chip.

   (d) Bakeat185C for 3min

6. It is always a good idea to inspect the chip under an optical microscope to make sure there are no pieces of dust, hairs or fibres. Measure the distance from the corner to the nearest alignment mark. This will come in handy at the Elionix.

7. Load in the Elionix, condition the beam, align and expose with parameters deter- mined by a dose test. We used 40 nA beam current, 250 μ m aperture. Two point works well for Ohmics.

8. Develop

   (a) 90s MIBK:IPA 1:3

   (b) 20s IPA

   (c) Blow dry with N2

9. O2 plasma clean. Same procedure as before.

Ohmic deposition

It appears that the new low density spin qubit materials are proving hard to contact electrically. After a few failures, we managed to fabricate low resistance ohmics using a modified version of a recipe originally developped by Xanthe Croot, from University of Sydney. Older theses might refer to "removing the oxide layer from the surface of the GaAs". This seems to be a misguided requirement as GaAs does not have any native oxides, and wafers with a cap layer do not benefir from aggressive oxide removal at all. For the evaporation of the metals we used the old "Edwards" thermal evaporator.

1. Load metals in the thermal evaporator using Tungsten boats. One on the second floor can take four. Load them in order Au, Ge, Ni, Ni. Why two Ni boats you might ask? Ni reacts strongly with tungsten and will burn through a boat if too much Ni is present. We therefore devide it in two smaller portions.
2. Clean the vacuum seals of the evaporator.
3. Write down which boat corresponds to which metal.
4. Pump down. Degas metals by warming them up.
5. Evaporate:
(a) 5nmofNi (b) 35 nm of Ge
(c) 72nm of Au (d) 18nm of Ni
(e) 50nm of Au.
6. Clean in warm (55 C) acetone or hot (70 C) NMP for around 2hours in a closed beaker

Ohmics anneal

The anneal recipe is saved in the rapid thermal annealer (RTA) at the second floor as "JB420". It appears that the old Harvard annealer was off by around 80 degrees, so dont use the old recipes. The correct temperature is 420C

Load the sample into the susceptor inside the cleanroom. Any junk left on the wafer will forever be branded into your device, so tread carefully

Fine gates pattern

This is the most crucial step in the process since it defines the depletion gates. There are two ebeam steps writing three layers of gates. The first step is the $150\mu m$ at 100pA. Step two is a 600 μm write-field 2nA. This achieves the best balance between resolution and writing time. The inner pattern is divided into two writing substeps, inner and outer features. This way the inner patterns are written together giving a higher tolerance for stage drifts.

1. 3 Solvent clean
(a) Sonicate in Trichloroethylene (TCE) for 5min.
(b) Sonicate in Acetone for 5 min
(c) Sonicate in Isopropyl Alchohol (IPA) for 5 min
(d) Blow dry with N2
2. Place chip on a 185C hotplate for at least 4min
3. Let the chip cool down for at least 15sec
4. Spin PMMA4 ebeam resist :
(a) 10s, 500 rpm
(b) 60s 4000 rpm
(c) Clean the bottom of the chip.
(d) Bake at185C for 3min
5. Inspect the chip under an optical microscope. Write down the distance to the nearest alignment marks.
6. Load in the Elionix, align and expose. For use the working parameters were: 150 μm write-field, 100 pA beam current, 60k Dots, 1.5 μs/dot, 40μm aperture. 600μm write-field, 2nA beam current, 60kDots, 0.6μs/dot, 40μm aperture.
7. (Cold)Develop:
(a) Put a glass beaker with MIBK:IPA 1:3 into the cooling station and let it cool down.
(b) Develop 90s in cold MIBK:IPA 1:3
(c) 20s room temperature IPA
(d) Blow dry with N2.
8. Inspect under an optical microscope. If any junk is present at this step - clean the wafer and reexpose.

Fine gates deposition

Load the sample into the AJA

Evaporate 5nm Ti, then 15nm Au.

Lift off in acetone for more than 5 hours, if you have time, leave overnight. It will normally not lift off by itself, so use a pipette to squirt some acetone while it is still submerged.

Dont sonicate. If you absolutely must sonicate - put the chip into a plastic beaker.

Flush with IPA, blowdry with N2

Outer gates pattern

1. 3 Solvent clean, Dont sonicate!
   (a) TCE bath for 5min
   (b) Acetone bath for 5 min.
   (c) IPA bath 5 min.
   (d) Blow dry with N2.
   2. Spin El-9 Copolymer:
   (a) 10s, 500 rpm
   (b) 60s 4000 rpm
   (c) Clean the bottom of the chip
   (d) Bakeat185C 3min
   (e) Spin PMMA4 ebeam resist
   (f) 10s, 500 rpm
   (g) 60s 4000 rpm
   (h) Clean the bottom of the chip.
   (i) Bake at 185C for 3min
   3. Inspect under the optical microscope
   4. Load in the Elionix, condition the beam, align and expose. For us worked: 40nA beam current, 250μm aperture. Two point alignment
   5. Develop:
   (a) 90s MIBK:IPA 1:3
   (b) 20s IPA
   (c) Blow dry with N2.

Outer gates deposition

1. Load the sample into the AJA
   2. Evaporate 5nm Ti and 1.2xmesa hight of Au
   3. Lift off in warm acetone or hot NMP for more than 3 hours. Leave overnight if have time.
   4. Flush with IPA, blowdry with N2
   Enjoy your new quantum device!

B

POWER AT THE SAMPLE

Every person coming to work at the setup goes through this procedure of figuring out what the power arriving at the sample actually is. This is important, because too much power can heat up the sample significantly and even drive transitions, which are normally inaccessible[46][45]. There is a lot of attenuation present in the demodulation circuit and on the lines both inside and outside the cryostat. Some is placed at a cerati position to match the rated input power of the various components in the circuit, other is to reduce the amplitude to reduce the negative effects on the sample.

It starts with the signal generator SRS SG384 which can source a given frequency at up to +16.5dBm[38]. The splitter has an insertion loss of $\approx 3.5dB$ in the frequency range we are operating in. The RF Switch has an additional $\approx 1dB$ attenuation when ON[39]. The phase shifter expects input power of 0dBm, but can take up to 5dBm, therefore there is a -12dB attenuator just before the phase shifter. Insertion loss is $\approx 2dBm$.

After the demodulation box the signal is further attenuated by 46dB outside the cryostat right after the DC block. Inside the cryostat on the way down to the directional coupler the signal is attenuated by an additional 28dB. The directional coupler reduces the signal by an additional 15dB.

In the end, the power at the sample is approximately -76dBm. This corresponds to a rms voltage of $35\mu V$[40]. For reference K_bT at 1K is around $86\mu V$.

[38] for any setting beyond 13dBm the signal generator was showing the UNCAL warning(not calibrated) We measured the power to be within 0.0025% of the set value at 16.5dBm

[39] as expected when the switch is off, no signal is going though. In fact the insertion loss when OFF is 109dB

[40] This is relatively high, since the effective temperature of the sample at equilibrium would be close to $0.4K$. However the electron temperature has been measured to be adequate and one could also imagine the components having slightly higher attenuation at close to base temperatures, since all equipment is rated down to 55°C

REFERENCES

[1] Richard P Feynman. Simulating physics with computers. *Int.J.Theor.Phys.*, 21(6/7):467–488, 1982.

[2] P W Shor. Algorithms for quantum computation: discrete logarithms and factoring. In *35th Annual Symposium on Foundations of Computer Science*, pages 124–134. IEEE Comput. Soc. Press, 1994.

[3] Lov Grover. Quantum Mechanics Helps in Searching for a Needle in a Haystack. *Physical Review Letters*, 79(2):325–328, July 1997.

[4] David P DiVincenzo and IBM. The Physical Implementation of Quantum Computation. *arXiv.org*, February 2000.

[5] J Cirac and P Zoller. Quantum Computations with Cold Trapped Ions. *Physical Review Letters*, 74(20):4091–4094, May 1995.

[6] Immanuel Bloch, Jean Dalibard, and Sylvain Nascimbène. Quantum simulations with ultracold quantum gases. *Nature Physics*, 8(4):267–276, April 2012.

[7] T A Kennedy, F T Charnock, J S Colton, J E Butler, R C Linares, and P J Doering. Single-Qubit Operations with the Nitrogen-Vacancy Center in Diamond. *physica status solidi (b)*, 233(3):416–426, October 2002.

[8] Y Nakamura, Yu A Pashkin, and J S Tsai. Coherent control of macroscopic quantum states in a single-Cooper-pair box. *Nature*, 398(cond-mat/9904003):786–788, April 1999.

[9] David G Cory, Amr F Fahmy, and Timothy F Havel. Ensemble quantum computing by NMR spectroscopy. *Proceedings of the ...*, 1997.

[10] Daniel Loss and David P DiVincenzo. Quantum computation with quantum dots. *Physical Review A*, 57(1):120–126, January 1998.

[11] D P DiVincenzo, D Bacon, J Kempe, G Burkard, and K B Whaley. Universal quantum computation with the exchange interaction. *Nature*, 408(6810):339–342, November 2000.

[12] F H L Koppens, C Buizert, K J Tielrooij, I T Vink, K C Nowack, T Meunier, L P Kouvenhoven, and K L M Vandersypen. Driven coherent oscillations of a single electron spin in a quantum dot. *Nature*, 442(cond-mat/0608459):766–771. 25 p, August 2006.

[13] J R Petta, A C Johnson, J M Taylor, A Yacoby, M D Lukin, C M Marcus, M P Hanson, and A C Gossard. Charge and spin manipulation in a few-electron double dot. *Physica E-Low-Dimensional Systems & Nanostructures*, 34(1-2):42–46, August 2006.

[14] E A Laird, J M Taylor, D P DiVincenzo, C M Marcus, M P Hanson, and A C Gossard. Coherent spin manipulation in an exchange-only qubit. *Physical Review B*, 82(7):075403, August 2010.

[15] M D Shulman, O E Dial, S P Harvey, H Bluhm, V Umansky, and A Yacoby. Demonstration of Entanglement of Electrostatically Coupled Singlet-Triplet Qubits. *Science*, 336(6078):202–205, April 2012.

[16] J Medford, J Beil, J M Taylor, S D Bartlett, A C Doherty, E I Rashba, D P DiVincenzo, H Lu, A C Gossard, and C M Marcus. Self-consistent measurement and state tomography of an exchange-only spin qubit. *Nature Nanotechnology*, 8(9):654–659, September 2013.

[17] W K Wootters and W H Zurek. A single quantum cannot be cloned. *Nature*, 299(5886):802–803, October 1982.

[18] P W Shor. Fault-tolerant quantum computation. In *37th Conference on Foundations of Computer Science*, pages 56–65. IEEE Comput. Soc. Press, 1996.

[19] Sebastian Mehl, Hendrik Bluhm, and David P DiVincenzo. Two-qubit couplings of singlet-triplet qubits mediated by one quantum state. *Physical Review B*, 90(4), 2014.

[20] V Srinivasa, H Xu, and J M Taylor. Tunable Spin Qubit Coupling Mediated by a Multi-Electron Quantum Dot. *arXiv.org*, December 2013.

[21] A P Higginbotham, F Kuemmeth, M P Hanson, A C Gossard, and C M Marcus. Coherent Operations and Screening in Multielectron Spin Qubits. *Physical Review Letters*, 112(2), 2014.

[22] C W J Beenakker and H van Houten. Quantum Transport in Semiconductor Nanostructures. pages 1–228. Elsevier, 1991.

[23] Jeremy Levy. Universal Quantum Computation with Spin-1/2 Pairs and Heisenberg Exchange. *Physical Review Letters*, 89(14):147902, September 2002.

[24] Michael J Manfra. Molecular Beam Epitaxy of Ultra-High Quality AlGaAs/GaAs Heterostructures: Enabling Physics in Low-Dimensional Electronic Systems. *arXiv.org*, September 2013.

[25] Christo Buizert, Frank H L Koppens, Michel Pioro-Ladrière, Hans-Peter Tranitz, Ivo T Vink, Seigo Tarucha, Werner Wegscheider, and Lieven M K Vandersypen. InSitu Reduction of Charge Noise in GaAs/$Al_xGa_{1-x}As$ Schottky-Gated Devices. *Physical Review Letters*, 101(22):226603, November 2008.

[26] R Hanson, Kouwenhoven, L. P., J R Petta, S Tarucha, and L M K Vandersypen. Spins in few-electron quantum dots. *Reviews of Modern Physics*, 79(4):1217–1265, 2007.

[27] J Medford. *Spin Qubits in Double and Triple Quantum Dots*. PhD thesis, Harvard University, Cambridge, MA, March 2013.

[28] H van Houten, C W J Beenakker, and A A M Staring. Coulomb-Blockade Oscillations in Semiconductor Nanostructures. *Single Charge Tunneling*, August 1992.

[29] M Field, C Smith, M Pepper, D Ritchie, J Frost, G Jones, and D Hasko. Measurements of Coulomb blockade with a noninvasive voltage probe. *Physical Review Letters*, 70(9):1311–1314, March 1993.

[30] C Barthel, M Kjærgaard, J Medford, M Stopa, C M Marcus, M P Hanson, and A C Gossard. Fast sensing of double-dot charge arrangement and spin state with a radio-frequency sensor quantum dot. *Physical Review B*, 81(16):161308, April 2010.

[31] D J Reilly, C M Marcus, M P Hanson, and A C Gossard. Fast single-charge sensing with a rf quantum point contact. *Applied Physics Letters*, 91(16):162101, October 2007.

[32] W G van der Wiel, S De Franceschi, J M Elzerman, T Fujisawa, S Tarucha, and others. Electron transport through double quantum dots. *Rev.Mod.Phys.*, 75:1–22, 2003.

[33] M R Delbecq, T Nakajima, T Otsuka, S Amaha, J D Watson, M J Manfra, and S Tarucha. Full control of quadruple quantum dot circuit charge states in the single electron regime. *Applied Physics Letters*, 104(18):183111, May 2014.

[34] A C Johnson, J R Petta, C M Marcus, M P Hanson, and A C Gossard. Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot. *Physical Review B*, 72(16), October 2005.

[35] C Barthel. *Control and fast Measurement of Spin Qubits* . PhD thesis, Harvard University, December 2010.

[36] Michael A Nielsen and Isaac L Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, New York, NY, USA, 10th edition, 2011.

[37] J M Elzerman, R Hanson, L H W Van Beveren, B Witkamp, L M K Vandersypen, and Kouwenhoven, L. P. Single-shot read-out of an individual electron spin in a quantum dot. *Nature*, 430(cond-mat/0411232):431–435. 13 p, November 2004.

[38] K C Nowack, F H L Koppens, Yu V Nazarov, and L M K Vandersypen. Coherent Control of a Single Electron Spin with Electric Fields. *Science*, 318(5855):1430–1433, November 2007.

[39] M Pioro-Ladrière, T Obata, Y Tokura, Y S Shin, T Kubo, K Yoshida, T Taniyama, and S Tarucha. Electrically driven single-electron spin resonance in a slanting Zeeman field. *Nature Physics*, 4(10):776–779, August 2008.

[40] J Taylor, J Petta, A Johnson, A Yacoby, C Marcus, and M Lukin. Relaxation, dephasing, and quantum control of electron spins in double quantum dots. *Physical Review B*, 76(3):035315, July 2007.

[41] J R Petta, A C Johnson, J M Taylor, E A Laird, A Yacoby, M D Lukin, C M Marcus, M P Hanson, and A C Gossard. Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science*, 309(5744):2180–2184, 2005.

[42] C Barthel, D J Reilly, C M Marcus, and M P Hanson. Phys. Rev. Lett. 103, 160503 (2009) - Rapid Single-Shot Measurement of a Singlet-Triplet Qubit. *Physical review ...*, 2009.

[43] J Medford, J Beil, J M Taylor, E I Rashba, and H Lu. Phys. Rev. Lett. 111, 050501 (2013) - Quantum-Dot-Based Resonant Exchange Qubit. *Physical review ...*, 2013.

[44] J M Taylor, V Srinivasa, and J Medford. Electrically Protected Resonant Exchange Qubits in Triple Quantum Dots. *Physical Review Letters*, 111(5), 2013.

[45] F R Braakman, P Barthelemy, C Reichl, W Wegscheider, and L M K Vandersypen. Long-distance coherent coupling in a quantum dot array. *Nature Nanotechnology*, 8(6):432–437, June 2013.

[46] Floris R Braakman, Pierre Barthelemy, Christian Reichl, Werner Wegscheider, and Lieven M K Vandersypen. Photon- and phonon-assisted tunneling in the three-dimensional charge stability diagram of a triple quantum dot array. *Applied Physics Letters*, 102(11), 2013.

[47] Austin G Fowler, Matteo Mariantoni, John M Martinis, and Andrew N Cleland. Surface codes: Towards practical large-scale quantum computation. *Physical Review A*, 86(3):032324, September 2012.

[48] M D Shulman, S P Harvey, J M Nichol, S D Bartlett, A C Doherty, V Umansky, and A Yacoby. Suppressing qubit dephasing using real-time Hamiltonian estimation. *Nature Communications*, 5:5156–, October 2014.

[49] A C Johnson, J R Petta, J M Taylor, A Yacoby, M D Lukin, C M Marcus, M P Hanson, and A C Gossard. Relaxation of Single Electron Spins by Nuclei in a Double Quantum Dot. *Nature*, 435(cond-mat/0503687):925, March 2005.

[50] Dennis Greywall. 3He specific heat and thermometry at millikelvin temperatures. *Physical Review B*, 33(11):7520–7538, June 1986.

[51] Frank Pobell. *Matter and Methods at Low Temperatures*. Springer Berlin Heidelberg New York, 3rd edition edition, January 2007.

[52] Oxford. *Triton 200/400 Cryofree dilution refrigerator manual*, 3 edition, November 2012.

[53] Lydia L Sohn, Kouwenhoven, L. P., and Gerd Schön. *Mesoscopic Electron Transport*, volume 345 of *Nato Science Series E*. Springer, October 1997.

[54] J Beil. Towards the coherent coupling of multiple three-electron spin-qubits . Master's thesis, University of Copenhagen, June 2014.

[55] F Koppens, K Nowack, and L Vandersypen. Spin Echo of a Single Electron Spin in a Quantum Dot. *Physical Review Letters*, 100(23):236802, June 2008.

[56] R J Schoelkopf. The Radio-Frequency Single-Electron Transistor (RF-SET): A Fast and Ultrasensitive Electrometer. *Science*, 280(5367):1238–1242, May 1998.

[57] Martin Kufahl. Experimental Methods for Implementing Electron Spin Qubits in Double Quantum Dots . Master's thesis, University of Copenhagen, June 2014.

[58] A C Johnson. *Charge Sensing and Spin Dynamics in GaAs Quantum Dots*. PhD thesis, Harvard University, September 2005.

[59] I Ziler, JEF Frost, V ChabasseurMolyneux, CJB Ford, and M Pepper. Crosslinked PMMA as a high-resolution negative resist for electron beam lithography and applications for physics of low-dimensional structures. *Semiconductor Science and Technology*, 11(8):1235–1238, August 1996.

[60] MicroChem. NANO TM PMMA and Copolymer data sheet. MicroChem Corp., January 2001.

[61] Valery Axelrad and Michael C. Smayling. 16nm with 193nm immersion lithography and double exposure, 2010.

[62] Bruce W Smith, Yongfa Fan, Michael Slocum, and Lena Zavyalova. 25 nm immersion lithography at 193 nm wavelength. In Bruce W Smith, editor, *Microlithography 2005*, pages 141–147. SPIE, May 2005.

[63] T E Everhart. Determination of Kilovolt Electron Energy Dissipation vs Penetration Distance in Solid Materials. *Journal of Applied Physics*, 42(13):5837, 1971.

[64] K Kanaya and S Okayama. Penetration and energy-loss theory of electrons in solid targets. *Journal of Physics D: Applied Physics*, 5(1):43–58, October 1971.

[65] A N Broers, A C F Hoole, and J M Ryan. Electron beam lithography—Resolution limits. *Microelectronic Engineering*, 32(1-4):131–142, September 1996.

[66] Giulio Ungaretti. III-V Semiconductor Nanowires growth and characterization. Master's thesis, University of Copenhagen, August 2014.

[67] J I Colless and D J Reilly. Modular Cryogenic Interconnects for Multi-Qubit Devices. *arXiv.org*, cond-mat.mes-hall, 2014.

[68] Tatsuki Takakura, Akito Noiri, Toshiaki Obata, Tomohiro Otsuka, Jun Yoneda, Katsuharu Yoshida, and Seigo Tarucha. Single to quadruple quantum dots with tunable tunnel couplings. *Applied Physics Letters*, January 2014.

[69] J M Taylor, H A Engel, W Dür, A Yacoby, C M Marcus, P Zoller, and M D Lukin. Fault-tolerant architecture for quantum computation using electrically controlled semiconductor spins. *Nature Physics*, 1(3):177–183, December 2005.

[70] R Brunner, T Kubo, K Yoshida, and S Tarucha. Single-Spin readout in a double quantum dot including a micromagnet. *Physical review ...*, 2010.

[71] S Amasha, K MacLean, Iuliana Radu, D Zumbühl, M Kastner, M Hanson, and A Gossard. Electrical Control of Spin Relaxation in a Quantum Dot. *Physical Review Letters*, 100(4):046803, January 2008.