FACULTY OF SCIENCE
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Comparative Study of Mechanically Exfoliated and CVD-Grown Graphene

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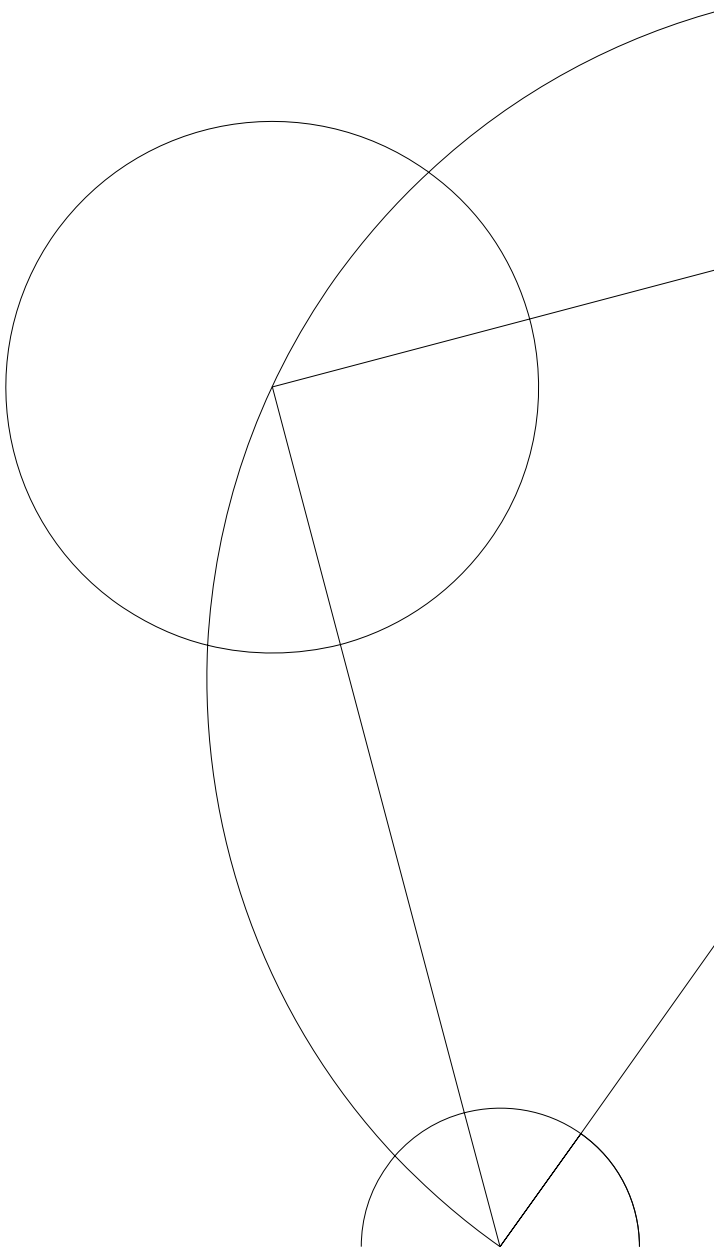

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Electrical conduction through mechanically exfoliated pristine graphene is compared with that made by chemical vapor deposition on a copper substrate. Both types of graphene are described in the theory, while the differences in electronic properties between the two are highlighted. Detailed explanation of the fabrication for pristine devices is given, while the making of CVD graphene, fabricated at the Technical University of Denmark (DTU), is only explained in the theory section. Pristine graphene is the closest one can come to ideal graphene, which is why resistance of pristine samples is expected to be lower than for CVD samples. However, due to technical difficulties, no working pristine devices could be made. Improvements were made on the fabrication procedure, which will be explained in detail. Also explained is how the procedure went wrong, accompanied with data for the current. A working CVD sample was provided, with resistance measured at room-temperature. Due to lack of time, no low temperature measurements could be made on the CVD sample.

Special thanks to Jakob Meyer for guiding me through the fabrication of pristine and giving great advice for writing the project. Also thanks to Rune Hviid, who helped me with the measurements and provided the CVD graphene samples. An extra thanks to Martin Kühnel for much help with the AFM. A big thanks to Jesper Nygård, for making the project possible. Finally, a thank to all members of QDev for making the process enjoyable.

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1 Introduction

Graphene, an allotrope of carbon, has gotten huge attention over the last decade, ever since its first observation in 2004 [5]. The reason is that graphene is a strictly two-dimensional material, being only one atomic-layer thick and having electronic properties largely different from traditional semiconductors. Graphene can be fabricated in various ways, like mechanical exfoliation of graphite, chemical vapour deposition (CVD), reduction of graphene oxide, or thermal decomposition of SiC. Though all methods yield graphene, each type of fabrication leaves its own mark, resulting in some being electrically inferior to others. Two types of these methods were the basis of this project, namely exfoliation and CVD on copper. Exfoliation generates the purest form of graphene, dubbed pristine graphene, which has been the best choice for studying graphene from the start. CVD graphene has properties making it less good for conduction than pristine graphene, explained in the theory section. Pristine graphene, however, can only be made in small sizes and require an considerable amount of luck to create, whereas CVD graphene grown on copper can be synthesized in large areas with a higher chance of success. Graphene has shown to be usable as a top contact in molecular junctions. The goal of the project was to compare pristine and CVD graphene to see how large a difference there is between the two, and if they are better than what earlier studies has presented. An explanation of earlier work, including important results, is given below.

The project is based on earlier work by Tao Li et al [1]. Their article introduced an alternative way of making molecular junctions with self-assembled monolayers (SAMs). They argued that poly(4-styrenesulphonic acid) (PEDOT:PSS) has certain disadvantages, such as an ill-defined polymer/SAM interface, limited processing window, and that the yield of the procedure was dependent on the SAM structure. An earlier study had used CVD graphene as the conductive interlayer in molecular junctions, but Li et al argued that pristine and CVD graphene either suffered from low-yield or high-cost issues [2]. So as and alternative, they use graphene oxide (GO) made by a modified Hummers' method. The GO is then spincoated onto an Si/SiO_2 wafer. With thermal treament, the GO is reduced to multilayer graphene films, which they dub chemically derived graphene (CDG). Sodium hydroxide (NaOH) is then added to the wafer with CDG, after which the wafer is placed in deionized water. This procedure leads to a floating CDG film that can be transferred to other substrates, while the Si/SiO_2 wafer remains at the bottom of the water.

To test how well the CDG films worked, they made two types of junctions, which were called junction I and II. In junction I, the CDG is used as a conductive interconnect between molecular junctions, so that transport in molecules could be studied in series without using metal contacts, which could potentially damage the molecules. Junction II was made to see, if the CDG film works as a conductive interlayer that protects molecules from evaporated top metal contacts. So junction I was for measuring horizontal current, while junction II was for vertical. A schematic showing both types of junctions is given in figure 1. The molecular junctions were made by thermally evaporating gold electrodes with a Ti sticking layer onto a Si/SiO_2 wafer, followed by atomic layer deposition of an insulating aluminium oxide (Al_2O_3) layer. Micropores (diameter of 1-2 μm) were then etched in the aluminium oxide with electron beam lithography. Thiolate monolayers are self-assembled in these holes, followed by transfer of the graphene as explained above. At this point, junction I devices are made. Further deposition of an Au top contact onto the graphene film results in a junction II device.

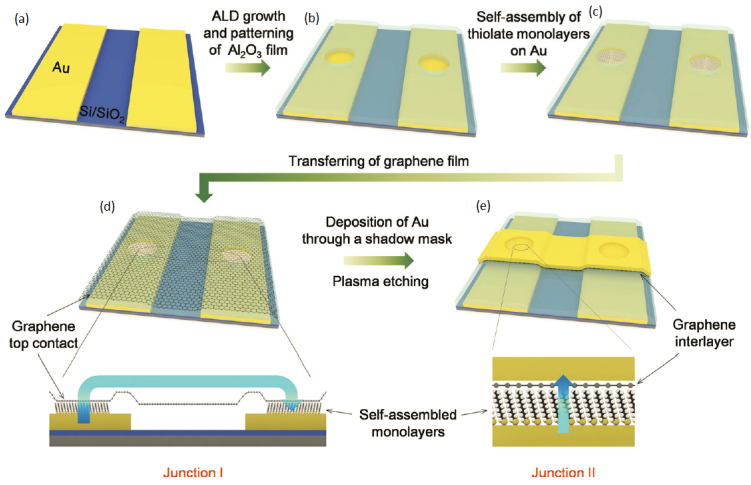

Figure 1: The steps leading to working molecular junction devices. (a) Shows gold electrodes on a clean Si/SiO_2 wafer. (b) ALD growth of an Al_2O_3 layer on the electrodes and wafer, followed by e-beam lithography of small wells through the Al_2O_3 down to the underlying gold. (c) Self-assembled monolayers grown in the wells. (d) Transfer of graphene, leading to junction I devices, or (e) further evaporation of gold electrodes on the graphene for junction II devices. Blue arrows indicate current direction. Figure adapted from [1].

Using a linear fit of the normalized resistance per molecule vs the number of carbon atoms, they found a rather high resistance of $3 \cdot 10^4$ MΩ for juncion I devices, which they attributed solely to the CDG film and contact resistances. To know why the resistance is so high, one has to look at the transport through a junction I device. If an electron, travelling through the CDG film, encounters an insulating domain, like oxidized regions, it will jump from that layer to another. This jumping between layers results in an increase of the resistivity of the device [4]. The other limitation of CDG is its temperature dependence. Li et al observed a large increase (factor of 3) of the resistance in both junction I and II devices, when going from room-temperature to very low temperatures, but these data were not shown. The temperature dependence of junction II devices was further investigated by Hauptmann et al [3]. The CDG used by them was derived from graphene oxide, which they simply called reduced graphene oxide (rGO). They confirmed that the temperature dependence could be ascribed to the rGO films by making devices without molecules (figure 2). The device was cooled from room-temperature to 10 K, and a large increase in resistance occurred at about 50 K, just like for devices with molecules (not shown here). The best fit for the conductance, according to them, was that of hopping conductance:

$$G(T) = G_1 exp(-B/T^{1/4}) \tag{1}$$

Where $G = I/V$, I and V are the current and voltage, respectively, T is the temperature, B is a constant given by $B = 2.1[1/k_B\alpha^3 D(\varepsilon_F)]^{1/4}$, k_B is the Boltzmann constant, α is the charge carriers localization length and $D(\varepsilon_f)$ is the electronic density of states.

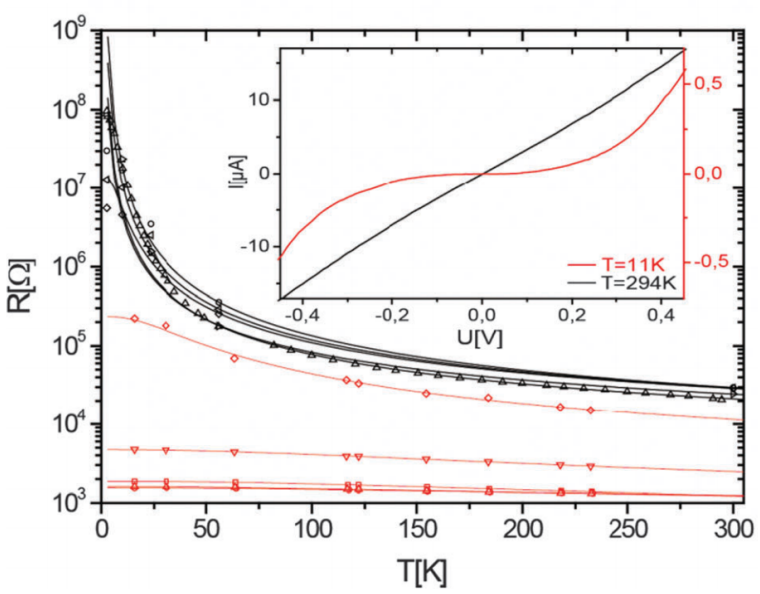

Figure 2: Temperature dependence of junction II devices without molecules. A marked increase in the resistance occurs at about 50 K. The red curve shows the resistance after electrical annealing of the rGO. Inset shows I-V curves for devices at room-temperature (black) and 11 K (red). Figure adapted from [3].

Finally, they discovered that above a certain voltage, the threshold voltage, the rGO could be annealed electrically. This resulted in much lower resistances. They argue that this decrease could be due to the Ti reacting with the rGO or the presence of water molecules at the Au/rGO interface, but a definitive explanation is not given. When heating the samples back to room-temperature, the resistance remains much lower than for samples before annealing (figure 2). The decrease due to electrical annealing is, however, a general property of graphene.

Pristine samples were fabricated by the author, while the CVD graphene was made in DTU. Therefore, fabrication of the CVD samples will not be explained (except for the overall explanation given in the theory section). The wafers with electrodes were also made on DTU, but an explanation for their fabrication is given here, since they were used for making pristine devices as well. The goal is to measure the resistance of pristine and CVD graphene devices, both at room-temperature, to see if the resistance is lower than for the CDG films, and to observe how it behaves as the temperature is decreased. Dependence of resistance on distance is equally important.

2 Theory

2.1 Pristine Graphene

2.1.1 Carbon Allotropes

Certain chemical elements have the ability to exist in more forms than one; these forms are called allotropes of the element. The mineral graphite is an allotrope of carbon. It has been used by humans for centuries as, for example, molds for cannonballs or as pencils. Graphite has a sheet like structure, with each layer consisting of tightly packed sp^2 hybridized carbon atoms arranged in a honeycomb lattice. Such a single two-dimensional layer of graphite is called graphene. It can be thought of as consisting of benzene rings stripped out from their hydrogen atoms. It is the basic building block for graphitic materials of all other dimensionalities [6]. Graphene can be wrapped up into zero-dimensional buckyballs, rolled up into one-dimensional carbon nanotubes, or, as mentioned earlier, stacked into three-dimensional graphite (see figure 3).

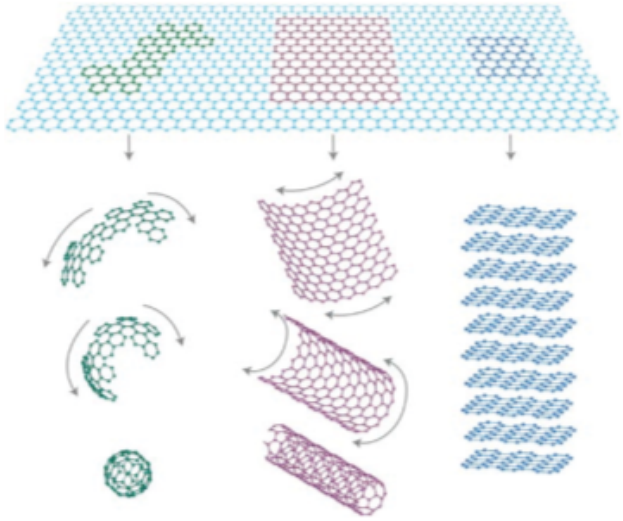

Figure 3: Graphene is the building block of all other graphitic materials. It can form fullerenes (green), nanotubes (red), and graphite (dark blue) (Figure adapted from [6]).

Strictly two-dimensional materials were considered thermodynamically unstable, confirmed by many experiments when the thickness of thin films was decreased. But layers of graphene in graphite are only weakly coupled by van der Waals forces, which is why it can be used for pencils. It is thanks to these weak forces that Andre Geim and Konstantin Novoselov were able to isolate single-layer graphene in 2004 by repeatedly peeling bulk graphite with adhesive tape, called mechanical exfoliation or the scotch tape method [5]. In fact, graphene has been produced ever since the pencil was invented, since writing on a piece of paper could in principle result in graphene, but no one was able to confirm it, since it could not be seen. Geim and Novoselov found out that placing graphene on a silicon wafer with a certain thickness of SiO_2 makes graphene visible in an optical microscope. The graphene obtained from mechanical exfoliation is the purest possible form of graphene. As such, it is called pristine graphene. Unless otherwise specified, all future reference to graphene is single-layer pristine graphene.

2.1.2 Electronic Structure

Graphene can be considered the perfect two-dimensional (2D) material, since it is exactly one atomic monolayer thick and carriers are confined in this 2D layer. Electrical conduction through 2D semiconductors has already been well-studied, but graphene has shown to behave quite differently from traditional 2D systems. To know why, one has to look at the electronic structure of graphene. Semiconductors are usually characterized by a small band gap between the top of the valence band and the bottom of the conduction band. Graphene, however, is unusual in that the valence and conduction bands meet at two points in momentum space [9]. This means that graphene is a zero-gap semiconductor. The reason why the bands intersect at exactly two points arises from the crystal lattice of graphene. As mentioned earlier, the carbon atoms are arranged in a honeycomb lattice. This hexagonal structure can be thought of as a triangular Bravais lattice with two atoms per unit cell, as shown in

figure 4. The corresponding 2D lattice vectors are

$$\boldsymbol{A_0} = \left(\frac{a}{2}\right)(3, \sqrt{3}) \tag{2}$$

$$\boldsymbol{B_0} = \left(\frac{a}{2}\right)(3, -\sqrt{3}) \tag{3}$$

where a = 0.142 nm is the carbon-carbon distance [8].

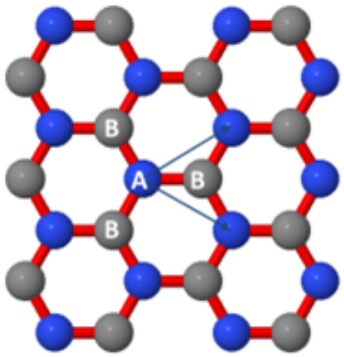

Figure 4: Triangular sublattice of graphene. Each atom in sublattice A has three nearest-neighbors in B and the other way around. Figure adapted from [9].

K and **K′** are the corners of the Brillouin zone, also known as the Dirac points. At exactly these points, the energy bands of graphene meet. There are two sets of three Dirac points, and since these two sets are not equivalent, graphene has a valley degeneracy $g_\nu = 2$. All the important physics of graphene happen at the Dirac point, just like the all the important physics in traditional semiconductors happen at the Γ point. The complete band structure of graphene is shown in figure 5a, including a zoom-in on a Dirac point.

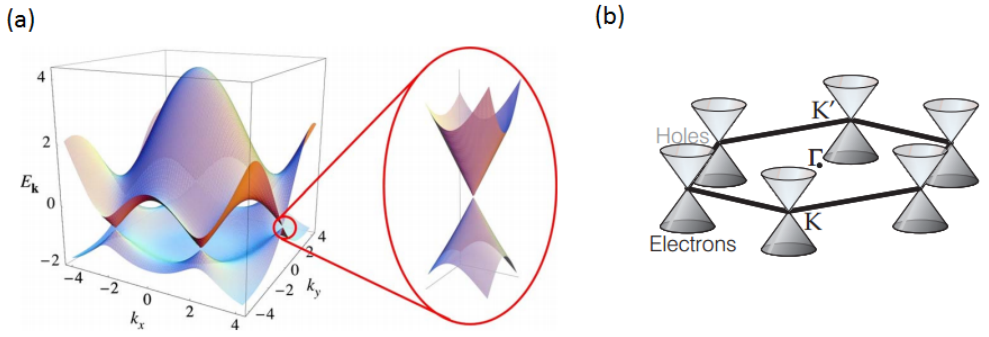

Figure 5: Dispersion relation of graphene. (a) Complete band structure of graphene. The bands intersect at six points, corresponding to the six carbon atoms in a hexagonal structure, but it can be considered two sets of three points, called the K and K' points. A zoom-in on one such Dirac point has been made, clearly showing the linear relation. (b) Band structure close to the Dirac points, showing that all carbon atoms in the hexagonal structure have a zero-gap dispersion relation. ((a) adapted from [7] and (b) adapted from [10]).

The importance of the Dirac points arises not only from the lack of band gap, but also from the fact that the dispersion relation is linear at the points. Figure 5a shows a zoom-in on one of the Dirac points, showing the cone-like shape. Electrons at the Dirac energy (energy at the Dirac point, E_D) follow a linear energy relation, given by

$$E(k) = \hbar v_f |k| \tag{4}$$

where $\hbar$ is Planck's constant divided by 2π, v_f is the Fermi velocity of charge carriers, and k is the wavevector. This dispersion applies to all carbon atoms in the graphene lattice (figure 5b). A linear dispersion normally characterizes particles whose kinetic energy vastly exceeds their rest mass. Therefore, electrons in graphene behave like photons or neutrinos, with an energy-independent velocity $v_f \approx 10^6$ m/s, or about 1/300 the speed of light. This means that carriers in graphene behave as massless Dirac fermions, which can be described by the

Dirac equation rather than the Schrödinger equation, since the Schrödinger equation applies to particles with a non-zero rest mass [11].

The linear dispersion relation arises from the two sublattices in the crystal structure. States in each branch close to E_D are independent, which indicates the existence of a pseudospin quantum number similar to the spin index, but independent of real spin. So carriers in graphene have a pseudospin index in addition to their spin and orbital index, leading to the Schrödinger equation

$$-i\hbar v_f \boldsymbol{\sigma} \cdot \nabla \Psi(\boldsymbol{r}) = E\Psi(\boldsymbol{r}) \tag{5}$$

where σ are the Pauli spin matrices and $\Psi(r)$ is 2D spinor wavefunction. The Hamiltonian corresponding to (4) is

$$\boldsymbol{\mathcal{H}} = \hbar v_f \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} = \hbar v_f \boldsymbol{\sigma} \cdot \boldsymbol{k} \tag{6}$$

where p = $\hbar$ k is the momentum vector measured from the K point [12]. This is the Dirac equation for massless relativistic particles.

2.1.3 Transport in Graphene

Figure 5b shows a schematic of the band structure near the Dirac point. In this figure, there are equal amounts of electrons and holes, which mean that the Fermi energy is equal to the Dirac energy. Due to the lack of a band gap, one can readily switch the carriers between electrons and holes, the principle of which is shown in figure 6. This can be verified experimentally by attaching a graphene flake on Si/SiO_2 to electrodes and then tuning the gate voltage. The gate voltage imposes a charge balance relationship

$$n = \frac{\varepsilon_0 \varepsilon V_g}{te} \tag{7}$$

where $\varepsilon_0\varepsilon$ is the permittivity of SiO_2, t is the thickness of the SiO_2 layer, and e is the electron charge. A positive gate voltage makes $E_f > E_D$, which induces electrons, while a negative gate voltage makes $E_f < E_D$, leading to a hole current. This phenomenon is referred to as the ambipolar field effect of graphene, the principle of which is shown in figure 6 [12]. Typically, charge density can be tuned from 10^{11} to 10^{13} cm^{-2} by applying a gate voltage, which moves E_f 10 to 400 meV away from the Dirac point.

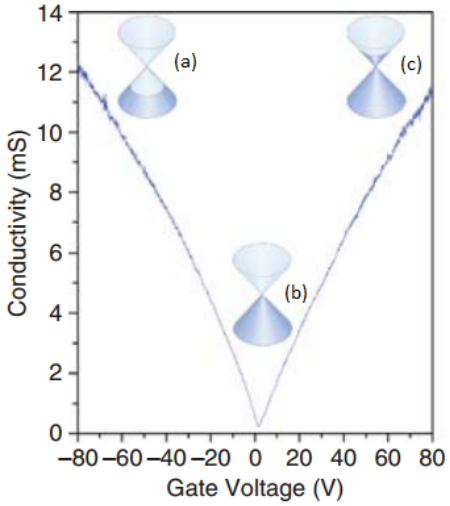

Figure 6: Ambipolar field effect in graphene. (a) A negative gate voltage induces holes. (b) With no gate voltage applied, $E_f = E_D$, where the minimum conductivity occurs. (c) A positive gate voltage induces electrons. Figure adapted from [12].

Theoretically, the conductivity for intrinsic graphene should be zero in the limit of vanishing n, or when $E_f = E_D$. This is further supported by the fact that the density of states (DOS) is also zero at the Dirac point. But when inspecting figure 6 more closely, one can see that the conductivity is non-zero even at zero gate voltage. This is a general phenomenon, known as the minimum conductivity in graphene, with a value close to the conductance quantum $\frac{e^2}{h}$. Minimum quantum conductivity has been predicted by theory for Dirac fermions. Most calculations suggest a minimum conductivity of $\frac{4e^2}{\pi h}$, with the four coming from the double

valley and double spin degeneracy. However, the values obtained experimentally are usually closer to $\frac{4e^2}{h}$, the reason for which remains unclear.

As earlier mentioned, charge carriers in graphene have an effective pseudospin index. Backscattering is therefore highly suppressed, since backscattering means reversing both the momentum and the pseudospin, which is forbidden for long-wavelength disorder. This results in extremely high carrier mobilities observed for graphene, since lack of backscattering means that transport is ballistic. These transport characteristics are only true, however, for ideal graphene, meaning undoped, free of defects and impurities, no interaction with the substrate and no phonon interaction. Experimental graphene generally suffers from one or more of these problems, leading to different forms of scattering. The presense of charged impurities was investigated by Chen et al by introducing pottasium ions into the graphene lattice and then increase the amount over time [14]. Their experiment confirmed the earlier calculated formula for conductivity as a function of carrier density $\sigma(n)$ in graphene:

$$\sigma(n) = Ce\left|\frac{n}{n_{imp}}\right| + \sigma_{res} \tag{8}$$

where C is a constant, n_{imp} is the concentration of impurities, and σ_{res} is the residual conductivity at n = 0. The conductivity became more linear and the mobility decreased. Impurity scattering is also known as Coulomb scattering or long-range scattering, since it occurs as a result of variations in the long-range electrostatic potential. They also found that higher doping caused a shift in the minimum conductivity in the negative directions, since potassium n-dopes graphene.

Scattering from defects is known as short-range scattering. Defects can be vacancies (lack of carbon atoms) or cracks in the graphene flake [15]. This type of defect is generally modelled as a deep potential well of radius R, which results in a conductivity given by:

$$\sigma_d = ne\mu_d = \frac{2e^2}{\pi h}\frac{n}{n_d}\ln^2(k_F R) \tag{9}$$

Here μ_d is the defect mobility, n_d the defect density, and $k_F = \sqrt{n\pi}$ the Fermi wave vector. Chen et al showed the effect of defects experimentally by irradiating a graphene sample with Helium and Neon ions in UHV, with more defects leading to lower conductivity.

Also important for this study is the effect of the underlying substrate. Due to the visibility of graphene on SiO_2 with a certain thickness, most exfoliated samples are made on Si/SiO_2 wafers, like in this study. But the mobilities of these devices are limited, which is thought to be because of charged impurities in the insulating SiO_2 substrate, or trapped charges [16]. Also the graphene samples have been shown to follow the morphology of the substrate [17]. This limitation can be overcome by suspending the graphene, leading to much higher carrier mobility [18].

2.1.4 Limit for Graphene

The linear dispersion is, however, only evident when being close to the Dirac point. Electrons within about 1 eV of the Dirac energy have a linear dispersion relation. Just as relevant is the fact that all these properties only apply to single-layer graphene. Graphite is a semi-metal, meaning that the valence and conduction bands overlap. The overlap of the bands already shows with the addition of just one layer, but the overlap for bilayer graphene is so small, that it can be regarded as a zero-gap semiconductor. But for few-layer graphene (3-10 layers) the bands start to notably overlap, and even thicker structures can be seen as thin films of graphite [6].

2.2 CVD Graphene

2.2.1 Growth

Though mechanical exfoliation offers the best possible graphene in terms of quality, it generally suffers from low-yield. A lot of luck is also involved, since flake thickness, size and location are largely uncontrollable. Therefore, other techniques have been employed for making graphene. One such method is chemical vapor deposition (CVD) of graphene onto metal substrates. CVD itself is a chemical process that involves depositing a solid material from a gaseous phase, often used in the semiconductor industry to make thin films.

To understand the growth mechanism, which is quite different from traditional thin films growth, one has to recognize the two-dimensional nature of graphene. The in-plane carbon-carbon bonds are extremely strong, while the out-of-plane bonds are very weak, and graphene interacts only very weakly with the underlying substrate. In fact, the graphene-metal interaction is only on the order of the van der Waals interaction ($<$ 100 mev per carbon atom) [19]. The lattice constants of neither metal nor graphene change significantly in response to the weak interactions, leading to the formation of Moiré patterns. These are interference patterns

that happen when two grids are overlaid at an angle on each other, in this case the lattices of graphene and metal substrate [21].

Evidence supports the idea that adsorbed carbon species diffuse to the edge of the graphene sheets, becoming part of the entire graphene lattice. Therefore, nucleation requires high concentrations of carbon atoms on the metal surface. The standard picture of epitaxial growth says that atoms diffuse until they reach a kink site, where they are incorporated (figure 7a, top). This means that film and substrate remain attached to each other during growth. Equally important, growth atoms only experience a small potential barrier, when attaching to the growing island. However, carbon atoms have to detach (break their bonds) with the underlying substrate in order to become part of the graphene crystal (figure 7a, bottom). These bonds are very strong though, close to the strong in-plane carbon-carbon bond strength in graphene. This suggests that a high concentration of carbon atoms are needed in order for growth to occur. For growth on ruthenium and iridium, it was shown that five carbon atoms are added to the graphene edge at a time [20]. Details for how growth occurs on other substrates, like Nickel (Ni) and Copper (Cu), has not been determined yet. Equally important is the fact that the addition of new layers in graphene is significantly different from normal crystal growth. In normal heteroepitaxy, additional layers are grown on top, due to the Ehrlich-Schwoebel barrier, which is the barrier for atoms deposited on top of the film to diffuse over descending edges (figure 7b, left). For graphene, however, evidence supports that growth occurs from below. The reason again lies in the carbon bond strengths, since the carbon adatom bonds are much weaker than atoms bonded to the metal substrate. Therefore, even carbon atoms on the graphene will migrate to the metal, if there is a pathway (figure 7b, right).

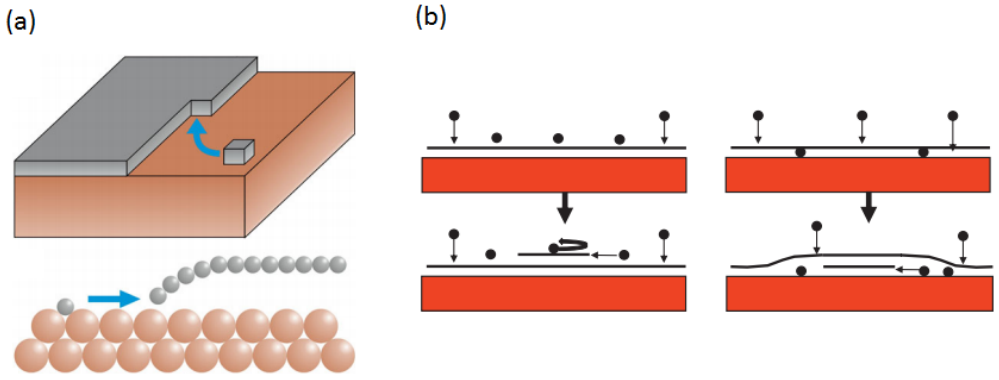

Figure 7: Graphene growth on metal surfaces. (a) Top schematic shows the standard solid-on-solid model of epitaxial growth, while the bottom figure shows graphene growth on metals. The carbon atoms (grey) either join the growing graphene island or remain as isolated adatoms. (b) Left figure shows layer-by-layer growth in normal heteroepitaxy, with growth species shown as black balls and substrate in red. The growth species are unable to descend down to the substrate, indicated by the self-reversing arrow, so new layers form on top of the former layer. The right figure shows layer formation for graphene, where carbon atoms diffuse to the metal interface, thereby growing new layers from below. Adapted from [19].

CVD graphene has been grown on Ni and Cu prior. Graphene grown on Nickel has shown mobilities on the order of 10^3 cm^2 V^{-1} s^{-1}. However, Ni has the limitation that the graphene films are small and not homogeneous over the entire surface. Also the amount of layers can not be controlled. Copper has been shown to catalyse the growth of several carbon allotropes, such as graphite, diamond, and carbon nanotubes. Recent experiments have shown large-area SLG's on copper foils through the CVD process [22]. Cu has the advantage of low-cost, large sizes, and can easily be dissolved without damaging the graphene.

Prior to growth, the copper substrate is covered with native oxide (CuO, Cu_2O), which reduces its catalytic activity (figure 8a). Therefore, it is annealed (usually for 30 minutes) at 1000 °C in an argon/hydrogen atmosphere. The high temperature is close to the copper melting point (1084, 62 °C). This procedure increases grain size, which leads to larger graphene islands. Structural defects are also removed, making the copper much cleaner in general. This clean copper foil is then exposed to a methane gas during the annealing, which leads to the formation of graphene (figure 8b). The graphene islands formed have different crystallographic orientations, depending on the orientation of the Cu film below. Increasing growth time increases flake size, until all different islands will join, forming a continuous graphene film, only limited by the underlying substrate size (figure 8c).

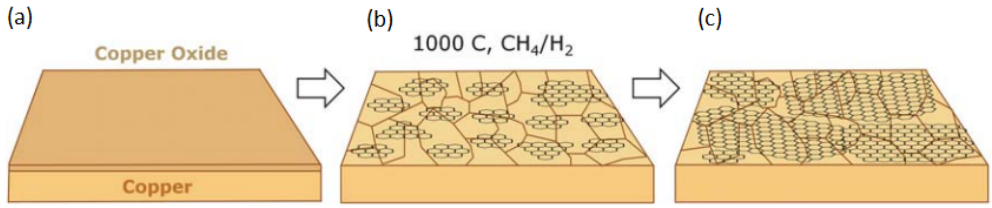

Figure 8: CVD graphene on copper. (a) A copper foil with native oxide on top. (b) Exposure to a methane/hydrogen atmosphere at very high temperatures, leading to formation of graphene islands. (c) Enlargement of the islands with different crystallographic orientations. Adapted from [21].

2.2.2 Electronic Properties

The electronic properties of pristine and CVD graphene are much the same, but there is a key difference between the two, which usually makes CVD grown graphene electrically inferior to exfoliated pure graphene. As mentioned in the former section, CVD graphene on Cu is composed of different islands, which are joined together during growth. These boundaries between different domains do not have the hexagonal structure of graphene, but instead consist of pentagons and heptagons. Boundaries between different islands are called grain boundaries [23]. They can also be called 1D interfaces between graphene islands of different crystallographic orientation, an example of which is shown in figure 9a. If a normal is made relative to the boundary, then the structure can be defined by two angles, θ_L and θ_R, which are the angles between the two domains and the normal.

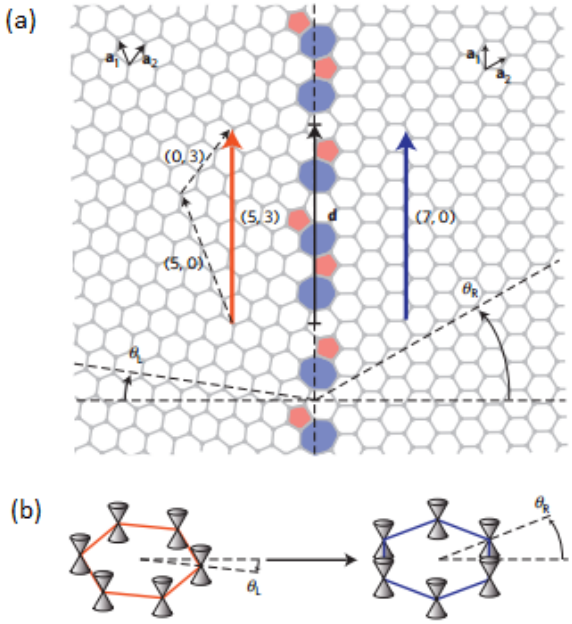

Figure 9: Structure of a grain boundary. (a) The grain boundary in graphene is composed of pentagons and hexagons, which seperate different crystallographic domains. The two domains are tilted an angle relative to the normal $\boldsymbol{d}$ of the grain boundary. (b) Rotation of the Brillouin zone experienced by charge carriers crossing the boundary in this example. Adapted from [23].

Charge carriers crossing a grain boundary experience a rotation of their Brillouin zone (figure 9b). Yazyev et al calculated, using conservation of momentum, that this flipping leads to the opening of a band gap given by

$$E_g = \hbar v_F \frac{2\pi}{3d} \tag{10}$$

where d indicates the periodicity. As such, charge carriers in CVD graphene has an additional scattering mechanism besides the one already mentioned in section 2.1.3, which is the reason for it being inferior to pristine graphene [24].

2.3 Molecular Junctions

Even though no molecules were used in this study, the ultimate purpose is to see if the graphene samples here are better suited for advancing in molecular electronics than reduced graphene oxide. A short introduction will therefore be given here. A molecular device is any electronic device, where molecules carry the current. This can be either single molecules or an assembly of such. A molecular junction is the current carrying region of the device, or the interconnect between the source and drain electrodes (figure 10).

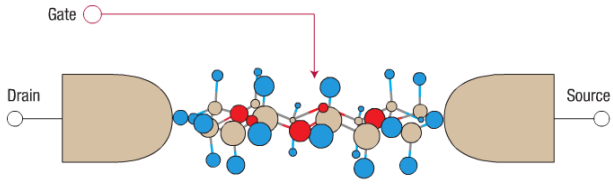

Figure 10: Illustration of a molecular junction. A single molecule is attached to two electrodes. Safe deposition of a top gate contact is a key challenge in molecular electronics, and one of the reasons for doing this project. With a top gate, electron transport through the molecule can be controlled and studied. Adapted from [25].

Molecular wires are an example of single molecules often studied, since they can provide interconnections for molecular devices. An example is alkane molecules consisting of saturated carbon-carbon bonds. These molecules have large gaps between their highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), and therefore poor conductors. The conductance has been shown to decay exponentially with increasing molecular length (meaning more carbon atoms). It also turn out to be temperature-independent, suggesting that the main transport mechanism is quantum tunnelling [26]. Due to the rapid decay in conductivity with length, only alkane samples 2-3 nm in length can be used. For long-distance transport, conjugated molecules are used, which contain both double and single bonds, and having a smaller HOMO-LUMO gap. At small lengths, conduction again happens through tunneling, while for longer lengths, it is replaced by a hopping conductance. Self-assembled monolayers (SAMs) are molecular assemblies formed on surfaces by adsorption. Since the molecules assemble themselves without any influence from the outside, these offer a cheaper method of producing molecular junctions than single molecules. Due to their large HOMO-LUMO gap of 8-10 eV, SAMs are insulating, and a tunnelling current is expected, which again decreases with increasing molecular length.

When making a junction, the electrodes are not fabricated simultaneously [27]. Instead, one electrode is made, after which for example a SAM is formed on it, fabricating the second electrode afterwards. Since the molecules are very small (around 2 nm), the surface of the metal electrode largely determines the final configuration of the junction. Furthermore, it is important for the surface to be as clean as possible, since a polluted surface leads to longer growing time or no growing at all. Depositon of the top electrode is more critical than the bottom electrode, since evaporating a metal contact on the SAMs likely results in filamentary growth of the metal atoms through the SAM. That is why a conductive interlayer is made between the contact and molecules. An example of such prior to graphene is poly(4-styrenesulphonic acid), shortened PEDOT:PSS [28]. With such a layer on top of the molecules, safe deposition of metal contacts can be made, leading to working devices.

2.4 Microscopy

2.4.1 Optical Microscopy

The optical microscope, or light microscope, is probably the most important tool used in this project, as it is an important factor in almost all steps of fabricating a pristine graphene device. In fact, it is used by all people exploiting the mechanical exfoliation technique for quick identification of graphene flakes. As the name suggests, an optical microscope uses visible light to visualize structures beyond the resolution of the human eye. Because of the wave nature of light, it does not follow straight paths, but instead travel through an optical system by different routes, resulting in interference between the paths, which causes optical diffraction effects [31]. If two waves reaching the same point by different paths are in phase, the amplitude of the resulting wave will be larger, making the light brighter. Out of phase waves, on the other hand, will cancel each other out, resulting in decreased brightness. An overview of how an optical microscope works is given in figure 11a. Lenses are used to focus the light on a given target. Optical microscopy is, however, limited by the wavelength of light, since a given radiation cannot probe structures much smaller than its own wavelength. Therefore, a light microscope can visualize objects between 0.4 μm (violet light) and 0.7 μm (deep red light). Objects smaller apart than this limit will appear as one single object.

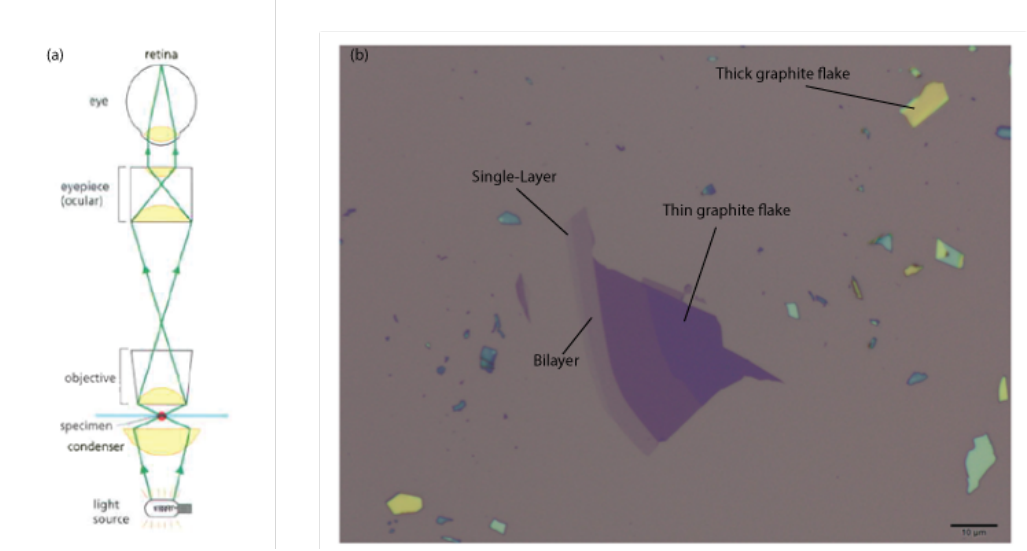

Figure 11: Optical microscopy of graphene. (a) The principle of an optical microscope. Light is focused on the substrate by lenses in the condenser. A combination of objective lenses and eyepiece lenses focus an image of the substrate in the eye. (b) Graphene on a silicon wafer with 285 nm of SiO2 at 100x magnification, made by mechanical exfoliation. The difference in contrast between single-layer and bilayer graphene can clearly be seen. (a) adapted from [31].

The first observation of graphene was with an optical microscope [5]. It turns out that graphene is clearly visible on Si wafers with a certain thickness of SiO2 on top, which is why people before Novoselov and Geim hadn't observed it. The reason for this peculiar behavior is given by Blake et al, but the calculations are not shown here [32]. They note that not only the SiO_2 thickness, but also the wavelength of the light used is important. The most used thickness's of SiO_2 are 90 nm, 285 nm, and 300 nm, even though, with appropriate filters, other values can be used as well. An example of a graphene sample on Si with 285 nm SiO_2 is given in figure 11b.

2.4.2 Atomic Force Microscopy

Even though optical microscopy offers a quick way of identifying graphene on Si/SiO2 wafers, one can often mistake for example SLG's and BLG's, since their difference in contrast is very small. Atomic force microscopy (AFM) offers another way of identification. AFM is a high-resolution type of scanning force microscopy (SFM), offering vertical resolutions down to 0.1 nm, while the lateral resolution is around 30 nm due to convolution. A sharp tip, usually a 3-6 μm tall pyramid, is mounted on the end of a millimeter-sized cantilever [33]. It operates by measuring the force between tip and sample. An image of the surface forms as the tip is scanned over the surface. Generally, a surface can be imagined using one of three different techniques, called contact-, non-contact, and tapping mode [34].

In contact mode, also called repulsive mode, the tip is in contact with the surface it scans, leading to a repulsive van der Waals force between tip and sample, while any other attractive force is strongly suppressed. In non-contact mode, the cantilever is set to oscillate at or just above its resonant frequency, where the amplitude of oscillation is typically less than 10 nm, detecting van der Waals forces between tip and surface. Since the attractive forces from the sample are substantially weaker than the forces used by contact mode, the tip must be given a small oscillation in order to detect forces by measuring the change in amplitude, phase, or frequency of the oscillating cantilever.

However, a soft material like graphene might be damaged by using contact mode. Tapping mode offers a reliable and non-destructive way of scanning graphene and other soft materials. In this mode, the cantilever is oscillating at or near its resonant frequency using a piezoelectric actuator like in non-contact mode. However, the amplitude of oscillation is much higher than for non-contact mode, typically 100 to 200 nm. During scanning, the tip is moved closer to the sample until it begins to lightly tap the surface. When the tip is close to the substrate, the amplitude of vibration changes according to the surface topography, which is due to energy transfer to the sample. A summary of all three modes is given in figure 12.

The thickness of single-layer graphene on Si/SiO_2 wafers is approximately 1 nm. So to know whether the sample is monolayer or not, one measures the height difference between wafer and sample. Bilayers are 0.335 nm thicker than monolayers (the interatomic distance between layers in graphite). For each layer added, another 0.335 nm is added to the thickness.

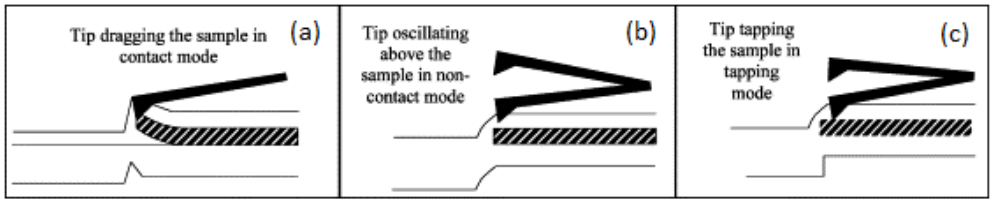

Figure 12: The three different modes in AFM. (a) contact, (b) non-contact, and (c) tapping mode. Figure adapted from [34].

3 Materials and Methods

3.1 Making the Chip

The chips were made at the Danish Technological Institute [3]. For junctions, thin 5 nm Ti/35 nm Au electrodes (made by UV-lithography) are thermally evaporated onto a clean silicon wafer with a 300 nm or 15 μm layer of SiO_2. The Ti acts as a sticking layer, since Au binds very poorly to other substrates. The electrodes are then covered with a 40 nm layer of aluminum oxide Al_2O_3 prepared by atomic layer deposition at 1 Å/cycle. Circular holes, or wells, with a diameter of 2 μm are then made in the Al_2O_3 by electron beam lithography. The principle is shown in figure 13a-d. Figure 13e-g shows real images of the chip, while zooming more and more in. For the bonding pads, 10 nm Ti and 100 nm Au is used.

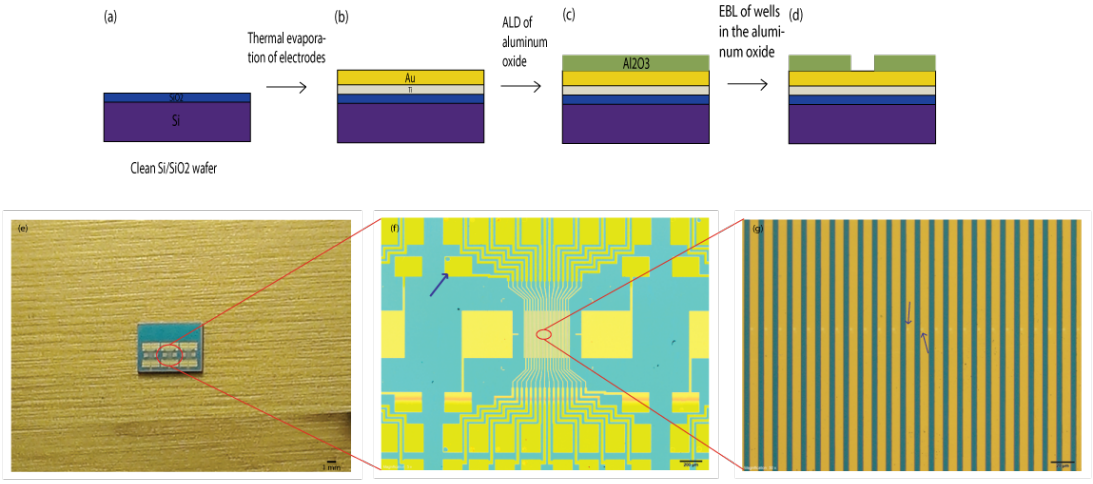

Figure 13: The chip design used for the project. (a-d) Schematic of the individual steps leading to a useable junction. (e) Picture taken at normal view of the chip. The area marked with a red circle is shown in (f) at 5x magnification. The blue arrow shows a bonding pad. (g) shows the circle in (f) at 50x magnification. The wells are clearly visible in the middle (blue arrows).

3.2 Micromechanical Exfoliation

All one needs in this part is a piece of adhesive tape and a chunk of graphite. A similar method was used for the isolation of graphene in 2004 [5]. The graphite used here is called graphenium, which is special graphite made to have large domains prior, so that the chances of getting large graphene flakes increases. Nitto Denko number BT-150E-CM tape was used, since this kind of tape doesn't leave glue marks on the wafer. When the tape is placed on a flat surface, the graphite is repeatedly placed on and taken off parts of the tape, covering an area approximately the same size as the wafer, which it will be deposited on. Then opposite halves of the tape come into contact, so that even thinner layers can be achieved (figure 14a).

Prior to deposition of graphene, the silicon wafer has to be as clean as possible. Therefore, it is washed in acetone, methanol, and isopropanol, followed by blowing dry nitrogen on it. Further cleaning is achieved by plasma ashing it for two minutes at a pressure of 0.5 bar to remove all organic material from the wafer. The adhesive tape is then placed on the wafer, while making sure that the best part of it comes into contact with it. Tape and wafer are squeezed together for a few minutes, after which the wafer with tape is placed on a 70 °C

hot plate, which makes removal of the tape easier. Immediately after placing wafer on hot plate, the tape is peeled off, leaving behind graphene and graphite on the SiO_2 surface (figure 14b) .

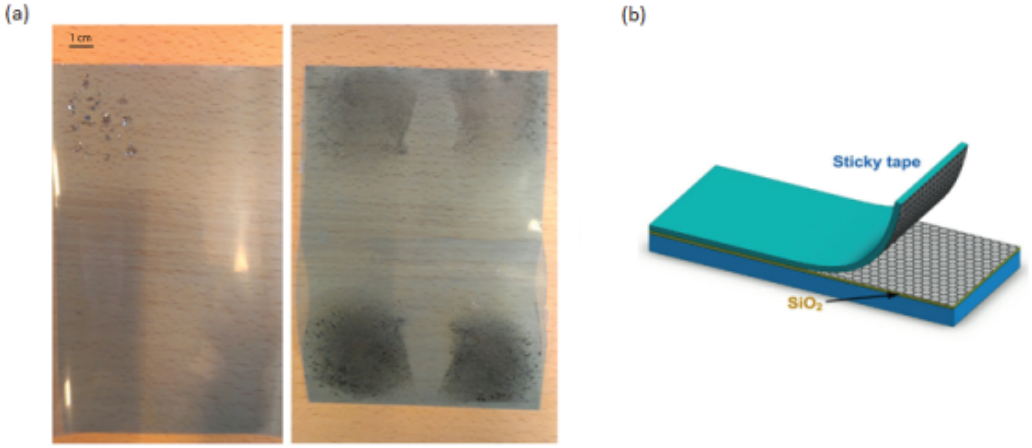

Figure 14: Mechanical exfoliation. (a) Adhesive tape just after the graphite is placed at various spots (left) and after making the layers thinner by joining different halves of the tape repeatedly (right). (b) The model shows the principle of putting graphene on the underlying Si/SiO_2 wafer. (b) Adapted from [29].

Once deposited, an optical microscope is used to find flakes of graphene. The microscope used is Olympus BX51M. The process is long, since graphene flakes are a minority among the thousands of thicker graphite flakes. Another limitation is the fact that graphene flakes needed for this project should have a length at least the same as the junction length, which is approximately 15 μm. They should also be at least 3 μm wide; the diameter of the micropores is 1-2 μm. Single layer flakes of this size are rare, and often one has to start over, since no SLG could be found. It should be noted that wafers used in this study contained alignment marks made prior to deposition of graphene. These numbers are reference points, making it much easier to localize a flake long after having found it, obviating the need for drawing the wafer and flakes to scale on a piece of paper.

3.3 Transferring to Substrate

Once a suitable graphene flake has been found, it has to be transferred to the chip with electrodes and wells. At first, the wafer is scribed to a smaller size before transfer. Poly(methyl methacrylate) (PMMA) has been proven to be a great as a support material for transferring graphene to arbitrary substrates [30]. Due to the small diameter of the wells, the PMMA should be as thin as possible, otherwise there won't be contact to the gold at the bottom. Therefore, 3% PMMA is used, since it follows the wells almost perfectly, confirmed with AFM (see section 4.2), while being relatively easy to handle. The PMMA film is deposited by spin coating at 4000 rpm for 45 seconds, since high rpm leads to thinner PMMA. Usually washing the PMMA off in acetone and then spinning again resulted in more uniform films with few or no ripples. After spinning, the wafer with PMMA is baked for 20 minutes at 115 °C. Then it is placed in 1 M sodium hydroxide (NaOH) until the hydrophobic PMMA/graphene film has detached from the underlying silicon, which usually takes 2-3 hours for the wafer size reported here. After detaching, the graphene is facing up, so it has to be flipped 180°, in order for the graphene and gold electrodes to have contact later. Since NaOH is corrosive, the PMMA film is transferred to a beaker with Milli-Q (high purity) water. The flipping is done by pushing the PMMA down with a glass slide, and then turning the glass slide around in the water. One has to be careful not to push too hard or too fast, since it can break the PMMA. To check if the PMMA film is turned upside down, the entire film is put on the glass slide and moved under the optical microscope. This is also why it is moved from NaOH to water, since NaOH could potentially damage the microscope. If the image of the graphene (from the same perspective) is mirrored, the sample has been flipped. With alignment marks, one can check it by looking at the coordinates; if the numbers are mirrored, one can continue.

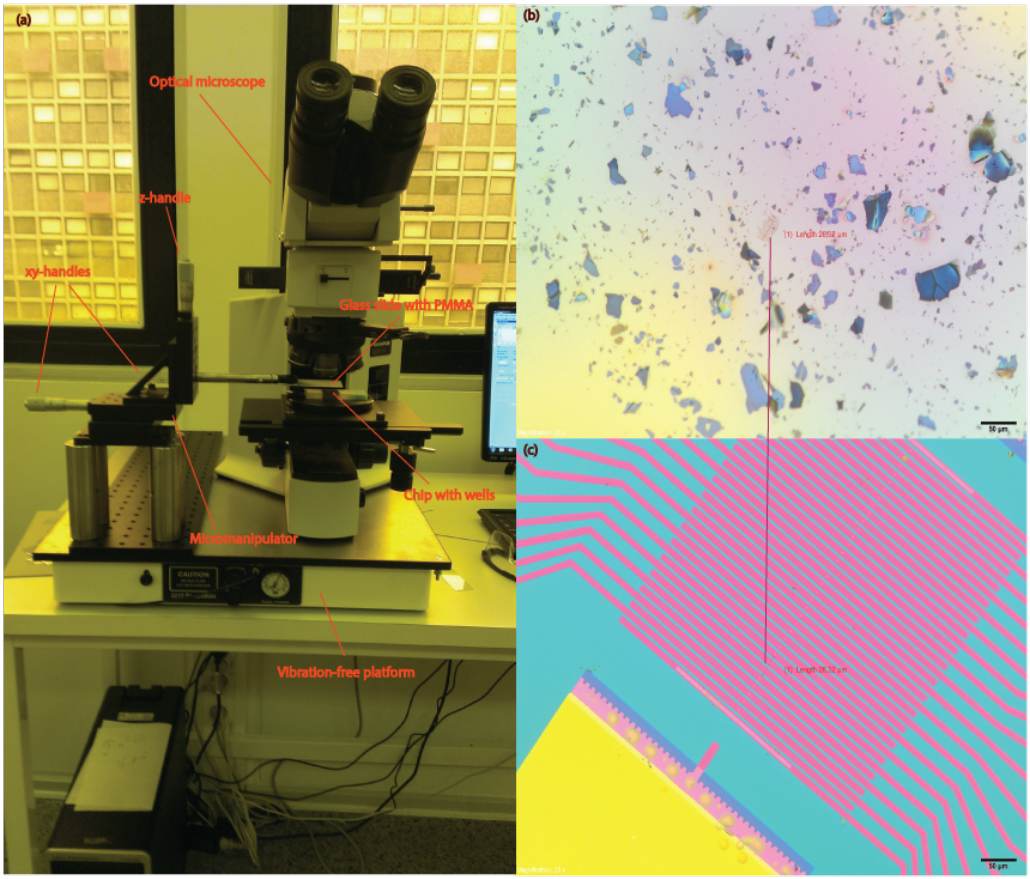

Figure 15: Depositing pristine graphene on electrodes. (a) Picture of the setup, showing that micromanipulator and microscope are placed next to each other on a vibration-free platform. (b) Optical image of a few-layer graphene flake in the PMMA. The flake remains in this position, while the underlying electrodes (c) are aligned with the flake using the microscope handles.

The final part of the experiment is the deposition of the graphene on the substrate. A device called a micromanipulator is used, which was ordered specifically for depositing graphene on electrodes. An illustration of the setup is shown in figure 15a. The manipulator is used in collaboration with the optical microscope (figure 15b-c). A glass slide with a tiny hole at the top is used for capturing the PMMA; one has to make sure that the graphene flake is suspended over the hole. The glass slide is then attached to the end of a handle on the manipulator using tape (see figure). The wafer is placed just below, attached to a stack of glass slides with tape. The graphene flake is now aligned with the electrodes below, which is done by first having the graphene in focus and then switching to substrate. After alignment, the wafer is moved up to the PMMA with the microscope handle. Once they are in contact, blowing dry nitrogen makes sure that PMMA and wafer stay together. Finally, the PMMA is washed off by the chip in a beaker with acetone for 20 minutes on a hot plate at 40 °C. A schematic of all steps are shown in figure 16.

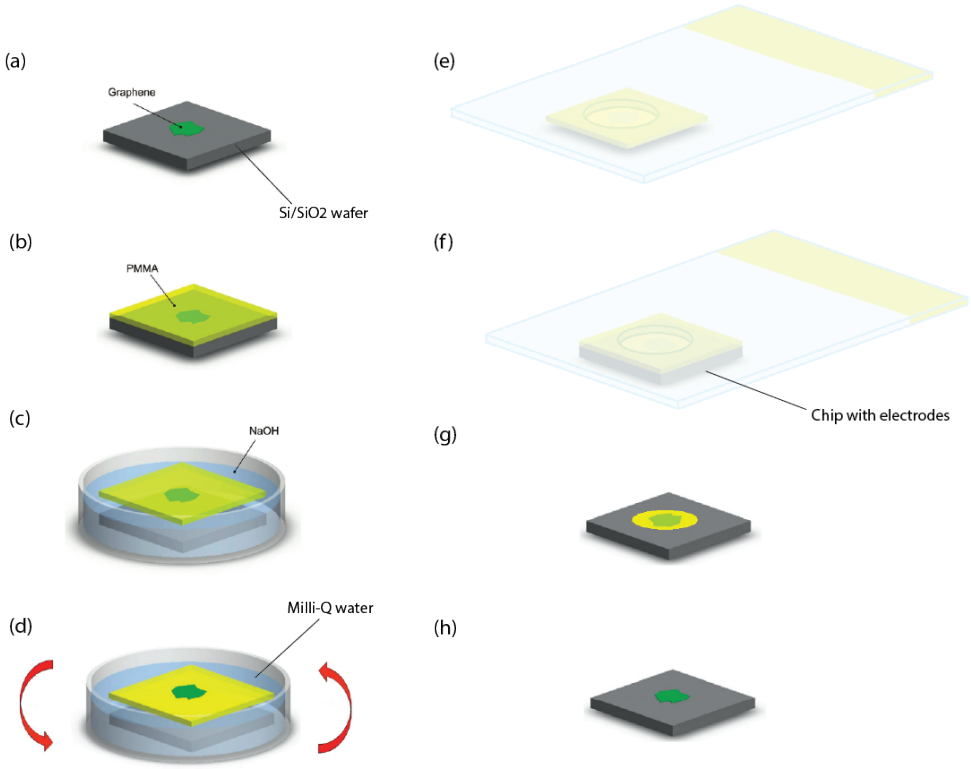

Figure 16: Schematic of all steps in the transferring process. The size of the graphene sample compared to wafer is greatly exaggerated. (a) Graphene on an Si/SiO_2 wafer. (b) Spin coating of a uniform PMMA film over the wafer. (c) The wafer with PMMA is placed in a NaOH bath, until the PMMA with graphene detaches from it. (d) The PMMA/graphene film is moved to a glass beaker with milli-Q water, where it is flipped 180° with a glass slide (not shown). (e) The PMMA is suspended over a porous glass slide, making sure that the graphene is suspended over the hole. (f) Using the micromanipulator, the graphene and chip (electrodes not shown) come into contact. (g) By blowing dry nitrogen and moving the glass slide back up, a chip with PMMA/graphene is left. (h) The PMMA is subsequently removed with acetone. Figure adapted from [29] with few changes made.

3.4 Measurement Setup

The schematic used for probing is given in figure 17. The numbers indicate what wells the bonding pads are attached to. When measuring the current, probes are put in contact with the pads connected to the graphene sample. Two types of measurements were done in this project, namely 2-probe and 4-probe measurements. Both types of measurements are depicted in figure 18. The figures only show few wells for simplification, but the principle is the same for other wells. R_g indicates graphene resistance, while R_c is the contact resistance. With the 2-probe technique, a current flows through the device with a known voltage, measuring the resistance as it passes from one well to another. A voltage divider is used to make the output voltage a small fraction of the input voltage. For measurements here, the voltage divider made the output voltage 1000 times smaller than the input voltage. Voltage was applied and changed with the computer, which is indicated with DAQ on figure 18a-b. All measurements were done with the LabView programme. The 2-probe technique is suitable for quick measurements of resistance. However, the resistance measured is for the entire system, meaning not only the graphene, but also the electrodes, giving a total resistance $R_t = R_g + R_c$. For the low resistances measured here, the contact resistance needs to be excluded for accurate measurement. Therefore, 4-probe measurements are used on functioning devices as well. With this technique, a second set of probes are used for sensing, with an voltmeter attached. The current flow through these additional probes is negligible, so only the voltage drop on the sample is measured, giving much more accurate results.

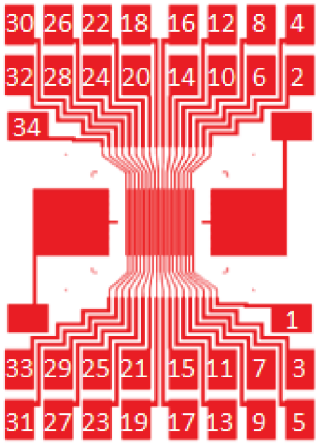

Figure 17: Drawing of a chip, with numbers on the bonding pads indicating to which well, they are attached. Resistance is measured by putting probes on the bonding pad attached to the graphene sample.

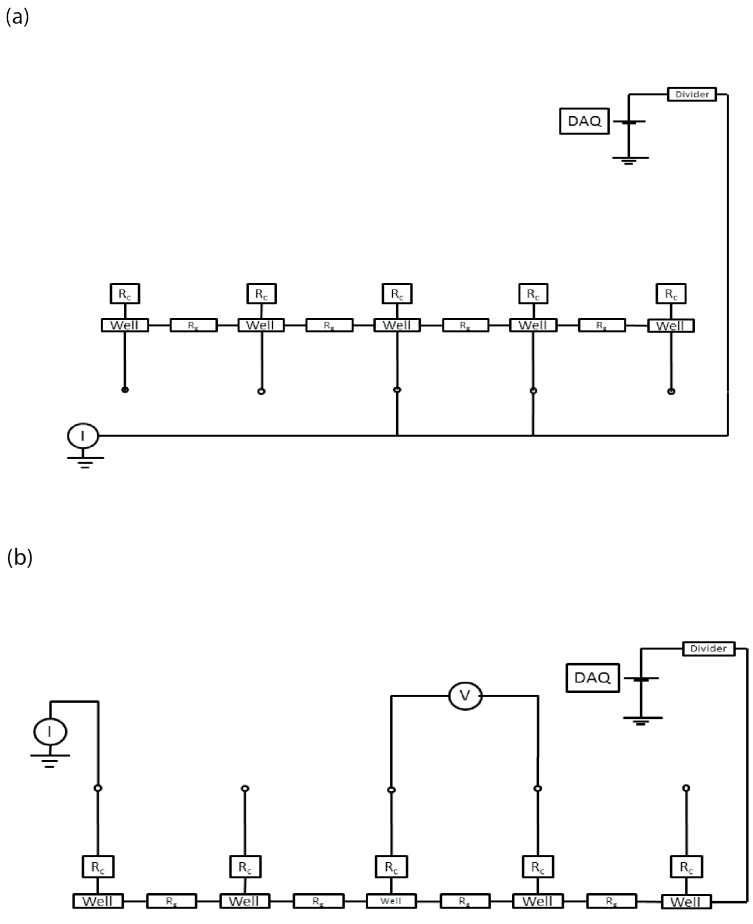

Figure 18: Schematic of the device setup. (a) The setup for 2-probe measurements with numbers indicating well number. The voltage divider makes the output voltage a fraction of the input voltage. (b) 4-probe measurements, where two additional probes are attached, so that only the resistance of the graphene is measured. R_g and R_c are the graphene and contact resistance, respectively.

4 Results and Discussion

The original purpose of the exercise was to compare electrical transport through CVD and pristine graphene. Due to problems in the fabrication of pristine devices, both in techniques and devices used, the goal was not met in time. However, certain improvements were made on the original experiment, and will be explained further below. First, appropriate single-layer graphene samples will be shown, followed by an explanation of the improvements made in fabrication. Then a correctly deposited, but not working, graphene device is shown. Finally, data for the CVD samples at room-temperature is shown and discussed.

4.1 Pristine Samples

Much of the project was spend on making appropriate pristine graphene samples. The making of graphene on Si/SiO_2 wafers is a rather short process, but the subsequent finding of flakes with the optical microscope is long, often resulting in many hours of search without any success. CVD samples from DTU are single-layered, so in order to compare the two properly, single-layer pristine samples were needed too, since the addition of just one layer changes the properties of graphene significantly. These can almost always be found, but due to the size of junctions and diameter of wells, not all samples are of use. The criteria for further use was a 15 μm length in order to connect two junctions, and minimum 3 μm width, in order to cover an entire well (though covering a well partially is enough for conduction). Much time was spent making sure the sample was single-layer or not. An example of two different graphene flakes are given in figure 19, where one of them is single-layer (19a), while the other is bilayer graphene (19b).

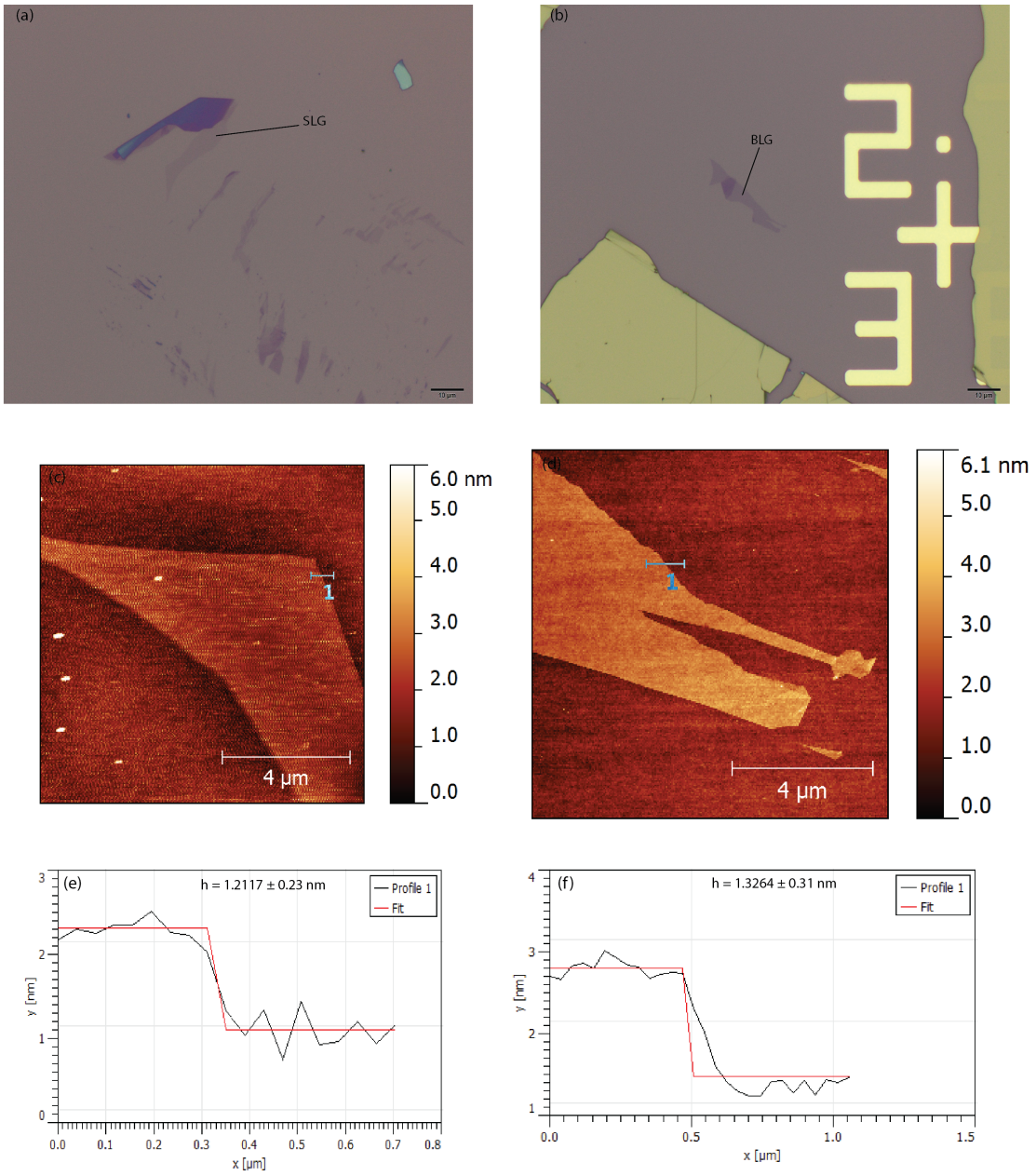

Figure 19: Graphene flakes on Si/SiO_2 wafers. (a) Optical image of a SLG suitable for molecular junctions. (b) An image of a BLG at the same magnification to show the small difference in contrast between the two. (c) AFM image of the flake in (a). Due to very high values of integral and proportional gain, the image came out with a lot of noise. The height profile in (e), however, still shows that it's an SLG (red curve indicates a fit of the height). (d) and (f) are the corresponding AFM image and height profile, respectively, for the BLG, where the AFM image is clearly better (much less noise and finer details).

Graphene on Si/SiO_2 has a height of approximately 1 nm, while the addition of extra layers increases this height with 0.34 nm (as mentioned in section 2.4.2). AFM data of both samples are shown in order to really grasp how little difference there is between the two (19c-d). Accompanied with the images are height profiles, which were made using the data visualisation and analysis program Gwyddion 2.31 (19e-f). Using this program, the height for the SLG was found to be $h = 1.2117 \pm 0.23$ nm, while the height for the BLG is $h = 1.3264 \pm 0.31$ nm. The profiles have a small variation at different edges of the samples, but the difference is very small (few nanometers). This was the best possible way of identifying SLGs in the short timespan of the project, even though better methods exist for characterization (e.g. Raman spectroscopy [36]). FLG flakes were often used to test whether a new method worked or not, but was not supposed to be compared with CVD graphene. In the end, however, FLG samples were used for deposition, due to lack of large SLG flakes.

4.2 Changing the Recipe

A great challenge was to safely transfer the graphene to the electrodes. Thicker PMMA is of course safer for transfer, since it is harder and, therefore, won't break that easily. Unfortunately, thick PMMA doesn't follow the wells and, when washed off, can break the graphene into many small pieces. 2% PMMA follows the wells perfectly. However, the PMMA film detaches from the wafer highly folded, so before the next step, it had to be unfolded. This often led to holes in the PMMA, marks that the glass slide left behind in the unfolding process. Even if the PMMA film survived the unfolding, it had to be flipped 180 °, which caused the PMMA film to break nearly every single time. Therefore, certain parameters were changed, the most important of which the thickness of the PMMA. The instructor had already informed that 4 % PMMA doesn't work, so 3 % PMMA was used instead. It turned out to be an excellent replacement of the inferior 2 % PMMA. Not only is it thicker and harder to break, it can follow the wells perfectly, confirmed with height profiles of the AFM images shown in figure 20. The images show the structure of two electrodes with wells. The black region between is the SiO_2 surface. The white line at the edge of the left electrode is due to bad lift-off in the fabrication process; such edges were up to 40 nm high, and were therefore avoided. The additional wells were the result of bad electron beam lithography. As expected, these additional wells turned out to be very shallow and, therefore, couldn't make a current flow (the graphene sample in figure 20 makes contact between two wells). The height of the actual well was h = 16.774 ± 1.0 nm before and h = 15.158 ± 1.1 nm after deposition of 3 % PMMA, while the shallow well had h = 1.7739 ± 0.50 nm before and h = 3.9114 ± 0.25 nm after.

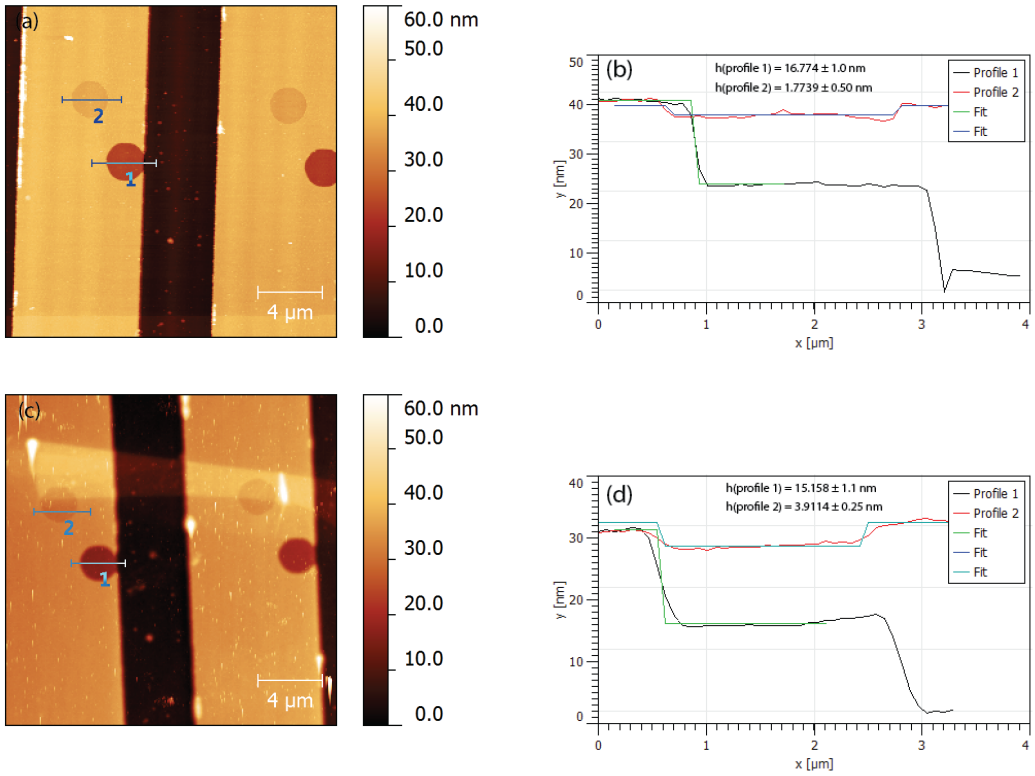

Figure 20: AFM images of two wells before (a) and after (c) deposition of a 3 % PMMA film. Also shown is height profiles of the wells before (b) and after (d) deposition. The height is almost the same, meaning 3 % can easily replace 2 %. The less visible wells in the middle were EBL gone wrong, so additional holes were made. It should also be noted that wells here were 15 nm in height, even though it should be around 40 nm (height of gold and titanium sticking layer). The transparent structure on the narrow wells is a deposition gone wrong (the sample shown in figure 19a.)

Si/SiO_2 wafers with graphene were also scribed larger, from 1 x 1 cm to 1.5 x 1.5 cm in dimensions instead. The last important change was in the micromanipulator step. At first, the equipment was put on the table in the cleanroom with the microscope next to it. The device, however, turned out to be highly sensitive to movement; taking one step could misalign a sample completely. That is why the vibration-free platform was put to use, since it made it possible to move around without disturbing the device fabrication process.

4.3 Pristine Graphene Device

As already mentioned, the pristine part of the project failed due to problems with both the recipe and the equipment. Many attempts were made, some of which are shown in figure 21. Figure 21b shows an example of how the PMMA got ruined during the final step, since part of the sample has been scratched off, rendering it useless. Though the vibration-free platform offered much help in making sure that the sample wouldn't shake as a response to movement in the cleanroom, it didn't offer a completely flat surface, since the optical microscope had bended it slightly downwards due to the long time standing on it. An example is shown in figure 21c-d, where the sample has been shifted quite a few μm above the wells, even though all steps prior were done correctly. In the end, this was the only issue left in the fabrication process, where the graphene flake lands perfectly aligned with the wells in the x-direction, while being displaced in the y-direction. Unfortunately, the naked eye cannot watch the small angle between PMMA and chip below, leading to a sample being displaced.

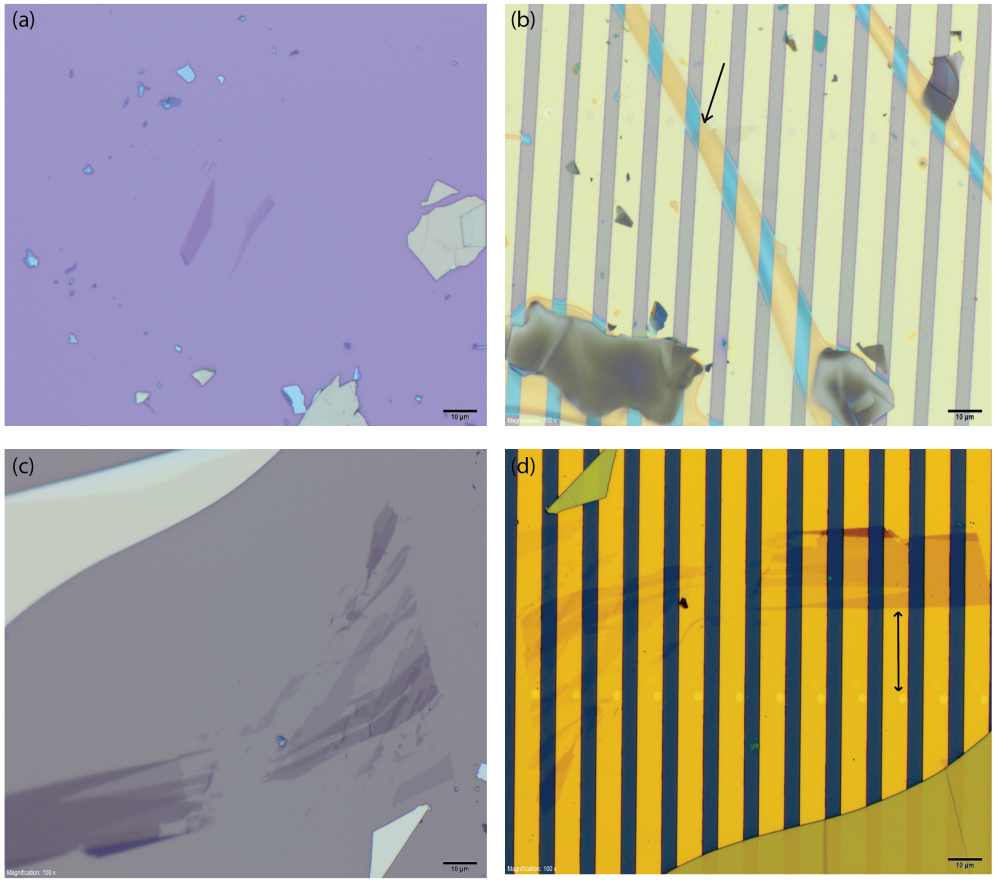

Figure 21: Failed attempts at depositing graphene. The PMMA film with the FLG shown in (a) on a Si/SiO_2 wafer, ended up folding at the final step (blowing dry nitrogen from top), resulting in only one well being covered, while the other was clean (black arrow in (b)). (c) Shows a rather large pristine samples (made by Jakob). The SLG part of it, however, was relatively small, so the FLG to the left was used instead. It ended up getting displaced in the y-direction (black double-arrow in (d)). The difference in color between (a) and (c) is due to (a) having 285 nm and (c) 90 nm SiO_2 below.

In principle, a device should work when two wells are hit completely or even partially. One of the SLG's had contact between two wells, which can be seen on figure 22 (where the sample in figure 22a was made by Jakob). Also shown is an AFM image, further confirming that the graphene and wells are in contact. But when probing the resistance with a bias voltage of ± 5 mV between the wells, no current would flow. The sample was subsequently thermally annealed for one hour at 350 °C, but no change was observed in the conductivity.

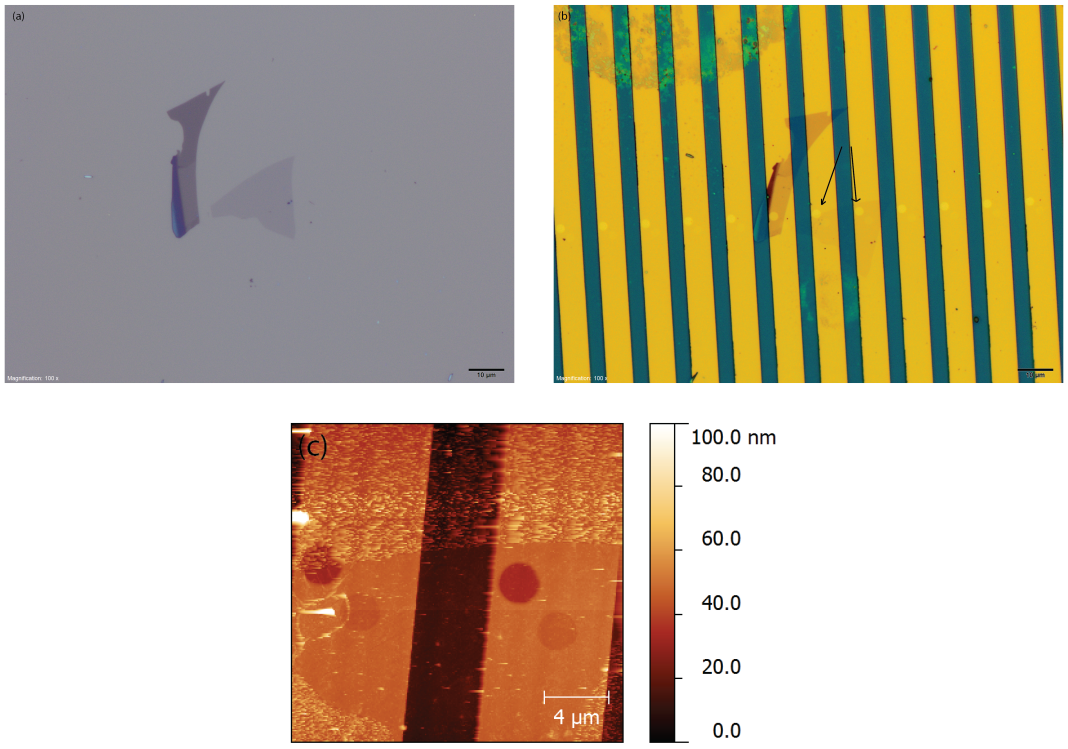

Figure 22: A correctly deposited graphene flake. (a) Optical image of the sample on Si/SiO_2. (b) Optical image of the sample on electrodes. As the arrows indicate, it clearly covers two wells (partial covering is enough for the device to function). (c) AFM image of the electrodes with graphene on. The sample shape can clearly be seen, at it covers the right electrode completely, while covering half the left electrode.

As a final attempt, the voltage was changed from ±5 mV to ±10 mV, ±50 mV, ±100 mV, ±300 mV and finally ±1 V. A plot of voltage as a function of time is given in figure 23a, with a corresponding plot for the current as a function of time given in figure 23b. Even though the voltage sweep changes drastically, the current remains much the same, showing that the graphene device doesn't conduct electricity. The large fall in noise for the current is due to the fact that the "box" in which room-temperature measurements are done was closed, leading to a 50 Hz noise reduction. A possible explanation for the lack of current could be that the wells on the chip was only 15 nm in height, indicating that some aluminium oxide could still have remained inside it. However, CVD devices made with the same well height did work (section 4.4), so the explanation is not conclusive.

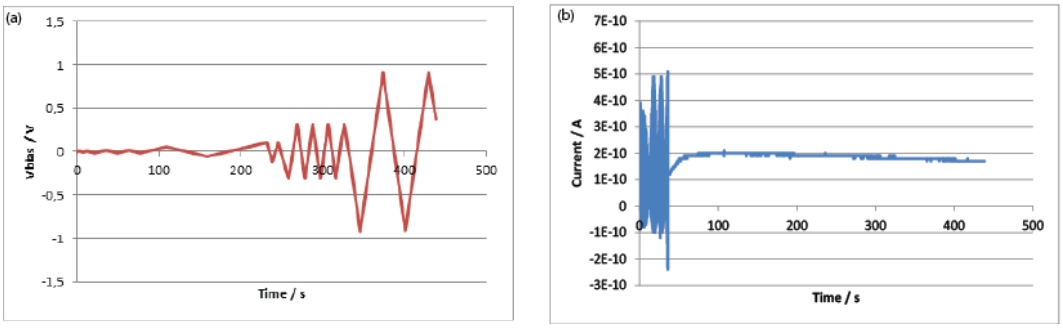

Figure 23: Voltage (a) and current (b) for the device shown in figure 22 as a function of time. The voltage was swept from ±5 mV up to approximately ±1 V, but no change in the current occurred. The reduction in noise for the current is explained in the text.

4.4 CVD Graphene Devices

The CVD graphene samples were made on DTU, but the final procedure was much the same, e.g. using PMMA to transfer to the chip. However, many samples were ruined, the reason for which is probably due to bad removal of the PMMA. An SEM of a working device is shown in figure 24. The CVD sample covers a total of twelve wells, meaning a current should flow through all these.

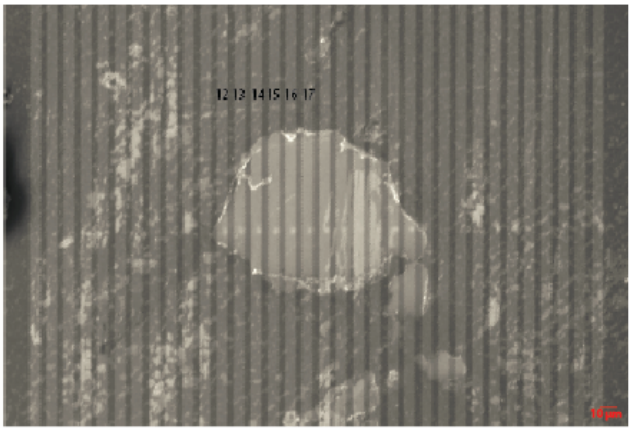

Figure 24: SEM image of a CVD sample made at DTU. It clearly covers twelve wells, with data given for wells 12-17 (indicated in drawing).

Data of the measured resistance is given in figure 25 and table 1. Measurements were done on wells 13-16 for the 2-probe setup with a bias of 10 mV, while the 4-probe measured the resistance from wells 12-17 with a bias of 16 mV. All measurements were done at room-temperature. One of the goals of the project was to see the dependence of the resistance on distance. Therefore, besides measuring through nearest-neighboors, the resistance, when going one or more wells further away, was measured. For the 4-probe setup, resistance from well 12 to 17 was also measured. For each setup, two sweeps were made, giving two resistance values each time. Rough estimates of the resistance for 2-probe and 4-probe measurements are given in table 1. Also shown is the difference in average resistance for both types of measurements.

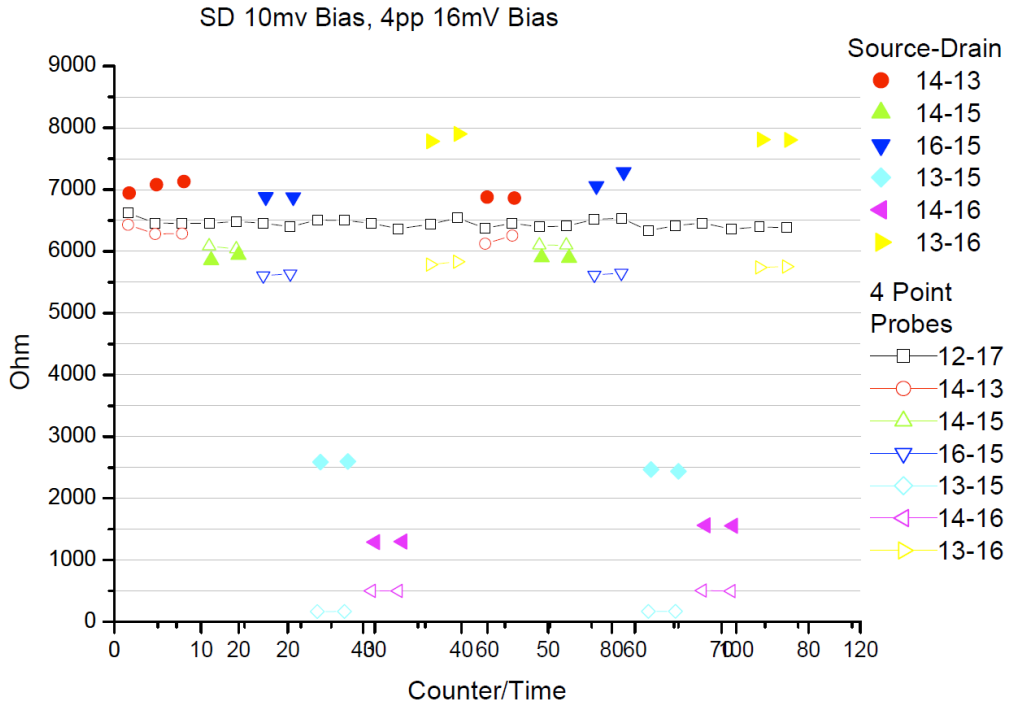

Figure 25: Resistance of the device in figure 24. Source-Drain indicates 2-probe measurements. Except for 14-15, all resistances drop when switching to a 4-probe setup. Most values seem to be around 6-7 kΩ, but a few of them are much lower, discussed in the text.

One can look at the data for 2-probe and 4-probe separately. 2-probe measurements gave resistance values ranging from 6-8 kΩ for most measurements. However, measurement 13-15 and 14-16 showed values much lower than the others, lying around 2.5 kΩ and 1.5 kΩ, respectively. With a 4-probe setup, the resistance for all setups, except 14-15, lowered substantially. Looking at the figure, most values fell with approximately 1 kΩ, indicating that this is the contact resistance. However, the resistance of setup 13-15 fell substantially more than the rest. Also, the values for 13-15 and 14-16 again were much lower than the rest. If not for these wells, the resistance would remain pretty much the same, indicating a lack of dependence on distance, however, this can

Table 1: Resistance values for 2-probe and 4-probe measurements of the device in figure 23.

Wells	2-probe R-value	4-probe R-value	Difference
14-13	7000	6300	700
14-15	6000	6000	None
16-15	7000	5500	1500
13-15	2500	200	2300
14-16	1500	500	1000
13-16	7800	6800	1000
12-17	Not measured	6500	None can be made

not be deduced from these data.

The main issue lied within setup 13-15 and 14-16. Both of them are examples of same-side measurements, meaning that the bonding pads are on the same side of the wells, unlike wells lying right next to each other or with an even number of wells between them. Looking at figure 24, one can see that the graphene flake covers an area much larger than the wells. Therefore, a current could in principle flow due to the bonding pads also, leading to better conductivity and therefore lower resistance. Why the resistance falls by so much when excluding contact resistance for 13-15 is not known. Nonetheless, the measured resistances are considerably lower than for Li et al, who measured resistances a factor of 10 larger at the same temperatures [1]. Also, when inspecting CVD graphene on copper by other authors, the resistances there also lie in the kΩ range, even though they were transferred to other substrates [35].

5 Conclusion

The original purpose of the project was to compare electronic transport in pristine graphene with CVD graphene using the device introduced in [1], to see if they could provide an improvement on the reduced graphene oxide. This goal was not met due to problems with the machinery and the short timespan of a bachelor project. However, improvements were made on the transferring of pristine graphene samples to electrodes, namely with the use of 3 % PMMA and the addition of a vibration-free platform in the setup. No final conclusion could be made on the CVD sample, since a few wells demonstrated oddly low resistance. However, the resistance was considerably lower than for the CDG films, which was one of the goals to check. There wasn't enough time left to see whether decreasing the temperature would change the resistance or not. With further improvement in the pristine fabrication part, a great comparison between pristine and CVD should be possible

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