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Fabrication and Characterization of As-Grown, Suspended Single-Walled Carbon Nanotubes

Bachelor Thesis in Nanoscience

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July 3, 2013

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In this thesis I describe the fabrication of so-called as-grown, suspended single-walled carbon nanotube (SWCNT) devices grown by chemical vapor deposition (CVD). The purpose of this project has been to describe and develop a fabrication scheme for producing clean, suspended and bottom gated SWCNTs allowing for electrical characterization at low temperatures. The major fabrication concerns includes the metal stack combinations for electrodes suitable for *in situ* CVD growth. The devices are characterized by room-temperature gate voltage measurements indicating small-band gab semiconducting SWCNT and low temperature measurements (0.3 K) indicating Coulomb blockade-like features. However, the produced SWCNTs are not defect-free and in general show multiple and ill-defined quantum dot (QD) behavior prompting several suggestions for the further development of cleaner devices. The interesting properties associated with the coupling of a SWCNT to superconducting electrodes are introduced as well as the first experiences with a superconducting alloy of rhenium and molybdenum.

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1 Introduction

This thesis presents the work of my bachelor project at the Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, Denmark. In the beginning of this project I joined efforts with M.Sc. stud. Morten L. Olsen, who was during his master project, concerning the development and characterization of as-grown, freely suspended SWCNT devices, facing the immediate issues regarding the choice of appropriate materials for the metal contacts of such a device. This device holds the possibility of choosing contact materials with many different properties and from the beginning of this project, it has been an interesting perspective to investigate the possibility of bridging a SWCNT between two superconducting contacts[1].

Traditionally, carbon nanotube (CNT) devices have been fabricated by either depositing CNTs on a substrate and aligning electrodes on top of them[2] or depositing CNTs on top of the electrodes[3]. Suspended CNTs could be formed by etching the substrate underneath[4]. I define a freely suspended SWCNT as having a segment only surrounded by the ambient atmosphere; outside this segment the SWCNT is connected to electrical contacts. The realization of an ideal, *in situ* grown or so-called *as-grown*, suspended SWCNT device has an appealing feature in the lack of direct surface interactions (e.g. van der Waals interactions) between the nanotube and the substrate. Furthermore, growing the nanotubes directly over a trench between the contacts as the last step in the device fabrication should prevent the introduction of defects into the SWCNT, which undergo no further treatment. Ultraclean and low-disorder SWCNTs are important for studying the intrinsic electrical and mechanical properties of nanotubes and the exploration of new phenomena, such as the strong spin-orbit coupling due to the nanotube curvature[5] or the formation of a one-dimensional Wigner crystal in a nanotube[6]. The first low temperature studies on ultraclean, as-grown suspended SWCNTs were done by J. Cao *et al.*[7][8] and their device recipe has been implemented by others[6][9][10]. They were able to produce clean, single electron transport features of few electron QDs in SWCNT with lenght $L \sim 1\,\mu$m in different transport regimes.

After a short introduction to CNTs, the methods and results of the device fabrication will be presented. The fabrication of a clean, suspended SWCNT device behaving as a QD would allow us to investigate zero-dimensional electron transport phenomena in the mesoscopic regime, which can be reached in a SWCNT at cryogenic temperatures ($< 1\,$K). After giving a theoretical overview of the electron transport through a SWCNT QD at low temperatures focusing at the Coulomb theory, the electrical measurements are presented. A brief phenomenological introduction to SWCNT coupled to a superconducting circuit is also included. Finally, the devices are visualized using scanning electron microscopy (SEM) followed by a discussion with focus on how to optimize and improve the quality of the suspended SWCNT devices.

1.1 Technological Applications of Suspended Carbon Nanotube Devices

Carbon nanotubes have, due to their structural properties, been implemented in different carbon fiber based materials improving their tensile strenght or in polymers and tissues (hydrogels) to adjust their mechanical properties[11]. The commercial applications are however today limited to the use of bulk CNT materials. For scientific purposes CNTs have been used as miniature nanotools; e.g. as tips for atomic force microscopy (AFM) or as tweezers[12]. More interestingly, single molecule electronic devices have been realized with SWCNTs acting as field-effect transistors or nano-electromechanical system (NEMS) for ultra-sensitive mass or force detection[13]. These are steps in the ongoing miniaturization of electronic devices and the development of a controlable QD for quantum computation devices[14]. A suspended CNT device could be implemented as a clean molecular sensor in a gas[15] that will completely surround the CNT, in bioelectronics as a sensor in liquids[16] or in optical experiments and applications[17].

1.2 Electronic Structure of Carbon Nanotubes

In 1991 a new class of fullerenes was discovered when S. Ijima reported the finding of needle-like carbon tubes[18]. These macromolecules have ever since created a lot of attention due to their fascinating electronic and structural properties. There are two types of CNTs: SWCNTs with a diameter of $\sim$1 nm and multi-walled CNTs consisting of concentric SWCNTs. Both of these types can be made in ropes or bundles, but only SWCNT will be considered here. Imagining a SWCNT as a single rolled-up graphene layer is a constructive starting point for understanding its electronic and geometrical structure. The sp^2-hybridized carbon atoms of a nanotube are arranged in a hexagonal lattice with a two-atom basis and described by two unit vectors a_1 and a_2 (fig. 1.1). The chiral or *roll-up* vector $\mathbf{C}$ uniquely defines the circumference and chirality of the tube and it can be written as a linear combination of the unit vectors: $\mathbf{C} = na_1 + ma_2$, where the indices (n, m) with $n \geq m \geq 0$ are used to define the specific tube[19]. This separates nanotubes into three different structural types: zigzag $(n, 0)$, armchair (n, n) and chiral (n, m) with $n > m > 0$. As with the construction, the electronic properties of SWCNT can be derived from the (band theory of) graphene. The band structure of graphene in fig. 1.1 is calculated in the tight binding approximation and shows how the conductance and valence bands are degenerate at the six (Fermi) points at the Fermi energy in the first Brillouin zone; thus it is a zero-gap semiconductor (semi-metal). By forming a tube, periodic boundary conditions are imposed on the electronic wavefunction around the tube – that is in the direction of the roll-up vector $\mathbf{C}$:

$$\mathbf{k} \cdot \mathbf{C} = 2\pi q,$$

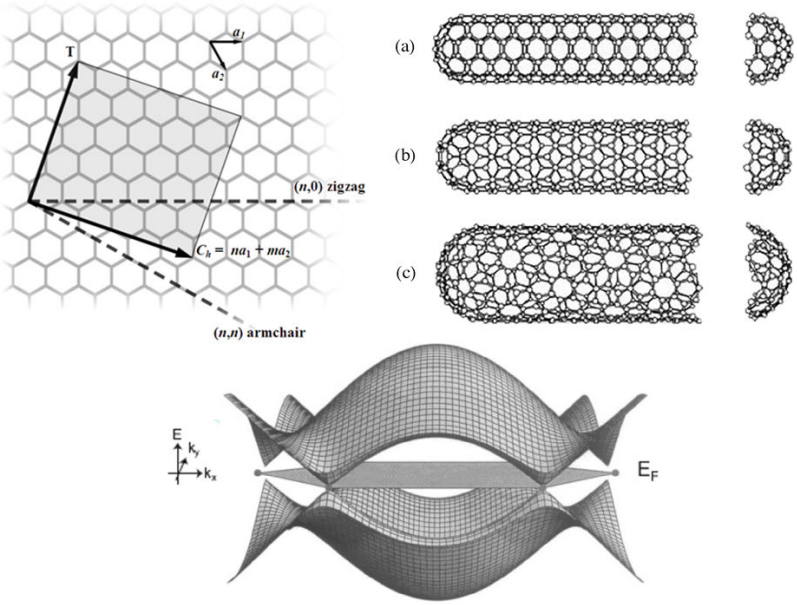

Figure 1.1. Construction of a CNT: The unit vectors and the roll-up vector are shown on the graphene sheet. **T** is the translation vector, that spans the unit cell. Below is the energy dispersion relation of graphene. SWCNTs in the **a)** armchair, **b)** zigzag and **c)** chiral configurations. It is also indicated how the tubes could be capped by hemisphere fullerenes. (Courtesy of K. Grove-Rasmussen and [20].)

where **k** is the wave vector and q an integer. Hence the component of **k** along the circumference is quantized and these quantization lines determine the one-dimensional band structure of a SWCNT. If some of the quantization lines pass through the corner (Fermi) points between the conduction and valence bands, there is no gap and the tube is metallic. This is the case for armchair tubes, where two lines cross the Fermi energy giving them an ideal conductance of two channels, i.e. $4e^2/h$ ($R = 6.5\,\mathrm{k}$) as desribed by the Landauer-Büttiker formalism. Zigzag or chiral tubes are only metallic when $(n - m) = 3p$, where p is an integer, otherwise they are semiconducting.

The above *zone folding* approximation does not concern the curvature of the tubes, which is crucial to small diameter tubes[21]. The curvature induces a shift of the Fermi points, which doesn't affect armchair SWCNTs (shifts along the tube), but can create a small band gab in metallic zigzag or metallic chiral SWCNTs (shifts along the circumference). Small band gab semiconducting zigzag and chiral SWCNTs can also become metallic due to curvature effects.

2 Device Fabrication

The device fabrication is done in seven general steps, which will be outlined in this chapter, where also the difficulties and results relevant to the fabrication methods are presented: **1)** Sample preparation. **2)** Electron beam lithography (EBL) defines the contacts followed by development and oxygen plasma ashing. **3)** Metal evaporation followed by lift-off. **4)** EBL defines the catalyst islands before development. **5)** Apply catalyst and lift-off. **6)** Nanotube growth by CVD. **7)** Mounting and bonding the sample in a chipcarrier.

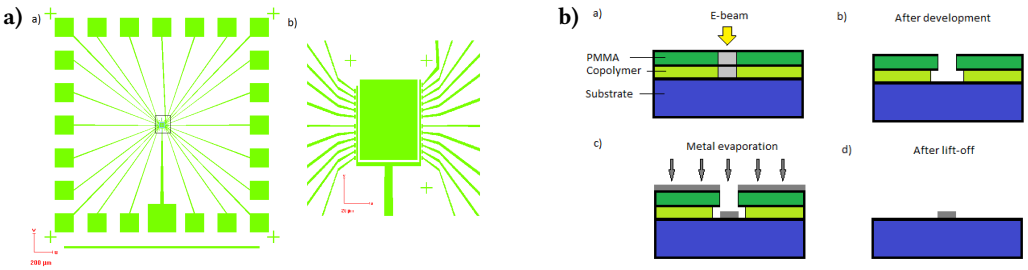

Figure 2.1. a) Image of the chip design with a 10 x zoom on the gabs and catalyst island. The crosses are alignment marks. **b)** Illustrates the formation of the undercut during the fabrication processes: EBL, development, metalization and lift-off as described in the text.

2.1 Sample Preparation

Before EBL. The chip is cut out of a silicon wafer (highly p-doped Si to remain conductive at low temperatures and with an insulating 500 nm SiO_2 layer on top) usually 20x20 mm and washed with methanol, acetone and isopropyl alcohol (IPA) and dried with N_2. The chip is then pre-heated at 185 ℃ for 3 min and a layer of 6 % copolymer (2-ethoxyethan-anylacetate) dissolved in anisole is applied to the chip by spinning (4000 rpm in 45 s) and baked at 185 ℃ for 6 min. Afterwards a layer of 4 % PMMA (polymethyl methacrylate) is applied in the same way.

After EBL. The sample is developed immediately after exposure in MIBK (methylisobutyl-ketone) diluted in IPA $1:3$ directly in an ultra sound bath without a plastic mesh for 60 s. This procedure was adopted after having had uneven developments from simply whirling the chip around in the developer by hand – a method only suitable for smaller chip sizes (< 5 mm).

Applying the catalyst. After metal evaporation and lift-off (section 2.3), a new layer of only 4 % PMMA is applied as above and the catalyst islands are written (EBL) by aligning the existing contacts to the design file (fig. 2.1b). After development as mentioned above, the sample is cut out into the individual devices (preferably quadratic chips) suitable for mounting in a chipcarrier before applying the catalyst. This makes it easier to spin on the catalyst and the cutting should be done before CNT growth. The catalyst ($Fe(NO_3)_3 \cdot 9\,H_2O$) is stirred for a couple of minutes before deposition. Many different parameters has been varied to optimize the catalyst deposit: One way is to apply a drop of catalyst to the chip at rest and use the capillary forces of a cleaning tissue to suck it almost dry and leave it to dry or slowly spin the chip to around 800 rpm for a couple of minutes. This way might leave a too thick catalyst layer resulting in a bad lift-off. Alternatively apply the catalyst to the chip while spinning and slowly accelerate up to maximum 1200 rpm for a couple of minutes. Spinning faster will usually result in the loss of too much catalyst. The catalyst deposit is always checked in the microscope and the procedure can be repeated before leaving the chip on a hotplate at 185 ℃ for 3 min to evaporate the solvent. Finally the lift-off is done in PG-remover at 70 ℃ for 45 min or at room temperature over night and ultra sound is used if needed.

2.2 Electron Beam Lithography

2.2.1 Principles of Operation and General Fabrication Concerns

The electron beam lithography (EBL) technique is based on the scanning electron microscope (SEM) providing a beam of thermionically emitted electrons which are strongly focused by a series of magnetic lenses (beam size 1-3 nm)[22]. EBL/SEM is operated under high vacuum (10^{-10} mbar) to prevent scattering of the beam apart from the mutual repulsion of the electrons. In EBL the beam is focused onto an organic resist material, which solubility is modified according to exposure time, beam current and resist properties. As mentioned above a double layer of positive resists is used: PMMA on top of copolymer; both long chain polymers, which are cut into smaller fragments under electron irradiation. The exposed resist is dissolved by immersing the chip in a developer (MIBK). The copolymer is more sensitive to electron exposure than PMMA, so during development an undercut is created (fig.2.1b), which should make the following metal lift-off process easier. On the other hand if the undercut is too deep the metal on top may collapse.

Inside the resist, the electrons undergo multiple elastic collisions (forward scattering), which slightly increases the beam size, but most of these electrons pass through the resist and into the substrate[23]. Some of the electrons, however, are backscattered into the resist again (fig.2.2) away from the beam spot, giving rise to the proximity effect, which can lead to overexposure of nearby feautures. A general concern during fabrication was the overexposure of the gaps between source and drain contacts (fig.2.1a).

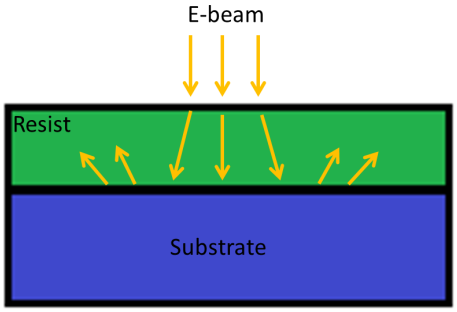

Figure 2.2. Schematic illustration of the EBL process: The electrons (yellow arrows) are inelastic forward scattered when entering the resist (green) causing the beam to broaden and they can be elastic backscattered from the substrate (blue), which gives rise to the proximity effect.

To obtain a sharper development of the gaps and to reduce the overexposure effects, developing in MIBK on ice has been tried. At 0 ℃ only the smallest fragments of the exposed polymer chains are dissolved, preventing the dissolutions of longer fragments more likely created by the backscattered electrons in the proximity effect. This requires much longer development times up to 10 min in ultra sound and the gaps were not significantly improved.

The EBL system used (Raith eLiNE) features a design program: The current device design (fig. 2.1a) was adopted from M. L. Olsen and it has been slightly modified during the project. The EBL system divides the design into several writefields and the stage is moved by a laser controlled piezo with each writefield. Drifting of the stage is caused by vibrations, thermal variations and charging effects, which limits the precision of stitching the writefields together. Therefore the eLiNE system is vibrationally isolated and airconditioned and to prevent electrostatic charging of the chip during exposure, due to the absorbed electrons not being able to escape below the chip, graphite is applied to the back of the chip. Proper writefield alignment and stitching errors has been a concern in the design; e.g. all the fine features in the center are placed within the same writefield.

During this project the eLiNE system faced a series of technical problems including a pump replacement and loss of laser stage control, so a few devices were written using the Elionix EBL-system. Elionix is capable of providing up to 100 kV acceleration voltage, thereby greatly reducing the proximity effect and enabling fine structures of a few nanometer in size. The smallest feature in the design is the 500 nm gap between source and drain contacts and the eLiNE user surface is conveniently reduced compared to Elionix.

2.3 Metal Contacts

2.3.1 Criteria for Metal Stacks Surviving CVD

The high temperatures of nanotube growth by CVD (900 ℃) constrains the choice of materials for the ohmic metal contacts. The procedure used is to stack different metals to create a sticking layer, ensuring adhesion to the substrate and a (bonding) layer on top suitable for wirebonding. Furthermore the sticking layer or another (blocking) layer at the bottom should be able to prevent metal diffuion into the doped substrate, which act as a backgate, creating a leakage current. In summary, the metal stack should during CVD: **1)** not melt, **2)** not react and diffuse, **3)** not act as a catalyst for nanotube growth, **4)** be able to wirebond to and **5)** remain conductive and ensure good electrical contact to the nanotubes. In addition to these criteria the metal combination should have a successful lift-off after metal evaporation maintaining well-defined 500 nm gaps.

2.3.2 Material, Evaporation and Lift-off Conciderations and Results

The metal film evaporation was done using an AJA International Evaporation System in a vacuum of 10^{-8} Torr. A target metal crucible is heated by an electron beam evaporating the metal into the chamber so it condensates at the sample. Lift-off is done in PG-remover[1] at 70 ℃ for 45 min and ultra sound is used if needed. Gold contacts, having a melting point of 1064 ℃[24], would form droplets or diffuse into the backgate and palladium is an excellent catalyst for growing MWCNTs[10]. Inspired by H. Churchill[10] a sticking/blocking layer of wolfram (W), which has a high melting point of 3410 ℃[24], and a bonding layer of platinum (Pt), with melting point 1768 ℃[24], were used initially.

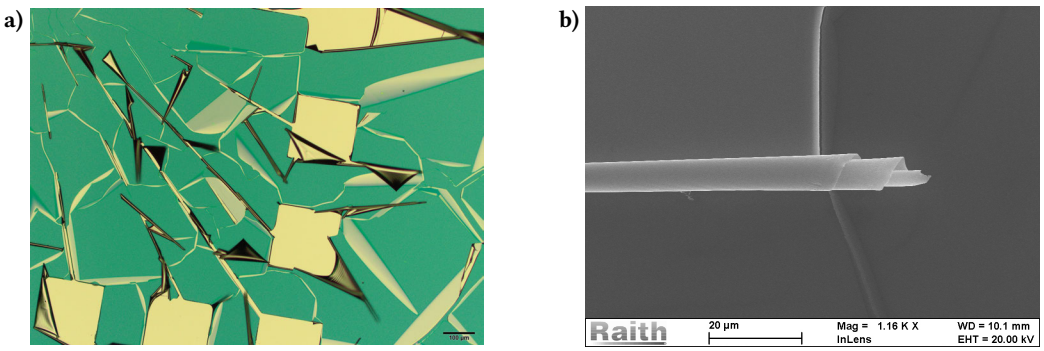

Figure 2.3. a) Optical microscope image of W/Pt 5/90 nm after lift-off. The surface was usually visibly cracked after metalization (before lift-off). **b)** SEM image of the same W-Pt chip showing in detail the curl of the metal flakes.

[1]Both hot and cold acetone has also been used, which in general resulted in a difficult and uneven lift-off.

A thick layer of W (> 20 nm) could catalyse the production of MWCNTs[10], but the opposite is also reported[25]. Using W was not a success in any way: the metal film cracked – in some cases immediately after metalization (fig. 2.3) or during the subsequent lift-off, when the edges would become rough and frayed and curl up as if released from some strain. This strain might have been induced if a thin metal film were covering the edges of the resist features (fig.2.1b: i.e. if the metal deposited on the wafer is not free of the metal on top of the resist).

In fig. 2.4 is another example of a thick Pt layer evaporation. Pao *et al.*[26] suggests that the Pt layer itself might be the source of a bad metal evaporation; they too obtained blisters and metal flakes after evaporating Ti/Pt/Au on PMMA resist. They suggest that because Pt e-beam evaporation produces an excess of electrons, they will charge the resist and hence cause a chemical reaction with it. This reaction (supposedly with the PMMA) should produce a gas trapped underneath the metal layers causing it to burst out or form blisters resulting in a cracked surface (fig. 2.4). The AJA evaporation chamber is not equipped with e.g. a magnetic field to bend of the free electrons from the e-beam, however, the sample holder is electrically grounded, which should provide a path for the excess electrons.

Appendix A summarizes chronologically some of the metal stack combinations, the thicknesses and evaporation rates used and the observed results. A 40 nm "terrace" of SiO_2 turned out to ease the lift-off process, probably by reducing the contact between the metal and resist edges. H. Churchill did not recommend the use chromium (Cr, melting point 1907 ℃)[24] underneath W, presumeably since it might diffuse. Our best devices were obtained using SiO_2/Cr/Pt (40/10/50 nm) stacks. A significant difference was observed between lift-offs with varying Pt thicknesses and evaporation rates. Empirically it was found that evaporating a relatively thin layer (40-50 nm) of Pt at a high and stable rate (2.0 kÅ/s) gave the best results (fig. 2.5), while Cr should be kept at

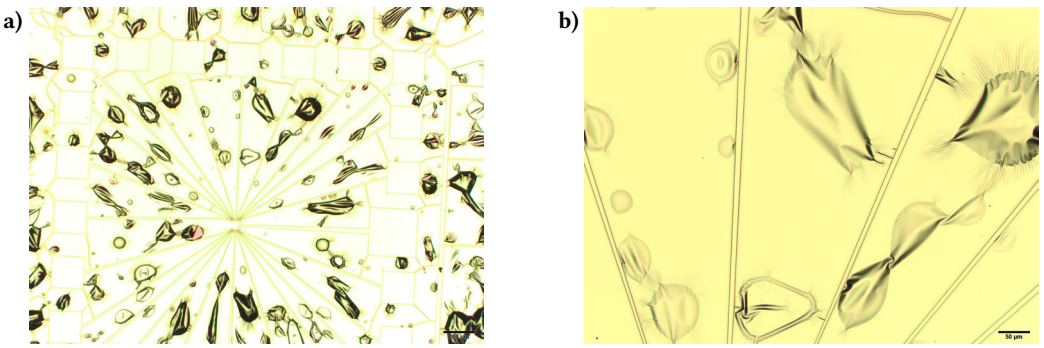

Figure 2.4. a) Optical microscope image of SiO_2/W/Pt 40/2/40 nm before lift-off. The blisters indicates the build-up of a gas underneath the Pt layer. The very thin W might not influence the metal stack. The gaps were not preserved after lift-off. **b)** A 4 x zoom of the same chip.

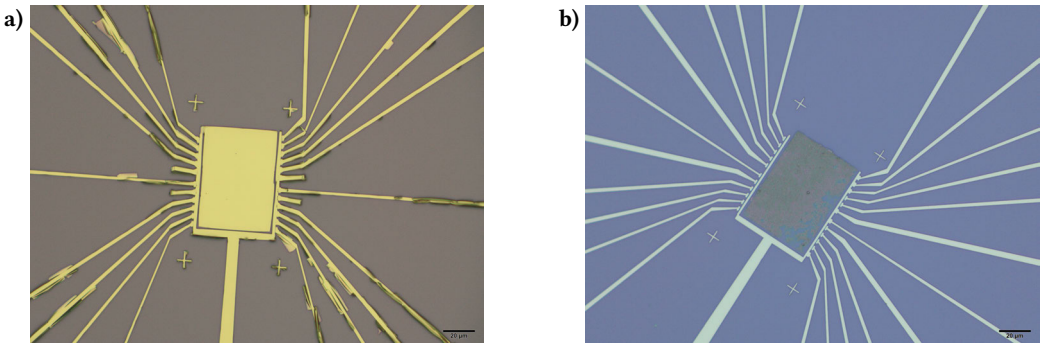

Figure 2.5. Optical microscope images of **a)** Cr/Pt 10/90 nm with an accidentally written catalyst island after lift-off and **b)** Cr/Pt 10/50 nm with a fine deposition of catalyst. 50 nm was the maximum Pt thickness while still preserving the gaps.

a lower rate (0.5 kÅ/s). The high Pt rate seems rather counterintuitive, but it works. Rotating the sample will minimize the shadowing effect in the undercut, which is not wanted.

2.3.3 Concluding Remarks on the Metal Contact Fabrication Process

Even though the metal stack combinations and lift-off problems turned out to be a non-trivial and time consuming task, which at some points was a trial-and-error process, we were able to fabricate a few succesful, but not consistently reproducible devices. The qualitative information given above and the data summarized in appendix A are however useful in a future development process. The optical microscope and SEM pictures resemble some of the pictures taken by H. Churchill[10], which have found an alternative use in the form of artistic wall decorations at the Center for Quantum Devices.

2.4 Carbon Nanotube Growth by Chemical Vapor Deposition

There are several methods to fabricate CNTs including arc discharge, laser ablation and CVD. The advantage of using CVD in the context of fabricating clean, suspended SWCNT devices is that SWCNT can be grown individually and the growth relatively precisely located to make the CNTs place themselves on top of the contacts. The CNTs are grown directly in the device without the use of a surfactant or substrate, as would generally be the case with the two other mentioned methods. CVD also holds the potential for an up-scaled production usage, however, the growth direction is random in our setup and the produced type of CNT varies with the temperature. Only scanning tunneling microscopy[27] or Raman spectroscopy[28] can be used to determine

the specific roll-up vector; that is the geometrical structure and helicity of the CNT. The criteria for a successful CNT growth by CVD includes obtaining CNTs that are: **1)** single-walled, **2)** individual, **3)** small diameter ($\sim$1 nm), **4)** sufficiently long (>3 μm), **5)** in the right direction, **6)** electrically contacted to source and drain contacts, **7)** not electrically shorted between multiple contacts.

2.4.1 CVD Procedure

The simpel CVD procedure is performed using a Carbolite furnace with three gas sources: argon (Ar), hydrogen (H_2) and methane (CH_4). Initially the furnace is pre-heated to 900 ℃ in an Ar atmosphere (0.8 L/min) without any samples to clean the furnace chamber. After cooling to a stable temperature below 200 ℃, using an air flow on the outside of the chamber, the samples are inserted into the furnace. After re-heating to 900 ℃, a flow of both H_2 (0.1 L/min) and CH_4 (0.65 L/min) are supplied initiating the growth. The Ar atmosphere prevents oxidation of the catalyst during growth and might dilute H_2 and CH_4 resulting in a slower growth and better quality SWCNTs[29]. After 15 min the H_2- and CH_4-flows are stopped and cooling is started maintaining the Ar atmosphere. At approximately 150 ℃ the samples are carefully removed: From now on the samples are protected from electrical and mechanical chock and stored on gel-pads or in chipcarriers on insulating foam.

This procedure was changed from having a 15 min segment after heating to 900 ℃ with only Ar and H_2 prior to adding a CH_4-flow. The reducing hydrogen might be effective enough (at 900 ℃) to etch the SiO_2 layer on the chip increasing the likelihood of a backgate leak, as suggested by Babíc *et al.*[30]. In the same reference it is shown that relatively low temperatures (750-850 ℃) gives MWCNTs or ropes of SWCNTs while higher temperatures (850-975 ℃) gives individual SWCNTs or bundles SWCNTs. At temperatures above 1000 ℃ amorphous carbon is produced.

The growth meschanism remains to be fully understood, but involves the precipitation of carbon at the transistion metal nanoparticle catalyst resulting in CNT growth either from the base (stationary catalyst) or the tip[31]. The randomized character of CVD growth has contributed to the low yield of functional devices on a single chip (section 4.1), however, we have shown that it is possible to re-grow nanotubes on unsuccesful chips using the same catalyst and without any preparation than ashing (20 s) to remove the first nanotubes.

2.5 Superconducting Contacts

During this project the superconducting metals rhenium and molybdenum (critical temperatures T_c of 1.7 K and 0.9 K respectively)[32] became available as sputtering targets. According to Schneider *et al.*[1], who used a 40/40 nm rhenium-molybdenum (ReMo) bilayer as contacts, the two layers would form an alloy in the subsequent CVD process.

Such a ReMo film is reported to have a T_c of 5.5 K[1] (or even 13.4 K)[33], which is much higher than T_c of both pure elements. Rhenium should also be a suitable sticking layer. To electrically test the alloy, a simple design for a 4-terminal measurement was made, which allows us to measure the resistance of the sample excluding the resistances of the wires.

2.5.1 Sputtering Calibration

Sputtering of Re and Mo were performed using the AJA Evaporation System, in which a gaseous Ar plasma is ignited over the surface of the sputter targets. Two different energy sources are used to maintain the plasma when sputtering Re (DC voltage) and Mo (RF voltage) at pressures of 3 mTorr and 5 mTorr respectively, but the basic principles of operation are similar: Accelerated electrons ionize initially neutral Ar atoms, which are accelerated towards the target material blasting loose neutral target atoms, that hits the sample (line-of-sight sputtering), and more electrons that maintain the plasma[2]. In order to calibrate the sputter process, the height of the deposited layer was measured using a profilometer (KLA-Tencor, AlphaStep Development Series) and compared to the adjustable sputter time. The profilometer tip performs simple direct linescans of the sample surface and parameters like the force and speed of tip can be adjusted to obtain sharp characteristics. Several linescans can be merged to calculate an average height of the layers relative to the flat wafer (data not shown). In this way time intervals of 340 s and 150 s for sputtering 40 nm of respectively Re (0.12 nm/s) and Mo (0.27 nm/s) were deduced (the sputtering was not linear with time). There were no difficulties with lift-off (in PG-remover as well as acetone) after sputtering, as can be seen from the images (fig. 2.6).

2.5.2 Bonding Issues and the CVD Metamorphosis

After heating the ReMo-chip to 900 ℃ in the CVD oven the thickness measured with the profilometer increased from 80 nm to approximately 180 nm (data not shown). A significant change in the color of the metal could also be detected after CVD; from a white/metallic appearance to a reddish surface that looked like a grainy image of a caleidoscope in the optical microscope (fig. 2.6). This unpredicted swelling is not understood, but it might be caused by incorporation of carbon during the alloy formation.

Bonding was not possible neither before nor after CVD in all ranges of the bonding parameters: force, power, time and ball size. When using the ball bonder (Kulicke&Soffa) the chip is heated to 80 ℃ and a small ball is created at the tip of a thin gold thread by an electric spike; therefore when bonding to CNT devices it is important to do this manually to prevent giving the CNTs an electric chock that will burn them over. To avoid this possibility a wedge bonder (Kulicke&Soffa) was also used, which simply presses an

[2] At the same time electrons recombine with the Ar^+ ions to release photons resulting in a pink (RF) or purple (DC) glowing plasma.

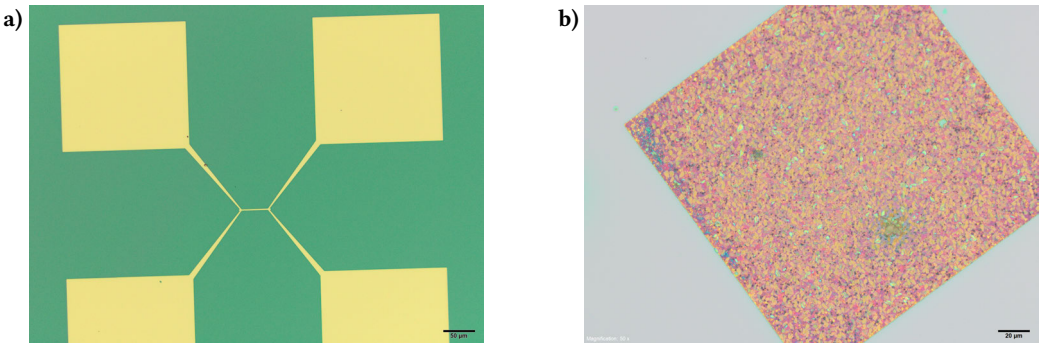

Figure 2.6. Optical microscope images of **a)** Re/Mo 40/40 nm bilayer after lift-off and **b)** the same ReMo chip after CVD. Note the chance in color and the surface pattern.

aluminium thread at the bonding pad without making a ball. To be able to bond to the ReMo-chip a second evaporation step of Cr/Pt 10/50 nm had to be performed. In relevance to section 2.3 it should be mentioned that this time a new Pt crucible was installed in the evaporation chamber making it difficult to obtain a stable rate (1.2-2.2 kÅ/s) resulting in a slightly cracked Pt surface. The wedge bonding had to be done at maximum power, which might have created a backgate leak and connections between multiple bonding pads on the chip. The superconductivity of the alloy has not yet been measured.

3 Mesoscopic Electron Transport Through a SWCNT

With a clean, suspended SWCNT device we wish to enter the world of mesoscopic electron transport, which is of fundamental difference from classical electron transport in bulk macroscopic materials. A mesoscopic system, where the electron can be thought of as a wave, can be experimentally realized by considering certain characteristic lenghts of the electron system. The sample size L must be smaller than the phase coherence lenght l_ϕ of the electron, the lenght over which the phase of electron decoheres due to inelastic scattering processes with phonons or other electrons. If $L < l_\phi$ the system is considered zero-dimensional. Furthermore, the sample size must be comparable to the mean free path of the elastic scattered electrons and to their (Fermi) wavelenght. At low temperatures the current is essentially carried by electrons with an energy close to the Fermi energy.

3.1 Quantum Dot Behavior in the Coulomb Blockade Regime

The Coulomb theory explaining the quantum dot behavior at low temperatures is well described in litterature[34]. In a small, strongly confined, conducting system virtually reduced to a zero-dimensional dot or "island for electrons" (QD), the quantized nature of the electron becomes apparent. The SWCNT constitutes a one-dimensional channel, but can be confined to a dot by the electrodes and the gate. The coupling between the SWCNT and the source and drain electrodes can be characterized by a resistance (R_s and R_d respectively) and a capacitance (C_s and C_d respectively) in parallel and a capacitive coupling to the gate (C_g) as schematized in fig. 3.1a. To observe single electron transport (SET) events, the electrons must be well localized on either the dot, the source or the drain allowing us to define the number of electrons on the dot N with charge Ne. In the quantum mechanical picture the resistive and capacitive barriers to the dot can be described as tunnelbarriers (fig. 3.1). For one electron to tunnel onto the dot the change in the electrostatic potential is related to the classical capacitor charging energy $E_c = {e^2}/{C_\Sigma}$ of the QD, where C_Σ represents the total capacitance of the dot to the environment assumed to be given by: $C_\Sigma = C_g + C_s + C_d$. In the constant interaction (CI) model this total macroscopic capacitance is assumed to be independent of the number of electrons N. In a well defined QD the charging energy is constituted by a single electron, resulting in charge quantization of the dot. This energy cost of transporting an electron to the dot is due to the electrostatic repulsion of the electrons

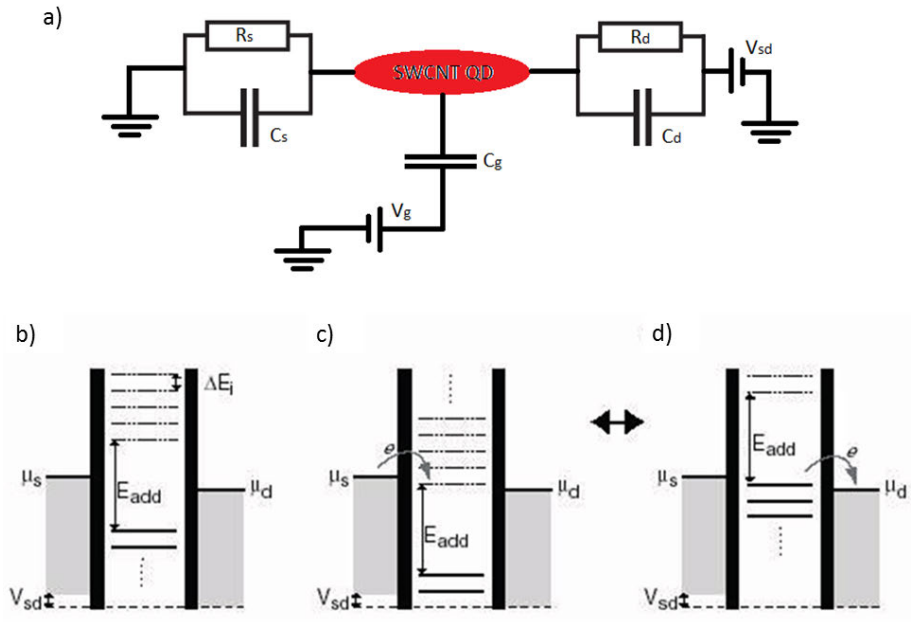

Figure 3.1. a) Schematic illustration of the coupling between the dot and the source, drain and gate as described by the constant interaction model. **b)** Potential energy landscape of a QD in CB defined by two tunneling barriers. **c)** The level of the dot is between the chemical potentials of the source and drain and an electron hops onto the QD. **d)** The electron is transported to the drain illustrating single electron transport. (Courtesy of T.S. Jespersen.)

on the dot. This can result in a Coulomb blockade (CB) of the current until the energy of the dot is raised (the gate effect) or the tunnelbarriers are lowered (the bias effect). The spatial confinement of the electrons on the dot results in size quantization giving the QD a discrete single-particle energy spectrum with the energy level spacing ΔE. In the CI model ΔE is assumed to be independent of the interactions and number of electrons in the dot. Thus a QD is expected behave as a so-called "articifial atom" with intrinsic energy levels and excited states. The SET pumping mechanism is briefly illustrated in fig. 3.1.

The criteria for observing CB experimentally can now be inferred: To prevent the electrons from overcoming the CB by thermal activation, the charging energy must exceed the thermal energy: $k_B T \ll {}^{e^2}/_{C_\Sigma}$. The quantized nature of the electron can only be distinguished if the discrete single-particle energy level spacing ΔE is not smeared out by the thermal energy, that is: $\Delta E \gg k_B T$. The capacitive description of the QD implies a classical charging time $\Delta t = R_t C_\Sigma$, which relates the energy uncertainty to

the tunnelbarrier resistance through (Heisenberg):

$$\Delta E \Delta t = \left(\frac{e^2}{C_\Sigma}\right) R_t C_\Sigma > h \Rightarrow R_t \gg \frac{h}{e^2} = 25.8k\Omega. \tag{3.1}$$

This is realized by having the dot weakly coupled to the source and drain through tunnel barriers. The schematic figure 3.1 illustrates the potential energy landscape of the source, drain and dot during a SET event. CB can also be overcome by applying a source-drain bias $eV_{sd} > E_c$. By varying the gate voltage the electrostatic potential on the dot is changed, hence the CB can be repelled allowing one electron at the time to tunnel through the dot, which gives rise to Coulomb oscillations in the I-V_g-characteristics. The addition energy E_{add} is the change in the electrochemical potential μ accompanying the addition of one electron:

$$E_{add} = \mu(N+1) - \mu(N) = \Delta E + \left(\frac{e^2}{C_\Sigma}\right). \tag{3.2}$$

The total ground state energy of the dot (at zero temperature) is given by the sum over the single electron energies plus the electrostatic energy $U(N)$, with the total charge $Q = -e(N - N_0)$, where N_0 is the number of bound electrons in the dot i.e. the number of electrons at $V_g = 0$. Considering fig. 3.1 the gate voltage can induce charge on the dot thereby placing the electrochemical potential of the dot μ_{dot} between μ_s of the source and μ_d of the drain. This can happen again when the gate voltage is changed by

$$\Delta V_g = \left(\frac{C_\Sigma}{eC_g}\right) E_{add} \Rightarrow \Delta V_g = \frac{E_{add}}{e\alpha}, \tag{3.3}$$

where we defined the coupling strenght factor $\alpha = {}^{C_g}/_{C_\Sigma}$. ΔE is zero when an electron is added to the same spin-degenerate level as the previous electron, and we obtain the classical situation: $\Delta V_g = {}^{e}/_{C_g}$.

3.1.1 Interpreting Coulomb Blockade Diamonds

Coulomb diamonds are the result of plotting the differential conductance ${}^{dI}/_{dV_{sd}}$ as a function of V_{sd} and V_g in a 2D heat map. From these bias spectroscopy plots, the characteristic energy scales, E_c and ΔE, can be deduced . A current is transported through the device when an energy level fulfills the criteria: $-|e|\,V_s > \mu(N) > -|e|\,V_d$. Considering the first limit and equ. 3.3 with $V_d = 0$ yields: $V_s = \Delta V_g \left({}^{C_g}/_{C_s}\right)$, which describes the slope incresing from left to right of the first transition line in a Coulomb diamond plot. Considering the other limit, the downwards slope can found from: $V_s = \Delta V_g \left({}^{-C_g}/_{C_g+C_d}\right)$. Further transition lines constitute excited state tunnelling, from which ΔE can be found. The height of the Coulomb diamond corresponds to E_{add} and the regular variation of E_{add} will resolve the spin-degeneracy (four-fold in SWCNTs) and shell-filling in the system[7].

3.2 SWCNT in a Superconducting Circuit

Some materials can enter a superconducting state below a certain critical temperature, current and magnetic field, in which they can exhibit macroscopic quantum phenomena such a zero-resistance and maintaining a persistent current. The first experiments coupling a rope of SWCNTs to superconducting leads were done by A. Kasumov *et al.*[35] and A. Morpurgo *et al.*[36], who both observed supercurrents at zero bias at low temperatures. A non-superconducting material in close proximity and with good contact to a macroscopic superconductor can show proximity-induced superconductivity owing to the Josephson effect, which is an established phenomena in the microscopic BCS theory of superconductivity[37]. The superconducting phase can be characterized by a complex order parameter related to the wavefunction of the superconducting electrons (loosely bound states of Cooper pairs). The superconducting wavefunction can be shown to leak into the non-superconducting material, with an exponential decaying spatial distribution, because of tunneling of Cooper pairs through the barrier. The electrons in the Cooper pair maintain their phase coherence over a certain lenght outside the superconductor thus maintaining their superconductivity. A SWCNT connected to superconducting electrodes (S-SWCNT-S) resembles a Josephson junction that enables a supercurrent to flow through the SWCNT[3]. A thin metal layer in addition to the superconducters could be used to ensure good contact to the CNT (e.g. Au[35] or Ti[39]).

Coulomb diamonds will be recognizable in a bias spectroscopy plot of a (proximity-induced) superconducting SWCNT, but there will also be two anomalous lines at a constant positive ($+\Delta$) and negative ($-\Delta$) bias voltage, which is the manifestation of the superconducting gap 2Δ around the Fermi energy. At small bias below the gab, where the density of states of the superconductor is zero, multiple Andreev reflection (MAR) is expected to mediate the current transport[37]: An electron is Andreev reflected as a time reversed hole and vice versa at the superconductor interface until its energy (depending on the applied bias) is high enough to enter the superconductor. This results in an increase in the current (resonances) every time a new MAR process is available giving rise to a sub-gab structure[39]. Even more interestingly, a biased superconductor could be contacted to the middle of a bended CNT confining two QDs in the same tube and enabling splitting of Cooper pairs (crossed Andreev reflection) into two normal contacts[40]. The Cooper pair electrons will remain entangled enabling the test of Bell inequalities[41]. A suspended SWCNT in a superconducting circuit could also act as a superconducting quantum interference device (SQUID) with the same SWCNT constituting two Josephon junctions in parallel, as shown by Schneider *et al.*[1]. The SQUID could be used to observe and manipulate the mechanical motion of the SWCNT or as a sensitive magnetometer.

[3] There have been few reports on intrinsic superconductivity in (small diameter) SWCNTs, which will not be considered here[38].

4 Electrical Measurements on Suspended SWCNTs

4.1 Electrical Measurements at Room-Temperature

To test before cooling whether a SWCNT might have contacted the source and drain electrodes and thus created a successful device, the samples were characterized at room temperature in vacuum ($< 10^{-4}$ mbar) in a probe station[4]. To get a fast characterization, the backgate voltage V_g was swept from -20 V to 20 V (red line) and back (blue line) at $V_{sd} = 5$ mV DC bias between source and drain electrodes on all electrical conducting potential devices: By measuring the current I the conductance $G = {}^{I}/_{V_{sd}}$ was plotted as a function of V_g in fig. 4.1. For some devices a shift in the gate characteristics was observed between measurements in vacuum and atmospheric pressure with a tendency to more pronounced features at lower pressure (data not shown), probably due to the evaporation of contamination on the devices. The gate dependency reflects the small band gap semiconducting properties of the SWCNT at room temperature[42]. All devices showed hysteresis. Interestingly, there was not necessarily a correlation between smooth recognizable features at room-temperature (fig. 4.1c) and clean SET behavior at low temperatures. The opposite was the case with the device showed in fig. 4.1b.

There are 23 source contacts per chip; each one a potential SWCNT device after the random directed CVD growth. Out of 437 probed potential SWCNT devices on slightly different electrode stacks of (SiO_2/)Cr/Pt on 19 chips, 41 devices on 10 chips showed gate-dependent conductance characteristics and no backgate leak before bonding; out of these, 17 devices on 4 chips were lost after bonding due to backgate leaks or from electrostatic discharge events.

[4] LakeShore Cryogenic Pump Station

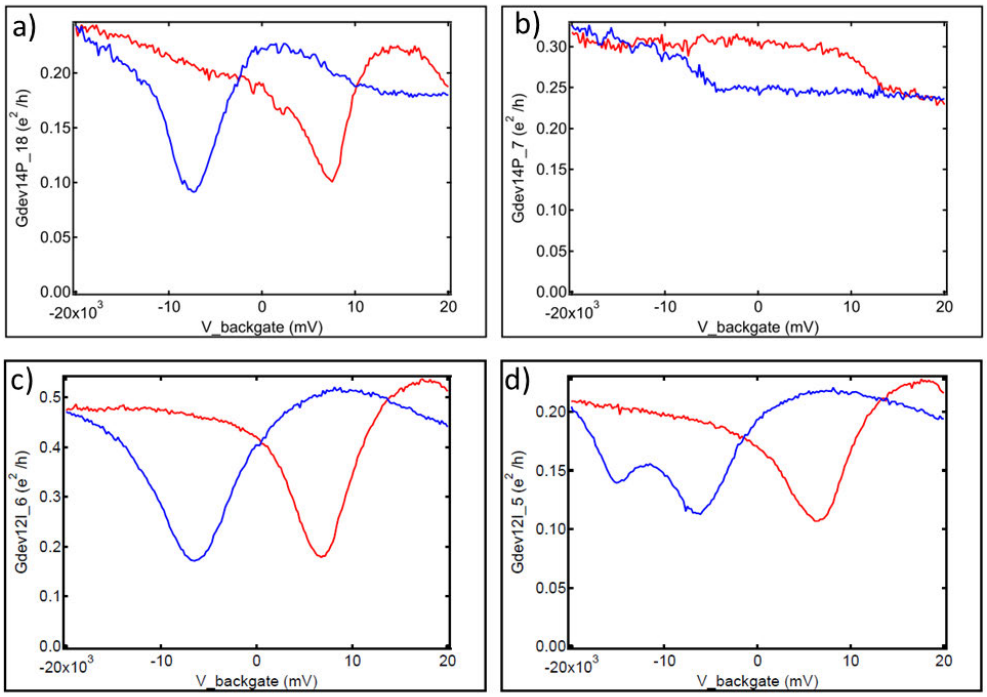

Figure 4.1. Room-temperature measurements of linear conductance, G, as a function of gate voltage V_g swept from -20 V to 20 V at bias $V_{sd} = 5$ mV. All mesurements exhibit hysteresis. **a)** Shows a semiconducting gap. **b)** Same device as low temperature measurement fig. 4.4 (and fig. B.1). **c)** Same device as low temperature measurement fig. 4.3. **d)** Shows an additional dip in the gate dependency, which was seen in several cases. It might be an attribute of multiple SWCNTs.

4.2 Experimental Setup and Cryogenics

Low temperatures are needed to avoid thermal smearing at the very small characteristic energies of CB: typically $\Delta E \sim 1$ meV, which requires $k_B T$ to be well below, e.g. at 1 K $k_B T = 0.086$ meV. An Oxford Instruments ^{3}H HelioxAC-V refrigerator is used to cool the samples to a base temperature of 300 mK in vacuum. In a closed cycle, a ^{3}H gas is initially released from the sorb (^{3}H adsorption pump) by heating it. The ^{3}H gas is then cooled by the pulse tube cryocooler 2^{nd} stage followed by the expansion of the gas into a dump causing further cooling of the gas, which condenses into the dump. Now the sorb is cooled via a heat switch and pumps vapour from the liquid ^{3}H in the dump (evaporative cooling) so the base temperature is reached[43].

The schematic setup shown in fig. 4.2 enables two-terminal DC measurements with a bias V_{sd} over the source (s) and drain (d) electrodes. The electrostatic potential of the

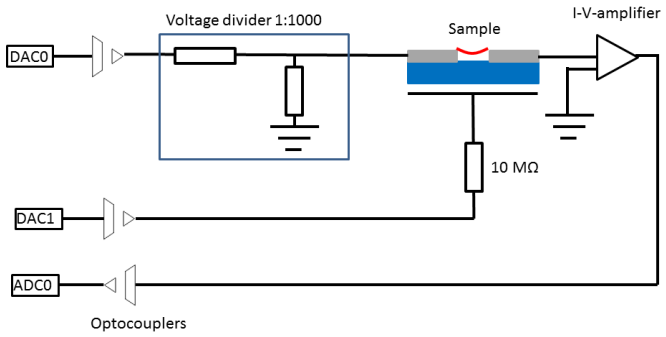

Figure 4.2. Schematic illustration of the experimental setup.

SWCNT can be varied by applying a gate voltage V_g to the doped substrate (the back-gate). The measurements are controlled with a LabView program. The bias voltage is reduced by a voltage divider ($1 : 1000$) and a current-to-voltage amplifier detects the current passing through the sample. The $10\,\mathrm{M\Omega}$ resistor, which is much larger than the sample resistance, protects the device by ensuring a constant small current. The optocouplers isolate the circuit from ground. To reduce noise, the setup was modified using a lock-in amplifier (not shown), which measures the amplitude and phase of the experimental signal and reduces the noise in the measurement by generating its own reference signal, which is multiplied by the input signal. This signal is passed through a low-pass filter, which removes the AC signal resulting in a DC voltage output proportional to the experimental signal amplitude. The lock-in was operated at a reference frequency of $123\,\mathrm{Hz}$ and applying a small bias of $75\,\mu\mathrm{V}$ to the sample.

4.3 Electrical Measurements at Low Temperatures

Some of the measurements at $0.3\,\mathrm{K}$ are presented here (generated using Spyview) and a few are shown in appendix B. A general feature observed is the large overall modulations of the Coulomb blockaded regions around zero bias in the gatesweeps resulting in very irregular Coulomb diamond plots (fig. 4.3). These gatesweeps from -10 V to 10 V as a function of the bias between -5 mV and 5 mV were initially made to characterize the devices and look for regularities. Hoping to resolve the expected degeneracy and shell structure or clearly identify SET transition lines, higher resolution measurements in smaller gate and bias segments in regions where the peak pattern seemed fairly regular were performed (fig. 4.4). Assuming these oscillations represents true CB features as expected, we can deduce the relevant energy scales as described in section 3.1, but with a significant uncertainty due to the quality of the devices and measurements. The slopes

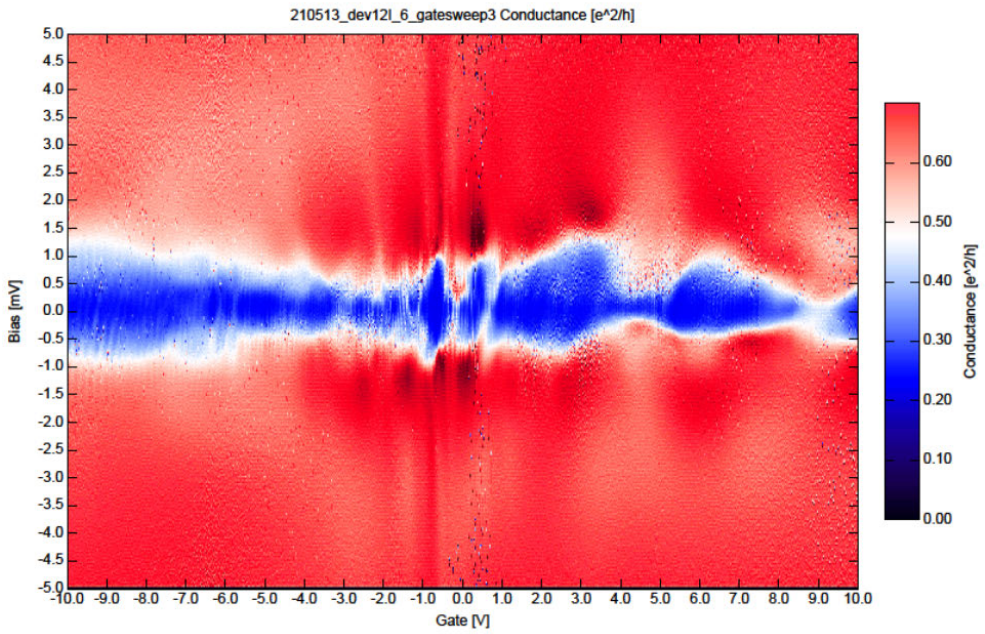

Figure 4.3. Differential conductance $^{dI}/_{dV_{sd}}$ in units of $^{e^2}/_{h}$ vs. bias and gate voltage at $T = 0.3\,\mathrm{K}$. It is the same device as in fig. 4.1c.

seem similar for positive and negative bias. The irregularities make it to uncertain to conclude anything about ΔE, but $E_{add} \approx E_c$ can be estimated from the height of the diamond to approximately $1.2meV$, which is very low compared to litterature[42][7]. Using equ. 3.2 the total capitance is estimated to $C_\Sigma = 1.3 \cdot 10^{-16} F$. From the width of the diamond ($\Delta V_g = 0.017V$) the coupling factor is found: $\alpha = 7.2 \cdot 10^{-2}$ and $C_g = 9.6 \cdot 10^{-18} F$. The positive slope yields $C_s = 5.3 \cdot 10^{-19} F$ and the negative slope $C_d = 1.7 \cdot 10^{-17} F$. As can be seen from fig. 4.4 and the fact that C_d is 33 times larger than C_s, there is a huge difference between the coupling of the SWCNT to the source and drain contacts respectively. The capacitance is inversely proportional to the distance, which suggests that the effective QD is defined closer to the drain.

Unfortunately, but clearly no excited state transitions can be resolved to extract further bias spectroscopy data. The overall modulation of the small Coulomb diamonds suggest that multiple QDs are interacting and the irregularities indicate defects in the SWCNTs. Several switching faults or charging effects are also visible in the data. Possible defects in SWCNTs include vacancies, doping and inhomogenities such as shifts in helicity along the tube direction, which could create barriers resulting in mulitple dots

in series. It will be significant from the SEM pictures in the next section (5.1) that the metal contacts are very unregular, which likely results in the ill-defined QD behavior.

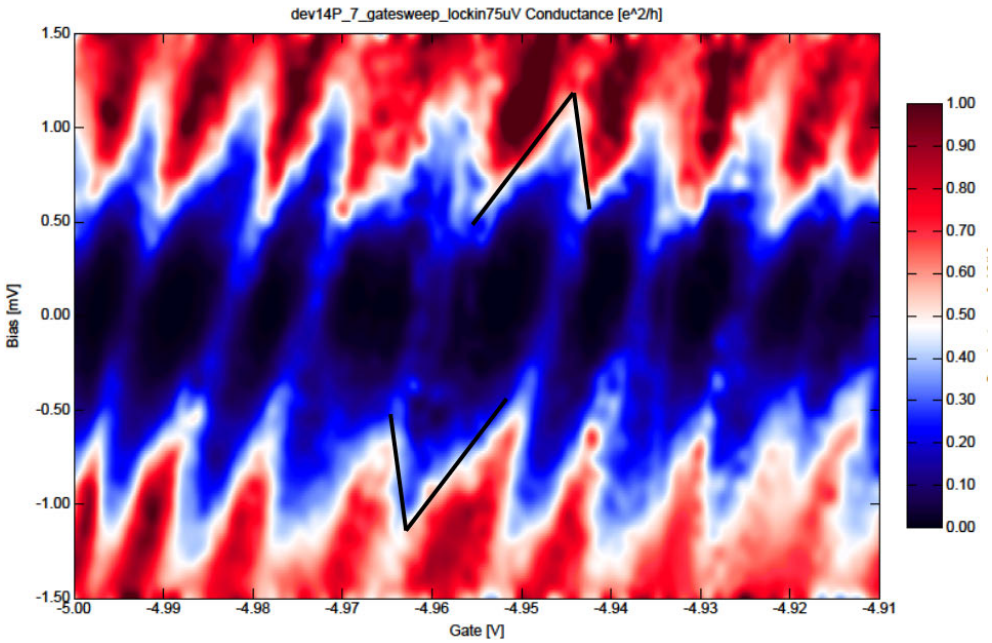

Figure 4.4. Differential conductance $^{dI}/_{dV_{sd}}$ in units of $^{e^2}/_{h}$ vs. bias and gate voltage at $T = 0.3\,\mathrm{K}$. The noise was reduced using a standard lock-in technique. It is the same device as in fig. 4.1b.

5 Visualization of the Devices

5.1 Scanning Electron Microscopy

A scanning electron microscope (SEM) is a powerful tool to visualize the particular structure of the device we have been measuring on, however, SEM can only be performed after the measurements are completed. A CNT under electron irradiation will degrade and probably defects will be introduced[44]. SEM pictures can not be used to characterize the intrinsic quality (defects) of CNTs and can only describe the morphology of the device. During direct exposure it can also easily be seen how the CNTs grow several hundred nm in size radially outwards from the tube in less than one minute even at low acceleration voltages (2-3 kV), see fig. 5.1. Probably hydrocarbon molecules attracted to the SWCNTs from the surroundings dissociate into immobilized amorphous or graphitic carbon under the electron beam, where it is deposited. F. Banhart[5] found that the amount of contamination deposit during SEM exposure increased with storing time of the CNTs in air[45]. Our devices were not stored in nitrogen or vacuum chambers, but SEM was supposed to be the last characterization step.

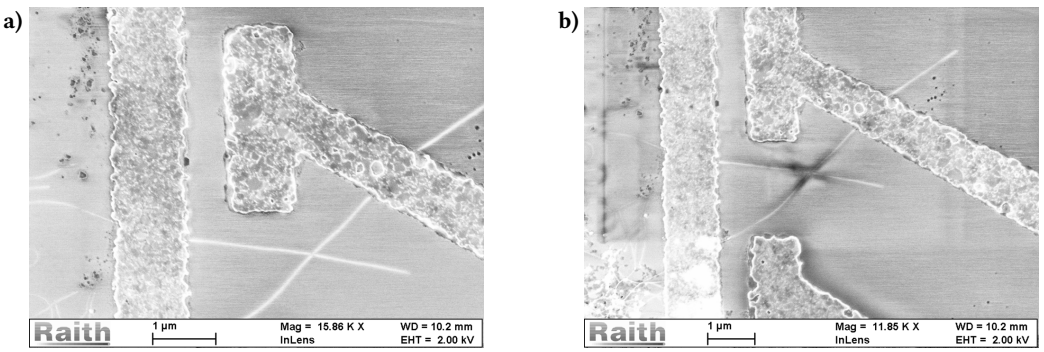

Figure 5.1. a) SEM image of a SiO_2/Cr/Pt (40/10/50 nm) chip showing two crossed SWCNT connected to source and drain, but not suspended. **b)** SEM image of the same device after e-beam irradiation at 2 kV for approximately 1 min.

The SEM pictures were taken using the same instrumentation as in the EBL process (section 2.2). In SEM a focused electron beam is scanned across the surface and the emitted secondary electrons are detected. The intensity of the scattered electrons varies as the beam scans across an edge or rough surface, resulting in a topological representation of the sample.

[5]Interestingly, F. Banhart used this deposition mechanism to join CNT junctions.

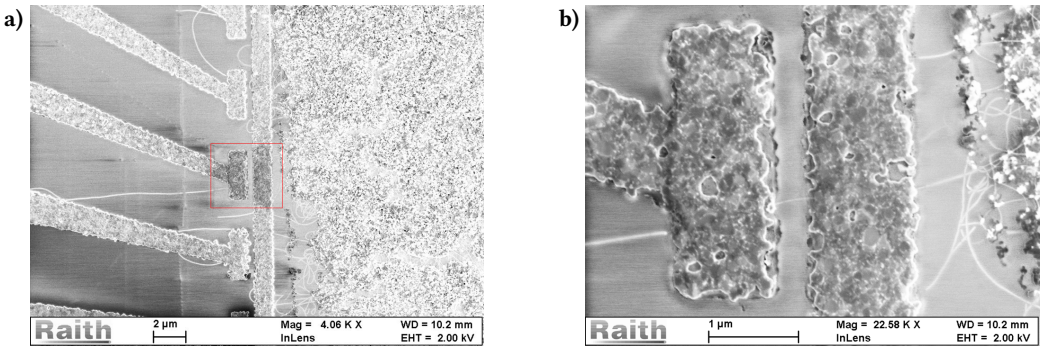

Figure 5.2. SEM images of the same chip as in fig. 5.1 (but a different device) showing a SWCNT placed across the trench. **a)** Unfortunately the long SWCNT is connected to several contacts. Note the darkened square (red), where image **b)** is focused. The contacts are very uneven and with frayed edges.

In general all metal contacts were rough, grainy and uneven; it appears as if the Pt forms droplets during CVD or is slightly melted. This does not create good contacts for the SWCNTs and it was not possible to recognize the segments of CNTs lying on top of the contacts – only in contrast to the flat wafer. Fig. 5.1 shows two connected, but not suspended SWCNTs, which can be compared to the electrical characterization of the same device in fig. B.2. The SWCNT junction results in multiple QD behavior and many different charging effects. However, there were SWCNTs, which had successfully contacted the source and drain over the trench (fig. 5.2). Note how the SiO_2 terraces underneath the contracted metal is slightly visible. Fig. 5.2 also shows that there is a fine production of nanotubes.

Atomic force microscopy has briefly been used to visualize the suspended SWCNTs, but it was more an instructive exercise, since the trenches could not be properly visualized. Apparently the contacts or catalyst material inferred too much with the tip. Outside of the contacts and trenches, the SWCNTs could be imaged on the flat wafer, yielding an approximate height of 3 nm (data not shown).

6 Conclusion

The experimental task of this project turned out not to be a simple one due to a large number of variable parameters in the device fabrication including the randomized nature and high temperature of nanotube growth by CVD. In conslusion, the methods needed to fabricate as-grown SWCNT has been described and implemented in a device recipe. A few devices have been cooled and a single gatesweep has been used to extract the characteristic energies of a Coulomb blockade situation. In general the electrical measurements indicate that the fabrication process still needs to be optimized. However, the measurements were limited in time and some devices remain to be thoroughly investigated at low temperatures.

6.1 Perspectives on the Development of As-Grown Suspended SWCNT Devices

The rate of successful devices was rather unsatisfactory and this should be a major concern for further development. Below optimization possibilties are outlined: A change in the design could be to apply the catalyst directly on top of the drain contact as done by e.g. Deshpande *et al.*[6]. This would decrease the amount of obstacles on the nanotube's way from catalyst island to source contact. However, one should have the proximity effect mentioned in section 2.2 in mind during EBL, since such a large drain contact could easily result in the overexposure of the trenches. In one case, both the contacts and the catalyst islands were accidentially written during the same EBL exposure (fig. 2.5). This would not necessarily have been a problem if it were not for the massive overexposure of the gaps.

Once the fabrication difficulties are overcome with our suspended SWCNT device, the randomized nanotube growth and directionality during CVD is a concern for the exact reproducibility and integration of the device. However, the CVD procedure holds the potential for a scaled-up production. When a clear single QD behavior can be observed in a suspended SWCNT device, it would of course be interesting to incorporate multiple bottom gates in the device and investigate double or triple dot behavior in a controlled manner. By applying a magnetic field, many interesting quantum transport phenomena could be investigated such as spin-orbit coupling[5][46] and Aharonov-Bohm oscillations[47] in the nanotube. The exciting physics emerging when connecting superconductors to a SWCNT was very briefly introduced in section 3.2, but is of course an obvious goal to pursue starting with the implemetation and clarifying experiments on the ReMo alloy. Perhaps Re is a better suited sticking layer for Pt as well or simply only using Mo as contacts[25] will yield better results.

Acknowledgements

I would like to thank my two supervisors Kasper Grove-Rasmussen and Jesper Nygård. I am also thankful for the help of Morten L. Olsen both during fabrication and device characterization, and the help of Shivendra Upadhyay and Merlin von Soosten. Finally I would like to thank members of the ”Qdev” group, who has showed interest in my project and engaged in discussions or helped me through all the daily difficulties an experimentalist faces.

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Appendix

A List and Images of Metal Stack Combinations for Electrodes

Metals:	Thickness:	Rates:	Comments:
W/Pt	10/90	0.2/1.0	Cracked, curled edges
W/Pt	5/90	0.2/1.0	Cracked, curled edges
Cr/W/Pt	5/5/50	0.7/0.2/1.0	Difficult, uneven lift-off
Cr/W/Pt	2/5/50	1.0/0.2/1.0	Difficult lift-off
SiO2/W/Pt	40/5/50	0.2/1.0	No pre-ashing = total lift-off
Cr/Pt (rot.)	10/50	1.0/2.5	OK, but very small gaps
Cr/Pt	10/90	0.6/1.5	Cracked, curled edges
Cr/Pt (rot.)	10/60	0.5/1.0	OK, but very small gaps
Cr/Pt (rot.)	10/60	0.5/1.0	Curled edges, very small gaps
SiO2/Cr/Pt	40/10/50	0.7/1.5	Difficult lift-off
Cr/Pt	10/50	0.9/1.2	OK lift-off
Cr/Pt	10/50	0.6/0.9	Frayed edges
SiO2/Cr/Pt	40/10/30	1.5/1.7	Good lift-off
SiO2/Cr/Pt	40/10/30	1.5/2.0	Good lift-off, missing contacts
SiO2/Cr/Pt	40/10/50	1.6/3.5	Cracked
SiO2/Cr/Pt	40/8/40	1.5/2.0	Good lift-off
SiO2/W/Pt	40/5/50	0.75/2.0	Cracked, blisters
SiO2/Cr/Ti/Pt	40/5/5/50	2.0/1.0/2.0	OK lift-off
SiO2/Cr/Pt	40/10/50	1.0/1.0/2.0	Good lift-off

Figure A.1. Some of the metal stack combinations (including SiO_2), their thicknesses in nm and evaporation rates in kÅ/s, that were used during the project, presented in chronological order to illustrate the progress. The comments are visual descriptions before CVD. "Rot." indicates that the sample was rotated during evaporation, which did not improve the result: The slightest tilt of the sample holder would result in metal deposition underneath the undercut (section 2.3).

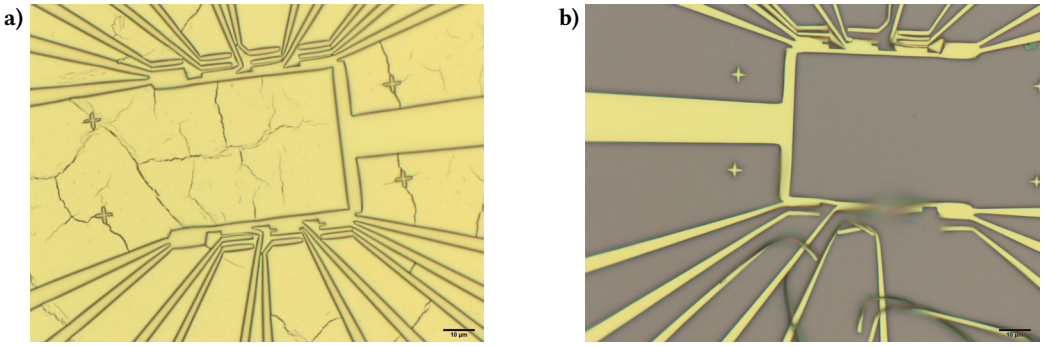

Figure A.2. Optical microscope images of a modified design with three trenches: 0.5 , 0.75 and 1.0 μm. **a)** Cr/Pt (10/50 nm) chip after metalization: The surface has cracked, but the largest trenches seems intact. **b)** The same chip after a difficult lift-off.

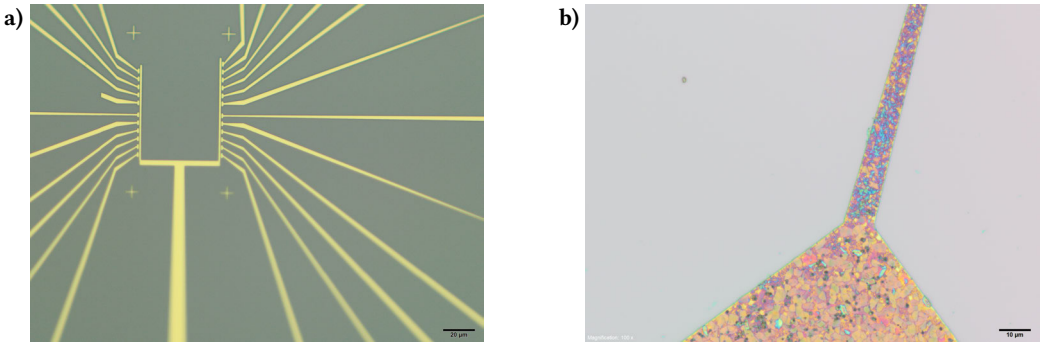

Figure A.3. Optical microscope images of **a)** a rather successful SiO_2/Cr/Pt (40/8/40 nm) chip after metalization. However, it illustrates a general issue; that the contacts are overexposed resulting in very small gabs. A re-calibration of the eLiNE dose-test might be one of the solutions. This chip also features a stitching fault. **b)** The same ReMo device as in fig. 2.6 after CVD, just to illustrate the unexplained pattern of colors.

B Electrical Measurements at Low Temperatures

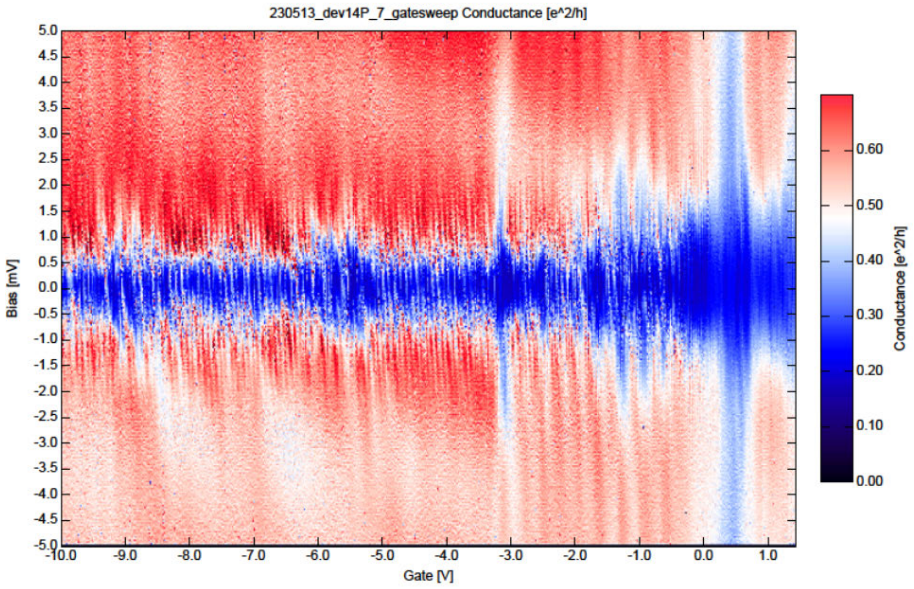

Figure B.1. A larger bias- and gatesweep of the same device in fig. 4.4, which were used to calculate the approximate energy scales. Unfortunately the device starts to heat up from around 0 V_g. The region from -5 to -4.9 V where fig. 4.4 was measured can be recognized as a regular region. This figure and fig. B.2 are representative of many of the measurements.

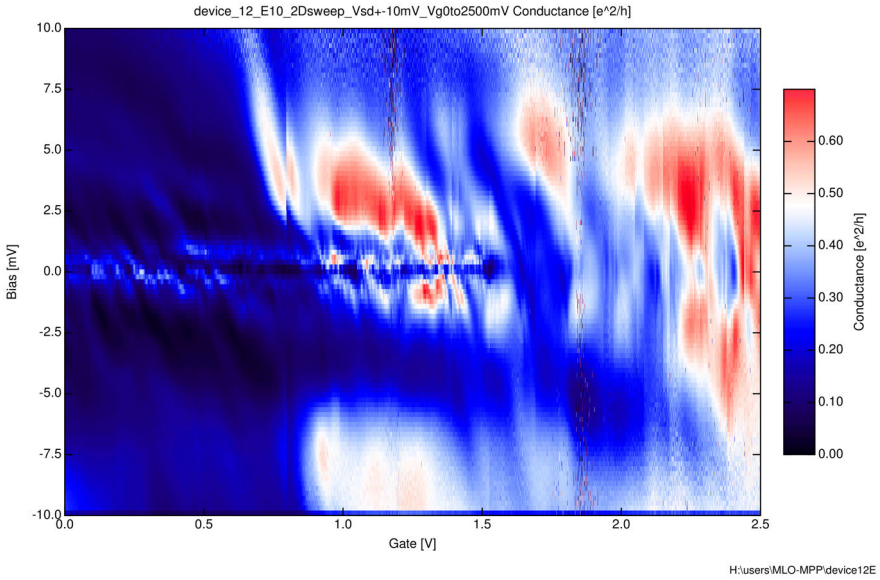

Figure B.2. The same device as in the SEM images in fig. 5.1.