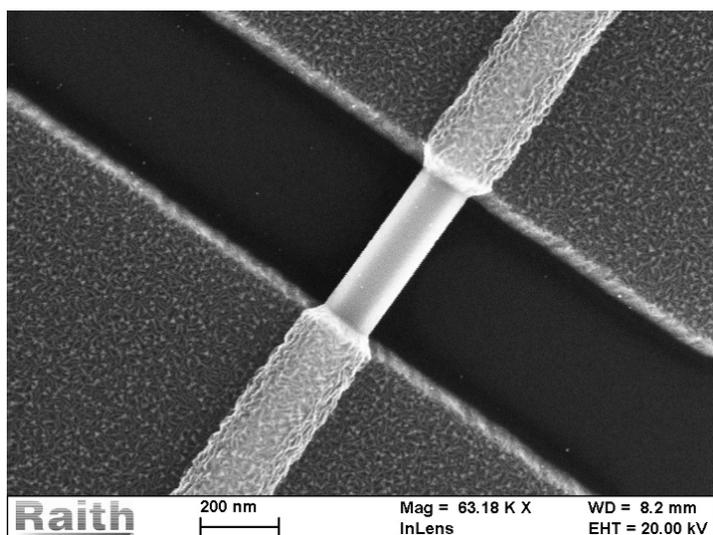




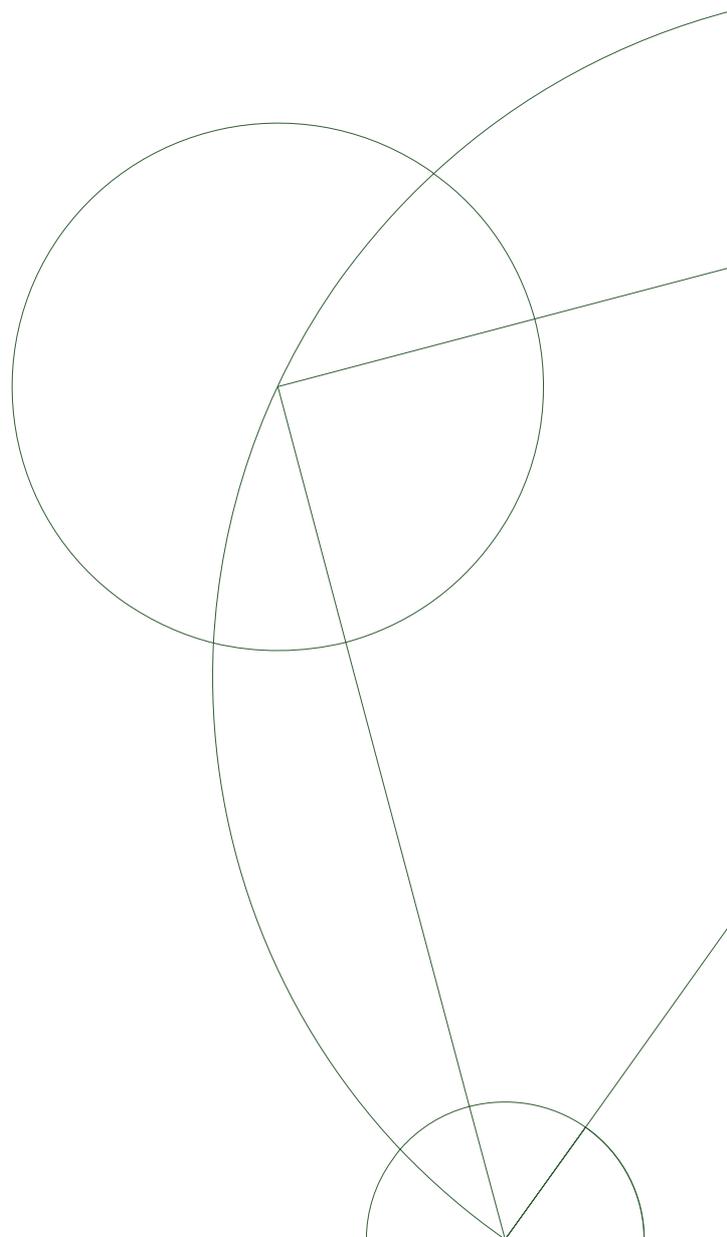
# High $B_C$ Josephson Field Effect Transistors

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# 1 Abstract

In this project we are aiming to maximise the superconducting critical magnetic field in a superconductor-semiconductor-superconductor junction. Topologically protected Majorana states, which can be used as qubits for topological computation, require topological superconductivity. We are interested in maximising the critical magnetic field in Josephson Field Effect Transistors (JoFET), to maximise the parameter space where topological superconductivity can exist. Using techniques such as e-beam lithography and metal evaporation, devices were fabricated, and designed with two superconducting leads, connected by a semiconductor. InAs nanowires were throughout all experiments used as semiconductor, whilst superconductors with high critical magnetic fields were chosen as leads, including vanadium and niobium, in most cases with a sticking layer of titanium in between superconductors and nanowire. Making a working JoFET with these superconducting leads, should prove to be somewhat challenging, and a JoFET with vanadium and niobium, was never fabricated in this project. However, through low temperature measurements, the superconducting band gap of vanadium was found, and its critical magnetic field was tested with a vector magnet. Determined to make a working JoFET, a device with aluminium contacts was then successfully fabricated, allowing experiments of backgate dependence, magnetic field dependence, and temperature dependence. These measurements resulted in indication of coulomb blockade, Kondo effect, Zeeman splitting and Shiba states.

## 2 Introduction

This thesis summarises the work done for our bachelors project. The aim of this work is fabrication of and measurements on Josephson Field Effect Transistors. The initial purpose was to maximise the superconducting critical magnetic field,  $B_c$ , in a JoFET. We aimed to achieve this goal by making JoFETs out of high  $B_c$  superconductors such as niobium and vanadium. After failing to fabricate a functioning JoFET on several attempts with high  $B_c$  materials, we eventually decided to check for faults in our recipe, by fabricating a device with aluminium contacts, as such a device had been shown to be functioning in the past [1]. This proved to be functioning.

The primary motivational factor for undertaking this project, is the development of a topological quantum computer. In topological quantum computers, the qubit states are separated spatially, protecting them from decoherence, thus minimising the error rate of computations. Majorana bound states have been proposed as possible building blocks for topological quantum computation [2], however Majorana states still only exists as a theoretical concept. Even so the field is not standing still, and within recent years many groups [3] [4], have made claims of Majorana detection. The existence of Majorana fermions is nevertheless yet to be convincingly confirmed by experiment. Numerous proposals have been put forward for Majorana detection [5] [6] [7] [8]. Some of the Majorana proposals involve topological superconductivity, and one of the methods to realise topological superconductivity, requires lifting the spin degeneracy in a superconducting proximitised nanowire without killing superconductivity. Lifting the spin degeneracy is related to the Zeeman energy,  $E_Z = \mu_B g B$ . We are interested in maximising the parameter space, where topological superconductivity can exist, and so since  $\mu_B$  is a universal constant, we are interested in maximising the g-factor for the nanowire and critical magnetic field for the proximity effect-induced superconductivity in the nanowire. For this purpose, the JoFET is one of the simplest experimental layouts available.

This thesis aims to start out by briefly providing the background theory needed to explain the physics behind the fabricated devices, as well as most of the observed physical phenomena. Then continue with a thorough description of the fabrication and experimental processes. Eventually we will display and discuss data measured on three different devices, including the functioning aluminium JoFET. Three further chips with devices were produced, two with niobium contacts, and one with vanadium contacts. None of these chips however proved functional. We present explanations of observed physical phenomena, and present suggestions for improving the probability of fabricating functioning JoFETs, using the metals that we were unsuccessful in using.

## 3 Theory

### 3.1 Metals and Band Gaps

Metals are characterized by high electrical conductivity due to the fact that a large number of valence electrons can move about freely when the metal is in solid phase. These electrons are said to be in an electron gas. Two ways to describe this electron gas are the free electron Fermi gas and the nearly free electron gas. In the free electron Fermi gas, valence electrons are considered to move freely throughout

the entire metal, whereas in the nearly free electron gas model, the ion cores are considered to have some impact on the electrons. The latter is important when explaining theory behind energy bands[9].

In quantum mechanics electrons are described as waves[10]. The time independent waves are represented by two standing waves in a periodic crystal where one has its distribution function centred on the positions of the ions and one has its distribution function centred exactly in between the ions. Since the positive ions attract the negative electrons, this causes a significant change in potential energy which is the origin of the energy gaps[9]. See figure 1.

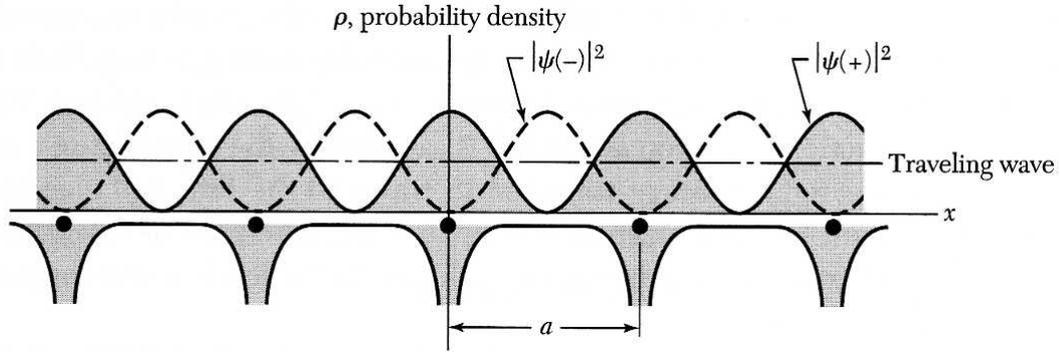


Figure 1: Distribution of probability density  $\rho$  of functions of two possible standing waves and one travelling wave in a periodic crystal lattice with lattice constant  $a$ . This illustration shows the origin of the band gaps from the theory of Nearly Free Electron Fermi Gas. Figure taken from [9]

If the valence band is filled and the Fermi energy lies between that and the conduction band, which is completely empty of electron states, it will require a large amount of energy to excite an electron into the conduction band, and the crystal will therefore be an insulator. If, however, the Fermi energy lies in the conduction band, there will already be electrons in the band, and therefore it will require an arbitrarily small amount of energy to excite the next electron, resulting in a conducting crystal.

### 3.2 Semiconductors and InAs Nanowires

In a semiconductor the band gap is like in an insulator, but the size of the gap is a lot smaller. Semiconductors are found in the groups **III - VI** in the periodic table. Semiconductors can be doped in numerous ways, changing their electrical properties enormously[11]. Semiconducting compounds can be made, consisting of elements from group **II - VI**. If semiconductors are combined into compounds, they can be designed to have an excess of either electrons (*n*-doped) or holes (*p*-doped). If a small concentration of dopant atoms are present in a compound, the effect of the doping will depend on its outermost number of electrons in comparison to the semiconducting compound. If the dopant have more electrons in the outermost shell than the main component of the semiconductor, it will act as a *donor*. If opposite, a dopant will act as an *acceptor*.

A nanowire is a wire-like structure, with a diameter constrained to tens of nanometres, and a length of typically  $10^{-6}$  to  $10^{-5}$  metres[12]. The short diameter confines the quantum states of the electrons in the transverse direction, and spreads out the allowed energy levels. In this report we are using InAs nanowires, which fulfil a number of criteria, that are relevant when looking to optimise the parameter space for searching for topological superconductivity. The charge carriers have a low effective mass, resulting in a larger energy spacing following the relation

$$\epsilon = (\hbar^2/2m)k^2 \quad (1)$$

This means that the states are better protected from disorder. The spin orbit length of the nanowire is  $\sim 100$ - $200$  nm [13] and the spin orbit coupling in the wires is strong. This couples momentum to spin and removes one degree of freedom, shifting the dispersion relation by  $\sigma k$ , where  $\sigma$  is the spin and  $k$  is the wave number, thus separating particles of opposite spin.

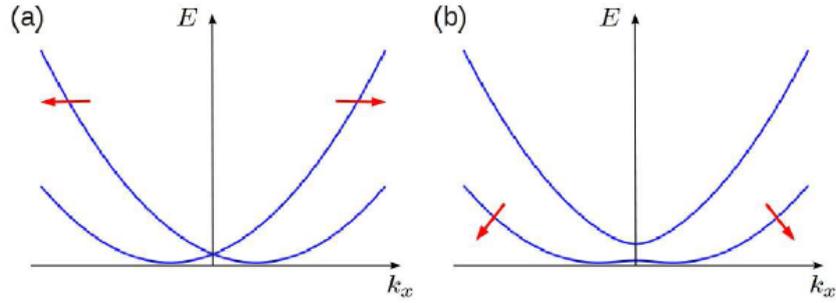


Figure 2: a) Dispersion relation for a spin orbit coupled nanowire at  $B=0$ . b) When  $B$  is switched on, the spin degeneracy is lifted. Figure taken from [7]

The  $g$ -factor of the wires is large. This enhances the lifting of spin degeneracy resulting from Zeeman splitting. The Zeeman energy is given by the relation

$$E_Z = \mu_B g B \sigma \quad (2)$$

Since the Bohr magneton  $\mu_B$  is a universal constant, this, as mentioned, leaves us with the task of maximising  $g$  and  $B$ . Finally InAs nanowires are easy to contact. The charge carriers are living on the surface of the wire making it easy to form ohmic contact.

### 3.2.1 Quantum Dot

In the data section we observe Coulomb blockade and the Kondo effect. Below are given brief explanations providing the necessary theoretical background for the observed phenomena.

When barriers between the nanowire and the leads are large, such that the following is true for the tunnelling resistance  $R_t$ :

$$R_t > h/e^2 \quad (3)$$

we enter the quantum dot regime, and the nanowire is weakly coupled to the leads. The low diameter of the wire confines the quantum states of the electrons in the lateral direction, and spreads out the energy level spacing. The confinement of charge by dot diameter and tunnel barriers effectively makes the dot zero-dimensional. The weak coupling makes the charge on the dot take on an integer multiple of the elementary charge,  $e$ .

When applying a source-drain voltage to the system, the potential of the source is shifted with respect to the drain, see figure 3.

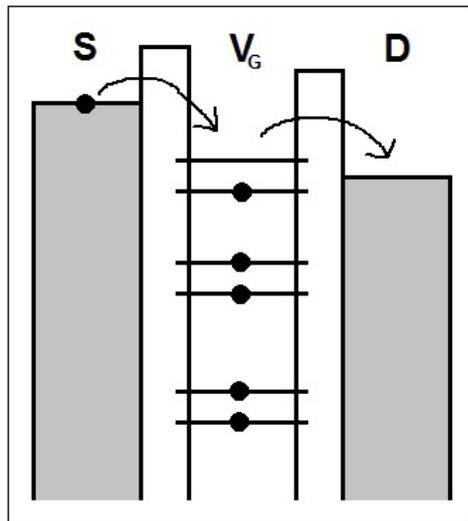


Figure 3: Electron transport through quantum dot

If there is a vacant state within the bias window, current will flow from the source to the drain. When there are no vacant states within the source drain bias window, electrons will have no way of tunnelling on to the dot.

Coulomb blockade is observed as a consequence of the split energy levels on the quantum dot, and the coulomb repulsion between the electrons, leading to two energies related to the quantum dot. The energy it costs to add another electron to the dot is called charging energy, and is given by  $E = e^2/C$ , where  $C$  is the capacitance of the dot. The cost for an electron to enter an unoccupied energy level is called the addition energy,  $\Delta E$ , which is the energy spacing between levels. Adding an electron to a spin-degenerate dot containing an even number of electrons will cost  $E = e^2/C + \Delta E$  whereas adding an electron to a dot containing an odd number of electrons will cost  $E = e^2/C$ .

If source-drain bias is swept over a back-gate voltage range, and the differential conductance is plotted, we can observe Coulomb Diamonds. In a Coulomb diamond plot, moving with increasingly positive back-gate, each successive diamond corresponds to adding one additional electron to the quantum dot.

### 3.2.2 Kondo Effect in quantum dots

If we strengthen the coupling between the leads and the quantum dot, the system will enter the Kondo regime [14]. The Kondo effect occurs in quantum dots as a zero bias conductance peak, where Coulomb Blockade otherwise would forbid conduction. If the total number of electrons is odd, a spin-degenerate state exists below the Fermi level, which is occupied by a single unpaired electron, so the total spin of the dot will be non-zero. An electron of opposite spin tunnels on to the dot, and the electron on the dot tunnels off, in a range of time  $\Delta t$ . This cotunneling process effectively costs no energy, but changes the spin of the dot. The process is allowed by Heisenberg's uncertainty principle

$$\Delta\epsilon\Delta t > h \quad (4)$$

as long as the time the process takes is shorter than  $h/\epsilon$ , where  $\epsilon$  is the energy difference between the leads and the dot.

As we need spin on the quantum dot and zero bias, odd diamonds will have a zero bias peak, whereas even diamonds will display no Kondo. If we apply a magnetic field, the Kondo peak will split into separate branches for spin up and down and no longer be at zero bias.

## 3.3 Superconductivity

Opposed to insulators, semiconductors and conductors, superconductors are metals which, when cooled below a critical temperature  $T_C$ , have electrical conduction without any resistance. Besides no resistivity, a superconductor also has some unique magnetic properties. These properties were explained by John Bardeen, Leon Neil Cooper, John Robert Schrieffer in the so called BCS Theory [15] for the first time in 1957, and builds on the concept of Cooper pairs.

### 3.3.1 Cooper pairs

When metals with abilities of superconductivity are cooled below a critical temperature  $T_C$  and aren't exposed to a magnetic field larger than its critical magnetic field  $B_C$ , its electrons will form Cooper pairs. A Cooper pair can be described as two electrons interacting through phonon scattering [16], as illustrated in figure 4.

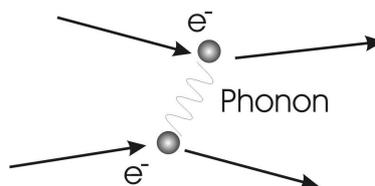


Figure 4: Two electrons interact through a phonon forming a Cooper pair. Figure taken from [17]

When one electron interacts with the crystal lattice a phonon is emitted and the electron is scattered and therefore changes direction and momentum. At some point the phonon interacts with another electron, and transfers its momentum to the electron, which therefore has gained the momentum that the original electron lost. Though Cooper pairs are described as two electron interactions, one single electron will in one instant make a Cooper pair with one electron, and the next instant it will interact with another. Through this

interaction the electrons, with opposite spin and momentum, undergo Bose-Einstein condensation which lowers their energy, and therefore they act as one single boson, which changes the properties of the entire superconductor at macroscopic level. A splitting of the two electrons from the boson state into fermions will require an energy, creating what is known as the superconducting energy gap around the Fermi level. The superconducting gap, is usually described by  $\Delta$ . Now, when the particles are bosons, they can all be in the same state and be described by the same wave function:

$$\Psi = n_s e^{i\varphi} \quad (5)$$

where  $n_s$  is the amplitude and  $\varphi$  is phase. Because they have the same wave function they also have the same energy, the Fermi Energy. This causes electrons around the Fermi level to either be condensed into bosons or pushed out into energy states around the energy gap. Due to this process the density of states is larger in the energy region around the gap.

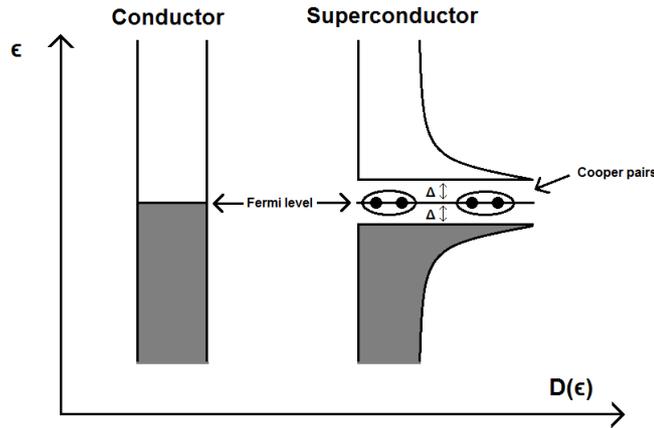


Figure 5: Illustration of band gap in a normal conductor and a superconductor. Density of states  $D(\epsilon)$  versus energy  $\epsilon$ . When a conductor is turned into a superconductor an energy gap is created due to the pair potential of Cooper pairs. Available energy states are pushed away from the Fermi level, creating a higher density of states around the energy gap.

### 3.3.2 Meissner Effect

The Meissner effect is the ability of superconductors to screen out any incoming magnetic field. When a superconductor is exposed to a magnetic field, it will create an internal current near its surface that expels almost all the magnetic field, effectively cancelling the magnetic field in the bulk of the superconductor. Near the surface of the superconductor, not all the magnetic field is cancelled. The London penetration depth  $\lambda$  describes how far into the superconductor the magnetic field is penetrating. When the magnetic field reaches a critical limit, the energy created from the shielding currents will become too large, and superconductivity will break down. These limits are called the critical current  $I_C$  and critical field  $B_C$ .

### 3.3.3 Andreev Reflection and Proximity Effect

In a superconductor-normal conductor junction there will be interference of the states from the opposite metal. The superconductivity will spill into the normal conductor over some length scale and vice versa. This is called the proximity effect. These processes are explained by the theory of Andreev reflection. The length scale of superconductivity spilling in to the normal conductor is called the coherence length  $\xi$ .

Andreev reflection states that when an electron from a normal conductor goes into a superconductor, it has to form a Cooper pair to maintain energy conservation. To form a Cooper pair, it needs another electron with opposite spin and momentum, meaning that if the first electron going into the superconductor is above Fermi level, the other electron has to be an equal amount of energy below the Fermi energy, and vice versa. At the energy where the second electron goes into the superconductor, energy conservation has to apply as well, resulting in a hole with momentum equal to the second electron going from the junction and back into the normal conductor, see figure 6.

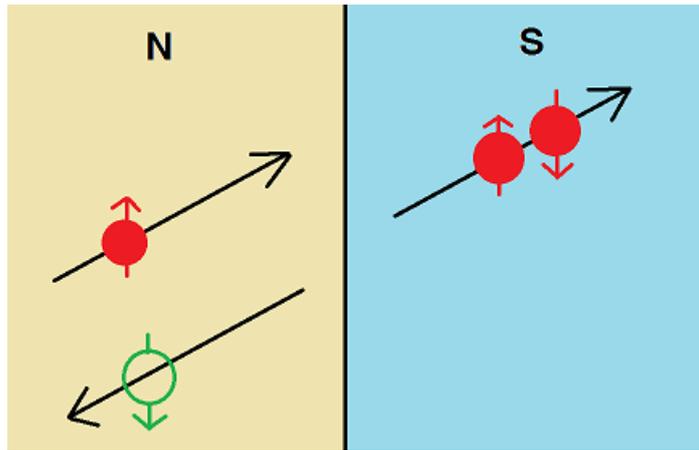


Figure 6: Illustration of Andreev reflection. Electron going through the S-N junction along with another electron to form a Cooper pair. Momentum is conserved due to the backscattered hole.

### 3.3.4 Josephson Junction

In a Josephson Junction two superconductors connected by a weak link, are located close to each other, which makes it possible for a supercurrent to flow through the weak link material, due to the proximity effect. This material can be insulating, semiconducting or conducting. The magnitude of the supercurrent across the non-superconducting region is given by the first Josephson relation, and is determined by phase difference of the two superconductors,  $\Delta\phi$ , and the critical current  $I_C$ :

$$I_S = I_C \sin(\Delta\phi) \quad (6)$$

The second Josephson relation shows that the change of phase  $\Delta\phi'$  has to take certain values.

$$2eV = \hbar \frac{\partial\Delta\phi}{\partial(\Delta t)} \quad (7)$$

where  $(\partial\Delta\phi)/(\partial(\Delta t))$  describes the change in phase with time. These relations have two remarkable consequences. Firstly a DC current will flow through the junction even when no external bias is present, known as the DC Josephson effect, and secondly applying a DC voltage across the junction, will result in an AC current, known as the AC Josephson effect. Both of these effects are caused by Andreev bound states, which is the repeating cycle of Andreev reflections in each side of the junction, illustrated in figure 7.

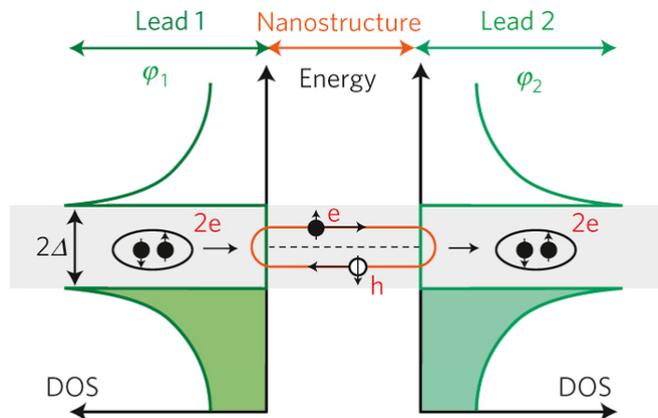


Figure 7: Illustration of how Andreev bound states moves through a Josephson junction. Figure taken from [18].

Andreev bound states are described as the effect of the phase of the hole and electron circulating around the Fermi level of the junction. This causes the phase to be equal to  $2\pi n$ , where  $n$  is an integer, and the

energy will therefore be in discrete levels. Same principle is seen in several branches of quantum mechanics, including atoms, quantum wells and quantum dots.

### 3.4 Josephson Field Effect Transistor

A semiconductor allows for control of charge carrier concentration by applying an electric field. This effect is the basis of a field effect transistor. A field effect transistor (FET) consists of a semiconductor connected to a source and a drain, and is capacitively connected to a backgate. The current through the FET is related to the number of charge carriers, so by applying a voltage to the backgate, one can control the conductance of the semiconductor. For example applying a positive voltage bias to the backgate, will pull the electrons of the semiconductor closer together and lower the Fermi energy of the semiconductor, thus allowing more electrons to enter, which in an InAs nanowire will lower the resistance of the semiconductor.

The Josephson Field Effect Transistor is a three terminal device, based on the combination of a Josephson junction and a field effect transistor.

Two superconducting contacts are connected by a semiconductor, functioning as a field effect transistor. The proximity effect causes the wave function of the superconducting Cooper pairs to continue into the semiconductor. If the distance between the superconducting contacts is shorter than  $2\xi_N$ , a supercurrent will run through the semiconductor. By changing the backgate voltage, we can control the charge carrier density in the wire. The coherence length is defined as:

$$\xi_N = \frac{\hbar v_F}{2\pi k_B T} \quad (8)$$

where  $T$  is temperature and  $k_B$  is the Boltzmann constant. This means that if we increase the number of charge carriers in the wire, and thereby increase the Fermi velocity

$$v_F = \frac{\hbar\sqrt{2\pi n_{2D}}}{m^*} \quad (9)$$

where  $n_{2D}$  is the carrier density and  $m^*$  is the effective mass, we cause an increase in the coherence length of the Cooper pairs. This effectively gives us a way to switch between supercurrent and infinite resistance.

## 4 Fabrication

*A detailed fabrication recipe is given in the appendix.*

### 4.1 Nanowire growth and deposition on chips

Fabrication is done on degenerately doped silicon wafers, with a 100 nm thick insulating thermal oxide layer on top. The ready for use chip already has predefined meanders, bondpads and alignment marks done by photolithography. The center of the layout is a  $500\mu\text{m}$  by  $500\mu\text{m}$  grid. This is the area on to which devices are fabricated.

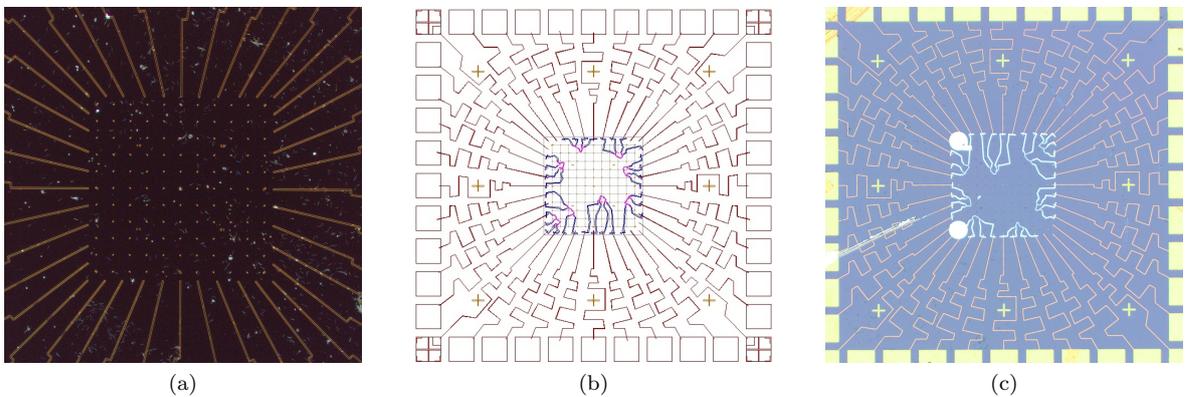


Figure 8: Images demonstrating various steps of the fabrication procedure of chip COP5KM5LL. a) Dark-field microscopy photo of the chip before metal deposition. Images like this were used to locate nanowires. b) DesignCAD file used to define contacts for e-beam lithography. c) The chip after metal deposition, image taken using bright-field microscopy.

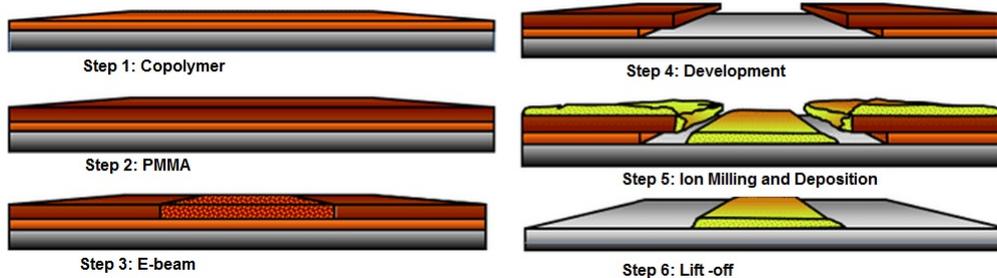


Figure 9: The process of fabricating illustrated in 6 steps. Figure taken from [19].

On to a chip were deposited wurtzite InAs nanowires. The wires were grown by molecular beam epitaxy, by P. Krogstrup, C. Sørensen and M. Madsen of University of Copenhagen. The diameter of the nanowires is  $\sim 100$  nm, and the length is about  $10 \mu\text{m}$ , making them large enough to be identifiable under an optical microscope. The nanowires were grown on an InAs substrate using Au nanoparticles as catalyst. The wires are liberated from the growth substrate by ultrasonication in methanol. A drop of this nanowire suspension is deposited on to a patterned chip, and eventually the chip is left to air dry. The wires are now deposited randomly across the chip.

The nanowires were located using optical microscopy, on bright- and dark-field settings, connected to a camera. The alignment marks of the grid were designed in a way that made it possible to identify the exact position on the chip. The entire  $500\mu\text{m}$  by  $500\mu\text{m}$  grid was imaged this way, and the images imported to designCAD, where they were aligned to an already designed graphical representation of the chip. With all the images aligned, we mapped out the locations of wires and any debris stuck on the chip. Figure 8 (a) shows a typical image, used to locate nanowires.

Wires that were unbent, looked uniformly coloured and had no other wires in their immediate vicinity, were selected for device fabrication. Wires were contacted from each side, creating an S-N-S junction. Each contact branched out into two and contacted each their bondpad, figure 10, allowing for 4-probe measurements. The length of the N-part of the junction, was 500 nm. Shorter distances were tried, but we eventually settled for 500 nm, as this gave the most consistent results. Figure 8 (b) shows a design made in designCAD. Once a design was made it was converted to a .cel file, and imported in to the e-beam lithography software.

## 4.2 E-beam lithography and metal deposition

For e-beam lithography, the chip was spin-coated with a layer of 9% MMA/MAA copolymer and a layer of 4 % PMMA on top. E-beam lithography was done on an Elionix system. E-beam lithography uses a focused electron beam to expose the resist as defined by the device design. The 9% copolymer is more sensitive to the e-beam than the PMMA layer, meaning that more will be removed during development with MIBK:IPA 1:3 developer. This creates an undercut, making lift-off easier.

The next step is ion milling and metal deposition. Ion milling is done to remove the native oxide layer on the nanowires, enabling good contact between the wire and the superconducting leads. Ion milling and metal deposition are done at high vacuum in the same chamber, in situ. This keeps the InAs from reoxidising between ion milling and metal deposition, and as such is a great advantage when trying to obtain good contact. Ion milling is done using a Kaufman milling source. The Kaufman source mills the sample by bombarding the surface with neutralised Argon ions, which kicks the atoms out of the surface. For metal deposition two different techniques are used, sputtering and evaporation. Table 1 lists the superconducting metals tried in this project as well as their critical temperature, superconducting gap and deposition method [9].

Superconductor	Critical Temp	$\Delta$ at T=0	Deposition
Niobium	9.50 K	3.05 meV	Sputtering
Vanadium	5.38 K	1.6 meV	Evaporation
Aluminium	1.14 K	0.33 meV	Evaporation

Evaporation, is a standard metal deposition process used for making thin films. An electron beam is accelerated at high voltage (10kV) towards a crucible containing the desired metal, located at the bottom of the evaporation chamber. The e-beam heats the metal and evaporates it. When the evaporated metal hits the substrate, it condenses on to it.

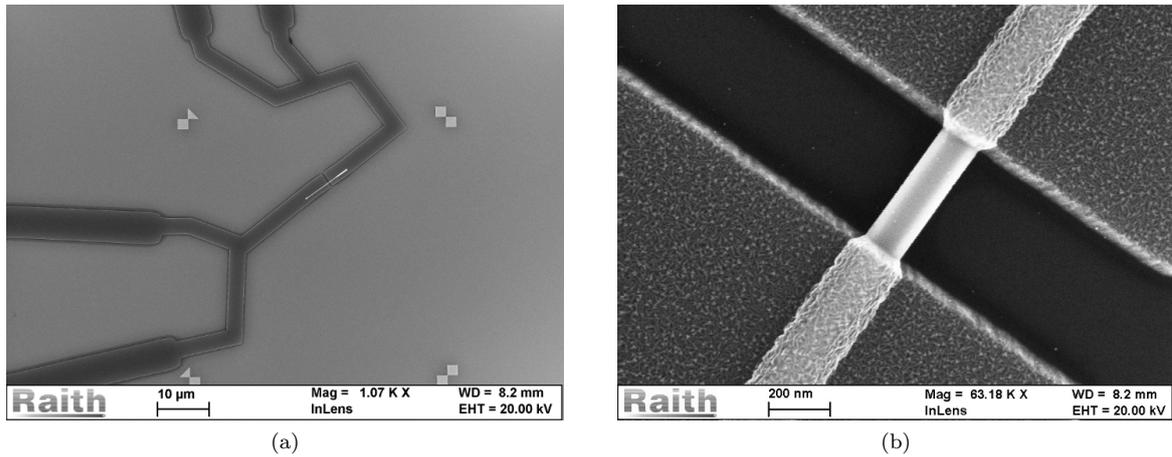


Figure 10: Device made from vanadium with titanium sticking layer

For Niobium contacts, sputtering was used instead of evaporation. This was done because the melting and boiling points of niobium, are so high, that the resist might melt during evaporation. That's why we used sputtering, as this is done at a lower temperature. Sputtering uses a high energy Argon plasma, to bombard the target metal. The momentum of the Argon plasma is transferred to the target material, ejecting atoms out in to the chamber. These atoms deposit on an all surfaces in the vacuum chamber, including the substrate[20].

After metal desposition the chip is placed in acetone for at least a few hours. This dissolves the resist layer, and allows lift-off. The lift-off is done mechanically by spraying the acetone-covered chip from the side, with acetone. Figure 8 (c) shows a finished chip. A finished device on chip COP5KM3 with vanadium and titanium sticking layer is presented in figure 10.

## 5 Experimental

Before the finished chip is cooled down, the individual devices on it are tested. The conductances of the devices should depend on the gate voltage, and the resistance at room temperature should be low (usually in the range from 1 k $\Omega$  to 100 k $\Omega$ ) and exhibit ohmic behaviour, as good ohmic contact is necessary for inducing superconductivity in the nanowire. We expect gate dependence because InAs is a semiconductor, meaning its charge carrier density, and therefore its resistance will change with an electric field. Showing gate dependence also witnesses that the two supercontacting contacts aren't shorted. The probe station allows you to test these dependences. A camera attached to a computer enlarges the chip, so that the movable probes can be directed to the bond pads. A source-drain voltage is swept from -5 mV to 5 mV on every single device from every single bond pad. Figure 11 shows 2-probe measurements on two different chips, which is done to see ohmic dependence and resistance.

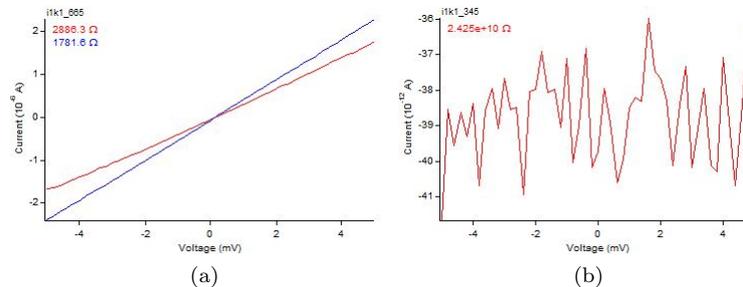


Figure 11: 2-probe measurements on devices testing for gate dependence before cool down. 11 (a) Shows ohmic resistance and gate dependence with a resistance of 2886  $\Omega$  at  $V_{BG} = 0V$  and of 1781  $\Omega$  when  $V_{BG} = 5V$ . 11 (b) shows no signs of ohmic behaviour.

In figure 11 (a) two linear dependences of current are present. One is at  $V_{BG}=0$  V and the other is at  $V_{BG}=5$  V, showing resistances of 2886  $\Omega$  and 1781  $\Omega$ , respectively. This measurement is an example of a device, which should be investigated further. Figure 11 (b) shows no sign of ohmic contact, implying that

something in the fabrication process went wrong, making the barriers from contact to nanowire too high. A device like this would be low in priority for further measurements at lower temperature.

## 5.1 Dilution Refrigerator

A fridge for low temperature physics is essential for these experiments. The dilution fridge used in this project is capable of cooling samples down to less than 10 mK. In the following, the fridge is described stepwise to give a clue of the construction making such low temperatures possible. It consists of several plates placed in sections on top of each other, where the lower the plate is situated, the colder it is. To separate it thermally from the surroundings, the entire cooling system is located inside a vacuum chamber, separating the different temperatures in the system. Figure 12 is a picture of the inside of the fridge, showing thermally connected cooling plates.

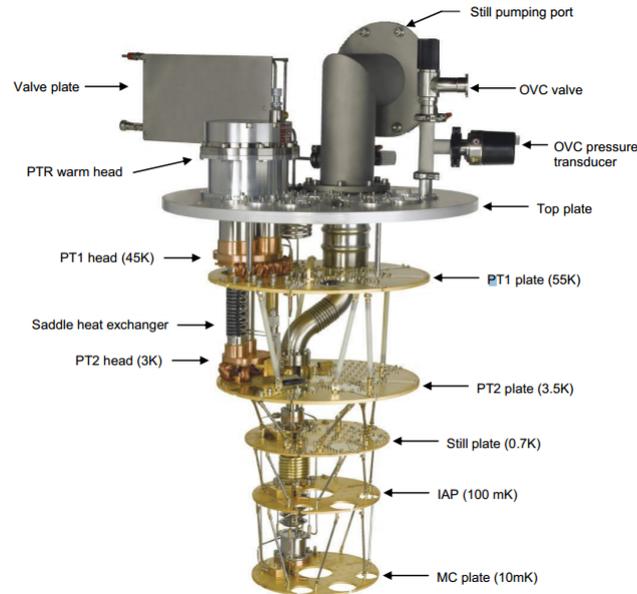


Figure 12: Inner, cooling parts of the Cryofree dilution refrigerator.

The uppermost horizontal plate is called the Top plate. This plate is at room temperature, and it is here the outer vacuum can is placed. Underneath the Top plate, the two plates PT1 and PT2 are situated, pre-cooling down to around 55 K and 4 K, respectively. These, along with the Top plate, are connected to a pre-cool loop using heat exchangers. During pre-cool down, the pre-cool loop is cooling the still, the 100 mK plate and mixing chamber plate. The three latter mentioned plates are all part of the dilution unit, which, after the pre-cool down starts diluting a flow of  $^3\text{He}$  in liquid  $^4\text{He}$ . In the mixing chamber there are two phases. The concentrated phase consists of  $^3\text{He}$  and the dilute phase consists of a mixture of 6-7%  $^3\text{He}$  and 93-94%  $^4\text{He}$ . The dilution unit makes the  $^3\text{He}$  evaporate, extracting heat from the dilute phase. This part of the fridge is the coldest, and it is here the sample is located. A construction called the cold finger is thermally connected to the mixing chamber. The puck containing the sample, can be connected to the cold finger.

To reduce the noise from other electrical components in form of electromagnetic waves, a sequence of filters are added to the circuit in between the breakout box and the sample. At first the electrical circuit goes through an RF filter, consisting of three low pass filter, filtering out frequencies in the range from MHz to GHz. The RC filter is placed after the RF filter and has a cut-off frequency in the range of kHz. Next comes the copper powder filter which filters out frequencies even higher than RF filter, then the sapphire box which thermalises the electrons to the fridge. Copper brackets are essential for enclosing filters. The currently used brackets for RC- and RF filters as well as the ones for copper powder- and sapphire filters were designed by the authors of this report. Figure 13 shows these silver and gold plated copper brackets.

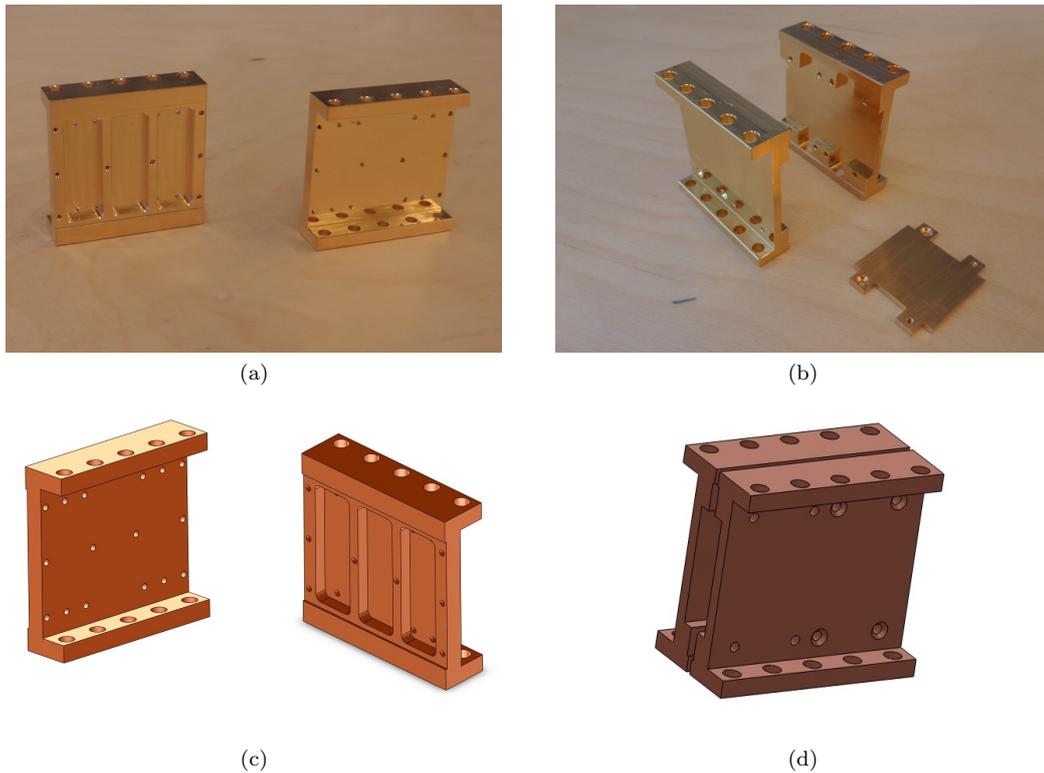


Figure 13: Pictures and 3D designs of brackets designed by Kasper Thue Langkjer and Mads Kasper von Borries. (a) and (c) are RC- and RF brackets, while (b) and (d) are brackets for sapphire- and copper powder filters.

The bulk of the brackets were made of copper, which is a good thermal conductor. The brackets were first silver- and then gold plated. The silver plating prevents gold from diffusing into the copper. The gold plating was to prevent copper from oxidizing, because oxidation result in bad thermal conduction. Besides, neither silver nor gold are ferromagnetic, meaning that these materials will not influence experiments. To increase thermal conduction further, the brackets were designed to have a large area pressed against the filters. This serves as good conduction as well as applying a large stabilizing force on the filters during cool down. To apply a large force on the filters through mounting screws, brackets were designed to have spacing in between each other. This causes a gap of a few millimetres all around the assemble, thus a good idea is to cover this area with copper tape, shielding filters more effectively from radiation. The innovative design allows the two different kinds of brackets to be mounted on top of each other, resulting in greater freedom, when deciding where in the dilution fridge to place them, and also allows for the user to choose a specific combination of different filters.

When the sample is at base temperature, the measurements begin. The chip is conductively connected to the chip-carrier, a holder for carrying the chip, figure 14 (a), by wirebonding the chip with aluminium wire. It is connected to a backgate by applying a drop of silver paint on the carrier, placing the chip on it, and wirebonding it to the carrier. The silver paint functions as a conducting adhesive. The chip carrier is carefully placed in a sample holder, figure 14 (b), allowing conduction from chip carrier to larger scales in form of outer sample holder. The sample holder is then placed in a puck - a holder for the chip carrier that connects it to the electrical wiring in the dilution fridge. An open and a closed puck is pictured in figure 14 (c) and (d), respectively. The electrical wiring in the fridge runs from the breakout box at room temperature, through several cooling stages and filtering, and terminates at the cold finger. An open breakout box (e), and a fully operating one connected to a circuit (f), is shown in figure 14, and is where the instruments used for experiments are connected. Thus the breakout box forms the link between the chip and the scientist.

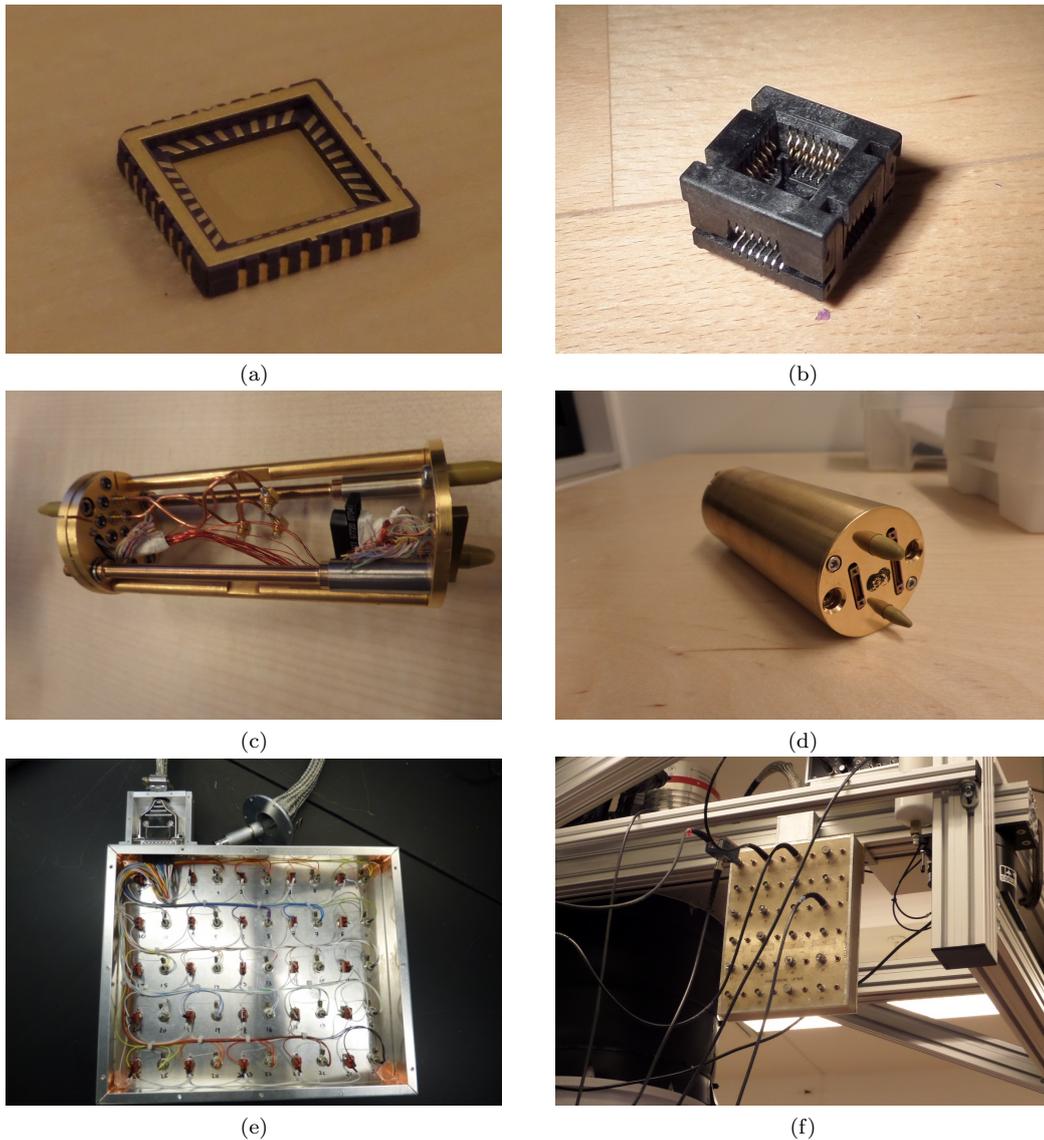


Figure 14: Picture of figure puck from the (a) outside and (b) inside. In (c) a chip carrier which is placed in (d) a sample holder is shown. An open breakout box is present in picture (e) while a functioning breakout box is shown in figure (f).

Depending on the desired measurement, various instruments are plugged into the outputs of the breakout box. Through the software, Igor Pro, the computer controls the instruments, including DMM, Keithley, Lock-in amplifier, current amplifiers, Decadac and Ithaco. Next a short description of the instruments will follow. The Keithley has different applications. It can send out a current, apply a voltage and also measure both current and voltage. The lack of precision, compared to the DecaDAC, is the disadvantage of the Keithley. A DMM is a multimeter, and measures current, voltage or resistance.

The Lock-in amplifier allows an adjustable AC voltage to be applied as well as measured as an input. The addition of an AC signal to a DC signal makes the Lock-in capable of filtering noise from other frequencies, and thereby achieve a cleaner signal [21]. Besides, in some situations it can be useful to have only an AC signal in an experiment.

For the conducted experiments, two different voltage preamplifiers were used. A low noise preamplifier, which amplifies voltage with a factor of 100. The limited number of settings, makes the preamplifier fast and easy to use. The other is an adjustable low noise preamplifier, which filter cut-off at specific frequencies and has an adjustable gain, ranging from a factor of 1 to a factor of  $10^4$ . Apart from these two, a current preamplifier, Ithaco, can be used. This is the most precise amplifier of the three mentioned. It converts current to voltage by a factor of up to  $10^{11}$  and has adjustable sensitivity.

The DecaDAC is one of the three versions of DACs (Digital to Analog Converter) made by Jim MacArthur at Harvard electronics shop [22]. It is capable of making biases from -10 V to 10 V, and has extraordinary low noise. The resolution of the DecaDAC is 16 bits, meaning that it, in its original range of  $\pm 10$  V, has a resolution of  $2^{16}$  steps. Channels of the DAC can be added to other channels,

with a division factor of 1/100, effectively making the resolution 100 times higher. From the DecaDAC, a voltage divider is often used. Mainly to lower the voltage output from the DecaDAC, but also to increase the resolution even further.

## 5.2 Experimental Setups

When the sample is in the dilution fridge, a variety of experiments can be conducted. In the devices this project focuses on, superconducting contacts and backgate dependence are crucial for device investigation. These dependences can be tested in different ways. One way of measuring superconductivity of the contacts is by feeding a constant current, and measure the voltage drop across a contact, whilst lowering the temperature to less than  $T_C$ . This can be done with a 2-probe measurement. In this case, when temperature is lowered to below  $T_C$ , the resistance will drop to a constant level, which is given by the line resistance. A schematic of such a measurement checking for superconductivity of the contacts, and a graph demonstrating superconducting contacts, is shown below in figure 15.

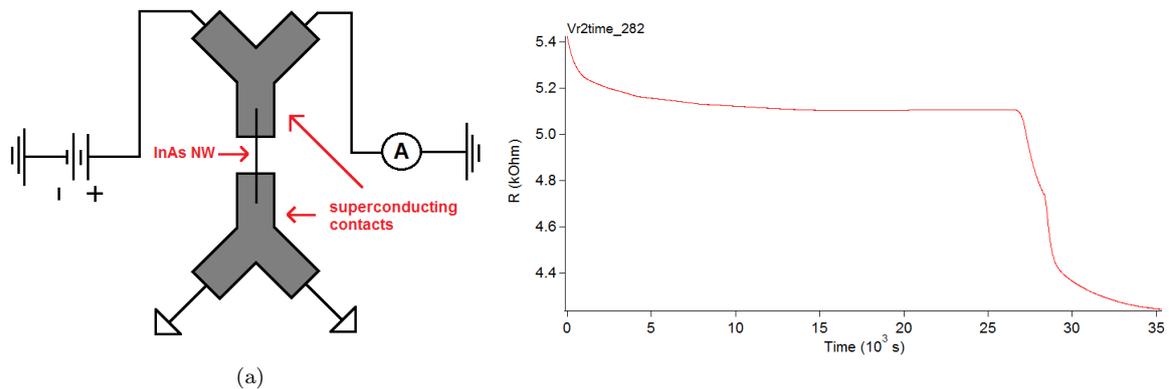


Figure 15: 2-probe measurement for detecting supercurrent in COP5KM4LL with 120 nm vanadium. 15 (a) is a schematic drawing of the set-up. 15 (b) is a measurement of a device cooled down to base temperature, reaching a resistance of 4.3  $k\Omega$  matching the line resistance and thereby showing signs of superconductivity, leading to further investigation.

Another criteria for a functioning JoFET is gate dependence, which in this case is tested by doing backgate sweeps. However before conducting backgate sweep measurements, it is necessary to check devices for backgate leakage. Scratches in the top most layer of the Si chip, the  $\text{SiO}_2$  layer, resulting from for example probing, can cause conduction through the bond pads or contacts directly into the backgate. A method for leakage testing is to apply a finite backgate voltage from the Keithley, because it, while sourcing a voltage, can also measure the current. When a backgate voltage is applied, all the channels in the breakout box are floated. The devices are then grounded one at a time, while the current is measured. If there is no leakage to the grounded device, no current will flow from the Keithley. If however, the device is leaking, a current will flow from the source, through the device, and into the ground. Before doing backgate sweeps, this test is done on all devices, and if leakage is detected, the device is isolated.

A backgate sweep is done by either 4-probe or 2-probe measurements. In the 2-probe measurement a constant source-drain voltage is applied from the DecaDAC. To reduce the voltage, a voltage divider is added in between the DecaDAC and the breakout box, connecting the voltage source to the device. A Keithley is connected to the breakout box in the channel leading to the backgate. From the other side of the device, a current to voltage amplifier is connected, allowing measurement of the output current. The current is measured as a function of the backgate sweep. In a semiconductor, such as an InAs nanowire, the current will increase as a function of increased positive backgate. An illustration of the setup is presented in figure 16 (a).

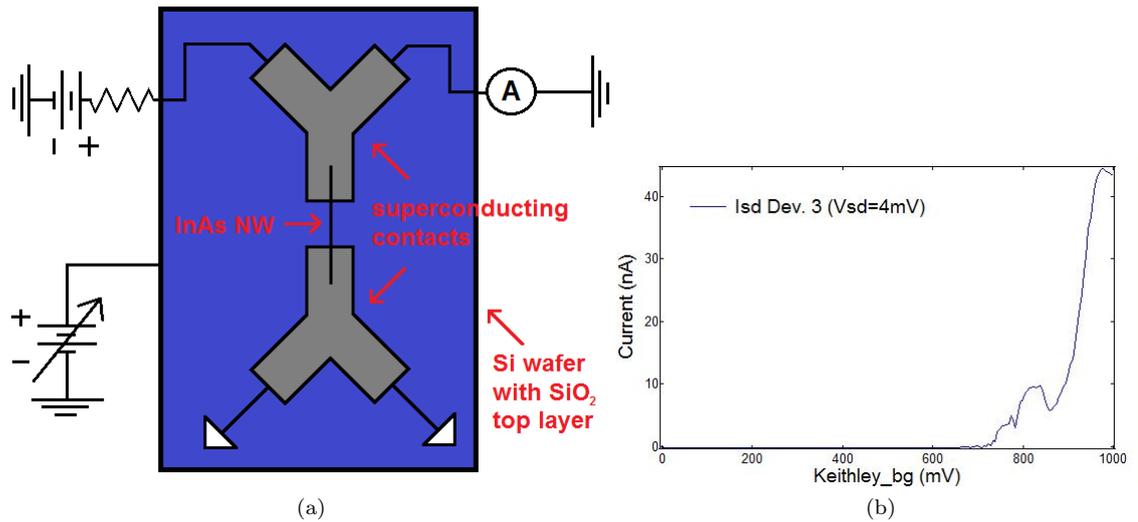


Figure 16: Measurement of the backgate dependence of COP5KM3LL, device 3 with 5 nm Ti and 120 nm V. 16 (a) is a schematic illustration of the setup. 16 (b) is a graph showing backgate dependence. The device has pinch off at approximately 700 mV backgate.

Figure 16 (b) shows the gate dependence of a device made up of 5 nm Ti and 120 nm vanadium. When the device has a positive backgate of above approximately 700 mV, the device turns on, and when the backgate is less than 700 mV, the device is completely depleted of charge carriers. From this point and on, the current is increasing and decreasing in a monotone oscillating fashion. From this, backgate dependence can be concluded, and interesting physics might follow from further investigation.

When a device has been tested for leakage, superconducting contacts and gate dependence, experiments for testing critical field and other physical phenomena can take place. These experiments are conducted using 4 probe measurements. Figure 17 is an illustration of a 4-probe setup.

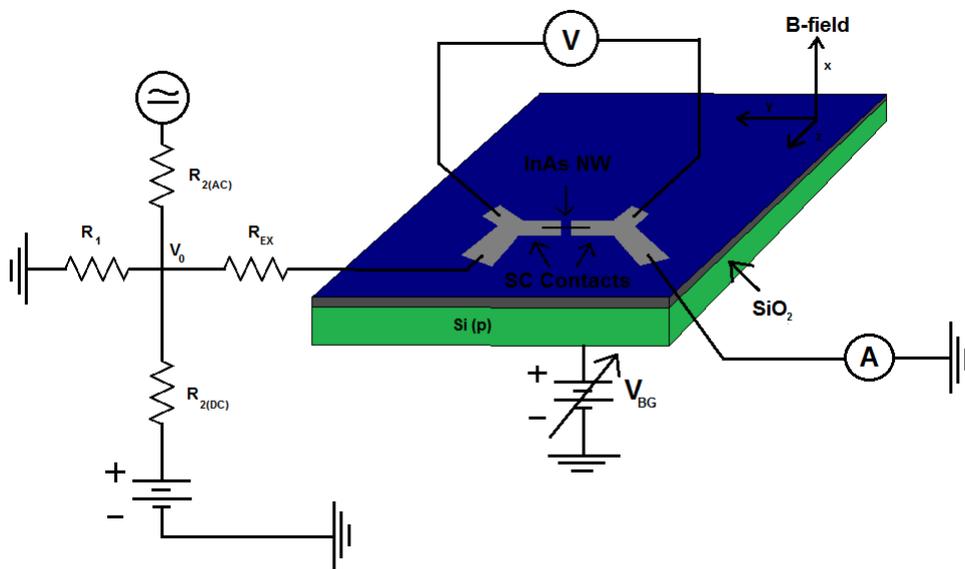


Figure 17: 4-probe setup. Both AC and DC current is applied to the sample in a circuit with resistors making this operation possible. The output current is measured after running through the wire. The voltage drop across the wire is measured by a Lock-in. The charge carrier concentration in the nanowire is controlled capacitively by adjusting the backgate voltage.

A voltage is applied, typically from the DecaDAC, and into a voltage divider with a channel for adding AC current. The voltage divider contains three resistors. Two large resistors in front of the AC and the DC source, and one in front of the ground connection. The voltage going to the breakout box is given by

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the relation,

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in} \quad (10)$$

where  $V_{out}$  is the voltage in front of the breakout box,  $R_2$  is the resistor between the circuit and the ground,  $R_1$  is the resistor between the voltage source and the breakout box, and  $V_{in}$  is the AC or DC voltage applied from the Lock-in or/and the DecaDAC. A Lock-in signal can be applied for strengthening the signal to noise ratio[23]. To get correct measurements  $R_2$  has to be much smaller than  $R_1$  and the resistance in the sample has to be a lot smaller than  $R_1$  and much larger than  $R_2$ . If this is not the case, the voltage divider will be the source of incorrect measurements. In the setup a predefined current is sent through the device. A predefined current can be made by applying an external resistor,  $R_{Ex}$  in between the voltage,  $V_0$ , and the sample with resistance  $R_{sample}$ . If the resistance of the sample is much smaller than the external resistor, serial resistance in this section will almost be equal to the external resistor. If so, a current can be defined from the resistance and the voltage in this region through Ohms law:

$$V = RI \quad (11)$$

where  $V$  is voltage,  $R$  is resistance and  $I$  is current. If the aforementioned resistance relations are not as described, this will be the cause of experimental errors. The current runs through the wire if barriers are low enough, and continue from the breakout box into ground. The voltage drop from the superconducting contacts, connected to each side of the wire, is measured by the lock-in.

In conclusion, the set-up allows determining the resistance of the wire, as both the current through the wire and the voltage across it are measured precisely. Conductance,  $G = 1/R$ , can also be found as it is related to resistance. A Keithley controlling backgate voltage, is connected through the breakout box to the Si chip, allowing measurements of gate dependence.

## 6 Results

In this section we present data taken from measurements done on three different chips. In addition to these, measurements were conducted on two additional chips. One with 5 nm Ti/120 nm V contacts, which gave data similar to that presented for COP5KM3LL. The other with 5 nm Ti/120 nm niobium contacts. None of the devices on this chip worked at cool-down. Fabrication of the chips follows the recipe given in the appendix, unless otherwise stated. Data was taken at a temperature of  $\sim 30$  mK, except for when testing for resistance dependence versus temperature.

### 6.1 Vanadium with titanium sticking layer - COP5KM3LL

The devices on this chip were made with a 5 nm titanium sticking layer, and 120 nm vanadium. The vanadium pellets were extensively oxidised on the surface, and hence we needed to outgas a lot before evaporation. This might have affected the quality of the thin film.

Gate dependence was measured on the device with a 4-probe lock-in measurement. A measurement was conducted with an AC current small enough to not exceed the critical current of vanadium, yet capable of efficiently finding the conductance. On the Lock-in an AC of 0.5 V was applied, followed by a 100 M $\Omega$  resistor, efficiently resulting in a current of 5 nA across the device. The frequency was chosen at 317.3 Hz, far from the most common noise frequency at 50 Hz, and checked with a spectrum analyser to make sure that the noise background at that frequency was low. Controllable backgate was applied from a Keithley. Voltage drop measurement over the device was provided by the Lock-in amplifier. Figure 18 presents a graph of backgate sweep from -10 V to 40 V.

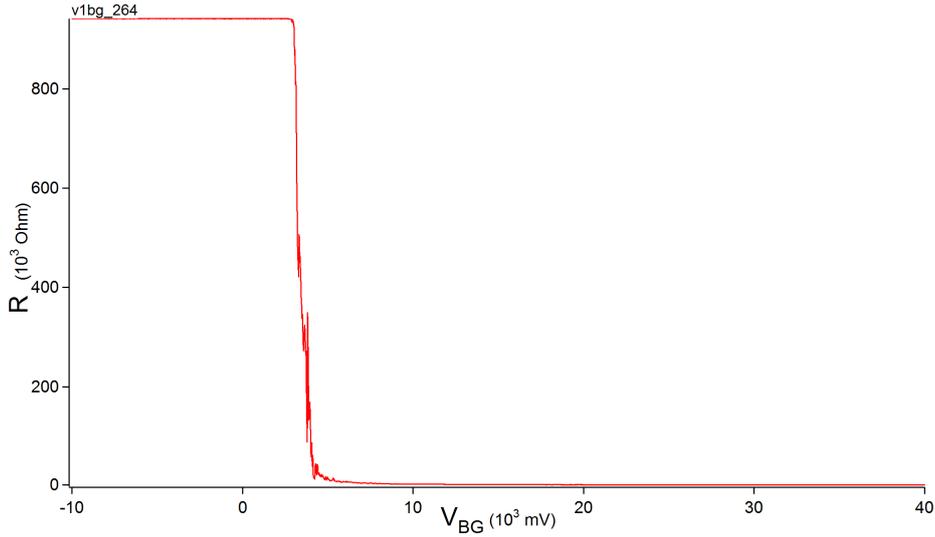


Figure 18: 4-probe AC measurement of backgate sweep, measuring the resistance across device COP5KM3LL. A clear gate dependence is observed. Device pinches off below  $\sim 3$  V. Resistance at high  $V_{bg} = 2.2$  k $\Omega$ . Taken at  $V_{SD} = 2$  mV

A drastical drop in resistance from  $\sim 1$  M $\Omega$  to the order of kilohm happens at  $\sim 3$  V, and eventually resistance drops to 2.2 k $\Omega$ . This demonstrates that the device is able to switch on and off. Further experiments were conducted at a back-gate above 3 V.

If a supercurrent was flowing through the nanowire, we would be able to suppress it by applying a magnetic field larger than the critical field of vanadium. This would show as an increase in resistance. Thus the next experiment performed on the devices was magnetic field dependence. The  $B_C$  along the nanowire axis was determined to be  $\sim 2$  T in a comparable device, by Lee et al.[26]. On the graph presented in figure 19, source-drain voltage is plotted versus current, without (red) and with (blue and green) exposure to magnetic field. The magnetic field was applied from a vector magnet, capable of rotating and tilting the magnetic field vector in three axes. The magnetic field strength had a total magnitude of respectively 1.4 T (green) and 4.1 T (blue).

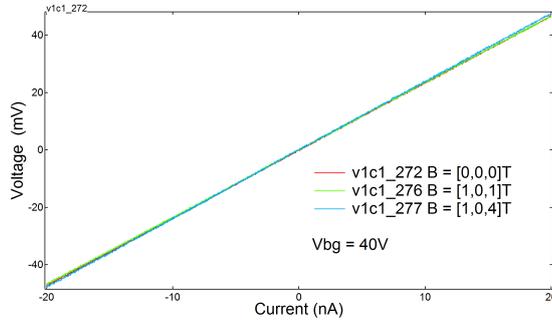


Figure 19: Current biased voltage measurement. Devices show Ohmic behaviour, indicating good contact between contacts and wire. Measurements taken at B-fields larger than  $B_C$  for vanadium, shows no change in resistance, indicating no superconductivity across the wire.

Ohmic behaviour is seen in all three cases, indicating good contact between vanadium and nanowires. However no magnetic field dependence is observed, indicating no superconductivity through the wire. A 2-probe measurement of resistance through contacts on the same side of the wire, going through vanadium only, was conducted to determine the characteristics of the vanadium. Applying voltage while measuring current, when heating up the fridge, enabled us to monitor the resistance of the vanadium contacts as the temperature exceeded the critical temperature. Figure 20 is a plot of resistance in the device when fridge is heated up to  $\sim 10$  K, which exceeds the critical temperature of vanadium,  $T_C = 5.38$  K.

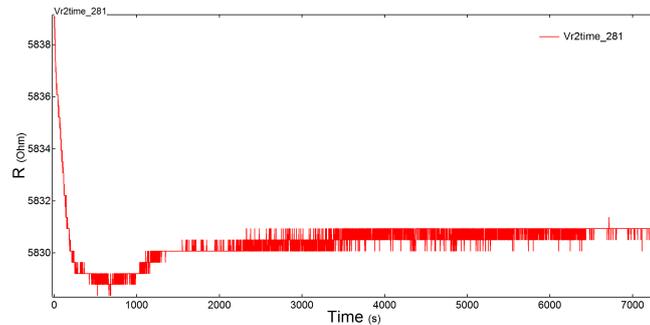


Figure 20: 2-probe measurement on vanadium contact, taken while heating up the dilution fridge. Resistance doesn't change as temperature goes over  $T_C$  for vanadium. This means that contacts are not superconducting. Line resistance is about  $4.5\text{k}\Omega$ , giving an estimated contact resistance of  $\sim 1\text{k}\Omega$ .

The resistance remains nearly constant at  $\sim 5.8\text{k}\Omega$  over a temperature range including temperatures both above and below  $T_C$  of vanadium. Line resistance of the fridge wiring is about  $4.5\text{k}\Omega$ , giving an estimated resistance of the vanadium film of  $\sim 1\text{k}\Omega$ . We therefore conclude that the vanadium contacts were not superconducting. As previously mentioned we suspect this might be due to a high level of impurities being incorporated in the thin film, as a consequence of the heavy outgassing performed on the vanadium, immediately before deposition.

## 6.2 Vanadium without sticking layer - COP5KM4LL

During the evaporation of vanadium for COP5KM3LL, we noticed a pressure drop in the vacuum chamber, leading us to believe that vanadium is a getter material and as such could stick to the chip without the titanium layer. Intuitively this was motivating, as removing a non-superconducting layer between the superconductor and the nanowire, would enhance the proximity effect. Realising that vanadium is used as a component in non-evaporable getters [27] [28] lead us to pursue this direction. The chip was made with  $120\text{nm}$  vanadium contacts, and no titanium sticking layer. Since no superconductivity was detected in the contacts of the previous device, the first experiment conducted on this device, was testing contacts for superconductivity. A 2-probe measurement was done, monitoring resistance during cool-down. If contacts were superconducting, the expectation would be to see the resistance drop, to a value of around  $4.5\text{k}\Omega$ , when reaching critical temperature. The  $4.5\text{k}\Omega$  is the line resistance of the wiring of the fridge, measured by previous users of the fridge. The measurement is presented in figure 21.

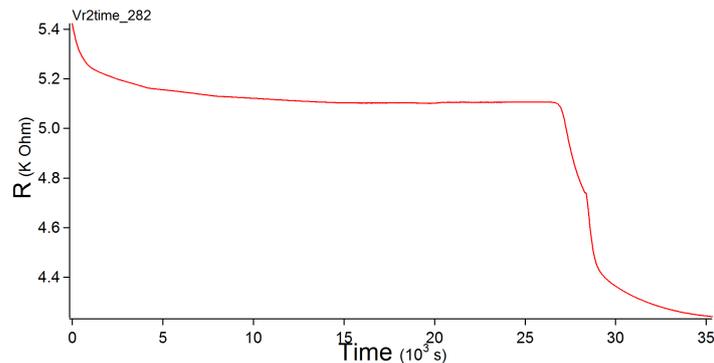


Figure 21: 2 probe measurement across contact, taken while cooling down fridge. Resistance drops to a constant level, equal to the line resistance as temperature is lowered. This indicates a transition to the superconducting state.

As hoped, a resistance drop to the level of line resistance, was observed. The resistance of the vanadium-film suddenly dropped by  $1\text{k}\Omega$ , providing a strong indication of a transition to the superconducting state. From this we interpreted that the vanadium contacts are superconducting, and supports the theory that contamination from outgassing was the reason for non-superconducting leads in previous vanadium device. Next, a source-drain biased current measurement was conducted to test for ohmic dependence, and a drop in resistance around zero. This would indicate superconductivity across the wire. Instead the device showed a higher resistance around zero. To examine this, a 2-probe voltage bias measurement was conducted sweeping voltage in the range of  $\pm 4\text{V}$ . The set-up is shown figure 17. The plot is presented in figure 22.

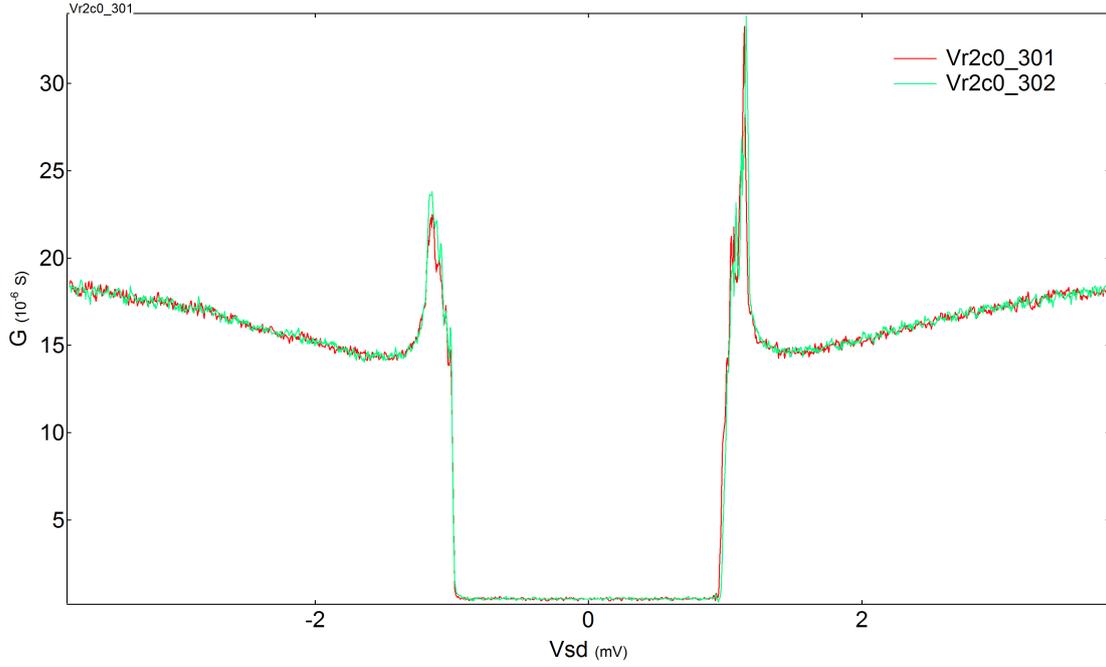


Figure 22: Conductance drops in the superconducting regime, indicating a tunnel barrier. The width of the conductance drop is a measurement of  $4\Delta$ . From this we calculated  $\Delta_{Vanadium} = 0.55$  meV.

This data indicates that there seems to be a strong tunnel barrier between the two vanadium contacts. Though this means that the device is not a functioning JoFET, this measurement shows other interesting physics. As the Cooper pairs from the vanadium do not conduct through the device, a measured current across the barrier has to come from filled energy bands in the superconductor, as seen in figure 5. For one superconductor to spill electrons in to the other, the filled valence band of superconductor A has to have the same or higher energy than the conduction band of superconductor B. To get this energy one superconductor has to gain a voltage equivalent to at least  $2\Delta$ . For current to flow in opposite direction, same rules count, thus the region with no conductance will be equal to  $4\Delta$ . The low conductance region has a change in voltage difference of 2.2 mV, and the  $4\Delta$  energy will therefore be 2.2 meV. From this, the superconducting gap of vanadium is calculated,  $\Delta = 0.55$  meV. This is in agreement with the value found by Lee et al. (2013) [26]. In a superconductor the density of states is greater near the energy gap [16], resulting in a higher conductance near the band gap, seen as the two peaks in the graph. To test for gate dependence, and to get more precise measurements of the band gap, a 4-channel measurement as described before, with variable backgate in addition, was plotted. Figure 23 shows two of these plots with source-drain voltage from -4 mV to 4 mV. One made with a backgate swept from 9.7 V to 10 V and one from 39.5 V to 40 V.

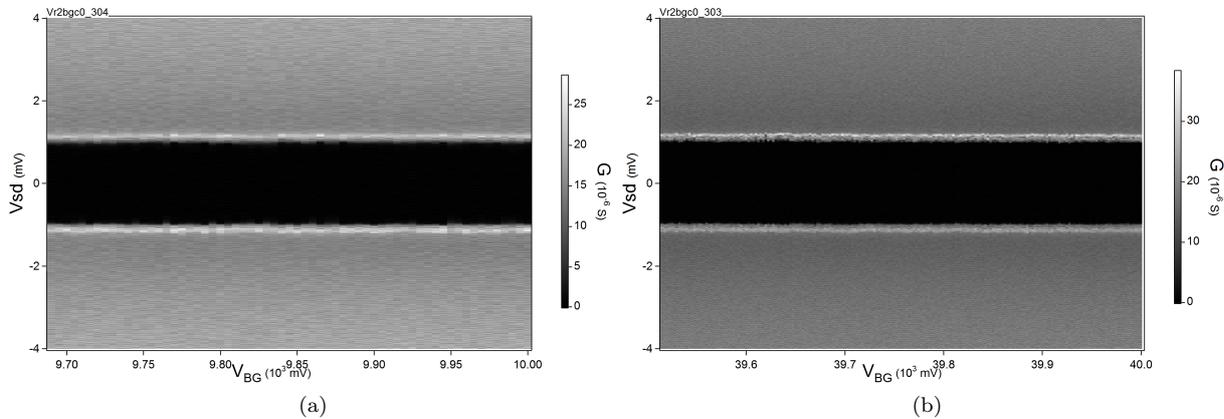


Figure 23: Source-drain sweeps from -4 V to 4 V at different backgates. In (a) the backgate is swept from 9.7 V to 10 V and in (b) the sweep is done from 39.5 V to 40 V.

The data displays tunnel barriers with no sign of gate dependence. The conductance through the device,

doesn't vary over a 40 V backgate range.

As the vanadium contacts in this device showed superconductivity, the angular magnetic dependence could be measured. Figure 24 shows magnetic dependence in plane and perpendicular to the plane.

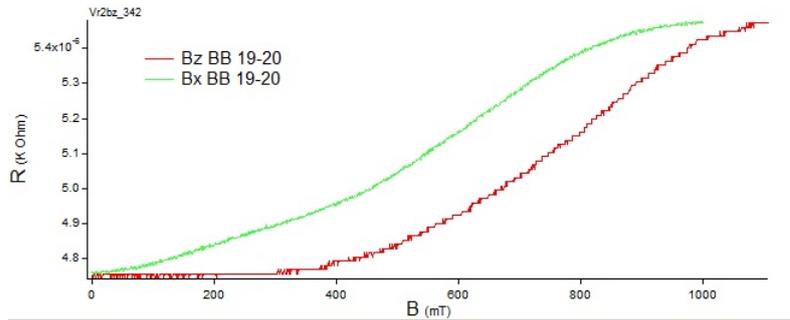


Figure 24: Magnetic dependence of superconducting vanadium. Magnetic field is applied in plane (red) and perpendicular to the plane (green). This is consistent with the fact that the smaller the superconductor area, the greater the critical field.

When magnetic field is applied in plane, the resistance in the vanadium leads start to increase at higher magnetic field, than when the field is perpendicular to the plane. The resistance starts out at the same value and ends at the same value, showing that, in both cases, the contacts are going from a superconducting regime, to a non-superconducting regime. The only difference is therefore that the leads are more affected when magnetic field is applied perpendicular to the plane. This is consistent with the fact that the smaller the superconductor area, the greater the critical field. The resistance of the film is rising slowly as a function of  $B$ , instead of exhibiting a sharp jump at  $B_C$ . We think this may be caused by impure regions in the film, turning normal conducting independently of the rest of the film, until the entire film has turned normal conducting. Both graphs reach the same stable level at higher magnetic field.

### 6.3 Aluminium with titanium sticking layer - COP5KM5LL

The devices on this chip were made with a 5 nm titanium sticking layer, and 120 nm aluminium. Ion milling was done for 2 minutes instead of the usual 1 minute. In total seven devices were fabricated on this chip. Of the seven devices, only one showed signs of superconductivity. Data from this device is presented in this section. Unfortunately only two contacts on this device were wired, due to the fact that the results from the probe station looked more promising for 5 other devices, so due to a limitation on the number of bondpads on the chip carrier, this device was given low priority. For this reason all measurements presented here are 2 probe measurements.

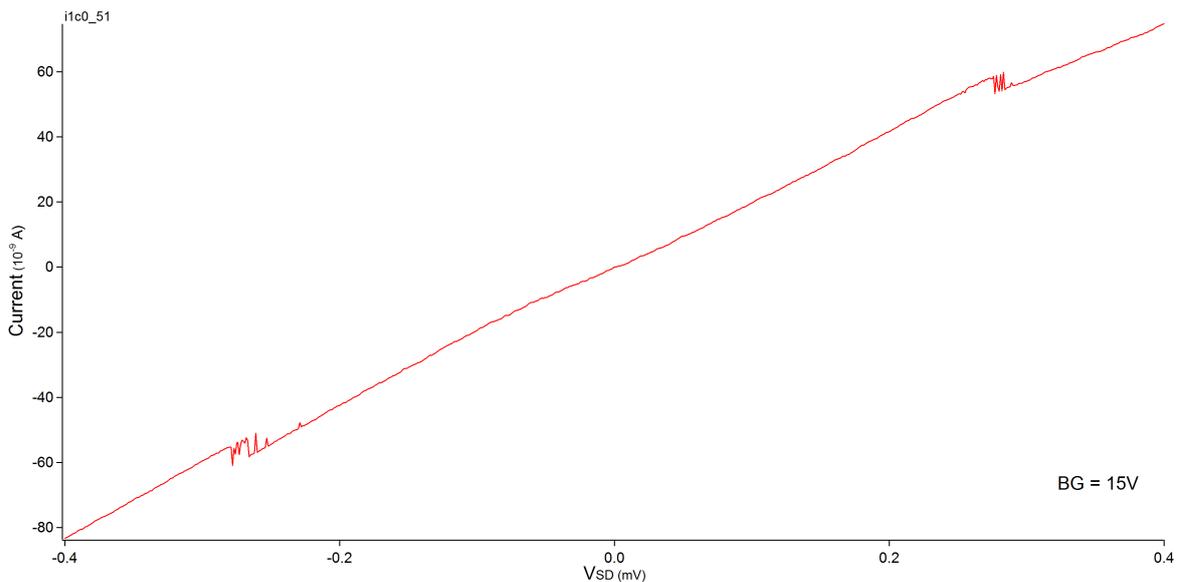


Figure 25: Current across Josephson Junction as a function of source-drain voltage. The kinks at each end of the graph indicates jumps between the normal and superconducting state.  $R_N + R_{Fridge\ wire} = 5156 \Omega$ .  $R_S + R_{Fridge\ wire} = 4630 \Omega$

Figure 25 shows a 2 probe voltage biased I-V measurement across the wire, taken at  $V_{BG} = 15$  V. The graph, shows two clear jumps, one in each end. This is interpreted as a transition from normal conductivity to superconductivity. The resistance outside the mid part of the graph, above and below  $V_{SD} \sim \pm 0.3$  V was calculated to  $5156 \Omega$ . For the mid region  $R = 4630 \Omega$ . The line resistance of the refrigerator is known to be around  $4.5 \text{ k}\Omega$ . This leads us to conclude that the resistance across the wire is equal to zero, and we therefore are observing superconductivity. From the graph we determine  $I_C = 50 \text{ nA}$ .

Having successfully fabricated a Josephson Junction, we tested the device for gate controllability. Figure 26 shows differential conductance as a function of source-drain voltage and back-gate voltage. It demonstrates a clear gate dependence. On the right hand side of the figure (lower negative gate voltage), the superconducting gap is well defined. On the left hand side the device pinches off around  $V_{BG} \sim -4000$  V. Having demonstrated superconductivity and gate controllability, means that the device is a functioning JoFET. Many of the features on figure 26 comes in repeating patterns. We interpret this as switching, possibly caused by impurities trapped between the wires and the substrate during wire deposition. To eliminate switching, the device was left to rest at the same back-gate voltage for a few hours before conducting further measurements. Figure 27 is recorded after a resting period. It displays a lot of interesting physical features. The superconducting gap of aluminium is clearly displayed, and was measured to be  $0.17 \text{ meV}$ . The diagonal yellow lines are interpreted as Coulomb diamonds. The yellow wavy peaks are interpreted as subgap resonance Yu-Shiba-Rusinov states [29] [30] [31] [32] [33] [34]. Further interpretation of these states is beyond the scope of this report.

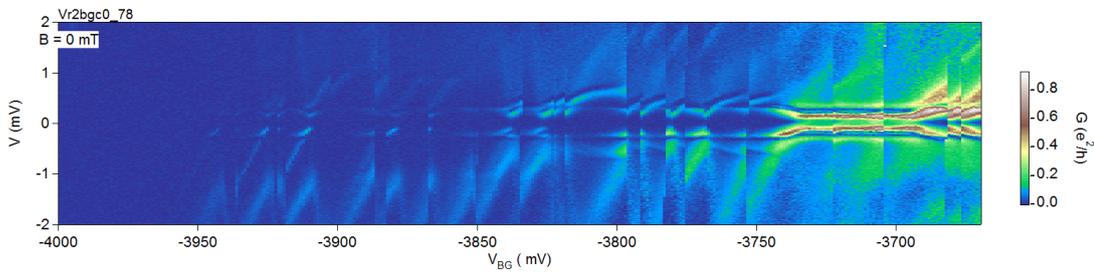


Figure 26: Differential conductance as a function of source-drain voltage and back-gate voltage. Showing gate dependence of device, and pinch-off at  $V_{BG} \sim -4000$  V. Device is switching a lot.

To determine the maximal critical field of the JoFET, systematic 360 degree magnet sweeps were taken to find the precise alignment of the wire. Once the angle had been determined, measurements of critical field dependence on angle were performed using a vector magnet. The results are shown in figure 28.

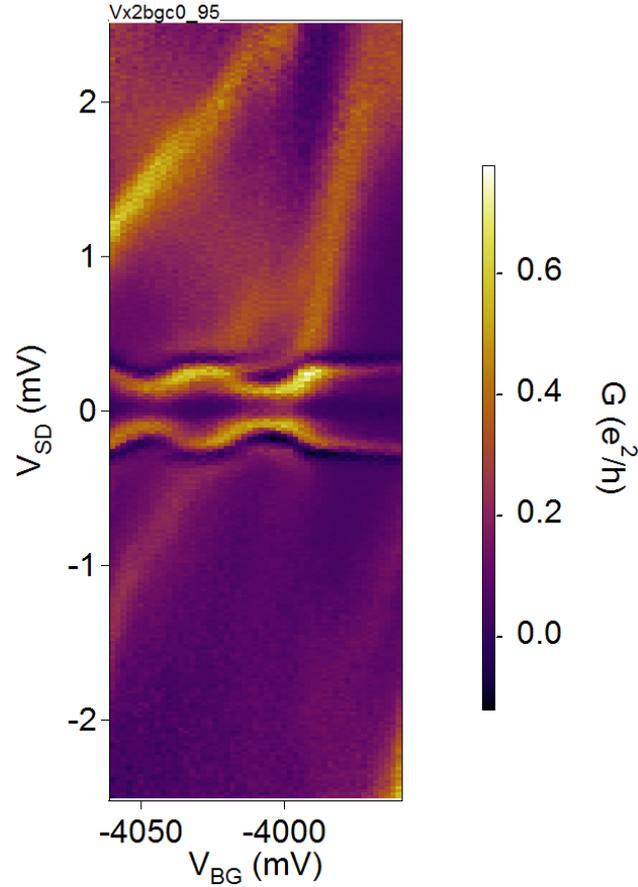


Figure 27: Differential conductance as a function of source-drain voltage and back-gate voltage.  $B = 0$  T. This graph displays Coulomb diamonds and Yu-Shiba-Rusinov states. The superconducting gap is measured to be  $= 0.17$  meV.

Figure 28 a) is taken with the magnetic field in plane and perpendicular. The critical field is  $\sim 45$  mT. Figure 28 b) has the magnetic field in plane and parallel to the wire. The critical field is  $\sim 75$  mT. Figure 28 c) has the magnetic field perpendicular to the substrate, and here the critical field is only  $\sim 10$  mT. This shows a clear angular dependence of the critical field. The largest critical field is obtained when the magnetic field is as parallel to the wire as possible. This is explained theoretically by the Meissner effect. The superconductor expels any magnetic field it encounters, by setting up a persistent current to counteract the magnetic field. The more surface the magnetic field lines encounter, the more they need to be displaced. More displacement requires a stronger counteracting current. A stronger current means larger kinetic energy. At a certain point, the kinetic energy will be large enough to overcome the superconducting gap, and consequently superconductivity breaks down.

Figure 29 shows a plot of the same back-gate region measured at different magnetic field strengths. The field was directed in plane. At  $B = 0$  mT the superconducting gap is clearly present. At  $B = 50$  mT the gap is still present, but nearly closed. The beginnings of a zero-conductance Kondo peak is showing. At  $B = 100$  mT the zero-conductance peak is clearly displayed. At  $B = 500$  mT the peak has split into two separating electrons of different spin at different energies, in accordance with the Zeeman effect. Figure 30 displays the evolution of states at a fixed gate voltage,  $V_{BG} = -3943$  V, as magnetic field strength is increased, confirming the observations done in figure 29. The superconducting state at  $V_{SD} = 0$ , evolves with increasing magnetic field strength, to a zero conductance peak around  $B = 100$  mT, eventually splitting linearly into two with increasing magnetic field. From the graph a Zeeman energy of  $0.2$  meV at  $B = 500$  mT is extracted. This corresponds to a g-factor of  $6.9$ .

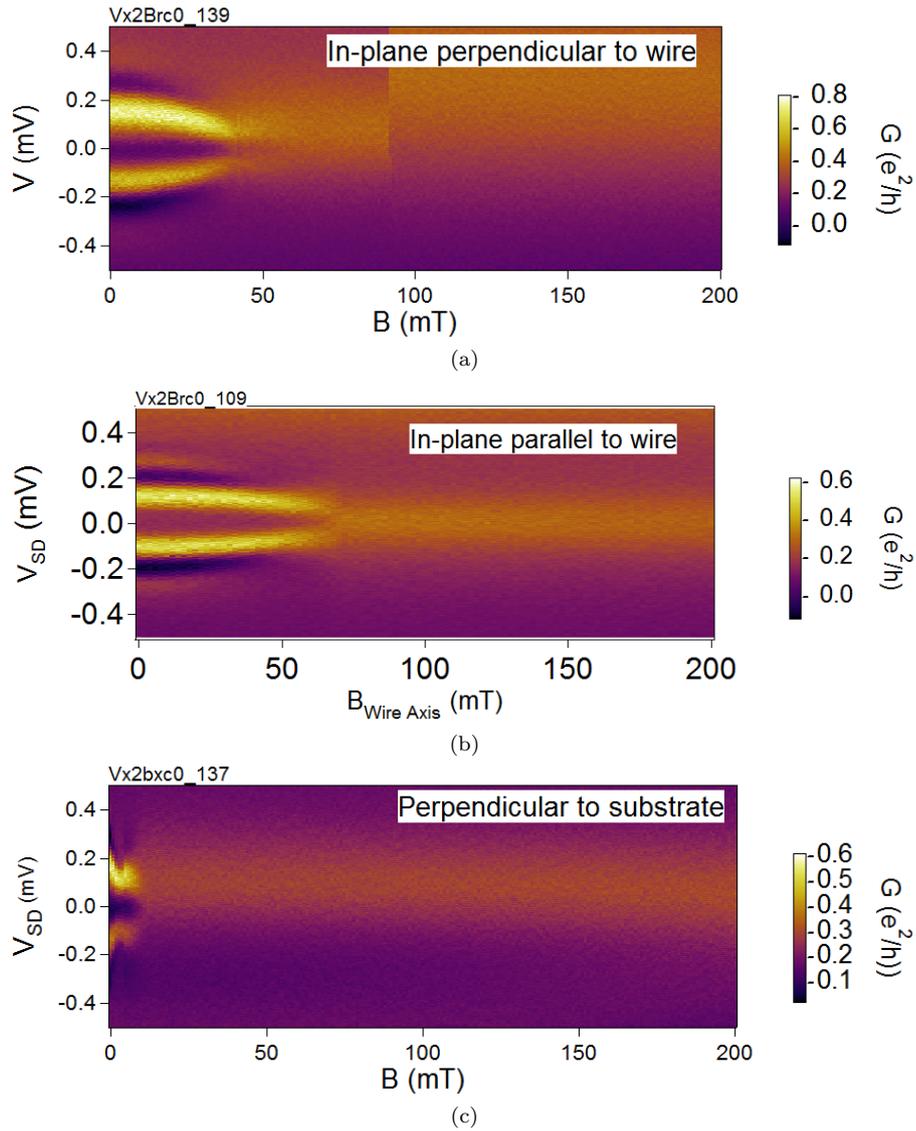


Figure 28: The critical field dependence on angle of magnetic field. The more parallel the magnetic field is to the wire, the larger the critical field. The critical fields are: a)  $\sim 45$  mT. b)  $\sim 75$  mT. c)  $\sim 10$  mT.

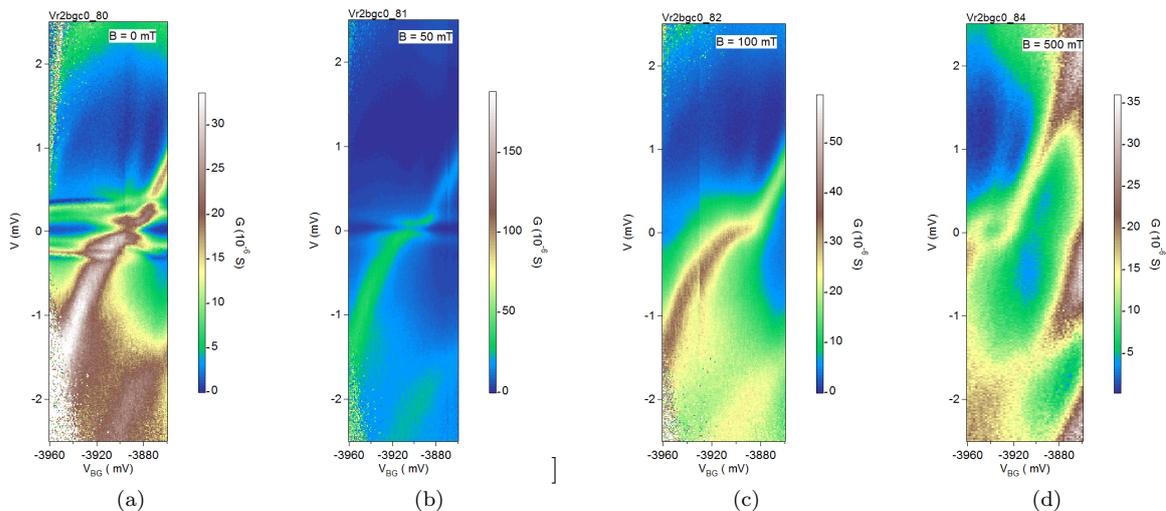


Figure 29: Differential conductance as a function of gate voltage, at different magnetic field strengths. a)  $B = 0$  mT, the superconducting gap is present. b)  $B = 50$  mT, the gap is closing. c)  $B = 100$  mT, the gap is now closed, a zero conductance Kondo peak is clearly visible. d)  $B = 500$  mT, the Kondo peak is split in two, by the Zeeman effect.

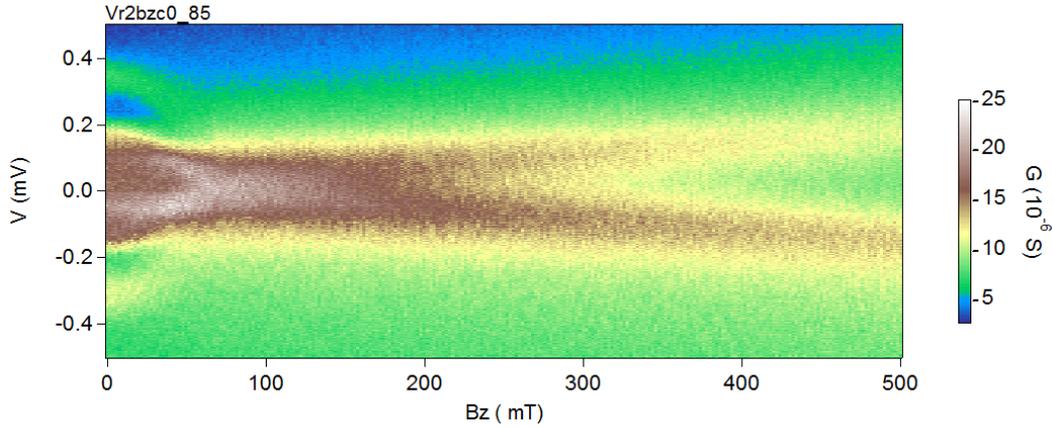


Figure 30: Magnetic field dependence taken at  $V_{BG} = -3943$  mV. At  $B = 0$  mT subband structures and the superconducting gap are visible. Around  $B = 100$  mT a Kondo peak is observed. At higher field the Kondo peak is subject to Zeeman splitting.

## 7 Conclusion

In the hunt for JoFET devices capable of withstanding high magnetic field, several physical phenomena were encountered, and with several different contacting materials, all with InAs nanowire as semiconductor. In the beginning of the process, niobium contacts were investigated, because of the high critical magnetic field it possesses. But because of the, at that time, inexperience of the fabricators, niobium contacts never resulted in any essential measurements.

Vanadium was investigated because of promising results from the article by Lee et al. [26], and because of its relatively high critical magnetic field. It was tested at first, with a sticking layer of titanium, but this resulted in non-superconducting contacts. We believe this was due to low metal purity, since the metal was old and highly oxidized. Because of a drop in pressure during vanadium evaporation, the getter effect was taken into account, and a pursuit of making a JoFET without sticking layer, made only with vanadium contacts, began. These experiments resulted in too high barriers from contacts to nanowires, and didn't result in a working JoFET, but provided other interesting results. Angular magnetic field dependent contacts were measured, showing that a magnetic field had a larger impact when applied perpendicular on the plane, as opposed to directly in the plane. The high barriers enabled measurements of the superconducting gap of vanadium, and showed a  $\Delta$  of 0.55 meV.

Determined to test the functionality of our recipe, and make a functioning JoFET, aluminium contacts were used next, as functioning devices with aluminium contacts had been possible to fabricate by others in the past [1]. Because of human mistakes, milling was done for 2 minutes instead of one. Despite initial worrying about the state of this device, the two minute milling certainly resulted in good contact, and a supercurrent was measured through the nanowire. Gate dependence was also measured, resulting in a working JoFET device with aluminium contacts and InAs nanowires. A critical current of  $\pm 50$  nA was measured, as well as an angular dependence of critical magnetic field, achieving a maximum critical field of  $\sim 75$  mT, in the direction along the wire axis. Besides, signs of Coulomb blockade, Kondo effect, and Shiba states were observed. From increasing magnetic field in the Kondo regime, Zeeman splitting of the Kondo peak was also seen.

Future research in fabricating JoFET devices capable of withstanding high magnetic field, would benefit from deeper investigation into both niobium and vanadium JoFETs. In both attempts using niobium we have been able to pinpoint human errors during the fabrication process, which if eradicated could lead to functioning devices. For the vanadium devices, we have, since the fabrication of the devices, been in contact with the authors of ref. [26], who have brought to our attention that vanadium leads in their experience tend to degrade in quality very easily when oxidised. They have circumvented this problem by adding an aluminium capping layer to their contacts. As such this is an obvious track to pursue in achieving a functioning vanadium JoFET. For better contact between the leads and the nanowire, the effects of longer milling time could be investigated further. General experiments in decreasing height and width of both contacts and nanowires, could also lead to higher critical B-field as this would lessen the current needed by the superconductor to uphold the Meissner effect.

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