Fabrication and measurement of hybrid quantum dot devices featuring Yu-Shiba-Rosinov sub-gap states

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Abstract: The aim of this bachelor project is to fabricate and study hybrid quantum dot (QD) devices featuring Yu-Shiba-Rosinov (YSR) sub-gap states, made on special InAs nanowires with 7 nm epitaxial aluminum coating on 3 facets. The advantage with these nanowires is the epitaxial aluminum, which can be etched away in a small window of semiconducting nanowire for creating QDs. These dots can be used for measuring the sub-gap states in superconducting materials due to the high degree of tunability. A device with a single QD featuring YSR sub-gap states was fabricated and analyzed, and a double QD system was afterwards made from the device using superconducting leads in the normal state, but not yet featuring YSR sub-gap states. The device does show the possibility for making an superconductor-double dot-superconductor device featuring YSR sub-gap states.

1 Introduction

Quantum dots (QDs) are sub-micron structures, confined in all dimensions, forming an island with a discrete energy spectrum working as an artificial atom [1] [2]. If made from a semiconductor, the island has most of its electrons bound, except for a small number of free electrons, which can be added or removed from the dot [1]. By taking advantage of Coulomb repulsion, an electron can be added to the quantum dot only if sufficient energy is provided to the electron, giving single electron transport. This provides the opportunity for studying energy spectrum for advanced electronic systems, for instance with superconducting electrodes (S), also known as hybrid-dot systems. By taking advantage of the single-electron control from a quantum dot, macroscopic quantum phenomenon in superconductors, involving large electron numbers, can be studied [3], such as Yu-Shiba-Rusinov sub-gap states (YSR) [4]. YSR sub-gap states are a hybrid phenomenon happening in S-QD systems with weak coupling between the electrodes. The states are seen within the superconducting gap Δ [5].

In this project, the focus is a fabrication and analysis of a double quantum dot system with superconducting leads of aluminum, to which the purpose is to show Yu-Shiba-Rusinov (YSR) sub-gap states. The quantum dots are based upon special InAs nanowires [6] with 7 nm of epitaxial aluminum coating on 3 of the facets, allowing them superconducting properties. This coating was then etched away in a region, after which the two quantum dots are defined, giving single electron transport at low temperatures.

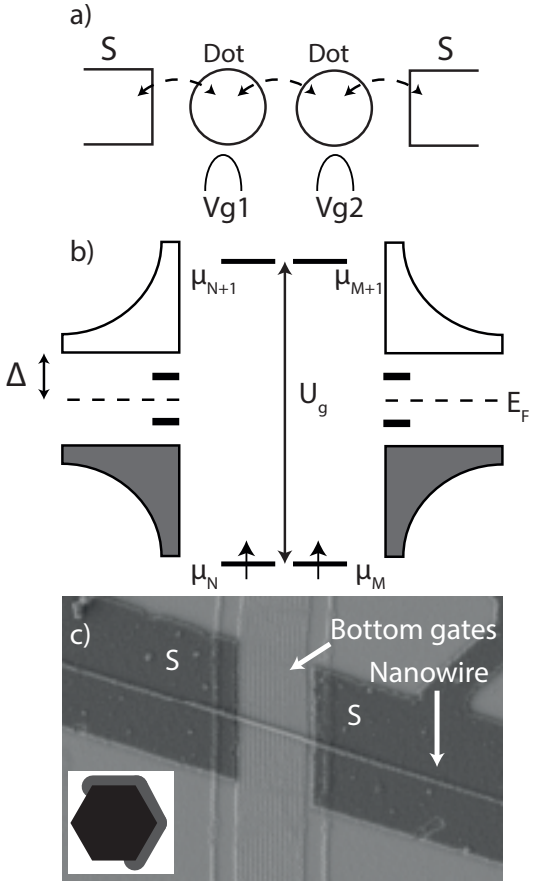

Fig. 1 a) Schematic view of a S-double dot-S system, showing tunneling behavior with a gate potential (Vg) coupled electrolytically to each dot. b) Schematic energy diagram of system showing S-state density of states on each side of the two dots, here just showing a single level. A single spin is added to each dot in order to show the ideal configuration for observing YSR sub-gap states. The next available states on the dots are also shown above Δ to show the condition $U_g \gg \Delta$. c) An SEM-image of system showing bottom gates and two Al-leads. Inset: A cross-section of the InAs nanowire showing the epitaxial aluminum on three of the facets.

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As shown in Fig. 1a the quantum dots will be in series and weakly coupled, creating a double-dot potential, where each dot has a plunger gate. The leads to the dots are superconducting, and will therefore have a density of states with a superconducting gap of width 2Δ[7], shown i Fig. 1b. The figure also shows that the quantum dots have a charging energy $U_g \gg \Delta$, and they have a single spin on each dot, which is needed to see YSR sub-gap states[5]. To avoid tunneling across the double dots, the thermal energy has to be much smaller than the charging energy, $U \gg k_B T$.
A SEM image of the finished device is shown in Fig. 1c, where both the bottom gates and the nanowire with the aluminum leads can be seen.

2 Fabrication

The devices were fabricated on Silicon wafers with 200nm SiO_2[a]. The bonding pads shown in Fig. 2a were the first structure to be made by optical lithography using a Heidelberg LED-writer and evaporation of 5 nm titanium (Ti) and 100 nm gold (Au). The 5 nm Ti is used for sticking layer. Afterwards the alignment marks, also shown in Fig. 2a, were made by electron beam lithography, also with 5 nm Ti and 100 nm Au. The next step was the bottom gates, which were made by electron beam lithography and evaporation of 5 nm Ti and 25 nm Au in the middle of the bonding pads pattern. The bottom gates were made in a grid of 8x4 sets of bottom gates. Each set has four bottom gates units, each unit with 17 bottom gates. They are 20 nm wide and spaced 40 nm apart, which gives a full bottom gate unit width of around a micron. An 20 nm oxide layer of HfO_2 was then applied on top of the bottom gates for both protection and for making sure they are gate coupled to the device only. The oxide was made by optical lithography and Atomic Layer Deposition (ALD). This was done in several steps in order to avoid the fencing effect[9] formed by the ALD (see Fig. 9 in supplementary for example). The device was also developed in MF321 with stirring to make a undercut, and after ALD, the device was left in N-Methyl-2-pyrrolidone (NMP) thermalized at 85°C for an hour for better lift-off. An SEM image showing 3 sets of 17 bottom gates with as oxide layer is shown in Fig. 2c.
Afterwards, the InAs nanowire with epitaxial aluminum was deposited on top and across the bottom gates. The nanowires epitaxial aluminum are 7 nm thick, and were grown by P. Krogstrup at NBI[10]. A window of 380 nm, corresponding to 7 bottom gates, was wet-etched on the nanowire in the middle of the bottom gates, removing the aluminum coating in the region, leaving only the semiconducting nanowire. Aluminum leads were then deposited by electron beam lithography and metal evaporation of 5 nm Ti and 100 nm Aluminum (Al) on the ends of the nanowire. A schematic of a finished device is shown in figure 2b. The final step was connecting the bonding pads with the leads and bottom gates, which was done by electron beam lithography and metal evaporation of 5 nm Ti and 100 nm Au. A optical image of the contacts is shown in Fig. 2d.

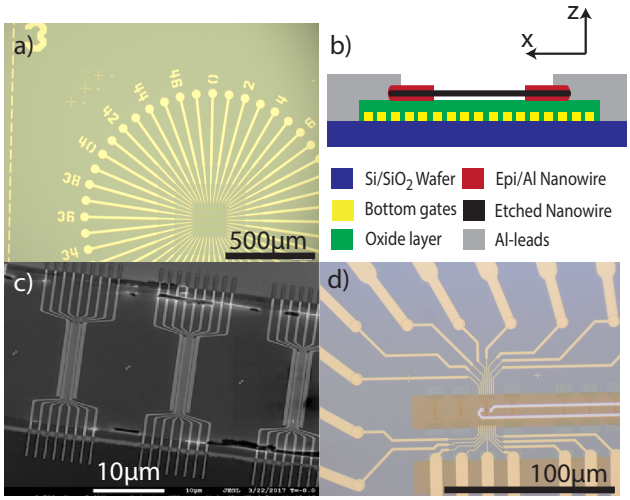

Fig. 2 a) An optical image of bonding pads and alignment marks, b) Schematic of cross-section of a finished device. There are 17 bottom gates for making the double-dot potential and 7 gates under the etch window. Not for scale. c) SEM image of bottom gates (here after oxide layer for protection). d) An optic image of the aluminum leads, the nanowire and the gold the bottom gates.

In Table 1 an overview of the devices fabricated and discontinued is shown. All measurements were made on one of the two devices from batch A2.

Table 1 Fabrication log: Overview of the generations of devices. Each generation included 7 lithography steps (counting oxide layer as one step). A device from batch A2 is the device in focus in this project, but others were also fabricated.

Generation	Working devices	Comment
A1	0	Misalignment between optical and e-beam lithography
A2	2	Same procedure as A1
A3	0	Bad lift-off for bottom-gates, batch was discontinued
A4	0	Last oxide layer went bad, batch was discontinued
A5	1	New design changes for the bottom gates for better gating

a The division of labor for fabrication was shared between myself, Anders Jellinggaard and Morten Hels (see Acknowledgment). Anders and I both made the bonding pads, while Anders and Morten made the alignment marks and the bottom gates. I deposited the oxide layers and the nanowires, while Anders and Morten made the etch window and made the aluminum and gold leads.

3 Measurement and analysis of the device

The setup measures dI/dV_{SD} and V^{AC} via lock-in techniques.[b] A AC signal from Lock-in Amplifier 1 and a DC signal from the DAC is sent through a 10000:1 and 1000:1 voltage divider respectively and sent into the sample. With a current amplifier, the AC signal is measured with Lock-in Amplifier 1 and the DC signal is measured with a Digital Multi-meter 1 (DMM1). The voltage across the sample is amplified with a voltage amplifier and the AC signal is measured with Lock-in Amplifier 2 and the DC signal is measured with Digital Multi-meter 2 (DMM2).

Electron transport measurements were performed on one of the finished devices from batch A2 (see table 1) at low temperatures (T= 30 mK). The setup can be seen in Fig. 3.

The first measurement was to see if the aluminum, both the epitaxial one on the nanowire and the deposited leads, was truly superconducting. Figure 4 shows the differential conductance as a function of bias voltage and magnetic field strength.

Figure 4 shows enhanced conductance around zero magnetic field and zero bias, which arises from Andreev reflections[11]. There is no supercurrent due to an asymmetric coupling to the leads. This indicates a good interface between the superconductor and the normal leads. The enhanced conductance is lost at lower field strength for the perpendicular magnetic field (Fig. 4a) than the magnetic field across the nanowire (Fig. 4b) as expected[7].

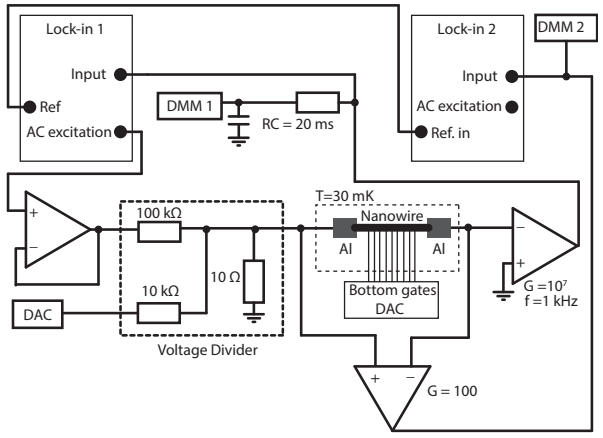

Fig. 3 Schematic of the measurement setup. Both Lock-in amplifiers are Stanford Research System model SR830. Lock-in Amplifier 1 measures the conductance $\frac{dI}{dV_{SD}}$, while Lock-in Amplifier 2 measures V^{AC}. The boxes labeled DMM are HP digital multi-meters model 34401A. The DAC connected to the bottom gates is the same as the one connected to the voltage divider, and is a Marcus decaDAC.

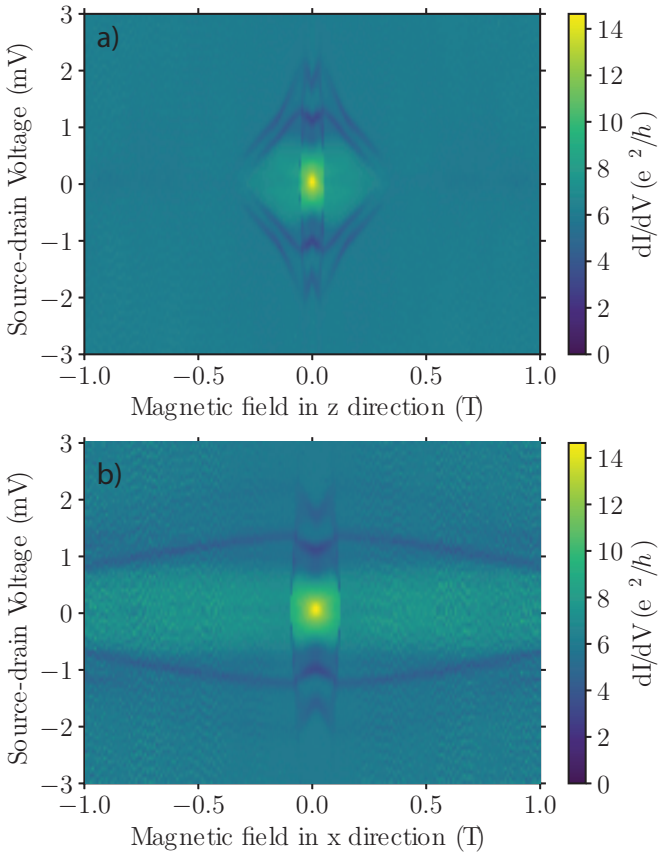

Fig. 4 Measurements of the differential conductivity as a function of bias voltage and magnetic field in two situations: a) out of plane for the device (z-direction) and b) in plane of the device (x-direction). See fig. 2b for directions

The critical field strengths for this device were estimated to be $B_C^{\perp} \approx 60$ mT for the B-field out of plane (B_Z) and $B_C^{||} \approx 140$ mT for the B-field in plane (B_X). The superconducting gap was estimated in the open regime to be $\Delta = 200\ \mu\text{eV} \pm 30\ \mu\text{eV}$. According to former research, Δ has not exceeded 250 μeV (see table 2[c]), which fits well with the observed in Fig. 4.

b The division of labor for measurements was shared between myself, Anders Jellinggaard and Morten Hels. Anders and I made the setup, while Morten and I tuned and measured the device.

c [c]It is not specified which angle the critical field for the first reference is measured at, or which device of the five measured in the article [11].

Table 2 Overview of former research papers values for similar devices and nanowires. $B^{\perp}$ is the z-direction and $B^{||}$ is the x or y-direction (see directions in Fig. 2).
NB: The dashed line means that the value was not mentioned or not measured.

Facets/ Aluminum	Thickness (nm)	Δ^*	$B_C^{||}$ or $B_C^{\perp}$
2	-	220 μeV [11]	$B_C \approx 2.2$ T[c]
2	10	190 μeV [10]	$B_C^{\perp} = 1.9$ T
Full	-	190 μeV [8]	$B_C^{||} = 75$ mT
Bulk	120	110 μeV [12]	-

The critical field strength also fits with some of the former research results. Figure 4 also shows some unexpected transitions (black lines). These lines shows values for B_C and Δ much higher than expected (table 2) and are therefore not understood.

After reassuring that the leads are superconducting, a quantum dot was tuned with zero field to keep the S-leads in the superconducting state. Bias spectroscopy of a QD-S system with a probe is expected to show YSR sub-gap states, due to alignment of the filled states in the probe with a QD state and the sub-gap states of the S-lead. Such a bias spectroscopy of the device was performed around the single-defined quantum dot and is shown in Fig. 5a. However, the results from Fig. 5a depends on the state of the probe. Figure 5b shows the energy in the N-QD-S system as a function of gate potential (V_{g1}), and shows the even-odd symmetric filling of the Coulomb Diamonds for the YSR sub-gap states. The figure also shows the excitation energy (ζ) for a specific gate potential. The excitation energy is the energy needed for exciting the electron from the ground state to the excited state (here the YSR sub-gap state). The excitation energy for this system can achieve any energy between zero and the superconducting gap Δ, due to the continuum of states in a normal lead. For a S-QD-S system, which is shown in Fig. 5c, the excitation energy can only achieve values between Δ and 2Δ. The reason can be seen in Fig. 5d, which shows the density of states for the two S-leads with a QD in between with asymmetric barriers. To align a filled state from the continuum of states in the probe (left S-lead) with a empty state in the S-lead (right S-lead), the probe's superconducting gap Δ need to be overcome by the applied bias, V_{SD}. At $eV_{SD} = \Delta$, states inside the gap of the S-lead strongly coupled to the QD (right S-lead) are being probed. If $eV_{SD} > 2\Delta$, the empty states over the gap Δ in the S-lead is being probed. So to see transition, the continuum of filled states in the probe has to align with either the empty sub-gap states at $|eV_{SD}| = \Delta + \zeta$ or the empty continuum of states in the S-lead at $|eV_{SD}| > 2\Delta$, as shown in Fig. 5c. Therefore, the YSR sub-gap states for a S-QD-S device is expected to have the gate dependency as illustrated in Fig. 5c.

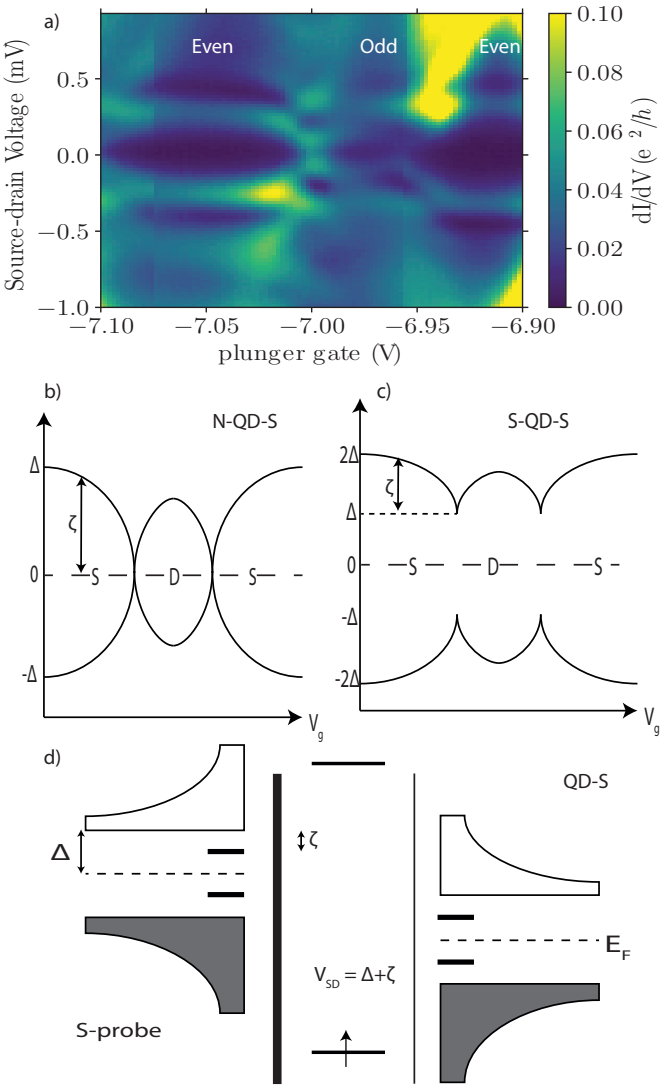

Fig. 5 a) A measurement of differential conductance as a function of gate voltage and bias voltage for a QD-S system with a S-probe at zero field. Clear YSR sub-gap states in Coulomb diamonds are visible. A even-odd symmetry can be seen. The states do not cross at $V_{SD} = 0$, but the gap is not clear. b) Schematic of the ideal QD-S configuration with a N-probe, showing YSR sub-gap states. The electron configuration show even-odd symmetry of singlets and doublets, changing with gate voltage. c) Schematic of the ideal QD-S configuration with a S-probe, showing YSR sub-gap states. The electron configurations show even-odd symmetry of singlets and doublets, changing with gate voltage. d) A schematic energy diagram of the S-QD-S system measured in a) and c) with a applied bias voltage and asymmetric tunneling barriers. The quantum dot shows a level with a single spin, and that the charging energy is much higher than Δ.

The YSR sub-gap states are clearly visible in Fig. 5a,

together with the even-odd symmetry. The YSR sub-gap states follows the illustration in Fig. 5b and 5c well within the Coulomb diamonds. The measurement also gives an unexpected result. The sub-gap states show the even-odd symmetry, but there is no gap at zero bias. Figure 5a shows an intermediate of the two situations illustrated in Fig. 5b and 5c, which makes an extraction of the superconducting gap Δ troubling. The states do not cross each other, since there is no increased conductance at zero bias. The height of the YSR sub-gap states are around 0.26 mV $\pm$ 0.06 mV, so Δ can be either 0.26 meV $\pm$ 0.06 meV for the N-QD-S situation of 0.13 meV $\pm$ 0.03 meV for the S-QD-S situation. For this device, Δ should be the second option, since both leads the QD is aluminum. The asymmetric coupling does that the sub-gap states in the probe does not make transition to the lead, so there should only be transition when the bias exceeds Δ. If the sub-gap states were probing, areas of negative differential conductance would be seen in Fig. 5a. Therefore, it is assumed that the probe is superconducting with a soft gap, which means it has a continuum of sub-gap states, thus the bias-symmetric sub-gap states meet at zero bias.

After confirming that the device shows YSR sub-gap states for a single dot and two S-leads, a double dot was the next step to examine. Since it is unclear what one is supposed to see, a magnetic field of 200 mT was applied to the device to make the lead normal conducting for the sake of simplicity. This will make the tuning of the double-dot potential simpler. Figure 6b shows the result of the double dot measurement of differential conductance as a function of the two plunger gate voltages, Vg1 and Vg2. Figure 6a shows the variables obtainable from the double dot charge stability diagram (honeycomb).

The four voltages differences shown in Fig. 6a can be obtained from a honeycomb measurement, and with them, parameters like the capacitances and the charging energy for the system can be calculated. The gate capacitances for the dots can be obtained with Eq. 1, while the inter-dot capacitances is obtained with Eq. 2:

$$C_{g1(2)} = \frac{|e|}{\Delta V_{g1(2)}} \left(1 + \frac{\Delta E}{E_{C1(2)}}\right) \tag{1}$$

$$C_m = \frac{\Delta V_{g1(2)}}{\Delta V^m_{g1(2)}} * C_{2(1)} \left(1 + \frac{\Delta E}{E_{Cm}}\right) \tag{2}$$

Where ΔE is the energy spacing between the levels, E_C is the charging energies for a given capacitor and $C_{1(2)}$ is the sum of all capacitances attached to dot 1(2):
$C_{1(2)} = C_{L(R)} + C_{g1(2)} + C_m$.
$C_{L(R)}$ is the capacitances to the leads.
For degenerate levels, ΔE is zero. For the sake of simplicity it is assumed that this is the case. From the honeycomb plot (Fig. 6b), the four variables were estimated to: $\Delta V_{g1} = 44$ mV $\pm$ 2 mV, $\Delta V_{g2} = 54$ mV $\pm$ 2 mV, $\Delta V^m_{g1} = 12.0$ mV $\pm$ 0.5 mV and $\Delta V^m_{g2} = 8.0$ mV $\pm$ 0.5 mV.

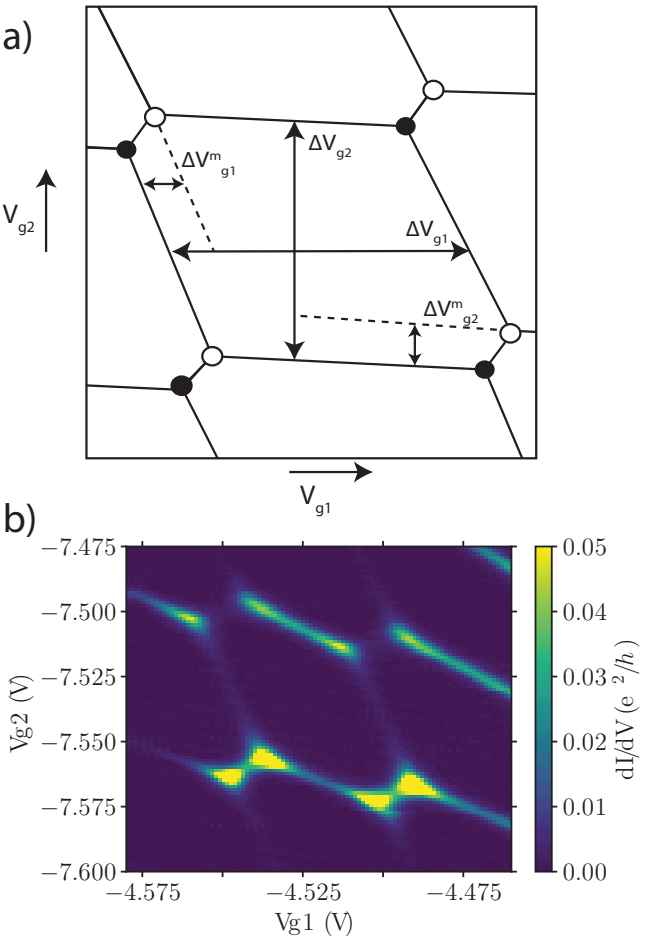

Fig. 6 a) A schematic of the double dot charge stability diagram (also known as honeycomb) with analysis possibilities. The small circles represent the triple point, where three charge states coexists. The filled circle represent electron transfer progress and the hollow circle represent hole transfer progress. b) Measurement of Coulomb honeycomb from a double dot system at $V^{DC}_{SD} = 0$, $B_Z = 200$ mT and with AC voltage with amplitude $V^{AC} = 5$ μV and frequency $f = 127$ Hz. NB: The z-axis is limited to range [0:0.05] to highlight the transition lines. Some transitions e.g. the triple points has higher differential conductivity than 0.05 e^2/h.

From the variables, ΔV_{g1} and ΔV_{g2}, the two gate capacitances were estimated for this measurement to be $C_{g1} = 3.6$ aF $\pm$ 0.2 aF and $C_{g2} = 3.0$ aF $\pm$ 0.1 aF.
To get the inter-dot capacitance and the capacitances to the leads, a third equation was needed for the lever-arms, which

is Eq. 3:

$$\alpha_{1(2)}\delta V_{g1(2)} = \frac{C_{g1(2)}}{C_{1(2)}}|e|\delta V_{g1(2)} = |eV_{SD}| \tag{3}$$

where δV_{g1} and δV_{g2} can be determined from a Coulomb honeycomb measurement with a finite bias[d]. Such a measurement can be seen on Fig. 7.

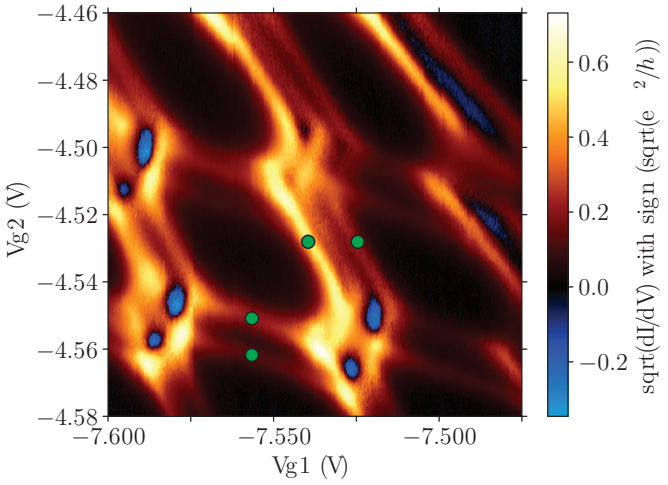

Fig. 7 Measurement of Coulomb honeycomb from a double dot system at $V_{SD}^{DC} = -1$ mV, $B_Z = 200$ mT and with AC voltage with amplitude $V^{AC} = 5\ \mu$V and frequency $f = 127$ Hz. The color scale is made of the square root of difference conductance to highlight the small transitions. The green dots shows there the measurement has been made for determining δV_{g1} and δV_{g2}.

The two parameters δV_{g1} and δV_{g2} were determined to be $\delta V_{g1} = 12.0$ mV $\pm$ 0.5 mV and $\delta V_{g2} = 12.0$ mV $\pm$ 0.5 mV. By using Eq. 3 and Eq. 2 together, the inter-dot gate capacitance was estimated to $C_m = 6$ aF $\pm$ 1 aF and the two lead capacitances were estimated to $C_L = 34$ aF $\pm$ 4 aF and $C_R = 14$ aF $\pm$4 aF. These capacitances can be used to determine charging energies for the three capacitors, with help from Eq. 4 and Eq. 5:

$$E_{C1(2)} = \frac{e^2}{C_{1(2)}}\left(\frac{1}{1-\frac{C_m^2}{C_1 C_2}}\right) \tag{4}$$

$$E_{Cm} = \frac{e^2}{C_m}\left(\frac{1}{\frac{C_1 C_2}{C_m^2}-1}\right) \tag{5}$$

The charging energies were estimated to: $E_{C1} = 3.8$ meV $\pm$ 0.5 meV, $E_{C2} = 7$ meV $\pm$ 2 meV and $E_{Cm} = 1.0$ meV $\pm$ 0.4 meV.

d Here we assumed that the onset of the honeycomb diamond appeared at zero bias even though the superconductors have a gap

From Eq. 3 the two lever-arms α_1 and α_2 were determined to be $\alpha_1 = 0.083\ \pm\ 0.002$ and $\alpha_2 = 0.13\ \pm\ 0.04$ respectively. Table 3 gives a overview of the different parameters measured and calculated throughout this double dot analysis.

Table 3 Overview of values estimated and calculated throughout this paper. The uncertainties on the measured values are estimated from the precision of the peaks positions.

Measured values:		
ΔV_{g1}	44 mV	$\pm$ 2.0 mV
ΔV_{g2}	54 mV	$\pm$ 2.0 mV
ΔV_{g1}^m	12.0 mV	$\pm$ 0.5 mV
ΔV_{g2}^m	8.0 mV	$\pm$ 0.5 mV
δV_{g1}	12.0 mV	$\pm$ 0.5 mV
δV_{g2}	12.0 mV	$\pm$ 0.5 mV
V_{SD}	-1 mV	
Calculated values:		
C_{g1}	3.6 aF	$\pm$ 0.2 aF
C_{g2}	3.0 aF	$\pm$ 0.1 aF
C_L	34 aF	$\pm$ 4 aF
C_R	14 aF	$\pm$ 4 aF
C_M	6 aF	$\pm$ 1 aF
C_1	44 aF	$\pm$ 5 aF
C_2	24 aF	$\pm$ 5 aF
E_{C1}	3.8 meV	$\pm$ 0.5 meV
E_{C2}	7 meV	$\pm$ 2 meV
E_{CM}	1.0 meV	$\pm$ 0.4 meV
α_1	0.083	$\pm$ 0.002
α_2	0.13	$\pm$ 0.04

As a final note, another measurement of the stability diagram for the double dot system was made with a broader range in gate voltages in order to see the honeycomb pattern, seen in Fig. 8:

The figure shows different sizes of the honeycombs for different number of electrons. This can for instance be seen for honeycomb (2,1), which $Vg2$ range is smaller than for honeycomb (2,3) or which $Vg1$ range is smaller than for honeycomb (1,1). This shows the assumption that the addition energy $\Delta E = 0$ is not met, for either dot. The figure shows that the addition energy for Vg2 is larger than for Vg1.

4 Conclusions

The measurements on the device presented in this paper have revealed two interesting features: Tunability for a double quantum dot and how Yu-Shiba-Rosinov sub-gap states for a single quantum dot evolve with plunger gate voltage. This makes it probable for the device in future studies to combine the two features and show YSR sub-gap states in a double QD configuration with a hybrid quantum dot superconductor-semiconductor nanowire. However, for the double dot device, we do not see clear Yu-Shiba-Rosinov sub-gap states.

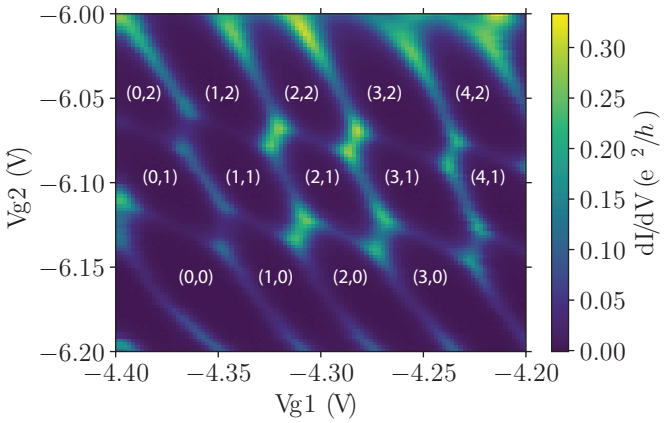

Fig. 8 A measurement of Coulomb honeycomb for the double dot system with a broader gate range for showing several honeycombs. The configuration $(0,0)$ is taken as the zero-point with electron configuration (N_1,N_2). The figure shows that the assumption of $\Delta E = 0$ is not met.

5 Acknowledgement

The authors thank Anders Jellinggaard and Morten Canth Hels for assistance in designing and fabrication of the device, especially steps involving Elionix EBL steps and metal evaporation (see tables 5, 6, 8, 9 and 10 in Supplementary), and with assistance in measurements and setup.
The authors also thank Peter Krogstrup for growing the InAs nanowires with 3 facets of epitaxial aluminum.

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6 Supplementary

6.1 Former projects: ALD fencing effect

A research project prior to this project was to determine a technique for fabricating isolating oxide layers by using Atomic Layer Deposition (ALD) and a Heidelberg LED-writer. The oxide layer were creating high walls, known as fences or Batman ears, around the edges of the defined oxide layer, which could create problems in making ohmic contact to the anything created on top of the oxide layer. These walls arose from the developed resist layer, where the ALD would climb the walls of the resist. A way found to avoid this was two-fold. By making a undercut through more development time made it more difficult for the ALD to climb the well-defined resist walls, and by making the lift-off progress longer and more ”violent” through sonication, the walls could be partly destroyed.

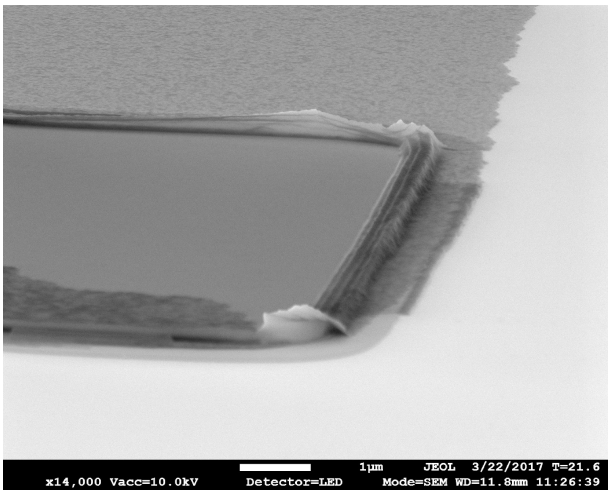

Fig. 9 SEM image of oxide layer deposited with optical lithography and ALD without bottom gates. The image shows high walls at the end of the oxide layer, which can give problems for making ohmic contact to anything made on top of the oxide layer.

6.2 New design for batch A5

The only design changes made to batch A5 was the design of the bottom gates. Here, the outer bottom gates have been made wider for better gating. The idea was to easier close of the quantum dots from the leads, giving better single electron transport with a better range.

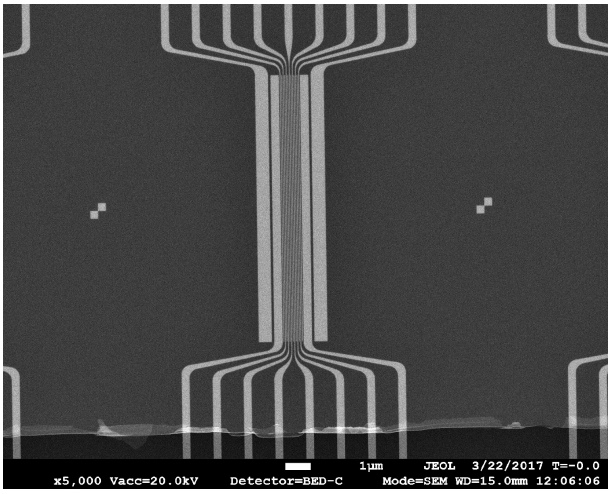

Fig. 10 SEM image of the bottom gates for the A5 batch.

6.3 Fabrication protocols

Table 4 Protocol for bonding pads: From wafer to lift-off

1	Sonicate Si/SiO_2 wafer in acetone for 6 min at frequency 80 kHz at 100%	2	Bake for 4 min at 185°C
3	Spin LOR3B resist at 4000rpm for 45s	4	Bake for 4 min at 185°C
5	Spin AZ1505 resist at 4000rpm for 45s	6	Bake for 2 min at 115°C
7	Expose in Heidelberg LED-writer for 20ms at -2 defocus	8	Develop in MF321 for 45s with mild stirring
9	Rinse in MilliQ water for 30s	10	Blowdry with N_2
11	Ash for 2 min	12	Evaporate 5 nm Ti and 100 nm Au
13	Scratch all four corners of wafer	14	Put wafer in 185°C pre-heated NMP and leave for 60 min
15	Flush with warm NMP	16	Transfer to NMP at room temperature
17	Flush with acetone and then IPA	18	Blowdry with N_2

Table 5 Protocol for alignment marks

1	Flush with acetone and then IPA	2	Blowdry with N_2
3	Bake for 3 min at 185°C	4	Spin 200 μL of EL9 resist at 4000rpm for 45s
5	Bake for 3 min at 185°C	6	Spin 200 μL of CSAR4 resist at 4000rpm for 45s
7	Bake for 3 min at 185°C	8	Expose Elionix EBL with 400 μC/cm^2, 500 pA current, field Size=150 μm and 40 μm aperture
9	Develop in O-xylene for 30s	10	Transfer to MIBK:IPA 1:3 for 40s
11	Rinse in IPA for 30s	12	Blowdry with N_2
13	Ash for 2 min	14	Evaporate 5 nm Ti and 100 nm Au
15	Put wafer in 185°C pre-heated NMP and leave for 60 min	16	Flush with warm NMP
17	Transfer to NMP at room temperature	18	Flush with acetone and then IPA
19	Blowdry with N_2		

Table 6 Protocol for bottom gates

1	Sonicate wafer for 1min in acetone at frequency 37 kHz 50% at 45°C	2	Rinse in IPA and blowdry with N_2
3	Ash for 30s	4	Bake for 4 min at 185°C
5	Spin A2 resist at 4000rpm for 45s	6	Bake for 4 min at 185°C
7	Expose in Elionix EBL with 1600 μC/cm^2, 500 pA current, field Size=150 μm and 40 μm aperture	8	Develop in 7:3 IPA:MilliQ water for 270s at -5°C
9	Blowdry with N_2 for 4min to thermalize wafer	10	Ash for 30s
11	Evaporate 5 nm Ti and 25 nm Au	12	Put wafer in 185°C pre-heated NMP and leave for 60 min
13	Flush with warm NMP for only 30s to avoid damaging bottom gates	14	Transfer to NMP at room temperature
15	Flush with acetone and then IPA	16	Blowdry with N_2

Table 7 Protocol for oxide layer: A minimum of 20 nm of HfO_2 is needed, and should be deposited over several steps. Recommended is 2-3 repetitions with 7-10 nm HfO_2 per repetition

1	Rinse in acetone and then IPA	2	Blowdry with N_2
3	Ash for 4 min	4	Bake for 4 min at 185°C
5	Spin LOR3B resist at 4000rpm for 45s	6	Bake for 4 min at 185°C
7	Spin AZ1505 resist at 4000rpm for 45s	8	Bake for 2 min at 115°C
9	Expose in Heidelberg LED-writer for 20ms at -2 defocus.	10	Develop in MF321 for 30s with stirring
11	Submerge in MilliQ water for 60s	12	Blowdry with N_2 for 4min to thermalize wafer
13	Ash for 2min	14	Deposit 20 nm of HfO_2 with ALD for 100s with 400s purge time at 90°C
15	Scratch all four corners of wafer	16	Put wafer in 185°C pre-heated NMP and leave for 60 min
17	Sonicate wafer in warm NMP at frequency 80 kHz 50% for 10s	18	Flush with warm NMP
19	Transfer to NMP at room temperature and flush again	20	Flush with acetone and then IPA
21	Blowdry with N_2		

Table 8 Protocol for Etch-window. NB: Do not strip resist when done to avoid removing the nanowire.

1 Spin A4/EL9 2:3 mixture at 4000rpm for 45s	2 Bake for 2min at 115°C
3 Expose in Elionix EBL^e with 800 μC/cm^2 and 500 pA current	4 Develop in MIBK:IPA 1:3 for 90s
5 Submerge in IPA for 30s	6 Blowdry with N_2
7 Ash for 1min	8 Bake for 30s at 115°C
9 Trans D at 55°C for 9s	10 Rinse in MilliQ water
11 Blowdry with N_2	12 Ash for 1 min

Table 9 Protocol for Al-leads

1 Spin A4 at 4000rpm for 45s	2 Bake for 2min at 115°C
3 Expose in Elionix EBL^e with 800 μC/cm^2	4 Develop in MIBK:IPA 1:3 for 90s
5 Submerge in IPA for 30s	6 Blowdry with N_2
7 RF milling for 5 min at 15 W and 18 mTorr	8 Evaporate 5 nm Ti and 100 nm Al
9 Submerge in pre-warmed NMP at 85°C for 1min	10 Sonicate for 5s in warm NMP at frequency 37 kHz 30%
11 Leave for 45min in warm NMP	12 Sonicate for 5s in warm NMP at frequency 37 kHz 30%
13 Rinse in warm NMP	14 Transfer to room temperature NMP for 20s
15 Rinse in IPA	16 Blowdry with N_2

Table 10 Protocol for Au-leads

1	Spin A4/EL9 2:3 mixture at 4000rpm for 45s	2	Bake for 4min at 115°C
3	Spin A4 at 4000 rpm for 45s	4	Bake for 4min at 115°C
5	Expose in Elionix EBL[e] with 800 μC/cm^2	6	Develop in MIBK:IPA 1:3 for 90s
7	Submerge in IPA for 30s	8	Blowdry with N_2
9	Ash for 2min	10	Evaporate 5 nm Ti and 100 nm Au
11	Submerge in pre-warmed NMP at 85°C for 1min	12	Sonicate for 10s in warm NMP at frequency 37 kHz 30%
13	Leave for 60min in warm NMP	14	Sonicate for 5s in warm NMP at frequency 37 kHz 30%
15	Rinse in warm NMP	16	Transfer to room temperature NMP for 20s
17	Rinse in IPA	18	Blowdry with N_2

e For these Elionix EBL steps, higher precision is not vital